Power Electronic Systems
Laboratory



IEEE Transactions on Plasma Science, Vol. 40, No. 10, pp. 2554-2560, October 2012.

# Balancing Circuit for a 5-k V/50-ns Pulsed-Power Switch Based on SiC-JFET Super Cascode

J. Biela
D. Aggeler
D. Bortis
J. W. Kolar



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

# Balancing Circuit for a 5-kV/50-ns Pulsed-Power Switch Based on SiC-JFET Super Cascode

Juergen Biela, *Member, IEEE*, Daniel Aggeler, *Member, IEEE*, Dominik Bortis, *Member, IEEE*, and Johann W. Kolar, *Senior Member, IEEE*

***Abstract*—In many pulsed-power applications, there is a trend to modulators based on semiconductor technology. For these modulators, high-voltage and high-current semiconductor switches are required in order to achieve a high pulsed power. Therefore, often, high-power IGBT modules or IGCT devices are used. Since these devices are based on bipolar technology, the switching speed is limited, and the switching losses are higher. In contrast to bipolar devices, unipolar ones (e.g., SiC JFETs) basically offer a better switching performance. Moreover, these devices enable high blocking voltages in the case where wide-band-gap materials, for example, SiC, are used. At the moment, SiC JFET devices with a blocking voltage of 1.2 kV per JFET are available. Alternatively, the operating voltage could be increased by connecting $N$ JFETs and a low-voltage MOSFET in series, resulting in a super cascode switch with a blocking voltage $N$ times higher than the blocking voltage of a single JFET. For the super cascode, auxiliary elements are required for achieving a statically and dynamically balanced voltage distribution in the cascode. In this paper, a new balancing circuit, which results in faster switching transients and higher possible operating pulse currents, is presented and validated by measurement results.**

***Index Terms*—JFETs, medium voltage switch, pulsed power systems.**

## I. Introduction

In MANY pulsed-power applications such as accelerators, medical systems, or radar systems, there is a general trend toward solid-state modulators based on semiconductor technology, as these offer adjustable pulse parameters, turnoff capabilities in the case of failure, and lower maintenance effort. There, high-voltage (HV), high-current, and fast semiconductor switches are required in order to achieve a high pulsed power and fast transients. Therefore, often, high-power IGBT modules or IGCT devices are used.

Since these devices are based on bipolar technology, the switching speed is limited, and the switching losses are higher (e.g., due to the tail current), what could limit the pulse-repetition rate and the converter efficiency and what increases the costs for cooling. Part of the switching speed limitation is caused by the parasitic elements of the power module packaging as has been shown in [1] and [2]. There, standard 4.5-kV IGBT chips for traction applications are mounted in a special low inductive housing, which allows significantly faster switching transitions than possible with standard high-power modules.

In contrast to bipolar devices, unipolar ones (e.g., SiC JFETs) basically offer a much better switching performance since these utilize only majority carriers for conduction. In the case where wide-band-gap materials, e.g., SiC or GaN, are used, these devices enable also a high blocking voltage. At the moment, normally on and normally off SiC JFETs with a blocking voltage of 1.2 kV [5]–[7] and first test samples of 6.5-kV devices are available.

In order to increase the blocking voltage capability, the JFETs can be connected in series, which requires either active or passive control of the voltage distribution. Alternatively, a super cascode where JFETs are cascaded and connected in series with a low-voltage MOSFET [8] could be used. The super cascode has the advantage of simple control and very fast switching transients but requires auxiliary elements for static and dynamic balancing of the voltage distribution.

In [3] and [9], a first auxiliary circuit has been proposed, and first results for the switching behavior with a resistive load have been presented. However, at the beginning, the turn-on changed from a very fast transient to a slower one (a kind of $RC$ behavior), resulting in a slower turn-on transient. Therefore, in this paper, a new balancing network of the super cascode is presented, which allows a turn-on exceeding a $dv/dt$ of 100 kV/$\mu$s and a 90% to 10% rise time below 50 ns [4]. First, the basic operation principle is explained shortly in Section II-A, and then, the auxiliary elements required for static and dynamic balancing are presented in Sections II-B and C.

With the new balancing network, the transient voltage distribution is significantly improved compared to that with the previous balancing network. For validating the proposed circuit, measurement results are presented in Section III.

## II. SiC-JFET Super Cascode

For increasing the blocking voltage capability of a semiconductor switch, a series connection of the devices could be used. With a series connection, however, the voltage distribution must be controlled either actively or by passive snubber elements. Active control requires a large number of fast gate drives and measurement systems, and with the passive snubber elements, the overall switching losses are increased.

Manuscript received September 30, 2009; revised July 26, 2011; accepted September 11, 2011. Date of publication October 21, 2011; date of current version October 5, 2012.

J. Biela is with the Laboratory for High Power Electronic Systems, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland (e-mail: jbiela@ethz.ch).

D. Aggeler is with the Power Electronics System Group, ABB Corporate Research Center, 5405 Baden-Dättwil, Switzerland (e-mail: daniel.aggeler@ch.abb.com).

D. Bortis and J. W. Kolar are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland (e-mail: bortis@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

Digital Object Identifier 10.1109/TPS.2011.2169090

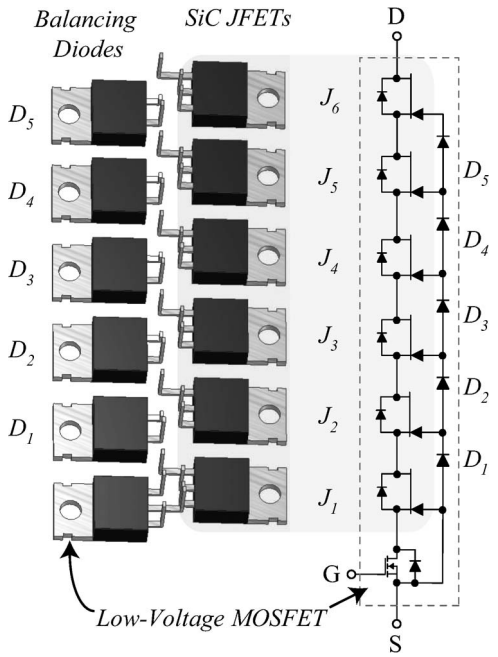


Fig. 1. Schematic of a super cascode consisting of six series-connected SiC JFETs and a silicon low-voltage MOSFET.

An alternative concept, which has just one control input/gate, is the JFET super cascode [8], which consists of a low-voltage silicon MOSFET and series-connected normally on JFETs as shown in Fig. 1. There, six 1.2-kV SiC JFETs and a low-voltage silicon MOSFET are used, resulting in a total blocking voltage of 7.2 kV. Due to the limited die size, the current rating of the SiC JFETs is limited to 5 A for continuous operation at the moment but will soon increase to 20 A and more as announced by SiCED [6].

The key elements for balancing the voltage distribution of the series-connected JFETs are five low-power avalanche rated Si diodes [8] with an avalanche voltage of approximately 800 V. For a reliable operation under static and transient conditions, however, additional elements are required as will be discussed in the following sections by enhancing the super cascode in Fig. 1.

### A. Basic Operation Principle

The super cascode in Fig. 1 is controlled only via the gate of the low-voltage MOSFET, and for turning the switch on, a positive gate voltage is applied to this gate. With a turned-on MOSFET, also, the bottom JFET $J_1$ (cf. Fig. 1) is conducting, since its gate is connected to its source via the MOSFET, i.e., $V_{\mathrm{gs},J_1} = 0$, and the JFET is a normally on device. Also, the second JFET $J_2$ is conducting since, first, the potential of the cathode of $D_1$, which is connected to the gate of $J_2$, could not be much lower than the diode forward voltage drop $V_F$ (given in the data sheet) with respect to the anode of $D_1$. Second, the source of $J_2$ is connected to the anode of diode $D_1$ via the turned-on JFET $J_1$ and the turned-on low-voltage MOSFET. Consequently, the gate voltage of $J_2$ must be higher than $-V_F$, which is above the threshold voltage of $J_2$ ($V_{\mathrm{th}} \approx -20$ V), so

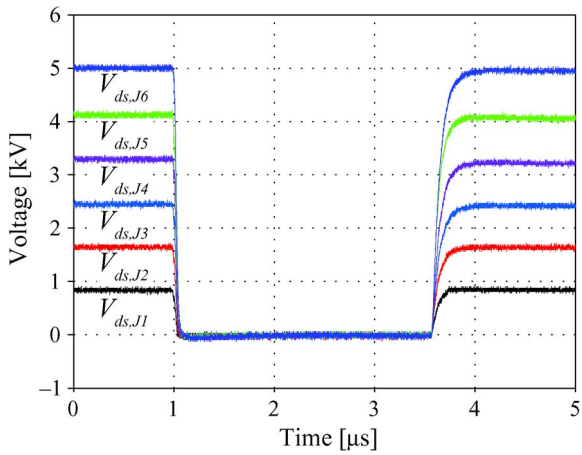


Fig. 2. Measured voltage distribution across the JFETs of the super cascode caused by the avalanche voltage of the gate diodes.

that $J_2$ is definitely turned on, assuming a zero voltage drop across $J_1$ and the MOSFET in a first step.

In a real circuit, the gate voltage of $J_2$ is in between $-V_F$ and $V_{F,J_G}$, which is the forward voltage of the gate diode of the JFET, depending on the leakage current distribution in the JFETs and diodes. In order to reduce the dependence of the gate voltage on the leakage currents, additional elements are needed as will be discussed in the next section.

The gate of the third JFET $J_3$ is connected via $D_1$ and $D_2$ to the source of the MOSFET; therefore, the lower limit of the gate voltage is given by $2 \times V_F$, and the upper limit is given by the forward voltage of the gate diode $V_{F,J_G}$, assuming again that there is no voltage drop across the MOSFET, $J_1$, and $J_2$. Similar considerations can be performed for the upper JFETs.

For turning the cascaded switch off, first, the MOSFET is turned off via its gate, and the drain–source voltage of the MOSFET rises until the pinchoff voltage of $J_1$ is reached. Then, $J_1$ turns off and blocks the rising drain–source voltage of the super cascode until the avalanche voltage of diode $D_1$ is reached. Due to the avalanche of diode $D_1$, the potential of the gate of $J_2$ is fixed with respect to the source of the super cascode and does not rise anymore. However, the potential of the source of $J_2$ continues to rise with the increasing drain–source voltage of $J_1$, so that the gate–source voltage of $J_2$ becomes negative and turns off as soon as its pinchoff voltage is reached. This sequential turnoff, which can be seen in Fig. 2, continues with the next JFETs until the blocking voltage is reached.

### B. Static Off Behavior

After the sequential turnoff, the static voltage distribution in the OFF state (cf. Fig. 2) is mainly determined by the avalanche voltage of diodes $D_1, \ldots, D_5$. For a controlled and stable avalanche, i.e., for a controlled static voltage distribution, a certain leakage current through the diodes is required [8]. In order to guarantee this leakage current independent of the JFET parameters, resistors must be connected between the gate and the source of the upper JFETs as shown in Fig. 3. With the resistors, the leakage current is mainly defined by the resistance

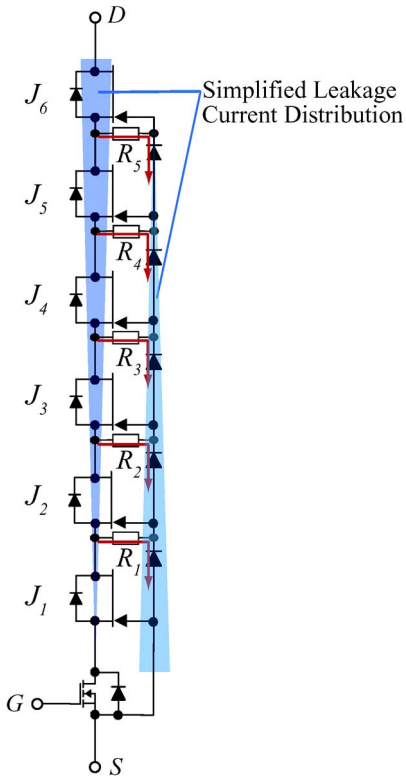


Fig. 3. Leakage current distribution in the SiC super cascode with additional balancing resistors for static off behavior.

value and the JFET's pinchoff voltage, which is equal to the voltage drop across the resistor in the OFF state [9], [10].

By inserting the resistor, also, a kind of control loop of the voltage distribution in the OFF state is initiated (cf. Fig. 3). In this case, for example, $J_2$ tends to turn off a bit more, i.e., increasing its drain–source voltage and/or resistance, the leakage current through $J_2$ would decrease. With the reduced leakage current through $J_2$, also, the current through resistor $R_1$, which flows via the voltage balancing diodes to ground, would decrease if it is assumed that the leakage current through $J_1$ is constant. This results in a reduced voltage drop across resistor $R_1$. Consequently, the gate–source voltage of $J_2$ decreases, so that $J_2$ is turning on a bit, which increases the leakage current through $J_2$ and stabilizes the gate–source voltage, as well as the drain–source voltage, of $J_2$. This control mechanism leads to a stable leakage current through the resistors and the diodes, so that the voltage sharing between the devices is stabilized by the avalanche voltage of the diodes, which determine the gate potentials of the JFETs.

The leakage current for the lower JFETs flows via the upper JFETs, so that the current in the JFETs decreases from the upper to the lower one and the current in the voltage balancing diodes increases from the upper to the lower one, as symbolized by the triangular arrows in Fig. 3. Additionally, with the resistors, a reliable switching-off operation is achieved, where the lowest diode reaches its avalanche voltage first, and therefore, the blocking voltage is built up from the lower to the upper JFET, since the lower diode must always conduct the leakage current of the upper ones. This stabilizes the turnoff switching transition.

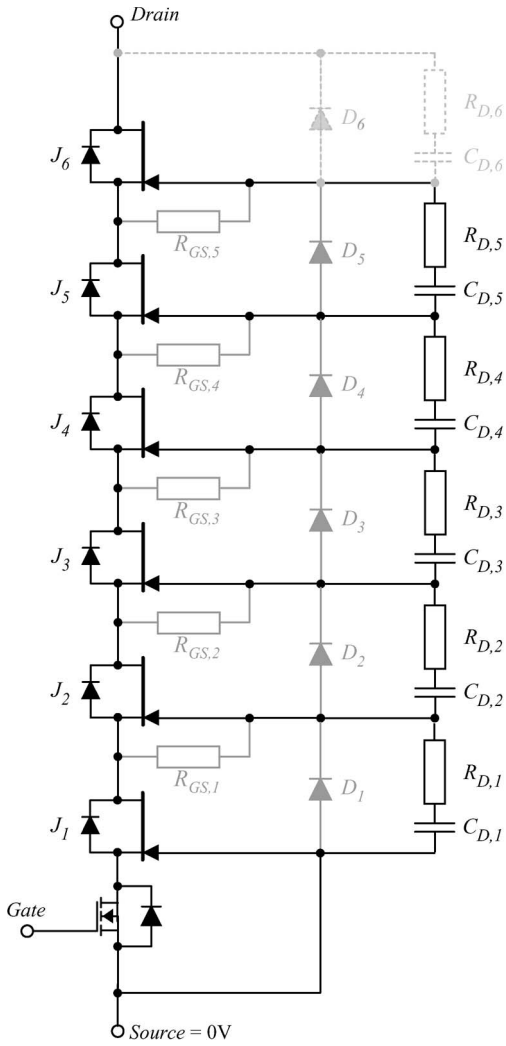


Fig. 4. Auxiliary resistors $R_{D,1}, \ldots, R_{D,6}$ and capacitors $C_{D,1}, \ldots, C_{D,6}$ for dynamically balancing the voltage distribution of the JFETs.

### C. Transient Behavior

In Section II-A, which is about the basic operation principle, a sequential turn-on process of the JFETs in the super cascode has been described. Such a sequential turn-on could result in overvoltages of the upper JFETs, particularly, for example, in the case of hard commutation of a diode in a bridge leg. There, first, the current must be commutated from the diode to the super cascode before the voltage could decrease, so that in a sequential turn-on, the most upper JFET would have to take the full blocking voltage for a short period of time. In order to avoid the overvoltages and achieve a synchronization of the JFETs during the switching transients, capacitors $C_{D,1}, \ldots, C_{D,5}$ and resistors $R_{D,1}, \ldots, R_{D,5}$ are added as shown in Fig. 4.

Starting in the OFF state and assuming a relatively small resistance value for $R_{D,1}, \ldots, R_{D,5}$ and that capacitors $C_{D,1}, \ldots, C_{D,5}$ are equally charged up, the MOSFET is turned on by a positive gate voltage. As described earlier, the potential of the source of $J_1$ and the gate voltage of $J_1$ is decreasing, so that $J_1$ starts to conduct when the gate voltage is close enough to 0 V. As soon as $J_1$ starts to conduct, the potential of the source of $J_2$ decreases. However, due to capacitor $C_{D,1}$, the

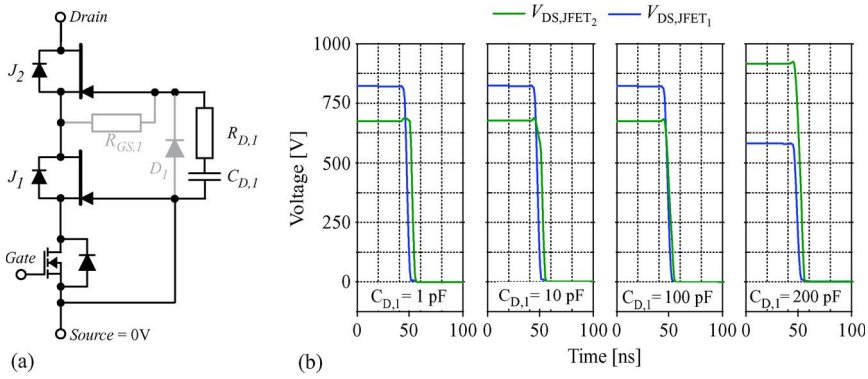


Fig. 5. (b) Drain–source voltages of the two JFETs in the super cascode in (a) for different values of the auxiliary capacitor $C_{D,1}$ ranging from 10 to 200 pF ($R_{D,1} = 50\ \Omega$, $R_{\mathrm{GS},1} = 240\ \mathrm{k}\Omega$, and $V_{\mathrm{dc}} = 1.5$ kV).

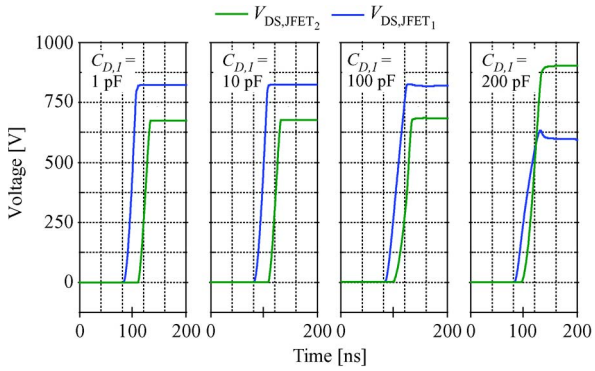


Fig. 6. Drain–source voltages of the two super cascode JFETs in Fig. 5(a) for different values of the auxiliary capacitors $C_{D,1}$ and $C_{D,2}$ ranging from 10 to 200 pF ($R_{D,1} = 50\ \Omega$, $R_{\mathrm{GS},1} = 240\ \mathrm{k}\Omega$, and $V_{\mathrm{dc}} = 1.5$ kV).

potential of the gate of $J_2$ is fixed for a limited time, so that the gate voltage of $J_2$ starts to increase as soon as the potential of the source starts to decrease. This means that $J_2$ starts to turn on as soon as $J_1$ is turning on, resulting in a synchronous switching of both JFETs. Analogue considerations can be performed for the upper JFETs.

In Fig. 5, a simulation of the drain–source voltages of a super cascode consisting of one MOSFET and two JFETs for different values of capacitor $C_{D,1}$ ranging from 10 to 200 pF is shown. There, it can be seen that, with increasing capacitance value, both JFETs tend to turn on more synchronously. Resistor $R_{D,1}$ in series to $C_{D,1}$ is added for damping oscillations during the switching transients. With $C_{D,1} \geq 100$ pF, the two JFETs turn on at the same time as can be seen in Fig. 5(b).

Looking at Fig. 5, it seems that a larger capacitance value for $C_{D,\nu}$ results in more synchronous switching transients. However, at turnoff, a too large value for $C_{D,\nu}$ results in a more synchronous switching operation but an unbalanced voltage distribution as can be seen in Fig. 6. The reason for this is that, at the beginning of the turnoff, the capacitors are discharged, so that they hold the gate potential of $J_2$ down. When $J_1$ now starts to turn off, the gate voltage of $J_2$ immediately becomes negative and turns off $J_2$ faster than $J_1$, so that $J_2$ is blocking the largest share of the voltage. With increasing $C_{D,\nu}$, first, the turnoff becomes more synchronous, and then, $J_2$ tends to take a larger share of the voltage than $J_1$, as can be seen in Fig. 6.

The parasitic capacitances of the balancing diodes $D_1, \ldots, D_5$ have a similar influence on the switching transients as capacitors $C_{D,1}, \ldots, C_{D,5}$. However, the value of the capacitance changes with the voltage across the diode, and it is the smallest, when the diode is in avalanche. Thus, the effect on turn-on is much smaller (where a large capacitance value is advantageous) than the effect on turnoff, where the capacitance value is maximal, but a small capacitance would be good. Therefore, it is difficult to achieve an optimal transient performance just with the parasitic capacitance of the diodes, and adding $C_{D,1}, \ldots, C_{D,5}$, as well as $R_{D,1}, \ldots, R_{D,5}$, is proposed in order to fully utilize the performance of the JFETs. For achieving an optimal transient behavior, i.e., fast and synchronous turn-on and turnoff, a tuning of the capacitors/resistors is required. This results in decreasing capacitance values from $C_{D,1}$ to $C_{D,5}$ as, also, the leakage current is smaller for the upper JFETs.

In order to make the super cascode more robust against tolerances, diode $D_6$ and/or capacitor $C_{D,6}$ and resistor $R_{D,6}$, as shown gray shaded in Fig. 4, can be added. The upper capacitor $C_{D,6}$ mainly leads to a more balanced voltage distribution for capacitors $C_{D,1}$ to $C_{D,5}$ as the circuit acts as a dynamic voltage divider. With diode $D_6$, a similar stabilization could be achieved, but also, the maximal blocking voltage of the super cascode is fixed to $6 \times V_{\mathrm{Avalanche}}$.

## III. Measurement Results

For investigating the switching behavior of the super cascode in detail, a half bridge with two switches consisting of a MOSFET and six cascaded SiC JFETs as shown in the schematic in Fig. 7 has been designed (cf. Fig. 8). In the following sections, the test platform with the components used and the measurement results obtained are discussed.

### A. Test Platform

For the gate drive of the super cascode, a standard 9-A gate driver from IXYS is used to drive the MOSFET with a gate voltage of $+12$ V/$-12$ V. The gate signal is transferred via fiber optics, and the gate power is transferred via a small HV transformer. For minimizing the stray inductance of the setup, ceramic capacitors mounted closely to the JFETs are applied

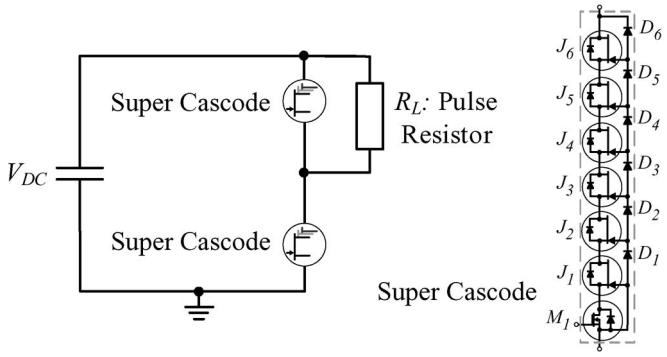


Fig. 7. Schematic of the measurement setup for the SiC super cascode, where the auxiliary components are not shown for the sake of simplicity.

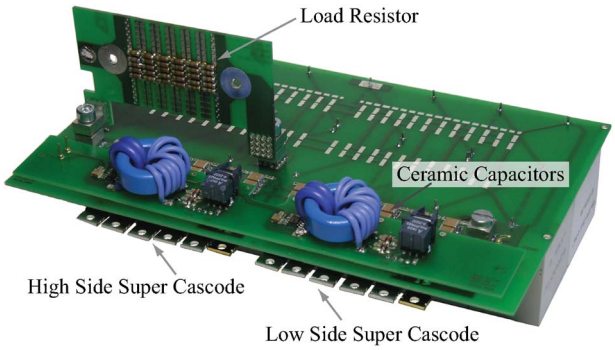


Fig. 8. Photograph of the measurement setup for the SiC super cascode (size: 155 mm × 170 mm × 50 mm/load: 90 mm × 50 mm × 5 mm).

besides the film capacitors. The load consisted of eight series-connected pulse resistors made by Vishay.

For the voltage balancing diodes, which require a stable avalanche voltage in order to guarantee a well-defined static and dynamic voltage distribution of the super cascode, a series connection of three fast-recovery rectifier diodes BZT03C270 made by Vishay is used. These diodes show a stable avalanche behavior at 270 V. In order to simplify the design, a single diode with an avalanche voltage of ≈0.8 kV would be required, but unfortunately, such devices were not available. Moreover, one has to consider that the parasitic capacitance of the single diode would be higher than the one of the series connection.

### B. Measurements

With the test benches for the super cascode, measurements of the switch voltage and the load current for a purely resistive load have been performed. The maximal load current for the super cascode is limited to approximately 6 A due to the relatively small chips, which are available at the moment, and due to the unipolar device characteristic. This characteristic leads to a pinchoff of the conducting channel as known from the MOSFET, if the current is too high.

The results for the super cascode are shown in Fig. 9, where it can be seen that the 90%–10% rise time of the voltage is significantly smaller than 50 ns. The fall time is also in the range of 100 ns, but depending significantly on the load current as shown in Fig. 10, since the cascode turns off very fast and then the $dv/dt$ is only determined by the output capacitance and the load current charging the capacitor.

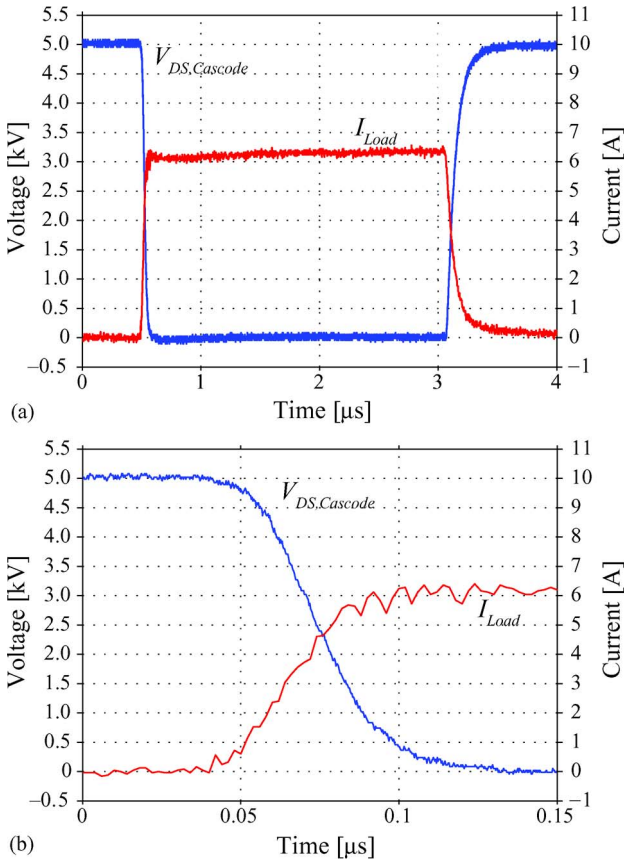


Fig. 9. (a) Measurement results for the super cascode with a gate voltage of 12 V and an 800-Ω purely resistive load. (b) Zoomed view around turn-on.

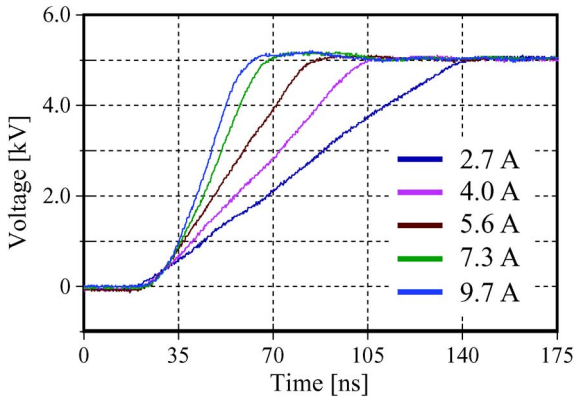


Fig. 10. Rising edge of the voltage pulse during turnoff of the super cascode for different load currents from 2.7 to 9.7 A and inductive load.

In Fig. 11, a comparison of the turn-on behavior of the super cascode with and without the auxiliary circuit given in Fig. 4 is shown. There, it can be seen that the switch turns on much faster with the auxiliary circuit—particularly at the end of the turn-on transient. Finally, in Fig. 12, results for a double-pulse measurement are shown, which demonstrate the superior performance of the super cascode.

## IV. Conclusion

In this paper, the basic operating principle of a super cascode based on 1.2-kV SiC JFETs and a low-voltage Si MOSFET

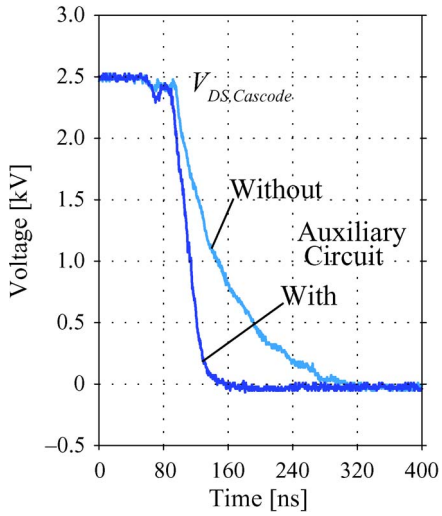


Fig. 11. Comparison of the super cascode turn-on behavior with and without the auxiliary circuit given in Fig. 4.

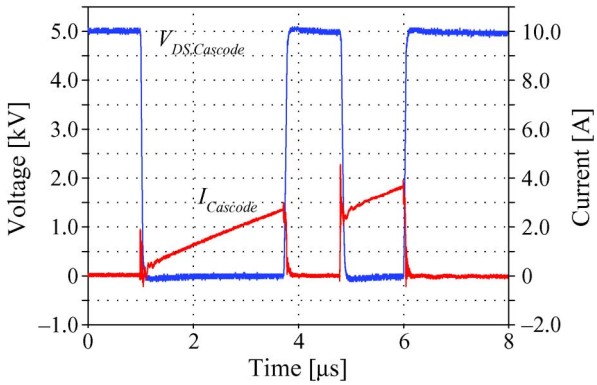


Fig. 12. Double-pulse measurement results for the super cascode with a gate voltage of 12 V, an inductive load of 5.6 mH, and the following: MOSFET: IRLR024N, balancing diodes: BZT03SERIES, $R_{GS,1},\ldots,R_{GS,5} = 240\,\text{k}\Omega$, $C_{D,1},\ldots,C_{D,5} = (76, 66, 55, 33, 15)$ pF, $R_{D,1},\ldots,R_{D,5} = 50\ \Omega$, and $R_G = 30\ \Omega$.

TABLE I
COMPONENTS AND SYSTEM PARAMETERS OF THE TEST BENCH FOR THE SUPER CASCODE WITH A DC-LINK VOLTAGE OF 5 kV

| | |
|---|---|
| SiC JFETs | 1.2kV / 5A (TO220/SiCED) |
| Si-MOSFET | IRLR024N / 55V ($D^2$-Pak) |
| Balancing Diodes | 3×BZT03C270 / 3×270V |
| Load Resistors | CMB0207 100Ω (Vishay) |
| DC-Link capacitor | ICEL $8\mu F/800V_{DC}$ (7×2)<br>Syfer 500V/560nF/X7R (12×2) |
| DC-Link Voltage | 5000V |
| Gate Driver | IXYS IXDI 9A / 35V |
| Pulsed Power | 5kV × 6A = 30kW |

has been presented. Here, also, the requirement for additional gate–source resistors/capacitors for guaranteeing a stable static voltage distribution and damping internal oscillations has been explained. Furthermore, an $R$–$C$ network for improving the dynamic behavior and the voltage balancing of the super cascode have been presented (Table I).

For evaluating the switching performance of the super cascode, measurements for a resistive load with a pulse voltage of 5 kV and a load current of 6 A have been performed. The rise time of the switch voltage is significantly below 50 ns, which is very fast. The falling edge of the output pulse is also in the range of 100 ns but depends significantly on the load current/load resistor, which charges the output capacitor of the super cascode.

## ACKNOWLEDGMENT

The authors would like to thank the ABB Corporate Research Center, Baden-Dättwil, Switzerland, for supporting research on future SiC power semiconductor applications.

## REFERENCES

[1] M. Giesselmann, B. Palmer, A. Neuber, and J. Donlon, "High voltage impulse generator using HV-IGBTs," in *Proc. IEEE Pulsed Power Conf.*, Jun. 2005, pp. 763–766.

[2] *QIS4506002 Datasheet, High-Voltage Discrete IGBT Module*, Powerex, Inc., Youngwood, PA. [Online]. Available: http://www.pwrx.com/

[3] J. Biela, D. Aggeler, D. Bortis, and J. W. Kolar, "5 kV/200 ns pulsed power switch based on SiC-JFET super cascode," in *Proc. IEEE Int. Power Modulator Conf.*, Las Vegas, NV, May 27–31, 2008, pp. 358–361.

[4] J. Biela, *SiC JFETs Based Switches & Applications*. [Online]. Available: http://www.acreo.se/Global/Meet-us-at/2009/SiC-090331/3-Juergen_Biela-100ns_super_cascode_high_power_switch_module.pdf

[5] CREE, *Power Product Specifications*, 2011. [Online]. Available: www.cree.com

[6] Infineon, *SiC Products*, 2011. [Online]. Available: www.infineon.com/sic/

[7] R. L. Kelley, M. Mazzola, S. Morrison, W. Draper, I. Sankin, D. Sheridan, and J. Casady, "Power factor correction using an enhancement-mode SiC JFET," in *IEEE PESC/IEEE Power Electron. Spec. Conf.*, Rhodes, Greece, Jun. 15–19, 2008, pp. 4766–4769.

[8] R. Elpelt, P. Friedrichs, R. Schorner, K. Dohnke, H. Mitlehner, and D. Stephani, "Serial connection of SiC VJFETs—Features of a fast high voltage switch," *REE. Revue de l'Electricite et de l'Electronique*, pp. 60–68, 2004.

[9] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage 25 kW, 50 kHz DC–DC converter based on SiC JFETs," in *Proc. IEEE APEC*, Feb. 2008, pp. 801–807.

[10] D. Aggeler, J. Biela, and J. W. Kolar, "Controllable du/dt behavior of the SiC MOSFET/JFET cascode an alternative hard commutated switch for telecom applications," in *Proc. 25th IEEE APEC*, Feb. 2010, pp. 1584–1590.

[11] N. Mohan, T. Undeland, and W. P. Robbins, *Power Electronics-Converters, Applications, and Design*, 3rd ed. Hoboken, NJ: Wiley, 2003.

**Juergen Biela** (S'04–M'06) received the Diploma (with honors) from Friedrich-Alexander Universität Erlangen–Nürnberg, Nuremberg, Germany, in 1999 and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2006.

During his studies, he dealt in particular with resonant dc-link inverters at the University of Strathclyde, Glasgow, U.K., and the active control of series-connected IGCTs at the Technical University of Munich, Munich, Germany. In 2000, he joined the Research Department, Siemens A&D, Erlangen, where he worked on inverters with very high switching frequencies, SiC components, and EMC. In July 2002, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, for working toward his Ph.D. degree, focusing on optimized electromagnetically integrated resonant converters. From 2006 to 2007, he was a Postdoctoral Fellow with PES and a Guest Researcher with the Tokyo Institute of Technology, Tokyo, Japan. From 2007 to mid-2010, he was a Senior Research Associate with PES. Since August 2010, he has been an Associate Professor in high-power electronic systems with ETH Zurich. His current research is focused on the design, modeling, and optimization of PFC, dc–dc and multilevel converters with emphasis on passive components, the design of pulsed-power systems, and power electronic systems for future energy distribution.

**Daniel Aggeler** (S'07–M'10) received the M.Sc. degree in electrical engineering and information technology and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2006 and 2010, respectively.

Since January 2010, he has been with the Power Electronics System Group, ABB Corporate Research Center, Baden-Dättwil, Switzerland. His current research interests are in the areas of medium-voltage power converters, high-frequency and high-voltage dc–dc converter systems, and concepts using wide-band-gap semiconductors as SiC.

**Dominik Bortis** (S'06–M'09) was born in Fiesch, Switzerland, on December 29, 1980. He received the B.Sc. degree in electrical engineering and the M.Sc. and Ph.D. degrees from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2005 and 2008.

During his studies, he majored in communication technology and automatic control engineering. During his diploma thesis, he worked with Levitronix, where he designed a galvanic isolation system for analog signals. Since 2008, he has been a Postdoctoral Fellow with the Power Electronic Systems Laboratory, ETH Zurich.

**Johann W. Kolar** (M'89–SM'02) received the Diploma degree in industrial electronics and the Ph.D. degree (*summa cum laude*) from Vienna University of Technology, Vienna, Austria.

From 1984 to 2001, he was with the Vienna University of Technology, where he was teaching and working in research in close collaboration with industry. He has proposed numerous novel converter topologies, e.g., the Vienna rectifier and the three-phase ac–ac sparse matrix converter concept. On February 1, 2001, he was appointed Professor and Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland. He has published over 300 scientific papers in international journals and conference proceedings and has filed more than 75 patents.