Life-Cycle Carbon Footprints of Low-Voltage Motor Drives with 600-V GaN or 650-V SiC Power Transistors

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Abstract

Based on a multi-objective Pareto optimization of efficiency, power density, and carbon footprint, we present a comparative evaluation of currently available 600-V GaN and 650-V SiC transistors in 400-V dc variable-speed drives (VSDs) with LC output filter for standard 3-hp motors in variable-load centrifugal systems like pumps. Interestingly, we do not identify significant performance differences between GaN-based and SiC-based VSDs. However, equipping a fixed-speed motor with a VSD reduces the average drive system losses and hence the life-cycle carbon footprint by up to 90%, which—complementing the NEMA Power Index (PI)—is captured by a proposed Loss Reduction Index (LRI).

1 Introduction

Driven by, first, the need for limiting global warming by the end of the 21st century to +1.5 °C above pre-industrial levels, and, second, by the awareness of limited availability of natural resources, i.e., critical minerals (with often geopolitically constrained access due to geographically concentrated sourcing and processing), there is a multitude of governmental/regulatory, industrial, and academic initiatives targeting not only energy efficiency but also material efficiency, Ecodesign, and ultimately a future circular economy. Being a key enabling technology for the efficient use of (electrical) energy, these concepts are also applied to power electronics. There, and in general, the quantification of environmental impacts of products and services by means of life-cycle assessments (LCAs, e.g., according to ISO 14040 and ISO 14044) is a prerequisite for Ecodesign [1, 2] and circular-economy compatibility [3–5]. Recently, ever more power-electronics-related LCA studies are being published by academia and industry, e.g., [3, 6–17]; we provide a more detailed discussion in [5].

In this context, motor-driven applications are of particular interest, as 45% of all electrical energy used worldwide is transformed to mechanical work by electrical motors [18]; in manufacturing plants, values as high as 80% are reached [19]. Further, depending on the industry, variable-load centrifugal systems like pumps, fans, or compressors, account for 34% to 44% of the motor electricity consumption, but less than 50% down to as little as 6% are equipped with a variable-speed drive (VSD) [19] as indicated in **Fig. 1a**—even though the characteristic quadratic torque-speed relationship shown in **Fig. 1b** (i.e., the power-speed relationship follows an affinity law with $P \propto \omega^3$) facilitates significant energy savings by adapting the motor speed depending on the load instead of operating a fixed-frequency motor from the mains at rated power while adapting the mechanical output power to the load by means of valves or dampers.

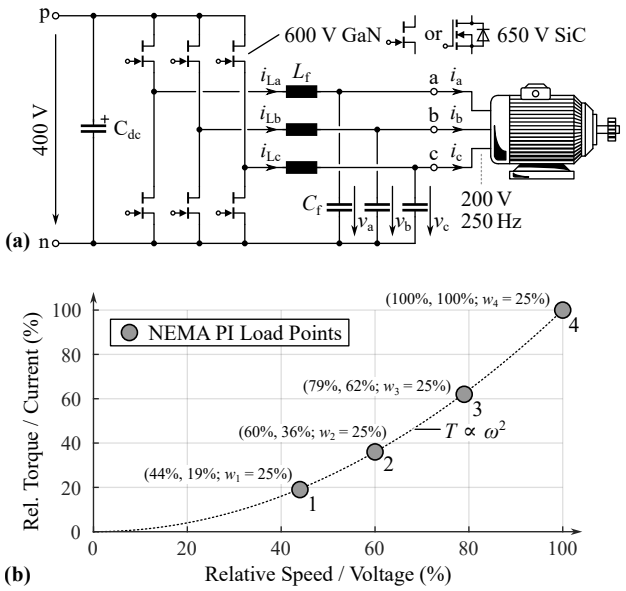

Figure 1 **(a)** Power circuit of the considered VSD inverter with a dc-link-referenced LC output filter that provides differential-mode (DM) and common-mode (CM) attenuation, i.e., smooth sinusoidal motor voltages; **Tab. 1** lists the key specifications. **(b)** Characteristic torque-speed (current-voltage) load points used by the NEMA Power Index (PI) [20] for variable loads with quadratic torque-speed characteristics like pumps, fans, and compressors; w_i denotes the weighting factor of load point i.

Drawing on IEC 61800-9-1/2 which defines Ecodesign guidelines and calculation/measurement procedures for energy efficiency indicators of power drive systems, NEMA (National Electrical Manufacturers Association) standard MG 10011-2022 [20] introduces the Power Index (PI) as a straightforward way of quantifying the reduction in energy consumption achieved by adding a VSD to a *typical* variable-load application. To do so, the standardized load profile (based on empirical data) indicated in **Fig. 1b** is em-

Table 1 Key specifications of the drive system from **Fig. 1a**.

Description	Symbol	Value	Unit
Nominal motor power	$P_{\mathrm{mot,N}}$	3	hp
Nominal inverter power	$P_{\mathrm{inv,N}}$	2.5	kW
Input dc voltage	V_{dc}	400	V
Motor voltage (l-l rms)	V_{M}	0 ... 200	V
Motor current (rms)	I_{M}	0... 7.2	A
Motor el. frequency	f_{M}	0 ... 250	Hz

ployed; further aspects are discussed below and interested readers consult [19] for extended explanations. Even though the system-level energy savings achieved by implementing speed control via a VSD are expected to be significantly larger than differences between VSD realizations, it is still interesting and necessary to systematically and comprehensively analyze the VSD design trade-offs, in particular with a focus on environmental impacts.

This paper does so considering an exemplary low-voltage VSD inverter[1] with a 400-V dc input voltage as shown in **Fig. 1a** with key specifications from **Tab. 1**; such low-power VSDs are widely used in applications like white goods, air conditioners, etc. Today, typically Si IGBTs are employed, whose relatively slow switching speeds ($dv/dt \leq 5\,\mathrm{kV/\mu s}$) are compatible with motor isolation systems. If, instead, wide-bandgap (WBG) transistors are used, the much higher dv/dt of their switching transitions requires filtering to prevent damage of standard motor isolation systems, but also to mitigate reflections and voltage overshoots on long motor cables and EMI issues as well as bearing currents [21]. On the other hand, the fast switching capabilities of WBG transistors facilitate low switching losses and hence high switching frequencies, which in turn results in comparably small LC output filters with low losses [22, 23]. Further, with a dc-link-referenced LC filter as shown in **Fig. 1a** present, smooth sinusoidal voltages are provided to the motor, which, first, enables the use of standard motors, and, second, avoids harmonic losses in the motor. As independently demonstrated in [22] and [24], GaN-based VSDs with 100 kHz switching frequency and LC output filter realize clear system-level (inverter and motor) efficiency improvements compared to IGBT-based VSDs without filter.

An inverter with a dc input voltage of 400 V requires transistors with a voltage rating of 600 V to 650 V. In this voltage class, two different WBG materials can be employed—SiC and GaN—which, according to [25], outperform each other depending on the operating conditions (switching frequency, temperature, etc.). Therefore, **Section 2** first provides a device-level comparison of exemplary commercially available SiC and GaN transistors for the considered VSD power rating in an idealized half-bridge configuration. Then, **Section 3** addresses the system level, i.e., the VSD inverter including the dc-link-referenced LC output filter, by means of a multi-objective Pareto optimization with a special focus on including not only classical performance metrics like efficiency (weighted according to the NEMA PI load profile from **Fig. 1b**) and power density but also the environmental impact (specifically, the carbon footprint or global warming potential, GWP) as proposed in [5, 17]. **Section 4** concludes the paper and discusses future developments: Since we consider commercially available devices and given the limited availability of environmental impact data for power electronic components [5, 9], the presented analysis must be read as a snapshot of the current state of affairs, which will change with technological progress and improvement of industrial manufacturing processes, as well with the availability of more accurate data.

[1] Strictly speaking, a VSD in the context of the NEMA PI includes a grid interface; however, in the interest of a clarity, we do consider only the inverter stage, to which we refer by the term "VSD" in the following; the grid interface could be included in the presented analysis in the future but likely without changing the outcome in a relevant way.

2 Device-Level Comparison

Basic material parameters [28] such as electron mobility and critical electrical field strength suggest advantages of GaN over SiC transistors (see also **Section 4**). However, the authors of [25] introduce a new figure of merit that represents the minimum theoretical semiconductor losses in hard-switching applications to compare currently available SiC and GaN devices in the 600-V/650-V voltage class: no clear winner could be identified; depending on the operating conditions, either GaN transistors perform better (lower operating temperatures, higher switching frequencies) or SiC transistors show advantages (higher operating temperatures, lower switching frequencies). Therefore, following the snapshot approach mentioned in the introduction, we consider two exemplary commercially available SiC and GaN transistors for an initial device-level comparison in this section, and later as the basis of a system-level comparative evaluation in **Section 3**.

2.1 Performance Characteristics

Fig. 2a shows the on-state resistance, R_{on}, versus junction temperature, T_{j}, characteristics of a 55-mΩ, 600-V GaN HEMT (Infineon IGOT60R070D1 in a top-cooled PG-DSO-20-87 SMD package) and of a 27-mΩ, 650-V SiC MOSFET (Infineon IMZA65R027M1H in a TO-247-4 package). A parallel connection of two GaN transistors shows the same on-state resistance as one SiC transistor at room temperature ($T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$). Note the much stronger temperature-dependency of the GaN transistor's on-state resistance which approximately doubles when increasing the junction temperature from $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$ to $T_{\mathrm{j}} = 125\,^{\circ}\mathrm{C}$. **Fig. 2b** presents calorimetrically measured switching loss data from [26] for the GaN transistor and from [27] for the SiC transistor, and linear fits. Being measured, the loss data includes contributions from parasitic capacitances of the PCB layout and of the load inductor, which are present in real-world applications and tend to penalize GaN transistors more than SiC transistors due to the former's lower stored charge in the device output capacitance, C_{oss}.

Next, we employ the idealized half-bridge circuit shown in **Fig. 2c** to evaluate the dependency of the semiconductor losses on the switching frequency and the load current, considering two parallel GaN transistors,, i.e., GaN and SiC solutions with equal nominal on-state resistance at room temperature. The half bridge operates with sinusoidal PWM, a modulation index of $M = 0.8$, and an ideal (ripple-

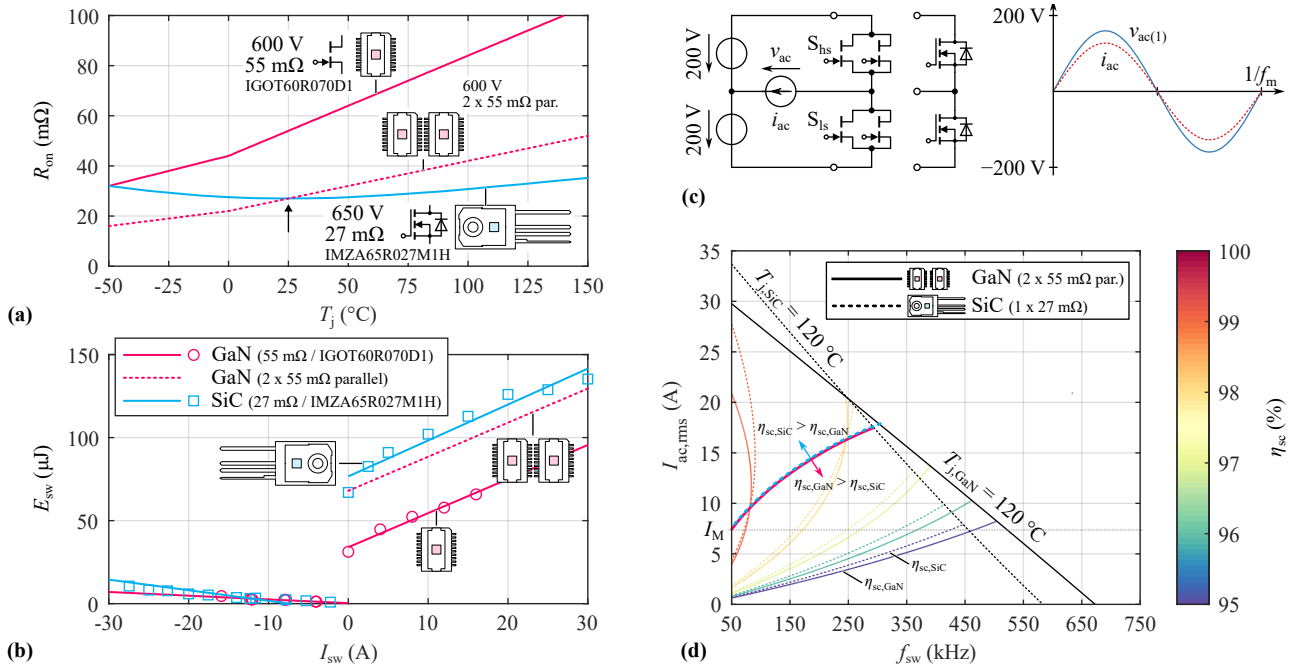

Figure 2 Performance evaluation of two exemplary commercially available 600-V/650-V GaN/SiC transistors, i.e., a 55-mΩ GaN e-mode HEMT (IGOT60R070D1) and a 27-mΩ SiC MOSFET (IMZA65R027M1H). **(a)** $R_{ds,on}(T_j)$ from the device datasheets; note that two parallel 55-mΩ GaN transistors result in equal $R_{ds,on}(T_j = 25\,°C)$ as a single 27-mΩ transistor. **(b)** Calorimetrically measured hard-switching (HS) and soft-switching (SS) losses (from [26] for the 55-mΩ GaN and from [27] for the 27-mΩ SiC transistor) and linear fits. **(c)** Simplified half-bridge evaluation circuit with ideal sinusoidal switch-node current (zero current ripple) and **(d)** resulting semiconductor efficiency η_{sc} in dependence of switching frequency, f_s, and output current, $I_{ac,rms}$, for realizations with either one 27-mΩ SiC transistor or two parallel 55-mΩ GaN transistors (solutions with equal nominal R_{on} at room temperature, see (a)) and a constant heatsink temperature of $T_{hs} = 80\,°C$. Note that the semiconductor efficiency contours of the two realization options are close, in particular for the nominal motor current of $I_M = 7.2$ A considered here.

free) in-phase ac load current. Further, assuming a fixed heatsink temperature of $T_{hs} = 80\,°C$ and a typical thermal impedance of about $0.3\,K\,in^2/W$ of the case-to-heatsink interface, the device junction temperatures are obtained by taking into account the temperature-dependency of the on-state resistance in an iterative manner.[2]

Under these side conditions, **Fig. 2d** shows the semiconductor efficiency contours ($\eta_{sc} = 1 - (P_{cond} + P_{sw})/P_{out}$) with P_{cond} and P_{sw} referring to the conduction and switching losses of the entire half bridge) for a range of switching frequencies, f_{sw}, and rms ac load currents, $I_{ac,rms}$, as well as the limiting curves where the device junction temperature reaches 120 °C (leaving some margin with respect to the maximum ratings). Consistent with the findings from [25], the GaN-based solution performs better at higher frequencies and lower currents, whereas the SiC-based solution performs better at lower frequencies and higher currents. The boundary between the two regions shifts when changing the underlying assumptions (e.g., if the number of parallel GaN transistors would be selected such that it shows equal on-state resistance as the SiC device at $T_j = 100\,°C$). The key conclusion is therefore of a qualitative nature: the differences in semiconductor efficiency between the GaN-based and the SiC-based solution are not large, particularly in the power (current) range considered here, and for practical switching frequencies below 200 kHz.

Note that the scaling the GaN transistors' chip area (through paralleling) such that the on-state resistance equals that of the SiC transistor at room temperature is arbitrary and not necessarily the optimum; in general, the chip area (number of parallel transistors) is a degree of freedom for optimizing the semiconductor losses for a given combination of load current and switching frequency. This is, of course, considered in the system-level multi-objective optimization discussed below in **Section 3**, which does not identify significant differences in performance of GaN-based and SiC-based VSD inverter realizations.

2.2 Carbon Footprints

The availability of reliable data on the embodied environmental burden of components used in power electronic converters in general, and of power semiconductors in particular, is scarce [5, 9]. To still estimate the carbon footprint, i.e., the global warming potential (GWP) measured in kilograms of CO_2-equivalent greenhouse gas emission, of a given GaN or SiC transistor, we rely on GWP per chip area values reported in recent literature and summarized in **Tab. 2**. These values include the wafer production and front-end processing, which are the most energy-intense manufacturing phases; the package is neglected (unless gold bond wires are used [16], which can be substituted by, e.g., copper, its impact is comparably small [17]).

The ecoinvent LCA database [30] provides chip-area-

[2] Note that we do not consider the temperature dependency of the reverse-recovery charge in case of the SiC MOSFET [29], as it is assumed to have comparably little effect on the overall switching losses at moderate switched currents, as typically given for high efficiencies.

Table 2 Employed values for GWP per chip area of Si, SiC, and GaN transistors[3] with sources (minor deviations for Si and SiC from these references due to newer version of underlying ecoinvent database and rounding; GaN scenario assumptions see text).

	Si	SiC	GaN
kg CO_2eq/m^2	28'000	91'000	27'000
Source	[9]	[9]	[16]

specific GWP data for Si MOSFETs, which [9] uses to derive a value for SiC by scaling the contribution of the substrate/wafer processing by a factor of 80 (higher energy demand due to higher required temperatures [12, 31]) and assuming equal contributions of the front-end processing.

The chip-area-specific GWP data for GaN is taken from [16], which reports a detailed LCA for GaN transistors based on data from a CEA-LETI's R&D clean room. From the different scenarios presented in a sensitivity analysis, we select a combination assuming the presence of gas abatement systems, global electricity mix, and a yield of 75%; this is then similar to the assumptions underlying the SiC data from [9].

The discussed GaN and SiC transistors feature about the same chip size. Hence, the solutions with equal nominal on-state resistances at $T_j = 25\,°C$ compared in **Fig. 2d** come with GWP footprints of 1.3 kg CO_2eq (two parallel GaN transistors) and 2.1 kg CO_2eq (one SiC transistor) per half bridge. It is important to highlight that these are coarse (yet currently the only possible) estimates due to the limited availability of reliable environmental impact data from suppliers. Further, because the energy consumption accounts for a large share of a power semiconductors' GWP (and other environmental impacts), the values vary strongly with the GWP-intensity of the energy/electricity mix used during production and hence with the geographic location of the manufacturing plant.

3 System-Level Comparison via Multi-Objective Optimization

As indicated above, a fair comparative evaluation of the performance limits achievable with GaN-based and SiC-based LV VSDs must include the entire inverter system, i.e., in particular also the output LC filter, and explore all relevant degrees of freedom (DOF). This is achieved by a multi-objective Pareto optimization, which essentially maps each feasible combinations of design DOFs—points in a multidimensional *design space*—into the *performance space* using component and system models [32]. The boundary curve or (hyper-) surface of the reachable subspace of the performance space is called the Pareto front. Typically, the performance dimensions considered are efficiency and power density. Here, we include the weighted efficiency corresponding to the NEMA load profile discussed in **Section 1** and shown in **Fig. 1b**, and, in particular, the GWP as one example of an environmental impact indicator that can and should be considered in the early design stages [5].

[3]Note that these are generic values and not specific to the devices considered in **Fig. 2** and for the Pareto optimization (listed in **Tab. 3**).

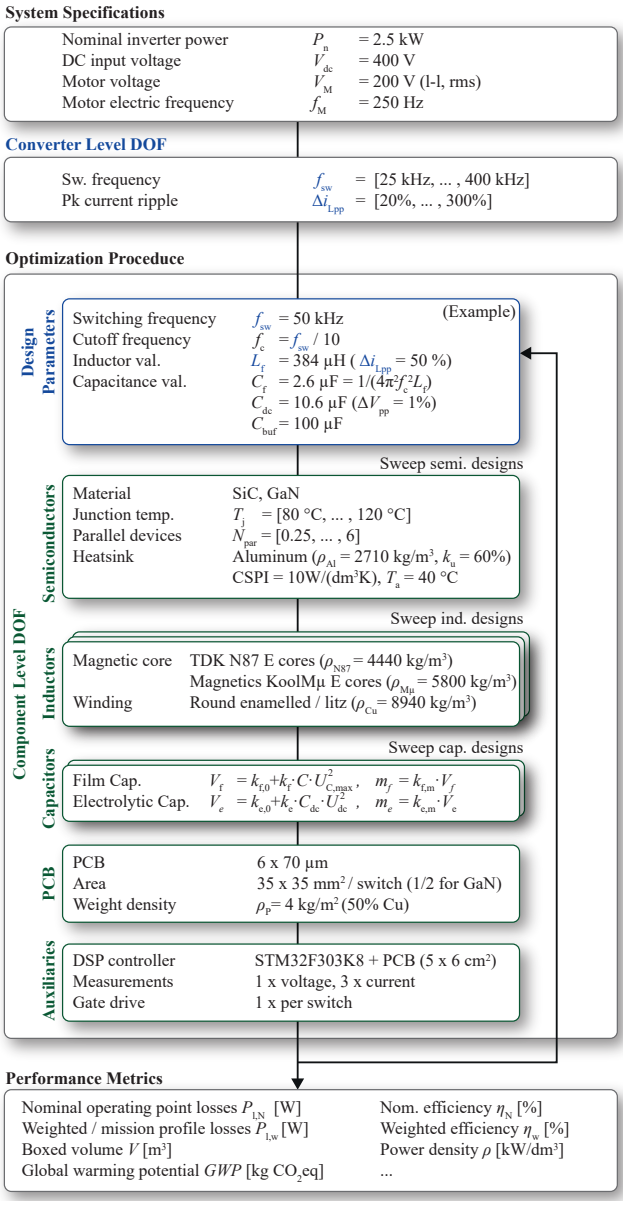

Figure 3 Flowchart of the multi-objective optimization routine implemented in MATLAB, which is an adaption of [17].

3.1 Multi-Objective Optimization Framework

The implemented optimization frameworks is best explained following the flowchart shown in **Fig. 3**. Note that we have discussed further details and the employed component models, etc. earlier in [17]; therefore, and for the sake of brevity, only salient aspects are repeated here.

3.1.1 System Model

First, the optimization is executed once for GaN-based and once for SiC-based VSDs with the same specifications from **Tab. 1**. On the system level, there are two main degrees of freedom (in addition to selecting the semiconductor technology): the switching frequency, f_{sw}, and the filter inductor current ripple, $\Delta i_{L,pp}$, which are varied over wide ranges. For a given combination (f_{sw}, $\Delta i_{L,pp}$), the routine designs the LC output filter by selecting the cutoff frequency

Table 3 Transistors considered in the optimization.

Mat.	V_{ds}, R_{on}	Manuf.	Model	E_{sw}
GaN	600 V, 55 mΩ	Infineon	IGOT60R070D1	[26]
GaN	600 V, 37 mΩ	Infineon	IGOT60R042D1	[33]
SiC	650 V, 27 mΩ	Infineon	IMZA65R027M1H	[27]

as $f_c = 0.1 \cdot f_{sw}$, which implies an attenuation of the switching-frequency content of the switched voltage by −40 dB or a residual peak-to-peak high-frequency voltage ripple at the output of about 2%. Designs with $f_c < 10 \cdot f_{M,N}$ and/or with a maximum reactive filter capacitor current exceeding $2 \cdot I_M$ are discarded.

A next step calculates the idealized electrical waveforms of one fundamental period at the nominal operating point, where (for the considered load profile) the highest component stresses occur.[4] For simplicity, we consider unity power factor only (which is approximately achieved for permanent-magnet synchronous machines), i.e., we model the motor as a resistive load. The electrical waveforms define the component stresses needed for exploring the component-level DOF.

3.1.2 Component Models

Transistors: As mentioned above in **Section 2**, transistor conduction losses are modeled based on datasheet values and switching losses based on calorimetrically measured data available in the literature (see **Tab. 3**). The chip area is an important device-level DOF that adjusts the trade-off between conduction and switching losses; therefore, the number of parallel-connected transistors, N_{par}, is varied (including fractional $N_{par} < 1$, which corresponds to—typically available—transistors with higher R_{on} than the considered baseline devices). Further, different design junction temperatures are considered; lower temperatures facilitate lower losses but will be penalized by larger heatsink volumes. Note that, whereas the junction temperature is fixed for the design and then the heatsink volume selected accordingly, an iterative electro-thermal model is used to calculate the junction temperature and the temperature-dependent on-state resistance when evaluating part-load operating points later. The transistors contribute to the GWP footprint of a design as discussed above in **Section 2.2**.

Heatsink: The thermal interface between transistors and heatsink considers mounting conditions and a thermal interface material (TIM) such that a typical thermal impedance of about 0.3 K in^2/W results. The required volume of the heatsink then follows from the design junction temperature, the semiconductor losses, an ambient temperature of $T_a = 40\,°C$, and a cooling-system performance index [34] of $CSPI = 10\,W/(dm^3K)$. Assuming a fill factor of $k_u = 60\%$ to account for the fins, the heatsink's GWP contribution follows from the aluminum mass.

Filter inductors: The variety of component-level DOF like core material (N87, KoolMmicro), core size, winding (litz/solid wire), etc. are explored using the design tool presented in [35]. The inductors' GWP contribution follows from the mass of core material and copper used.

Capacitors: The ac-side filter capacitors (with values given by the filter cutoff frequency and the filter inductor value defined by the design's current ripple specification) and the dc-link capacitor (for a max. high-frequency peak-to-peak ripple of 1%) are modeled via typical volumetric energy densities of commercially available film capacitors; on the dc-side, a bulk electrolytic capacitor is considered similarly. The losses of the film capacitors are modeled via $\tan\delta = 0.001$ and are typically very small. The GWP contributions are based on literature as detailed in [17].

PCBs and Auxiliary Components: The power PCB area follows from the number of parallel transistors and the package sizes. Assuming a 6-layer stack with 70 µm copper layers, a typical weight density has been empirically established and is used to estimate the PCB weight and ultimately its contribution to the GWP [17]. The control PCB is treated similarly, but a fixed area is assumed. The control circuitry consists of one gate driver per transistor, current and voltage sensors, and a DSP (in all cases, typical ICs and a typical population of SMD resistors and capacitors is considered). The GWP contributions are then obtained from the weight-specific data from the ecoinvent database [30] and other literature as detailed in [17]. Note that the GWP contribution of these auxiliary components can be surprisingly large [9].

3.1.3 Performance Evaluation

Finally, the optimization routine recombines all feasible component realizations for a given combination (f_{sw}, $\Delta i_{L,pp}$) to obtain a set of converter realizations; the process is then repeated for all other (f_{sw}, $\Delta i_{L,pp}$) combinations. Then, only converter realizations that do not overstress any component at any of the three remaining characteristic load points of the considered load profile are retained. For each valid converter realization, characteristic performance metrics are calculated: nominal efficiency η_N, boxed volume V (taking into account 50% air between components) and power density ρ, and the overall GWP footprint as the sum of the component's GWP contributions; note that we do not consider any housing of structural elements here.

Finally, targeting applications with variable loads following the affinity law, a weighted efficiency η_w and weighted relative losses ψ_w are calculated using the NEMA PI load profile [20] shown in **Fig. 1b**, i.e.,

$$\eta_w = \frac{\sum_i w_i P_{inv,i}}{\sum_i w_i (P_{l,inv,i} + P_{inv,i})} \text{ and } \psi_w = \frac{\sum_i w_i P_{l,inv,i}}{\sum_i w_i P_{inv,i}}, \quad (1)$$

which relate the (weighted) average losses to the (weighted) average output power of the inverter; the weighting factors of the four load points are $w_i = 0.25\ \forall\ i$ (see **Fig. 1b**).

Thus, the optimization routine ultimately generates two sets of possible converter designs—GaN-based or SiC-based—utilizing the full ranges of all relevant DOF. Each design corresponds to a point in the (here) three-dimensional performance space: nominal or weighted efficiency, $\eta_{N/w}$, power density, ρ, (or, equivalently, nominal or weighted relative losses, $\psi_{N/w}$, and volume V), and GWP; therefore, those designs that offer the best possible trade-offs among the three performance dimensions span a three-dimensional Pareto surface.

[4] In contrast, in servo drives, operating points at full torque but (almost) zero speed/voltage could be critical regarding the thermal design.

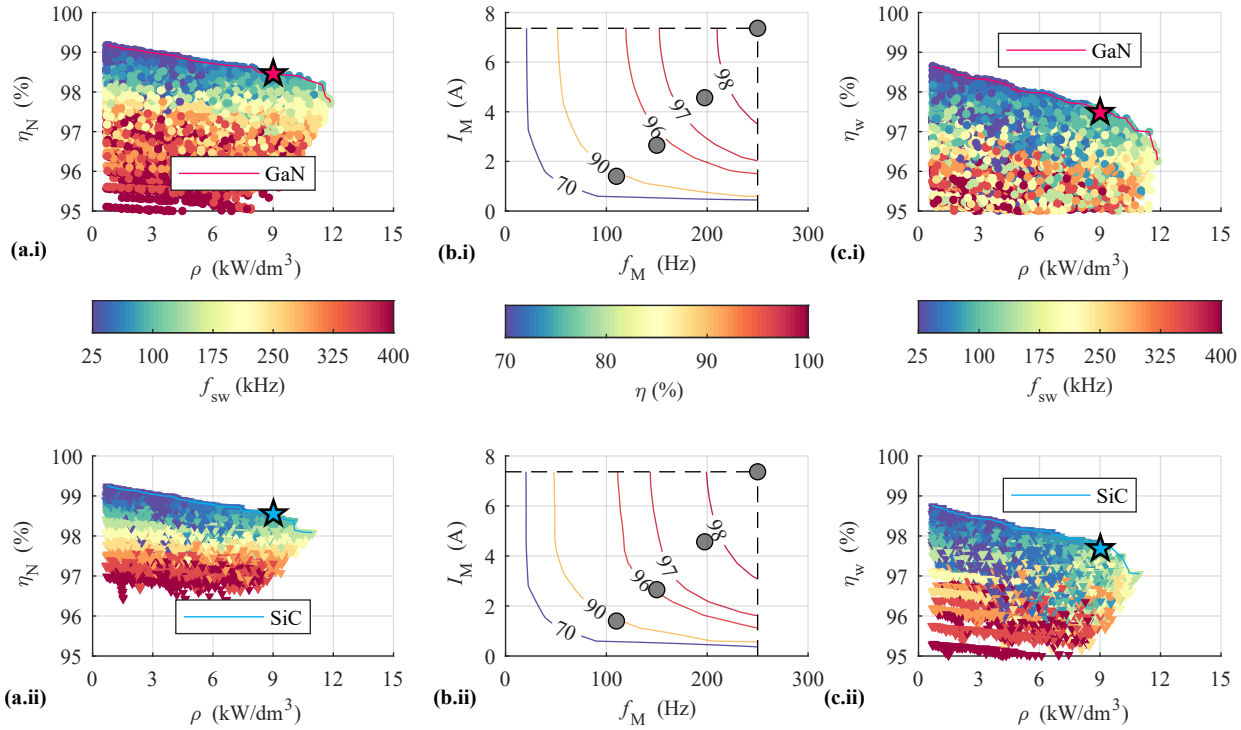

Figure 4 From efficiency to weighted efficiency for **(x.i)** GaN-based and **(x.ii)** SiC-based designs. **(a)** η_N-ρ performance space and **(b)** efficiency contours of exemplary designs wit η_N = 98.5% on the Pareto fronts in (a). The characteristic NEMA PI load points (see **Fig. 1b**) used for obtaining the weighted efficiency η_w according to (1) are highlighted, and **(c)** shows the resulting η_w-ρ performance space; note that the exemplary designs are now slightly behind the new $\eta_w\rho$-Pareto front.

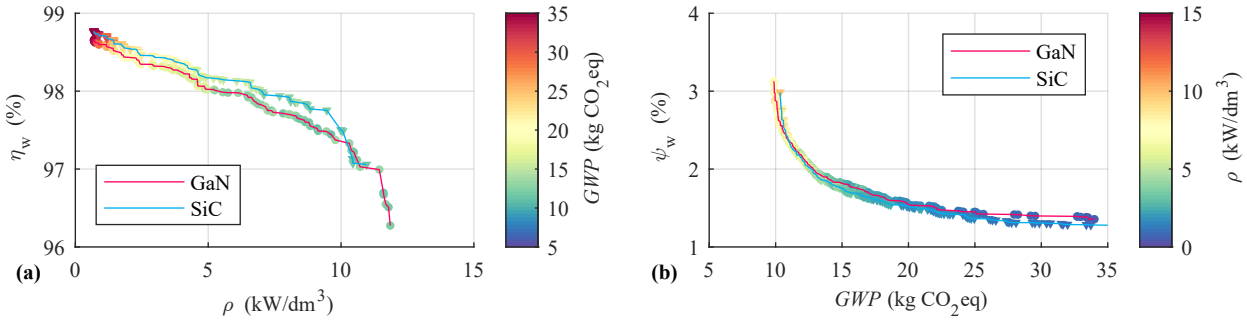

Figure 5 Pareto fronts of GaN-based and SiC-based designs with respect to **(a)** weighted efficiency η_w and power density ρ, and **(b)** weighted relative losses ψ_w and global warming potential, GWP, i.e., the embodied carbon footprint.

3.2 Multi-Objective Optimization Results

Fig. 4a shows the projection of all designs onto the η_N-ρ plane and the corresponding efficiency-vs.-power-density Pareto fronts for GaN-based and SiC-based designs. High efficiency implies low switching frequencies and high compactness (high power density) implies high switching frequencies but, alas, higher losses, which explains the typical negative slope of these Pareto fronts. Taking an exemplary Pareto-front design with η_N = 98.5%, **Fig. 4b** shows the efficiency characteristics over the entire speed-torque (voltage-current) range; clearly, the efficiency for some of the NEMA PI load profile operating points is relatively low. Therefore, weighted efficiencies $\eta_w < \eta_N$ result in **Fig. 4c**.[5] Note that the designs that were on the η_N-ρ Pareto fronts are now slightly behind the η_w-ρ Pareto fronts, although not far (this is understandable since in absolute terms, the nominal operating point at full load contributes heavily to the average losses in (1)). Interestingly, the clear trend of how the switching frequency modifies the trade-off between η_N and ρ is less pronounced if the weighted efficiency η_w is considered instead.

[5]It is important to highlight again the definition of η_w in (1): η_w is *not* the average of the efficiencies at the four operating points but the average efficiency of the load profile—these two values differ because the base values, i.e., the output power, of the four operating points is not equal.

3.2.1 Comparative Evaluation

Finally, **Fig. 5** provides the targeted comparison of the performance limits of GaN-based and SiC-based designs. **Fig. 5a** shows the η_w-ρ Pareto fronts and **Fig. 5b** compares the ψ_w-GWP Pareto fronts. The color scales encode the respective third performance dimension, i.e., GWP in (a) and ρ in (b); indicating, e.g., that designs with high volume tend to have a high GWP. Clearly, in (a) and (b), the two Pareto fronts essentially overlap or are at least so close that the differences must be considered to lie within the ultimately limited accuracy of the employed models, in particular regarding GWP.

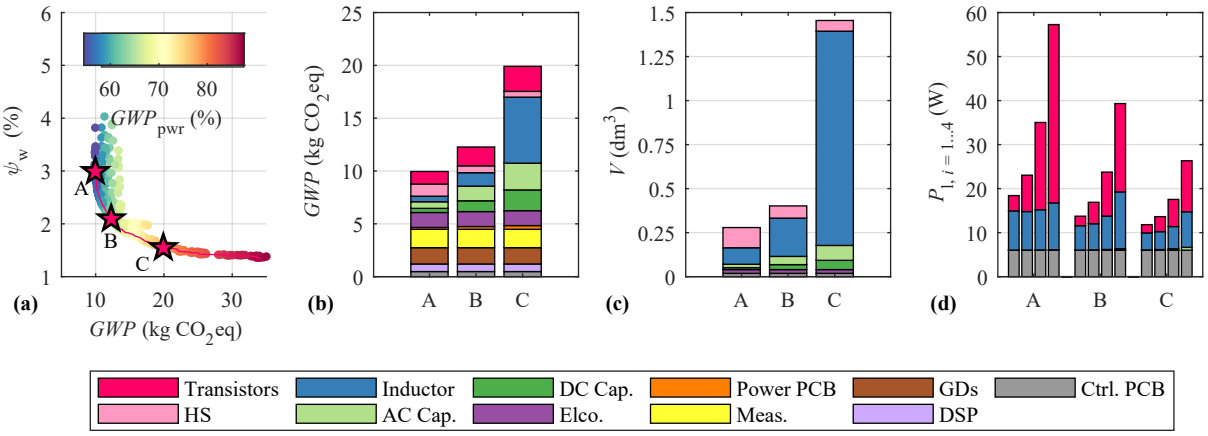

Figure 6 Details of GaN designs. **(a)** ψ_w-GWP-Pareto front with all designs that are on the ψ_w-GWP-V-Pareto *surface* which is projected on the ψ_w-GWP-plane; the color scale indicates the power stage's share of the overall GWP. For three highlighted designs, **(b)** shows GWP breakdowns, **(c)** volume breakdowns, and **(d)** loss breakdowns at the four NEMA PI load points. Designs A and B are selected with $\psi_w = 3\%$ and $\psi_w = 2\%$, respectively, and design C with $GWP = 20\,\mathrm{kg\,CO_2eq}$.

Given the similar performance of GaN-based and SiC-based designs, **Fig. 6** shows further details for GaN-based designs only. Interestingly, for designs with low GWP, the power stage only accounts for about half of the carbon footprint (see **Fig. 6a**), i.e., the auxiliary electronics become limiting,[6] which is also illustrated by the GWP breakdown of design A **Fig. 6b**. In contrast, the low-loss design C has a higher GWP, which is due to a larger contribution of the power stage. Note further that even though the filter inductors dominate the volume of design C (see **Fig. 6c**), their contribution to the GWP is less pronounced. The loss breakdowns for the four NEMA PI operating points (see **Fig. 6d**) illustrate again how the nominal-load operating point strongly influences the average losses, especially in compact designs (A) with consequently lower efficiency.

This is an example of the type of trade-off analyses enabled by multi-objective Pareto optimization; including environmental impacts such as GWP footprints in such optimization frameworks allows the designer to assess long-term environmental consequences in the early design stages—of course, the accuracy and trustworthiness of the results improves with more accurate models and, in particular, the availability of high-quality environmental footprint data for power electronic components.

3.2.2 NEMA Power Index

The inverter is part of a drive system that also includes a motor. The NEMA PI [20] has been introduced to quantify the reduction in energy consumption achieved by equipping a motor with a VSD in a typical variable-load applications with a quadratic torque-speed relationship [19]. Essentially, the PI is defined as

$$PI_{\mathrm{vl}} = 100 \cdot \left(1 - \frac{\sum_i w_i P_{\mathrm{in},i}}{0.9 \cdot P_{\mathrm{in,baseline}}}\right) \approx 100 \cdot \left(1 - \frac{\sum_i w_i \left(P_{\mathrm{mot},i} + P_{\mathrm{l,mot},i} + P_{\mathrm{l,inv},i}\right)}{0.9 \cdot \left(P_{\mathrm{mot,N}} + P_{\mathrm{l,mot,N}}\right)}\right), \quad (2)$$

[6]This limitation depends on the rated power, i.e., for inverters with higher power rating, the contribution of the auxiliary electronics can be expected to be less pronounced.

Table 4 Ranges of the NEMA PI and of the proposed LRI for all designs on the respective Pareto surfaces; with variable load profile and default motor from [20].

	SiC VSDs	GaN VSDs
Power Index, PI_{vl}	46.0. . . 47.2	45.7. . . 47.1
Loss Reduction Index, LRI_{vl}	85.7. . . 87.5	85.4. . . 87.4

where the nominator is the weighted average input power of the drive system considering the four NEMA PI load points for variable load[7] shown in **Fig. 1b**, and $P_{\mathrm{in,baseline}}$ is the input power of the baseline fixed-frequency motor running at rated power. Then, $P_{\mathrm{in},i}$ can be calculated with the useful motor output power, $P_{\mathrm{mot},i}$, (matching the load), the loss characteristics of a default motor, $P_{\mathrm{l,mot},i}$, defined in the standard [20], and the weighted losses of each inverter design obtained from the optimization routine.[8]

Fig. 7a and **Tab. 4** illustrate that the resulting PI_{vl} values (index $_{\mathrm{vl}}$ for "variable load") do not vary significantly between different designs. A $PI_{\mathrm{vl}} \approx 46$ implies that the energy consumption of the system with VSD is only about 54% of the baseline without VSD, i.e., that the overall energy consumption reduces by about 46% if the designed VSD is added. For comparison, the considered variable load profile results in a theoretical maximum $PI_{\mathrm{vl}} \approx 50.3$ when assuming an ideal (lossless) VSD and a lossless motor; including the losses of the default motor puts the maximum for an ideal VSD at $PI_{\mathrm{vl}} \approx 47.8$. This highlights that the PI mostly depends on the (load-profile-specific) ratio of average useful (mechanical) power required by the load to the average motor power, which is greatly improved by implementing controllability of the motor by adding a VSD; the PI does then not strongly vary with VSD efficiencies.

[7]Note that [20] defines two load profiles, for variable load and for constant load, with different w_i; throughout this article, we only consider the former (variable load) for the sake of brevity.

[8]Strictly speaking, the VSD includes also a grid-side rectifier stage, which is neglected here; assuming the same loss characteristics as for the inverter, i.e., using $2P_{\mathrm{l,inv},i}$ instead of $P_{\mathrm{l,inv},i}$ in (2), the PI values would reduce from about $PI_{\mathrm{vl}} \approx 46$ to $PI_{\mathrm{vl}} \approx 45$.

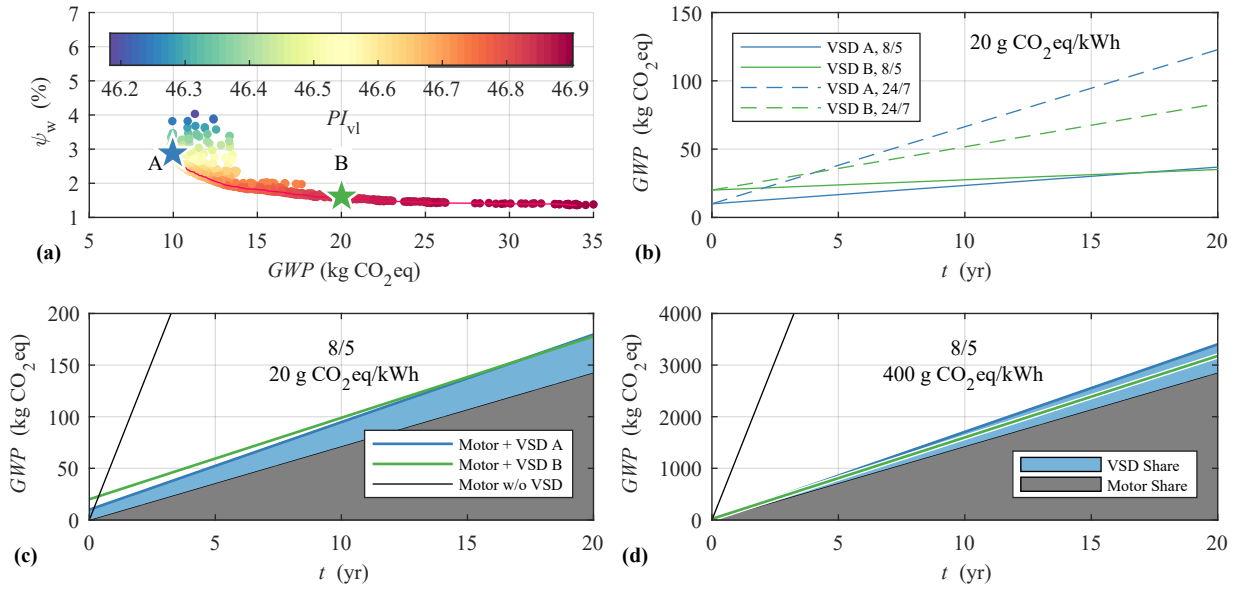

Figure 7 **(a)** GaN designs on the ψ_w-GWP-V-Pareto surface which is projected ψ_w-GWP-plane; the colors indicate the NEMA Power Index for variable loads, PI_{vl} [20]. **(b)** Accumulation of GWP during the use phase for the two designs highlighted in (a), considering a green electricity mix (20 g CO_2eq/kWh, roughly corresponding to the renewable share of the power generation in Switzerland [30]) and two scenarios (8 h on 5 d and 24 h on 7 d per week). **(c)** As in (b), but including the loss contributions of a default motor defined in [20]. **(d)** As in (c), but considering a fossil-fuel dominated electricity mix (400 g CO_2eq/kWh, roughly corresponding to the German consumption mix [30].)

3.2.3 Use-Phase Emissions and Loss Reduction Index

As $\eta_w < 100\%$, any VSD design dissipates part of the electrical energy input when in operation. Depending on the geographic location, electricity is generated from a varying combination of fossil, nuclear or renewable sources and hence each kWh of electricity comes with a certain impact on the environment; carbon intensity measured in g CO_2eq/kWh is the most prominent characteristic. Therefore, the energy losses during the use phase of the VSD increase the overall GWP footprint, which is illustrated in **Fig. 7ab** for two exemplary GaN-based designs A and B. Design A features a very low embodied GWP but relatively high weighted losses whereas design B shows opposite characteristics. Therefore, the slopes of the GWP accumulation during the use phase shown in **Fig. 7b** is lower for design B. Depending on the scenario (and the electricity mix), a break-even point is reached very quickly (high usage and/or electricity mix with high GWP intensity) or only towards the end of an assumed lifetime of 20 years (low usage and/or electricity mix with low GWP intensity). The use case and location are therefore important modifiers regarding the selection of a design with optimum/minimum life-cycle GWP footprint, which, for a specific scenario, could be included as performance dimensions of the multi-objective Pareto optimization [5].

Fig. 7cd show the evolution the overall GWP footprint of the drive system consisting of VSD A or B and the NEMA PI default motor defined in [20], considering two different electricity mixes. Note that the embodied GWP of the motor is not included, as it is a common offset to both VSD realizations. The differences between the VSD designs A and B even after twenty years of operation are relatively minor; still, the more efficient design B overcompensates its higher GWP offset quickly if the carbon intensity of the electricity mix is high (scenario from **Fig. 7d**); specifically, a system with VSD B saves 230 kg CO_2eq (or about 7%) compared to a system with VSD A after a lifetime of 20 years. On the other hand, **Fig. 7cd** also indicate very large emission savings of both variants compared to the baseline case of operating the motor *without* a VSD (i.e., at full power with mechanical valves or dampers to supply the varying load power); specifically, the system with VSD B saves 21 t CO_2eq in 20 years, or 87%, compared to the baseline without VSD.

The NEMA PI captures reductions in the system energy consumption (and hence in overall use-phase emission reductions), and therefore includes the useful (mechanical) power ultimately delivered to the load. Emissions associated with that share of the total input power, however, should not be assigned to the drive system's life-cycle GWP but to that of the load. Therefore, we propose complementing the NEMA PI by a *Loss Reduction Index* (LRI) defined as

$$LRI_{vl} = 100 \cdot \left(1 - \frac{\sum_i w_i \left(P_{l,mot,i} + P_{l,inv,i}\right)}{P_{l,mot,N}}\right), \quad (3)$$

which is essentially obtained from the PI by leaving out the mechanical load power terms, $P_{mot,i}$ or $P_{mot,N}$, in the nominator and the denominator of (2), respectively; further aspects like load profile variants, etc. could be defined like for the NEMA PI [20]. The LRI_{vl} is a measure for the expected *loss savings* achieved by equipping a motor with a VSD in the standard NEMA PI variable load application. Because the LRI focuses only on the drive system (VSD and motor) but excludes the load, it is a measure for the reduction of the drive system's use-phase GWP footprint. **Tab. 4** indicates that all GaN-based and SiC-based VSDs result in LRI values of around $LRI_{vl} \approx 86$, i.e., imply a 86% lower use-phase GWP footprint compared to the baseline

without VSD. These values show good correspondence to the relative emissions savings observed in the context of **Fig. 7d** above, even though the LRI_{vl} does not and cannot include the (embodied) GWP of the VSD designs, which is, however, typically very small compared to the use-phase emissions caused by the baseline motor without VSD even with green electricity mixes.

4 Conclusion

Low-voltage VSDs operating from a 400-V dc voltage can be realized with 600-V GaN or 650-V SiC transistors and should be equipped with an LC output filter for compatibility with standard motors. Considering the NEMA Power Index (PI) load profile for variably loaded centrifugal systems (pumps, fans), we have compared VSD inverter realizations based on commercially available SiC and GaN transistors by means of a comprehensive multi-objective Pareto optimization regarding weighted efficiency, power density, and embodied global warming potential (GWP) or carbon footprint. The Pareto fronts for GaN-based and SiC-based VSDs are found to be very close, i.e., within the expected modeling accuracy; in particular given the high uncertainty and scarce availability of accurate GWP data for components of power electronic systems.

Whereas the presented comparison method, which, in particular, includes GWP as an exemplary environmental performance indicator, is universal, the specific results must be understood as a snapshot of current commercially available technology. As indicated by **Fig. 8**, the specific on-state resistance of SiC MOSFETs is close to the theoretical limit, whereas there is significantly more room for improvement for currently available lateral GaN transistors. E.g., multi-channel GaN technology with multiple, stacked 2D electron gas channels [36] or vertical GaN transistors [37] promise significant reductions of specific on-state resistances, which would translate into lower chip area for given current and hence lower GWP values. Further, industry provides favorable cost projections for GaN transistors [31]. On the other hand, technological progress in SiC manufacturing promises up to 70% reduction of CO_2 emissions associated with the energy-intense wafer manufacturing through reuse of substrates [38].

Taking a life-cycle perspective, adding a VSD to a motor greatly reduces the energy consumption of a typical pump application (or similar), which is captured by the NEMA PI, but also reduces the share of *wasted* electricity even more. Therefore, inspired by the NEMA PI, we introduce the Loss Reduction Index (LRI) that captures the power/energy *loss* reduction and hence directly the reduction of carbon emissions associated with the electricity mix used to cover the losses. Almost irrespective of the VSD realization, a significantly lower life-time GWP footprint results compared to the baseline scenario with a fixed-speed motor without VSD; in other words, the VSD's embodied GWP footprint is quickly offset during the use phase, i.e., the GWP payback time for adding a VSD to a typical pump application (or similar) is very short even in a scenario with relatively low usage and green electricity mix.

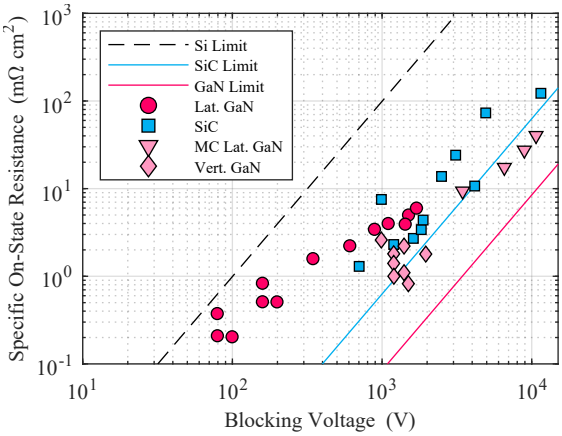

Figure 8 Theoretical limits of specific on-state resistance and blocking voltage for unipolar vertical Si, SiC and GaN devices, with reported values highlighted (data extracted from [28, 37, 39–41]; MC: multi-channel). Note that existing SiC devices approach the theoretical limit even at relatively low blocking voltages, whereas commercially available lateral GaN devices are still comparably far from the limit.

There is a clear need to include performance metrics like GWP footprint in multi-objective optimizations carried out in the early concept or design phases of power electronic systems to allow the designer to make informed choices regarding the life-cycle environmental impacts. A key challenge in doing so is the very limited availability of accurate data [5, 9]. Ideally, component suppliers would gather and publish environmental impact footprints in a standardized manner (to ensure comparability) as part of future (smart/digital) datasheets. The presented multi-objective optimization framework is capable of considering further environmental impact indicators like damage to human health or resource depletion [5, 17], and should be extended to include, e.g., (life-cycle) cost, resource usage, and reliability/lifetime estimations as, e.g., a longer lifetime might justify a higher embodied GWP footprint. Further, aiming for compatibility with a future circular economy, aspects such as repair, reuse and recycling should be addressed by future VSD or, in general, power electronic converter designs.

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