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Analysis of Low Frequency Grid Current Harmonics Caused by Load Power Pulsation in a 3-Phase PFC Rectifier

J. Böhler,
F. Krismer,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Julian Böhler, Florian Krismer, and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich
Physikstrasse 3, 8092 Zurich, Switzerland
boehler@lem.ee.ethz.ch

***Abstract*—This paper investigates implications of Low-Frequency (LF) phase current distortions that emanate from a grid-connected three-phase PFC rectifier, which powers a single-phase load inverter via a common DC-link. The presented study reveals the computation of the grid-side distortions that result for LF operation of the load inverter and determines the limits of the allowable distortion currents imposed by relevant standards (IEC 61000-3-11 and IEC 61000-3-12 with regard to harmonic currents and flicker, respectively). In the course of a design example, a PFC rectifier with a rated power of 20 kW and a DC-link voltage of 700 V is examined and it is found that, in case of a strong grid with an inner impedance of 21 mΩ, full compliance with IEC 61000 is achieved with a DC-link capacitance of 27 mF. However, in case of a weak grid with an assumed inner impedance of 212 mΩ, a very high DC-link capacitance exceeding 50 mF would be required. In this case, the presented design procedure is rather used to identify the frequency-dependent power limitation characteristic that enables the implementation of deratings in critical frequency ranges.**

***Index Terms*—PFC, rectifier, grid current, harmonics, DC-link, capacitor, pulsating power, 3-phase, distortion**

I. Introduction

Due to the limited internal energy storage capability of a PFC rectifier, e.g., because of limited DC-link capacitance, grid current distortions occur if a power stage that is connected to the load-side of the PFC rectifier demands for a sinusoidal power waveform of adjustable amplitude, offset, and low frequency (here, frequencies less than 200 Hz are considered), since a substantial part of this fluctuating power may appear at the grid side. In this regard, different regulations exist, e.g., the IEC 61000 harmonic and flicker standards, which define limits for the maximum allowable levels of distortion.

A review of the current state-of-the-art reveals advanced concepts for the control and the operation of single-phase and three-phase PFC rectifiers, to achieve reduced grid current distortions. This includes the use of (self-tuning) notch filters [1]–[3], fuzzy controllers [4], adaptive PI-voltage controllers [5], the subtraction of a precalculated correction signal to reject the ripple voltage [6], and three-phase systems where the power fluctuations in the three different phases are phase-shifted by 120° [7]–[11]. However, the presented methods investigate power fluctuations with characteristic frequencies equal to twice the mains frequency or compensation mechanisms in three-phase systems, which, both, denote restrictions that cannot be transferred to the converter system investigated in the case at hand.

This paper presents a detailed analysis of the grid current disturbances and the identification of related design constraints for the DC-link capacitor of the system depicted in **Fig. 1(a)**. **Section II** details a calculation of the rectifier's grid current waveforms for sinusoidal load-side power levels, **Section III** summarizes the limitations set by the relevant IEC 61000 harmonic and flicker standards, and **Section IV** investigates the implications of the rectifier's controller settings on the obtained grid current waveforms. **Section V** combines the analytical findings to identify the frequency characteristic of allowable levels of output power, i.e., without violating the corresponding standards, and presents a dimensioning procedure for the DC-link capacitance of a PFC rectifier with a rated power of 20 kW. The derived analytical expressions are verified using the results of detailed circuit simulations.

II. Grid Current Waveforms

Fig. 1(a) depicts the circuit schematic of the considered three-phase PFC rectifier with grid-side boost inductors, L_b, a linear grid model, which is composed of three voltage sources with inner impedances, $\underline{Z}_\mathrm{g}$ (underlined designators denote

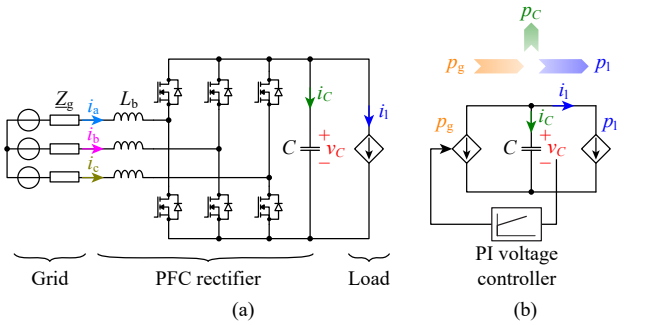

Fig. 1. (a) Schematic drawing of a two-level three-phase boost type PFC rectifier and (b) equivalent circuit illustrating the relations between instantaneous power levels at the DC side. The output load features a controlled-power sink characteristic, i.e., $p_\mathrm{l}(t)$ tracks a defined time-varying reference.

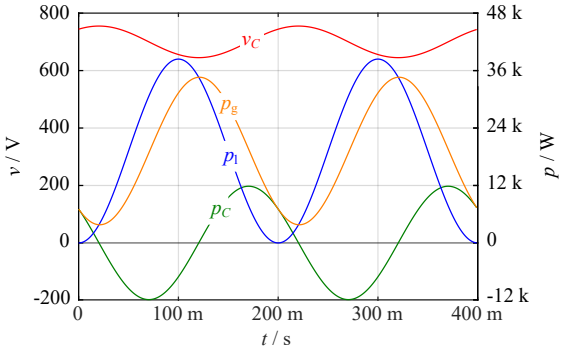

Fig. 2. Simulation waveforms of DC-link voltage, v_C, and instantaneous power levels, p_g, p_C, and p_l (cf. Fig. 1) for $C = 10\,\text{mF}$ and $p_l(t) = 20\,\text{kW}[1 - \cos(2\pi\,5\,\text{Hz} \times t)]$. Due to the low load frequency of 5 Hz and the specified maximum allowable amplitude of the DC-link voltage of 70 V, the energy storage capability of the DC-link capacitor is insufficient to cover the energy demand of the load and a high fluctuation of the power demand from the grid, p_g, results.

complex-valued variables), and the load. **Tab. I** lists the main system specifications.

The calculation of the PFC rectifier's grid current is based on the instantaneous value of the input power,

$$p_g(t) = p_C(t) + p_l(t), \tag{1}$$

where $p_C(t)$ is the instantaneous power of the DC-link capacitor,

$$p_C(t) = v_C\, C \frac{\mathrm{d}v_C}{\mathrm{d}t}, \tag{2}$$

and $p_l(t)$ the fluctuating, sinusoidal power demand of the load,

$$p_l(t) = P_0 - \hat{P}_l\, \cos(2\pi f_l\, t), \tag{3}$$

featuring DC bias, P_0, AC amplitude, $\hat{P}_l$, and frequency, f_l. The analysis further considers small-signal excitations at the DC-link and, in this regard, assumes a sinusoidal voltage ripple being superimposed on the DC-link voltage, $V_{C,0}$,

$$v_C = V_{C,0} + \hat{V}_C\, \cos(2\pi f_l t + \varphi_C), \tag{4}$$

with amplitude $\hat{V}_C$ and phase-shift φ_C, which will be determined using the transfer functions derived in Section IV for the controlled system. The frequency of the superimposed voltage ripple stems from the load power demand (3). **Fig. 2** provides an illustration of the above equations, using

$$\begin{aligned} &P_0 = \hat{P}_l = 20\,\text{kW}, \quad K_p = 0.586\,\text{A/V}, \quad T_i = 850\,\text{ms}, \\ &C = 10\,\text{mF}, \quad \hat{V}_C = 55\,\text{V}, \quad f_l = 5\,\text{Hz}, \quad \varphi_C = -36.7°, \end{aligned} \tag{5}$$

i.e., for a selected design, a defined voltage controller, and a typical operating point of the PFC rectifier.

Expressions (1) to (4) enable the derivation of the grid current i_d, which, in the synchronous dq reference frame, is

$$\begin{aligned} i_d = \frac{p_g}{\frac{3}{2}\,v_d} = \frac{2}{3v_d}\big[&P_0 - \hat{P}_l \cdot \cos(2\pi f_l t) \\ &- V_{C,0}\,\hat{V}_C\,2\pi f_l C\, \sin(2\pi f_l t + \varphi_C)\big], \end{aligned} \tag{6}$$

if the second-order terms are neglected that arise in the course of the evaluation of (2); v_d denotes the amplitude of the grid voltage in dq-coordinates. **Fig. 3(a)** depicts the corresponding

TABLE I
SPECIFICATIONS OF THE PFC RECTIFIER.

Parameter	Value
Grid voltage amplitude (phase-to-neutral), v_d	$\sqrt{2} \times 230\,\text{V}$
Grid frequency, f_g	50 Hz
DC-link voltage, $V_{C,0}$	700 V
Nominal output power, P_{nom}	20 kW
Output frequency, f_l	DC to 200 Hz
Maximum voltage ripple, $\hat{V}_{C,max}$	70 V (10 % $V_{C,0}$)
Boost inductance, L_b	1.63 mH
Switching frequency, f_s	20 kHz

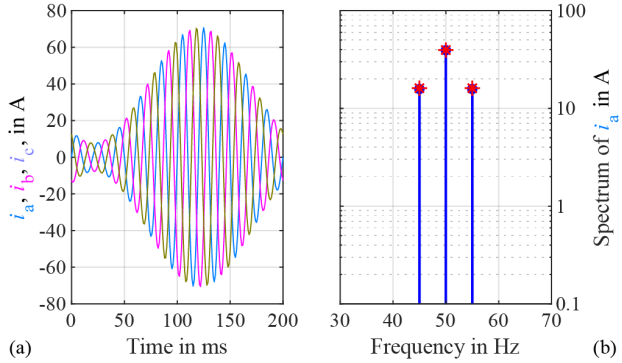

Fig. 3. (a) Simulated grid-side phase currents and (b) corresponding amplitude spectrum of each phase (same spectra result for all three phases; blue: simulation, red stars: calculation with (9)). The shown results consider operation according to (5), i.e., DC-link voltage and instantaneous power waveforms of Fig. 2 apply. The common envelope of the phase currents is directly proportional to $p_g(t)$, since the amplitudes of the grid voltages are assumed to be constant.

phase currents,

$$i_{\{a,b,c\}} = i_d\, \sin(2\pi f_g t + \varphi_{\{a,b,c\}}), \tag{7}$$

$$\varphi_{\{a,b,c\}} = \{0,\, -120°,\, 120°\}, \tag{8}$$

for the operating point defined with (5). The spectra corresponding to $i_{\{a,b,c\}}(t)$, cf. **Fig. 3(b)**, reveal sidebands located at $f_g - f_l$ and $f_g + f_l$, where both sidebands feature same amplitudes,

$$\begin{aligned} \hat{I}_{g,1} = \frac{1}{3v_d}\Big[&\hat{P}_l^2 + 2\,\hat{P}_l\,V_{C,0}\,\hat{V}_C\,2\pi f_l\,C\,\sin(\varphi_C) \\ &+ (V_{C,0}\,\hat{V}_C\,2\pi f_l\,C)^2\Big]^{\frac{1}{2}}. \end{aligned} \tag{9}$$

It is worth noting that (9) defines a linear relation between $\hat{I}_{g,1}$ and $\hat{P}_l$, since the ripple amplitude $\hat{V}_C$ scales linearly with $\hat{P}_l$. Expression (9) has been successfully verified by means of circuit simulations at numerous different operating points and different DC-link capacitances. Fig. 3(b) reveals close matching of calculated (blue circles) and simulated (red stars) results for the operating point defined with (5). For the considered system it is found that the relative error between calculated and simulated sideband amplitude, $\hat{I}_{g,1}$, is below 2 %.

III. HARMONIC LIMITS AND FLICKER

This Section summarizes maximum allowable grid current distortions defined in the grid standards IEC 61000-3-11 and IEC 61000-3-12, for flicker and grid current harmonics,

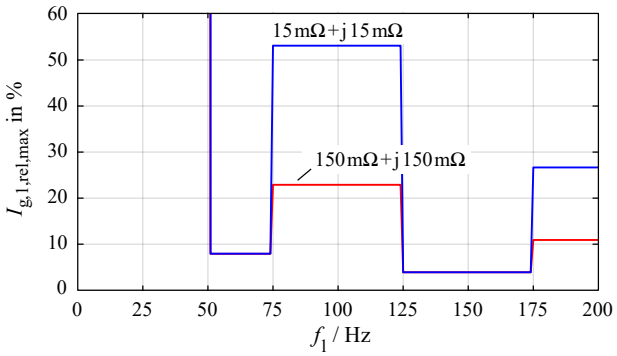

Fig. 4. Frequency characteristic of the maximum allowable sideband amplitudes of the grid currents to comply with IEC 61000-3-12 (grid current harmonics) and shown for two different grid impedances. The amplitudes are given as percentages of the frequency component at mains frequency, $\hat{I}_{g,0}$, which is proportional to the average output power, i.e., $\hat{I}_{g,0} = 2\,P_0/(3\,v_d)$.

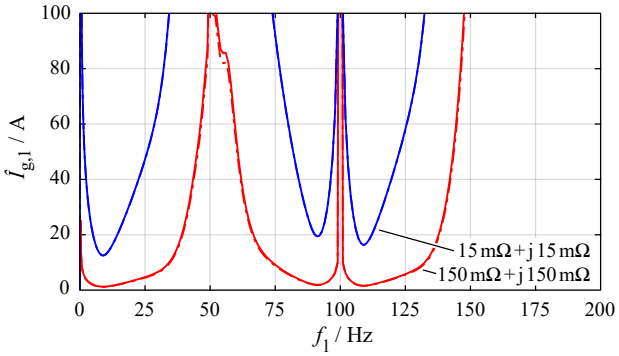

Fig. 5. Maximum acceptable sideband amplitudes of the grid currents to comply with IEC 61000-3-11 (flicker), being evaluated for two different grid impedances. The shown limits are the maximum amplitudes of the sideband currents.

respectively. Both standards apply to the considered converter system with a rated power of $P_{nom} = 20\,kW$. Since the evaluation of the limits defined by both standards requires a defined value of the grid impedance, $\underline{Z}_g$, two substantially different grid impedances of $\underline{Z}_g = 15\,m\Omega + j\,15\,m\Omega$ and $\underline{Z}_g = 150\,m\Omega + j\,150\,m\Omega$ are taken as examples for a strong and a weak grid, respectively.

A. Harmonic Current Limitations (IEC 61000-3-11)

IEC 61000-3-12 defines relative current amplitudes that depend on the short circuit power ratio,

$$R_{sce} = \frac{S_{sc}}{P_{nom}} = \frac{3\,v_g^2}{2\,Z_g} \cdot \frac{1}{P_{nom}} = \begin{cases} 374 \text{ for } Z_g = 21\,m\Omega, \\ 37.4 \text{ for } Z_g = 212\,m\Omega, \end{cases} \tag{10}$$

where $Z_g = |\underline{Z}_g|$ denotes the absolute value of the grid impedance. **Fig. 4** shows the envelopes of the maximum allowed relative rms values of the sideband currents (calculated with (9)),

$$I_{g,1,rel,max} = \frac{\hat{I}_{g,1,max}}{\hat{I}_{g,0}}, \tag{11}$$

that result for the two short circuit power ratios of (10) and as a function of the load frequency f_l ($\hat{I}_{g,0}$ denotes the amplitude of the spectral current component at mains frequency, i.e., at 50 Hz in Fig. 3(b)). The depicted result applies to a mains with a rms phase voltage of 230 V and a frequency of 50 Hz. The discontinuities in the presented envelopes arise from the processing of the spectral components required by IEC 61000 which is also described in [12]. For $0 < f_l < 50\,Hz$ no limitation is given, since both of the according interharmonic components end up at frequencies smaller than 100 Hz, where the standard does not specify any limitation.

B. Flicker Limitations (IEC 61000-3-12)

Concerning flicker, the maximum allowable voltage amplitudes are limited. Thus, the current components at the sideband frequencies need to be multiplied with the grid impedance to determine the distortion of the grid voltage. The obtained waveforms of the phase voltages are processed according to the procedure specified in IEC 61000-4-15 (named *flicker-meter*) that models the response of a human brain to flicker. In this paper, a readily available implementation has been used [13] to assess flicker,[1] which implements the individual blocks of the human eye-brain model described in the standard.

Fig. 5 presents the results of the conducted computation, i.e., the envelopes of the maximum allowed absolute rms value of each current sideband derived in Section II as function of the load frequency f_l and for two different grid impedances. Even though, the value of the spectral current component at mains frequency, $\hat{I}_{g,0}$, may have an impact on the calculated limits, since the signal processing of the flicker-meter is highly nonlinear, the results of numerical evaluations for different values of the mains frequency component reveal that this dependency is negligible.

Most stringent limitations are found to apply at low load frequencies, $f_l \approx 9\,Hz$, as well as in the vicinity of $f_l = 100\,Hz$. In both cases, at least one of the two sidebands ends up at frequencies close to the mains frequency where the standard defines the strictest limits, since the human eye exhibits the highest sensitivity to the eponymous flicker effects occurring in light bulbs at these frequencies.

IV. DC-Link Voltage Controller

Fig. 6(a) presents the considered dynamic model of the controlled PFC rectifier in the synchronous *dq* reference frame, which is valid for Low-Frequency (LF) excitations, e.g., $f_l < 200\,Hz$. The control system employs a cascaded controller structure, however, the considered model omits the inner control loop, i.e., the phase current control loop used to realize PFC operation, since the bandwidth of the inner control loop is assumed to be much greater than the maximum considered excitation frequency. The outer control loop serves for the stabilization of the DC-link voltage and comprises a PI voltage controller and the dynamic LF model of the PFC rectifier's power stage, which resembles the power balance

[1] According to the definitions given in IEC 61000-4-15, equal flicker qualifiers, $P_{lt} = P_{st}$, have been considered in order to correctly take the operation of the investigated converter system, with continuous LF AC output power, into account. Further related details are described in IEC 61000-4-15.

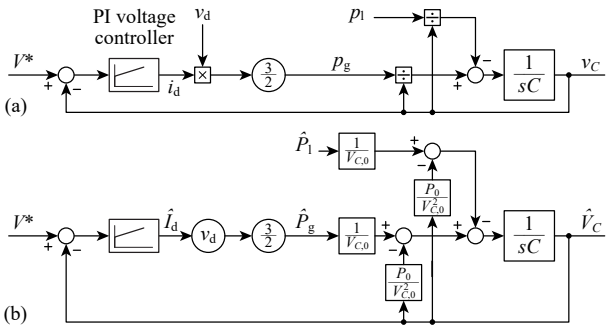

Fig. 6. (a) LF large-signal and (b) small-signal models of the PFC rectifier in the synchronous *dq* reference frame, for operation with defined load power.

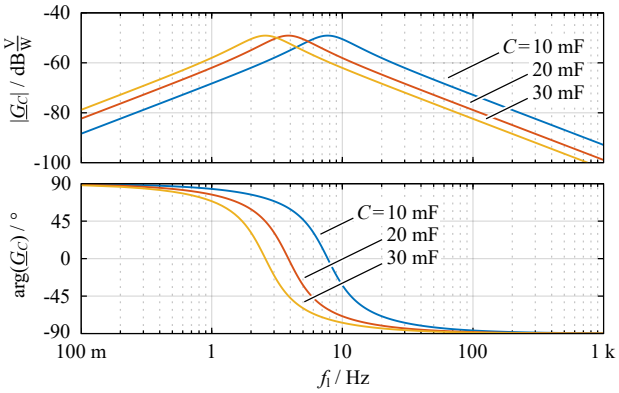

Fig. 7. Disturbance transfer function of the PFC rectifier, $\underline{G}_C$, for three different DC-link capacitances. Since the proportional gain of the PI controller is the same for all three cases, also the maximum values of the disturbance transfer functions are of same value.

scheme depicted in Fig. 1(b): the power delivered to the DC-link capacitor is the difference between input power and load power,

$$p_\mathrm{g} - p_\mathrm{l} = \frac{3}{2} i_\mathrm{d} v_\mathrm{d} - p_\mathrm{l} = p_C = v_C i_C, \tag{12}$$

and is used to determine the capacitor current and the DC-link voltage,

$$i_C = \frac{p_\mathrm{g} - p_\mathrm{l}}{v_C}, \quad v_C(t) = v_C(0) + \frac{1}{C}\int_0^t i_C(\tau)\mathrm{d}\tau. \tag{13}$$

In the course of the development of a small-signal model, the product $i_\mathrm{d} \times v_\mathrm{d}$ is replaced by a gain of v_d, since v_d is assumed to be constant, and the division in (13), used to determine i_C, is linearized. Thus,

$$\frac{p_\mathrm{l}}{v_C} \approx -\frac{P_0}{V_{C,0}^2}\hat{V}_C + \frac{1}{V_{C,0}}\hat{P}_\mathrm{l} \tag{14}$$

applies to p_l and a similar expression results for p_g.

Fig. 6(b) depicts the corresponding small-signal model of the PFC rectifier system, which enables the derivation of the transfer functions, e.g., from load power to DC-link voltage,

$$\underline{G}_C = \frac{\hat{V}_C}{\hat{P}_\mathrm{l}} = -\frac{s\,T_\mathrm{i}}{s^2\,C\,V_{C,0}\,T_\mathrm{i} + K_\mathrm{p}\,(1+sT_\mathrm{i})\,\frac{3}{2}\,v_\mathrm{d}}. \tag{15}$$

Fig. 7 shows the Bode plots of $\underline{G}_C$ for three exemplary capacitor values of $C = \{10\,\mathrm{mF}, 20\,\mathrm{mF}, 30\,\mathrm{mF}\}$, $K_\mathrm{p} = 0.586\,\mathrm{A/V}$,

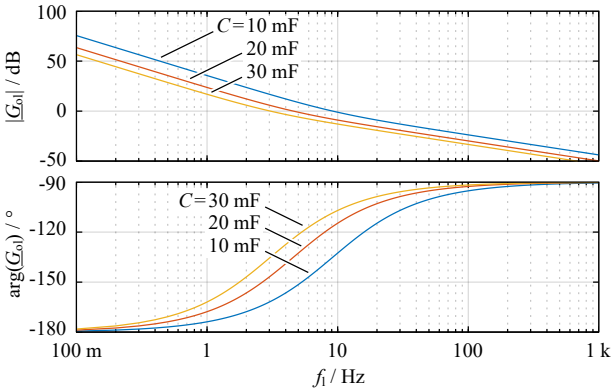

Fig. 8. Open-loop transfer functions of the PFC rectifier, $\underline{G}_\mathrm{ol}$, for $K_\mathrm{p} = K_\mathrm{p,min}$, a phase margin of 45°, the specifications listed in Tab. I, and three different capacitance values, $C = \{10\,\mathrm{mF}, 20\,\mathrm{mF}, 30\,\mathrm{mF}\}$.

and $T_\mathrm{i} = \{17.3\,\mathrm{ms}, 34.7\,\mathrm{ms}, 52.0\,\mathrm{ms}\}$. This transfer function is found to exhibit a maximum of

$$|\underline{G}_C|_\mathrm{max} = \frac{2}{3\,v_\mathrm{d}\,K_\mathrm{p}} < \frac{\hat{V}_{C,\mathrm{max}}}{\hat{P}_{\mathrm{l,max}}} \Rightarrow K_\mathrm{p} \geq K_\mathrm{p,min} = \frac{2\,\hat{P}_{\mathrm{l,max}}}{3\,v_\mathrm{d}\,\hat{V}_{C,\mathrm{max}}} \tag{16}$$

that is independent of C and T_i. This provides a design constraint for K_p since $|\underline{G}_C|_\mathrm{max}$ denotes the ratio between maximum ripple of the DC-link voltage, $\hat{V}_C$, and the given load power fluctuation, $\hat{P}_\mathrm{l}$.

In a final step, the controller's integrator time constant, T_i, is determined for a defined phase margin of the open-loop transfer function,

$$PM = \arctan\left(\frac{3v_\mathrm{d}K_\mathrm{p}}{2CV_{C,0}}\sqrt{\frac{T_\mathrm{i}^2}{2} + \sqrt{\frac{T_\mathrm{i}^4}{4} + \left(\frac{2\,C\,T_\mathrm{i}\,V_{C,0}}{3\,v_\mathrm{d}\,K_\mathrm{p}}\right)^2}}\right). \tag{17}$$

Fig. 8 depicts the Bode plots of the open-loop transfer functions for $C = \{10\,\mathrm{mF}, 20\,\mathrm{mF}, 30\,\mathrm{mF}\}$, $K_\mathrm{p} = K_\mathrm{p,min}$, $PM = 45°$, and the specifications listed in Tab. I and reflects a decrease of the resulting transition frequency, from 9 Hz to 3 Hz, for increasing DC-link capacitance.

V. Dimensioning Example

Fig. 9 illustrates the flowchart of the procedure that is used to determine the maximum allowable power fluctuation according to IEC 61000 with respect to load frequency. The procedure considers a discrete number of load frequencies and the load profile of an ohmic AC load, i.e., $\hat{P}_\mathrm{l} = P_0$,

$$f_\mathrm{l} \in \{f_{\mathrm{l},1}, f_{\mathrm{l},2}, \ldots f_{\mathrm{l},n}\}, \tag{18}$$

$$p_{\mathrm{l},i} = \hat{P}_\mathrm{l}[1 - \cos(2\pi f_{\mathrm{l},i} t)] \quad \forall\, i \in \{1, \ldots n\}. \tag{19}$$

The values $f_{\mathrm{l},1} \ldots f_{\mathrm{l},n}$ of (18) are selected such that improved frequency resolution is achieved in frequency ranges where strong implications on the allowable power fluctuations are expected, i.e., for $f_\mathrm{l} < 10\,\mathrm{Hz}$ and $90\,\mathrm{Hz} < f_\mathrm{l} < 110\,\mathrm{Hz}$.

In the course of a binary search, the core function of the procedure, denoted *IEC 61000 fulfilled* in Fig. 9, first determines the phase current distortions according to (6),

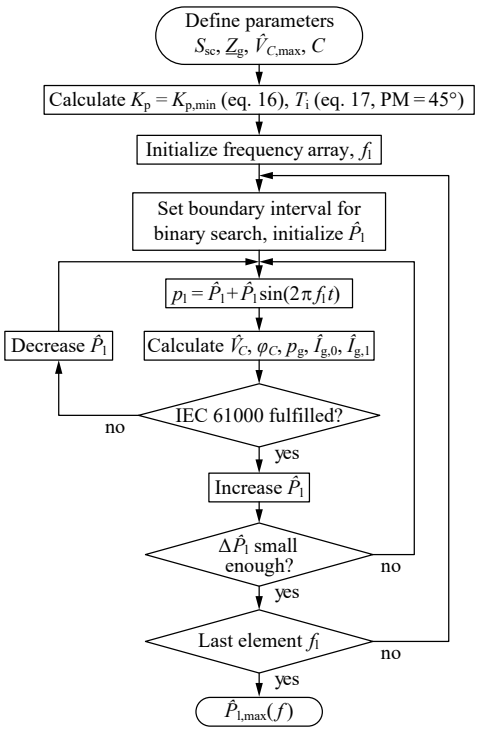

Fig. 9. Flow chart of the procedure to determine the maximum available load power at the PFC's output without violating IEC 61000. The maximum feasible power for a predefined set of distinct frequencies is determined by means of a binary search algorithm. An ohmic AC load is assumed, i.e., $\hat{P}_l = P_0$; still, any other relation between $\hat{P}_l$ and P_0 could be used.

(7), and (9) for given operating conditions and for known disturbance transfer function, $\underline{G}_C$,

$$\hat{V}_C = \hat{P}_l\,|\underline{G}_C(2\pi f_l)|, \quad \varphi_C = \arg[\underline{G}_C(2\pi f_l)], \qquad (20)$$

cf. Section IV and (15).[2] In a second step, the phase voltage distortion is calculated for a defined grid impedance and, finally, the algorithm tests whether the requirements of IEC 61000, as summarized in Section III, are fulfilled.

Figs. 10 and **11** illustrate the dependency of the maximum allowable power levels on frequency and DC-link capacitance, $\hat{P}_{l,max}(f_l, C)$, for a strong grid and a weak grid, respectively, where

$$C \in \{5\,\mathrm{mF}, 12\,\mathrm{mF}, 20\,\mathrm{mF}, 27\,\mathrm{mF}, 34\,\mathrm{mF}, 41\,\mathrm{mF}, 49\,\mathrm{mF}\} \qquad (21)$$

is selected for evaluation. The characteristics depicted in Figs. 10 and 11 are mostly related to flicker limitations, since IEC 61000-3-11 specifies relative limits for the harmonic current components, i.e., relative to the total rms value of the phase current, cf. (9). For this reason, and because $P_0 = \hat{P}_l$ is considered, the relative distortion is found to be independent of $\hat{P}_l$ and, at a considered frequency, IEC 61000-3-11 is

[2]The implemented binary search starts with a sufficiently high initial value for $\hat{P}_l$ (here, $\hat{P}_{l,init} = 500\,\mathrm{kW}$ has been selected), uses an initial increment or decrement of $\Delta\hat{P}_l = \hat{P}_{l,init}/2$, and successively, i.e., after each evaluation of the methods that test for compliance with regard to IEC 61000, cuts $\Delta\hat{P}_l$ into one half ($\Delta\hat{P}_l \leftarrow \Delta\hat{P}_l/2$) and determines the next value of $\hat{P}_l$. This is repeated until $\Delta\hat{P}_l < \hat{P}_{l,init} \times 10^{-4}$ applies.

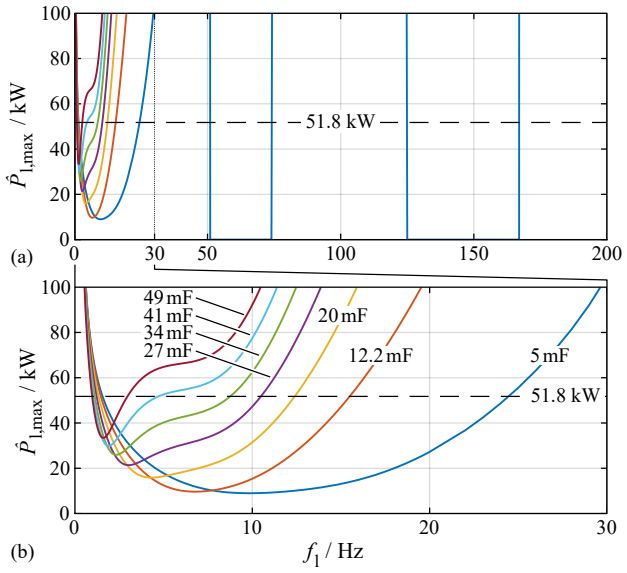

Fig. 10. (a) Maximum allowable output power over the entire load frequency range for different DC-link capacitances and a grid impedance of $\underline{\boldsymbol{Z}}_{\mathbf{g}} = \mathbf{15\,m\Omega + j\,15\,m\Omega}$. For $C = 5\,\mathrm{mF}$ the harmonic current limitations cannot be fulfilled for $50\,\mathrm{Hz} \le f_l \le 75\,\mathrm{Hz}$ and $125\,\mathrm{Hz} \le f_l \le 167\,\mathrm{Hz}$. (b) Magnified view on $f_l \le 30\,\mathrm{Hz}$. A minimum is found for $f_l \le 10\,\mathrm{Hz}$, where the requirements for flicker set the most stringent limitations. According to these results, a capacitance of $C \ge 27\,\mathrm{mF}$ is needed to allow for operation with nominal power of $P_{nom} = 20\,\mathrm{kW}$ over the entire range of load frequency. Please note that the considered IEC 61000 standard only apply to grid currents $\le 75\,\mathrm{A}$, which corresponds to a maximum power level of $51.8\,\mathrm{kW}$.

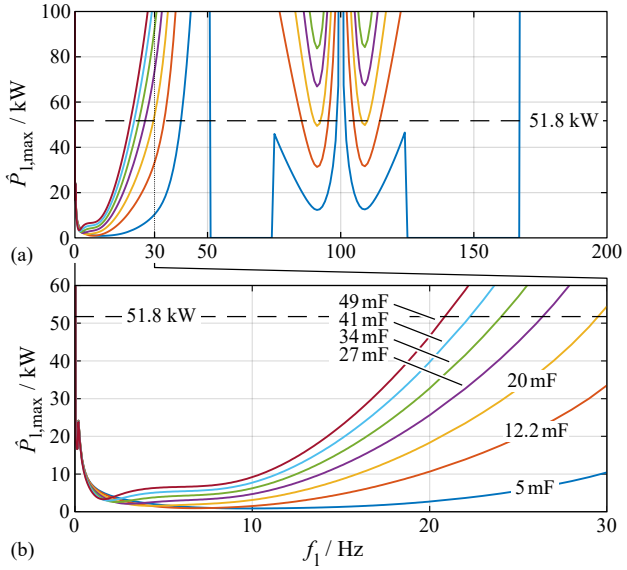

Fig. 11. (a) Maximum allowable output power over the entire load frequency range for different DC-link capacitances and a grid impedance of $\underline{\boldsymbol{Z}}_{\mathbf{g}} = \mathbf{150\,m\Omega + j\,150\,m\Omega}$. For $C = 5\,\mathrm{mF}$ the harmonic current limitations cannot be fulfilled for $50\,\mathrm{Hz} \le f_l \le 75\,\mathrm{Hz}$ and $125\,\mathrm{Hz} \le f_l \le 167\,\mathrm{Hz}$. (b) Magnified view on $f_l \le 30\,\mathrm{Hz}$. In comparison to Fig. 10, even with a high DC-link capacitance of $49\,\mathrm{mF}$ it is not possible to deliver output power levels exceeding $3.5\,\mathrm{kW}$ over the entire frequency range without violating the limits set for flicker.

either fulfilled or cannot be fulfilled at all, which occurs for $C = 5\,\mathrm{mF}$ and $50\,\mathrm{Hz} < f_\mathrm{l} < 75\,\mathrm{Hz} \wedge 125\,\mathrm{Hz} < f_\mathrm{l} < 167\,\mathrm{Hz}$. Different to IEC 61000-3-11, the flicker standard IEC 61000-3-12 defines absolute values for the maximum allowable phase voltage distortions and the corresponding identified maximum allowable load power levels exhibit a minimum in the vicinity of $9\,\mathrm{Hz}$ for $C = 5\,\mathrm{mF}$, since the flicker standard sets the most stringent limitations, there. This minimum is shifted to lower frequencies with increasing DC-link capacitance, which can be observed in the magnified graphs presented in **Figs. 10(b)** and **11(b)**, because larger DC-link capacitances are capable of providing a larger amount of fluctuating energy for a defined capacitor voltage ripple. From Fig. 10 it can be concluded that a capacitance of $C = 27\,\mathrm{mF}$ is sufficient for a strong grid. In case of a weak grid with $\underline{Z}_\mathrm{g} = 150\,\mathrm{m\Omega} + \mathrm{j}\,150\,\mathrm{m\Omega}$, the specified output power of $20\,\mathrm{kW}$ would require very high DC-link capacitances exceeding $50\,\mathrm{mF}$. For this reason, a derating of the output power, according to the characteristics shown in Fig. 11, may be considered instead. Another solution could be the implementation of an active power pulsation buffer [14] in order to decrease the size of the output capacitor, which, however, increases the complexity of the system.

VI. Conclusion

This paper develops a procedure to design the DC-link capacitor and the PI DC-link voltage controller for a converter system that utilizes a grid-connected three-phase PFC rectifier to provide LF pulsating power to a single-phase load inverter supplied from the DC-link, such that compliance with the relevant IEC 61000 grid standards is achieved. The requirements defined by IEC 61000-3-11 (harmonic current limitations) and IEC 61000-3-12 (flicker) are summarized, the computation of the emitted LF disturbances of the system is detailed, and the small-signal model that is required to identify design constraints for the voltage controller is discussed.

The developed procedure is explained in the course of an example system with a rated power of $20\,\mathrm{kW}$ and a DC-link voltage of $700\,\mathrm{V}$, where a capacitance of $27\,\mathrm{mF}$ is found to guarantee full-power operation over the entire output frequency range in case of a strong grid (assumed grid impedance of $15\,\mathrm{m\Omega} + \mathrm{j}\,15\,\mathrm{m\Omega}$). In case of weak grids, very high capacitances exceeding $50\,\mathrm{mF}$ may be required or the implementation of a derating according to the computed power limitation characteristic may be considered, instead.

The results for the $20\,\mathrm{kW}$ converter system reveal that the requirement of a large DC-link capacitance is mainly related to flicker limitations that are most stringent at low frequencies. Thus, the result is subject to a physical constraint (high energy storage requirement) and only limited improvements are expected with extended concepts, e.g., nonlinear voltage control methods according to [15], [16], for controlling the DC-link voltage. For this reason, the immediate next steps rather focus on experimental verification and the evaluation of the impact of the shape of the fluctuating output power, i.e., if $p_\mathrm{l}(t)$ is not sinusoidal, on the characteristics of the limitations.

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