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## Scaling and Balancing of Multi-Cell Converters

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# Scaling and Balancing of Multi-Cell Converters

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***Abstract*—In this paper, the potential of the multi-cell approach for power electronic converters with efficiencies and power densities beyond the barriers of state-of-the-art systems is discussed. Based on fundamental scaling laws the benefits of splitting a system into multiple converter cells are derived in terms of lower volume and/or higher power density for a given cooling capacity. In addition, the conditions for equal current and/or voltage balancing of multi-cell systems is reviewed. The advantages of the mulit-cell systems are examined in more detail based on the example of a DC-DC boost converter realized with either parallel- or series-interleaved boost cells. It is shown, that the multi-cell systems can offer lower switching and conduction losses and/or an improved voltage spectrum depending on the choice of the switching frequency relative to a single system. Furthermore, the effects of parasitic capacitances on unwanted ground currents are investigated for both configurations.**

***Index Terms*—Multi-cell converters, scaling laws, series-interleaving, parallel-interleaving**

## I. Introduction

The development of power electronic converter systems towards more efficient, compact and cost effective systems is nowadays to a large extent driven either by the performance improvement of power electronic components or by a higher level of integration. These improvement processes, however, evolve only over longer periods of time that often span decades; the development and market introduction of wide-bandgap semiconductors which started about two decades ago could serve as an example here. In contrast, the development of new topologies is able to shift the system performance (e.g. efficiency, power density and system cost) to new levels in a much shorter time. However, many newly developed topologies are based on adding components to standard topologies with added components [1] which improves individual performance aspects of the basic system but also leads to a higher system complexity and often reduced reliability since the failure rate increases with increasing component count [2].

In this paper, a multi-cell (MC) topology approach is presented which allows to break the barriers of traditional single-stage converter systems by employing basic converters as individual converter cells. The paper is structured as follows: First, general scaling laws of power electronic converters are derived in Section II in order to provide the basis for general statements about the advantages of MC converters. The operation and balancing of multi-cell systems is discussed and reviewed in general in Section III. In a third step, the exemplary multi-cell realization of a DC-DC boost converter in either parallel or series configuration is presented in Section IV and its performance is comparatively evaluated against a single stage converter system. In Section V the leakage current caused by parasitic ground capacitances is assessed for both multi-cell converter realizations in comparison to a single boost converter. Finally, the findings are summarized in Section VI.

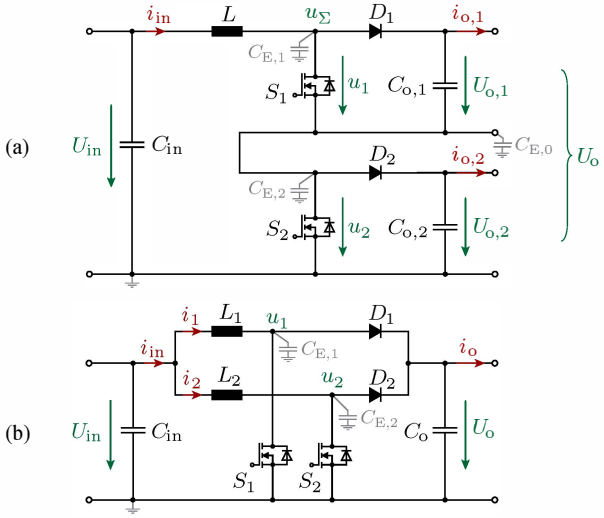


**Fig. 1:** Multi-cell converter realizations of a DC-DC boost converter: (a) series interleaving of two boost stages and (b) parallel interleaving of two boost stages.

## II. Scaling Laws of Multi-Cell Converters

Multi-cell topologies can in general be classified as converter systems consisting of two or more subsystems that are connected in one of the following configurations: input-series output-parallel (ISOP), input-series output-series (ISOS), input-parallel output-series (IPOS) or input-parallel output-parallel (IPOP) [3]. As an example of multi-cell converters a standard DC-DC boost converter is shown in **Fig. 1(a)** realized as series-interleaved MC converter (ISOS) and in **Fig. 1(b)** as a parallel-interleaved MC converter (IPOP). These configurations allow to either share the input current between the converter cells (i.e. IPOP) or distribute the output voltage between the converter cells (i.e. ISOS). As a result of splitting either the current or the voltage among the converter cells, the system power is also split in such way that each cell transfers only a fraction of the total power.

The concept of splitting the overall system into smaller subsystems with relatively low power rating leads to benefits that can be leveraged to improve one or more of the performance criteria mentioned in Section I, as will be shown in the following paragraph.

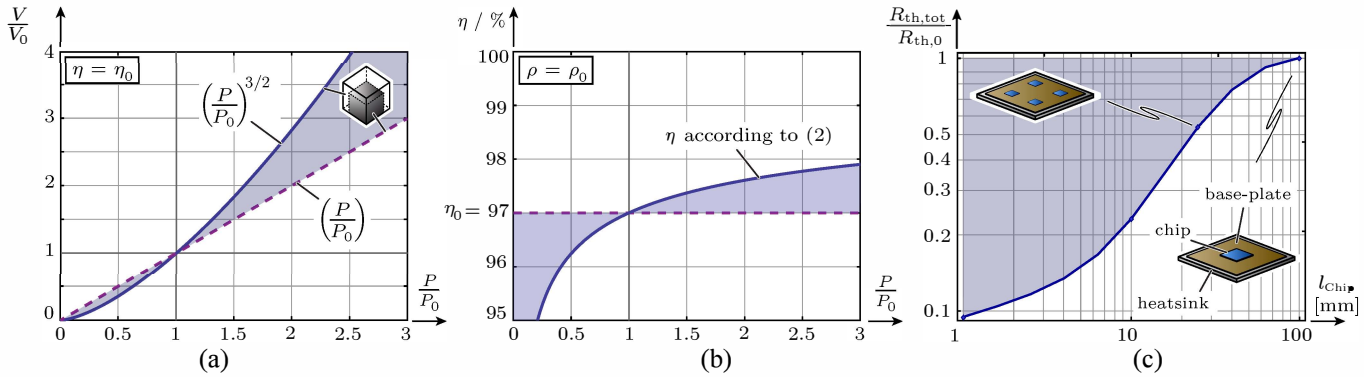


**Fig. 2:** General scaling laws of power electronic converters: (a) scaling of converter volume $V$ with the converter power $P$ at a constant conversion efficiency $\eta$ and (b) required scaling of converter efficiency with the converter power at a constant power density $\rho$, both under the assumption of a constant heat dissipation per converter surface area; (c) reduction of the total thermal resistance of semiconductors by distributing the total chip area to multiple chips with shorter edge lengths.

As derived in Appendix A the volume $V$ of a power electronic system with output power $P$ scales compared to a reference system ($V_0$, $P_0$) with

$$\frac{V}{V_0} = \left(\frac{P}{P_0}\right)^{3/2} \tag{1}$$

under the assumption of a constant efficiency (i.e. $\eta = \eta_0$). This is visualized in **Fig. 2(a)**. As a result, the total boxed volume of MC converters with multiple converter cells scales advantageously compared to a single converter with the same total power rating as the MC converter.

With a similar approach (cf. Appendix A), assuming a constant power density (i.e. $\rho = P/V = \rho_0 = P_0/V_0$), it can be found that the efficiency of a converter system has to be scaled with the rated system output power by

$$\eta = \frac{\eta_0 \cdot \left(\frac{P}{P_0}\right)^{1/3}}{1 + \eta_0 \cdot \left(\left(\frac{P}{P_0}\right)^{1/3} - 1\right)} \tag{2}$$

since only a fixed amount of losses (dissipated as heat) can be extracted per surface area. This relationship is depicted for $\eta_0 = 97\%$ in **Fig. 2(b)** and shows that, for example, doubling the system power while keeping the same power density requires to increase the efficiency to $\eta = 97.6\%$.

By splitting the system into lower rated subsystems due to parallel or series interleaving, the semiconductor ratings can be reduced, resulting in a smaller silicon area of the employed chips. Due to the better heat-spreading of smaller chips on a (comparably large) base-plate, the total thermal resistance $R_{\text{th,tot}}$ of the lower-rated chips reduces compared to the thermal resistance $R_{\text{th,0}}$ of the full-rated semiconductor, as shown in **Fig. 2(c)**. The values were determined with FEM simulations for a chip structure based on a TO-247 package with $350\,\mu\text{m}$ thick silicon, $2\,\text{mm}$ thick copper base-plate, $40\,\mu\text{m}$ thick phase-change material ($\lambda = 0.3474\,\text{W}/(\text{m}\cdot\text{K})$) and a $5\,\text{mm}$ thick heat-sink connected to a reference temperature of $T_{\text{amb}} = 40\,^\circ\text{C}$. The copper area was chosen to be ten times larger than the silicon area. As the thermal resistance decreases with decreasing chip length, the overall heat-sink volume can be decreased by applying the MC approach.

As a result of the above mentioned fundamental scaling laws, which are independent of the employed converter topology, the MC approach offers advantages in terms of converter efficiency and/or power density and potentially also costs since lower rated semiconductors and/or smaller heat-sinks can be employed.

## III. Balancing and Control of MC Converters

The balancing of currents and/or voltages is an important issue in multi-cell converter systems as the design of the converter cells relies on an equal current and/or voltage sharing among the cells such that the overall system power is equally distributed. Thus, any conditions that lead to a violation of the power sharing might cause an overloading and ultimately a destruction of individual converter cells possibly resulting in a failure of the system. Therefore, current and/or voltage sharing among the converter cells has to be guaranteed for steady state condition and transients. Also the influence of component mismatches, such as slightly different inductance values of parallel connnected converter cells, on the system balancing needs to be addressed.

The operation of multi-cell systems with common-duty-ratio control, where all converter cells are operated with the same duty cycle, relies upon the natural balancing capabilities of a multi-cell topology and is thus only feasible for IPOS and ISOP systems [3]–[5]. For those topologies any component mismatch leads to slightly unequal sharing conditions but not to a runaway situation. In general, ISOS and IPOP are considered to have no natural balancing mechanism and thus require additional control means to guarantee a balanced operation (even though also for the ISOS converter some rebalancing mechanisms could be found [6]). For the IPOP converter it is sufficient to control an equal sharing of the output current as the input current will then also be equally shared [7]. Different control schemes such as droop methods and active control schemes have been published and reviewed in literature [8]–[11]. For ISOS converter structures it was found that controlling the output voltage sharing does not ensure input voltage sharing due to the presence of a right-half-plane pole and thus control efforts should focus on input voltage sharing [12].

## IV. Multi-Cell Boost Converters

In this chapter, the operation and the scaling benefits of series-interleaved and parallel-interleaved DC-DC boost converters are investigated.

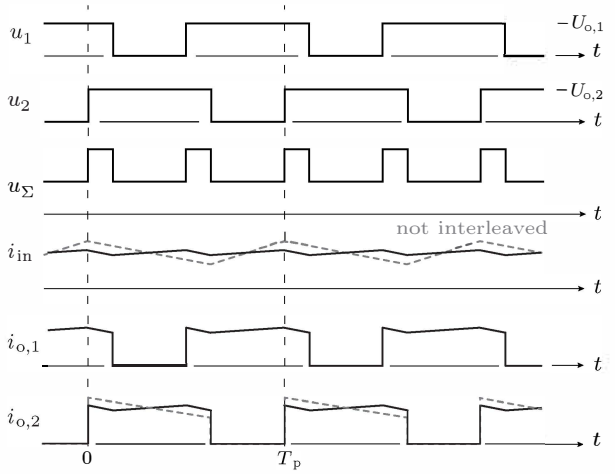


**Fig. 3:** Schematic waveforms of the operation of two series-interleaved DC-DC boost converters. Dashed lines denote the waveforms for operation without phase shift, i.e. non-interleaved operation.

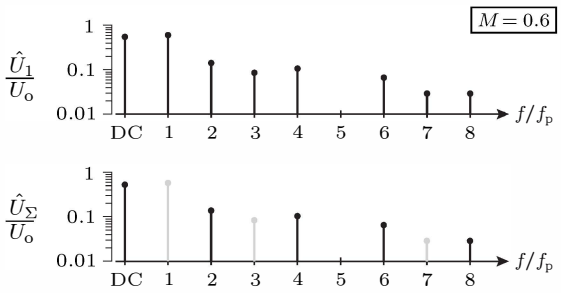


**Fig. 4:** Comparison of the harmonic spectrum of a single boost converter (top) with the harmonic spectrum of two series-interleaved boost converters (bottom) at a modulation index of $M = 0.6$. Harmonics shown in grey are canceled in the spectrum of the interleaved converters.

### A. Series-interleaved boost converters

In the series-interleaved boost converter (cf. **Fig. 1(a)**), with $N_s$ series connected converter cells, the total output voltage $U_o$ is shared among the output capacitors $C_{o,1}, C_{o,2} ... C_{o,Ns}$ of the individual converter cells, such that $U_{o,i} = U_o/N_s$. The system is advantageously operated with a phase-shifted (interleaved) modulation scheme with a phase shift of $\delta = 2\pi/N_s$ as shown in **Fig. 3**. This results in an effective switching frequency of the total switch node voltage $u_\Sigma = \sum_{i=1}^{N} u_i$ of $f_{sw,eff} = N_s \cdot f_{sw}$ with $f_{sw}$ being the switching frequency of one converter cell. Hence, the peak-to-peak current ripple $\Delta i_{in}$ of the input current $i_{in}$ can be calculated in dependency of the modulation index $M = U_{in}/U_o$ by introducing an effective modulation index $M_{eff} = (M \text{ modulo } 1/N_s)$ as

$$\Delta i_{in} = \frac{U_o}{L \cdot f_{sw}} \cdot M_{eff} \left( M_{eff} - \frac{1}{N_s} \right) . \quad (3)$$

The maximum value of $\Delta i_{in}$ can be found for $M_{eff} = 0.5/N_s$ as

$$\Delta i_{in,max} = \frac{U_o}{4 N_s^2 f_{sw} L} \quad (4)$$

yielding a $\propto 1/N_s^2$ decrease of the ripple amplitude in dependency of the number of converter cells.
Furthermore, the harmonic spectrum of the multi-cell converter voltage $u_\Sigma$ can be derived from a single converter system by considering only the harmonics with orders that are multiples of the number of cells $N_s$, as visualized in **Fig. 4**.

*Semiconductors:* The losses caused by semiconductors can be divided into conduction and switching losses and their dependency on the number of converter cells is described in the following.

*Conduction losses:* For standard MOSFETs the fundamental relation between the blocking voltage $U_{DS}$ and the lowest achievable on-state resistance $R_{DS,on}$ of a device is determined by the so-called silicon limit [14], which can be expressed for a given semiconductor area $A_{Si}$ as

$$R_{DS,on,(1)} \cdot A_{Si} = 8.3 \cdot 10^{-9} \cdot U_{DS}^{2.5} [\Omega cm^2] = k_{Si} \cdot U_{DS}^{2.5} [\Omega cm^2] . \quad (5)$$

This relation holds true for MOSFETs where the $R_{DS,on}$ is mainly influenced by the resistance of the drift region of the device, i.e. only for devices with blocking voltages larger than around $50\,V$ [15]. In the multi-cell system with series-interleaved boost converters, the required blocking voltage of $U_{DS} = U_o$ is divided to $N_s$ series connected switches, i.e. each switch has to be capable of blocking a voltage $U_{DS}/N_s$, as shown in **Fig. 5(a)**. It can either be assumed that the chip area of each semiconductor is equal to the chip area of the full-rated switch (i.e. $N_s$ devices with $A_{Si}$, (2) in **Fig. 5(a)**) or that the total chip area $A_{Si}$ is equally distributed among the semiconductors (i.e. $N_s$ devices with $A_{Si}/N_s$, (3) in **Fig. 5(a)**). For option (2) the total resistance can be calculated as

$$\begin{aligned} R_{DS,on,N,(2)} &= N_s \cdot \frac{1}{A_{Si}} \cdot k_{Si} \cdot \left( \frac{U_{DS}}{N_s} \right)^{2.5} [\Omega cm^2] \\ &= \frac{1}{\sqrt{N_s} \cdot N_s} \cdot \frac{1}{A_{Si}} \cdot k_{Si} \cdot U_{DS}^{2.5} [\Omega cm^2] . \end{aligned} \quad (6)$$

whereas the total resistance of option (3) equals

$$\begin{aligned} R_{DS,on,N,(3)} &= N_s \cdot \frac{N_s}{A_{Si}} \cdot k_{Si} \cdot \left( \frac{U_{DS}}{N_s} \right)^{2.5} [\Omega cm^2] \\ &= \frac{1}{\sqrt{N_s}} \cdot \frac{1}{A_{Si}} \cdot k_{Si} \cdot U_{DS}^{2.5} [\Omega cm^2] . \end{aligned} \quad (7)$$

Both equations can be interpreted as a shift of the silicon limit towards lower specific on-state resistances [16], which can be expressed as

$$R_{DS,on,N,(2)} = \frac{R_{DS,on,(1)}}{\sqrt{N_s} \cdot N_s} \text{ and } R_{DS,on,N,(3)} = \frac{R_{DS,on,(1)}}{\sqrt{N_s}} . \quad (8)$$

This relationship is visualized in **Fig. 5(b)**. The fundamental limits of wide bandgap materials such as GaN and SiC can be shifted in the same manner, since their on-state resistance for a given semiconductor area also increases more than quadratically with the break-down voltage (i.e. $R_{DS,on,GaN} \propto U_{DS}^{2.5}$ and $R_{DS,on,6H\text{-}SiC} \propto U_{DS}^{2.6}$) [17].

*Switching losses (Option 1):* The first option of calculating switching losses considers the overlapping of voltage and current across the transistor (NB: mainly applicable to circuits with IGBTs). The switching losses of $N_s$ series connected switches can be compared to a single switch with full blocking voltage by assuming equal rates of $du/dt$ and $di/dt$ for all switches [13]. The switching losses of the single full-rated switch are

$$P_{Sw,loss,1} = E_{sw} \cdot f_{sw,1} = \frac{1}{2} \cdot (T_{r,i} + T_{f,u}) \cdot I_i \cdot V_{DC} \cdot f_{sw,1} . \quad (9)$$

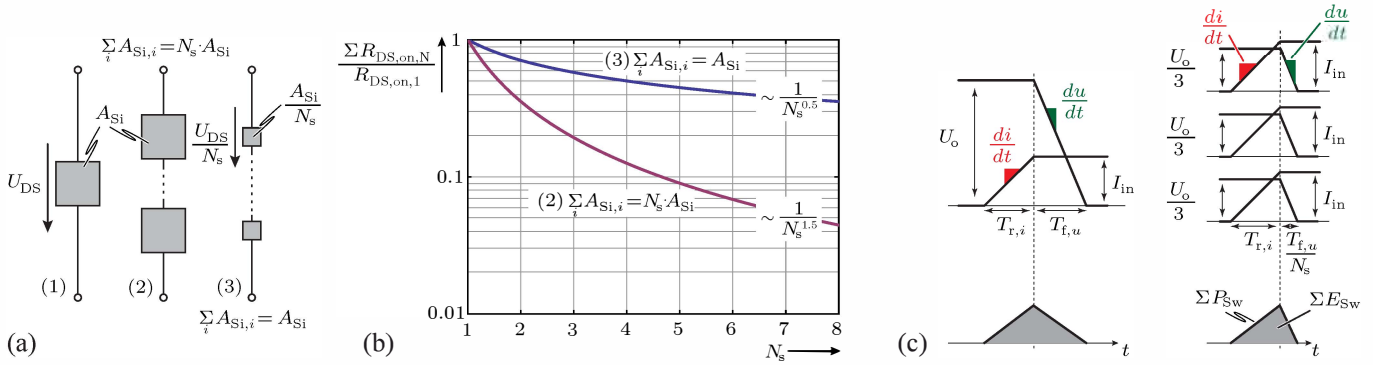


**Fig. 5:** Scaling laws of conduction and switching losses for series-interleaved boost converters: (a) replacing a single semiconductor with a blocking voltage of $U_{DS}$ (1) with $N_s$ semiconductors with blocking voltages of $U_{DS}/N_s$ where each has either the same silicon area $A_{Si}$ as the full-rated semiconductor (2) or where the total chip area is equal to $A_{Si}$; (b) improvement of the total $R_{DS,on}$ for scenarios (2) and (3) with the number of series converter cells; (c) reduction of switching losses in a series-interleaved multi-cell system with the same $du/dt$ and $di/dt$ as the single converter system [13].

As can be seen from (4), the switching frequency of a system with $N_s$ cells can be scaled by $1/N_s^2$ while keeping the same current ripple amplitude for a certain inductance. Since the voltage across one switch is equal to $U_o/N_s$ and the same $du/dt$ is assumed, time $T_{f,u}$ decreases by a factor of $1/N_s$. Thus, the overall switching losses of $N_s$ series connected switches become

$$\begin{aligned} P_{Sw,loss,Ns} &= N_s \cdot E_{sw,cell} \cdot \frac{f_{sw,1}}{N_s^2} \\ &= N_s \cdot \frac{1}{2} \cdot \left( T_{r,i} + \frac{T_{f,u}}{N_s} \right) \cdot I_{in} \cdot \frac{U_o}{N_s} \cdot \frac{f_{sw,1}}{N_s^2} \\ &= \frac{1}{2N_s^2} \cdot \left( T_{r,i} + \frac{T_{f,u}}{N_s} \right) \cdot I_{in} \cdot U_o \cdot f_{sw,1} \ . \end{aligned} \quad (10)$$

Neglecting $T_{f,u}/N$ (compared to $T_{r,i}$) in first step or assuming low values of $T_{r,i}$ (i.e. low values of the input current $I_{in}$), an improvement of the switching losses of

$$P_{Sw,loss,Ns} \approx \frac{P_{Sw,loss,1}}{N_s^2} \ldots \frac{P_{Sw,loss,1}}{N_s^3} \quad (11)$$

can be found.

*Switching losses (Option 2):* The second option of calculating switching losses considers the energy stored in the parasitic capacitances of the transistor and the diode of a half-bridge. The energy stored in a parasitic non-linear capacitance ($C_{T,OSS}$ or $C_{D,OSS}$) can be calculated by introducing an energy-equivalent capacitance

$$C_{OSS,E,eq}(U_{DS}) = \frac{2 \cdot E_{OSS}(U_{DS})}{U_{DS}^2} = \frac{2 \int_0^{U_{DS}} v \cdot C_{OSS}(v) \mathrm{d}v}{U_{DS}^2} \ ; \quad (12)$$

furthermore, a charge-equivalent capacitance

$$C_{OSS,Q,eq}(U_{DS}) = \frac{Q_{OSS}(U_{DS})}{U_{DS}} = \frac{\int_0^{U_{DS}} C_{OSS}(v) \mathrm{d}v}{U_{DS}} \ . \quad (13)$$

can be defined for the switch and the diode. This allows to calculate the energy $E_{on,1}$ lost per switching cycle in a system with only one converter cell (i.e. $N_s = 1$) to be

$$\begin{aligned} E_{on,1} = &\frac{1}{2} \cdot C_{T,OSS,E,eq,1}(U_o) \cdot U_o^2 \\ &- \frac{1}{2} \cdot C_{D,OSS,E,eq,1}(U_o) \cdot U_o^2 \\ &+ C_{D,OSS,Q,eq,1}(U_o) \cdot U_o^2 \end{aligned} \quad (14)$$

(cf. [18]) since the turn-off transition of the MOSFET can be regarded as loss-less (ZVS) and thus $E_{off,1} = 0$. The above equation can be simplified since the contribution of $C_{D,OSS,E,eq,1}$ is typically small compared to the other terms and thus negligible, such that

$$E_{on,1} = \frac{1}{2} \cdot C_{eff,1}(U_o) \cdot U_o^2 \quad (15)$$

by introducing an effective capacitance

$$C_{eff,1}(U_o) = C_{T,OSS,E,eq,1}(U_o) + 2 \cdot C_{D,OSS,Q,eq,1}(U_o) \ . \quad (16)$$

Hence, the switching losses for a single cell system are

$$P_{Sw,loss,1} = E_{on,1} \cdot f_{sw,1} = \frac{1}{2} \cdot C_{eff,1}(U_o) \cdot U_o^2 \cdot f_{sw,1} \ . \quad (17)$$

In a system with $N_s$ converter cells the voltage across each switch is only $U_o/N_s$. Thus, in the same manner as before, the power dissipated in the switches of a multi-cell system can be calculated as

$$\begin{aligned} P_{Sw,loss,Ns} &= N_s \cdot E_{on,N} \cdot \frac{f_{sw,1}}{N_s^2} \\ &= \frac{1}{N_s} \cdot \frac{1}{2} \cdot C_{eff,Ns}(U_o/N_s) \left( \frac{U_o}{N_s} \right)^2 f_{sw,1} \\ &= \frac{1}{2N_s^3} \cdot C_{eff,Ns}(U_o/N_s) \cdot U_o^2 \cdot f_{sw,1} \end{aligned} \quad (18)$$

and/or

$$P_{Sw,loss,Ns} = \frac{1}{N_s^3} \cdot \frac{C_{eff,Ns}(U_o/N_s)}{C_{eff,1}(U_o)} \cdot P_{Sw,loss,1} \ . \quad (19)$$

Depending on how the values of the effective capacitances of the employed low voltage switches (i.e. at $U_{DS} = U_o/N_s$) compare to those of the higher voltage switch (i.e. at $U_{DS} = U_o$) a significant improvement of the switching losses can be achieved in the multi-cell system.

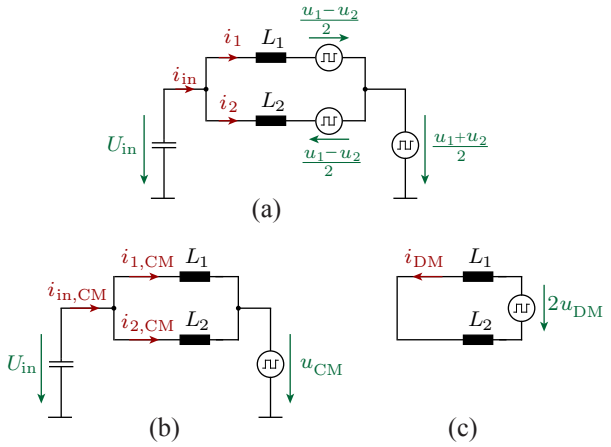


**Fig. 6:** Equivalent circuit diagram of two parallel-interleaved boost converters: (a) replacement of switch node voltages with rectangular voltage sources and splitting into (b) common mode and (d) differential mode equivalent circuits.

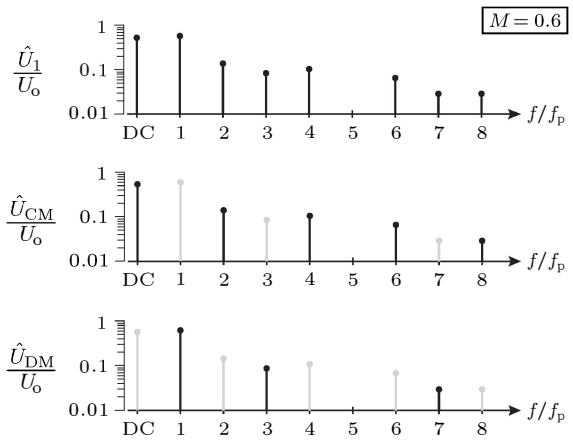


**Fig. 8:** Comparison of the harmonic spectrum of a single boost converter (top) to the common mode voltage spectrum (middle) and the differential mode voltage spectrum (bottom) of two parallel-interleaved boost converters.

### *B. Parallel-interleaved boost converter*

In the parallel-interleaved boost converter (cf. **Fig. 1(b)**) with $N_p$ parallel connected boost converters, the DC value of the input current $I_{in}$ of the system is equally shared among the converter cells, i.e. average input current values of $I_1 = I_2 = ... = I_{Np} = I_{in}/N_p$ are occuring. The operation of the individual converter cells is phase shifted with the same phase shift $\delta = 2\pi/N_p$ as for the series interleaved system. This mode of operation allows to derive the equivalent circuit of **Fig. 6(a)** for a system with two parallel-interleaved boost converters. In this circuit the switches are replaced with rectangular voltage sources in order to accurately model the influence of the switch node voltages $u_1$ and $u_2$ on the input currents $i_{in}, i_1$ and $i_2$. The rectangular voltage sources can be divided into a common mode voltage component (cf. **Fig. 6(b)**)

$$u_{CM} = \frac{u_1 + u_2}{2} \tag{20}$$

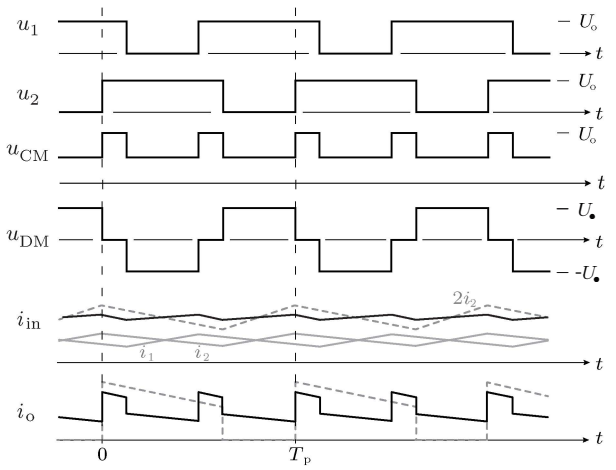


**Fig. 7:** Schematic waveforms of the operation of two parallel-interleaved phase shifted boost converters. Dashed lines denote the waveforms for operation without phase shift.

and a differential mode voltage component [19] (cf. **Fig. 6(c)**)

$$u_{DM} = \frac{u_1 - u_2}{2} \ . \tag{21}$$

Based on these equivalent circuits it can be concluded, that the input current of the system $i_{in}$ is only influenced by the common mode voltage component $u_{CM}$ (hence $i_{in} = i_{in,CM}$), whereas the current $i_{DM}$, driven by the differential mode voltage component $u_{DM}$, circulates only between the boost stages and does not contribute to the power transfer from the source to the load. The schematic waveform of those quantities (cf. **Fig. 7**) illustrates the similarity between the common mode voltage $u_{CM}$ of the parallel-interleaved boost converters and the voltage $u_\Sigma$ of the series-interleaved boost converters of **Fig. 3**. Both exhibit an effective switching frequency of $f_{sw,eff} = N_p \cdot f_{sw}$ or $f_{sw,eff} = N_s \cdot f_{sw}$, respectively. The harmonic spectrum of multiple parallel-interleaved boost converters can also be derived from the harmonic spectrum of a single boost converter. The spectrum of the common mode voltage $u_{CM}$ is basically identical to the spectrum of the single converter but contains only harmonics with orders that are multiples of the cell number $N_p$, as shown in **Fig. 8**. The spectrum of the differential mode voltage $u_{DM}$ contains the remaining harmonics, i.e. those harmonics of the original spectrum that are not present in the spectrum of $u_{CM}$. It is important to note, that the common mode voltage exhibits the same spectrum as the voltage $u_\Sigma$ of the series-interleaved boost converters for the same number of converter cells.

*Stored energy and converter volume:* The peak-to-peak current ripple of the inductor current in any of the parallel interleaved boost stages can be calculated for a given modulation index $M$ as

$$\Delta i_i = \frac{U_o \cdot M \cdot (1 - M)}{f_{sw} \cdot L} \tag{22}$$

whereas the DC value of the inductor current equals

$$I_i = \frac{I_{in}}{N_p} \tag{23}$$

under the assumption of equal power sharing between the parallel boost stages. The total peak energy stored in the inductors of a

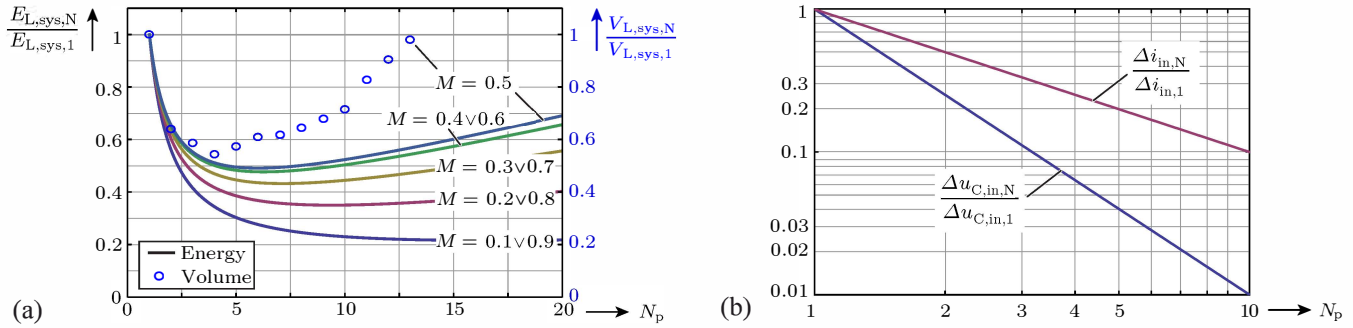


**Fig. 9:** Scaling laws of parallel-interleaved boost converters. (a) Dependency of the normalized total peak energy stored in the inductors ($E_{\mathrm{L,sys,N}}/E_{\mathrm{L,sys,1}}$) with the number of converter cells and the modulation index. The total normalized inductor volume ($V_{\mathrm{L,sys,N}}/V_{\mathrm{L,sys,1}}$) of parallel-interleaved boost converters is shown for $M = 0.5$ for efficiency-constrained designs with N87 core material and litz wires (cf. [20]). (b) Reduction of the normalized system input current ripple and normalized input voltage ripple with the number of converter cells.

system with $N_\mathrm{p}$ parallel-interleaved boost converters is

$$E_{\mathrm{L,sys,N}} = N_\mathrm{p} \cdot \frac{1}{2} \cdot L \cdot \left( I_i + \frac{\Delta i_i}{2} \right)^2 . \tag{24}$$

The energy stored in a system with interleaved boost converters can now be compared to the energy in single boost converter system as depicted in **Fig. 9(a)** for $U_\mathrm{o} = 400\,\mathrm{V}$, $L = 200\,\mu\mathrm{H}$, $f_\mathrm{sw} = 100\,\mathrm{kHz}$ and $I_\mathrm{in} = 15\,\mathrm{A}$. It has to be pointed out that for this and the following considerations the inductance $L$ of each converter cell is equal to the inductance of a single boost converter (i.e. resulting in an increased relative ripple of the inductor currents). The result shows that for each modulation index an optimum number of parallel-interleaved boost converters can be found where the total peak energy is minimized. The relation between stored energy in inductive components and their corresponding volume has been studied in [20] where it was shown that the inductor volume is largely proportional to the stored energy as long as low frequency losses dominate compared to high-frequency losses. The total inductor volume of parallel-interleaved boost converters with efficiency-constrained inductor designs is also shown in **Fig. 9(a)** for a modulation index of $M = 0.5$. Thus, for a fixed switching frequency, minimizing the total energy also minimizes the overall inductor volume until high frequency losses predominate.

The peak-to-peak current ripple of the input current can be derived for a given number of parallel boost converters $N_\mathrm{p}$ and an effective modulation index $M_\mathrm{eff} = (M \text{ modulo } 1/N_\mathrm{p})$ as

$$\Delta i_\mathrm{in} = \frac{U_\mathrm{o} \cdot N_\mathrm{p}}{f_\mathrm{sw} \cdot L} \cdot M_\mathrm{eff} \left( \frac{1}{N_\mathrm{p}} - M_\mathrm{eff} \right) . \tag{25}$$

with a maximum value at $M_\mathrm{eff} = 0.5/N_\mathrm{p}$ of

$$\Delta i_\mathrm{in,max} = \frac{U_\mathrm{o}}{4 f_\mathrm{sw} N_\mathrm{p} L} . \tag{26}$$

The ripple of the input current introduces a voltage ripple on the input capacitor $C_\mathrm{in}$ which can be calculated with the relation of $u = \int i \mathrm{d}t / C$ as

$$\Delta u_\mathrm{C,in,max} = \frac{\Delta i_\mathrm{in,max}}{4 N_\mathrm{p} f_\mathrm{sw} C_\mathrm{in}} = \frac{U_\mathrm{o}}{16 N_\mathrm{p}^2 f_\mathrm{sw}^2 C_\mathrm{in} L} \tag{27}$$

(assuming a constant current current drawn from the voltage source powering the converter system). These scaling laws are shown in **Fig. 9(b)** normalized to the values of a single boost converter system.

*Switching losses (Option 1):* The switching losses can be calculated by considering the overlap of voltages and currents of the switches of the multi-cell converter, as shown in **Fig. 10**. Based on the result of (26) the switching frequency of each stage can be reduced by a factor of $1/N_\mathrm{p}$ compared to the switching frequency of a single boost converter to obtain the same peak-to-peak amplitude of the input current. By assuming the same rates of $\mathrm{d}u/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ as in the single converter system the switching losses can be found to be

$$\begin{aligned} P_\mathrm{Sw,loss,Np} &= N_\mathrm{p} \cdot E_\mathrm{sw,cell} \cdot \frac{f_\mathrm{sw,1}}{N_\mathrm{p}} \\ &= N_\mathrm{p} \cdot \frac{1}{2} \cdot \left( \frac{T_{\mathrm{r},i}}{N_\mathrm{p}} + T_{\mathrm{f},u} \right) \cdot \frac{I_\mathrm{in}}{N_\mathrm{p}} \cdot U_\mathrm{o} \cdot \frac{f_\mathrm{sw,1}}{N_\mathrm{p}} \\ &= \frac{1}{2 N_\mathrm{p}} \cdot \left( \frac{T_{\mathrm{r},i}}{N_\mathrm{p}} + T_{\mathrm{f},u} \right) \cdot I_\mathrm{in} \cdot U_\mathrm{o} \cdot f_\mathrm{sw,1} . \end{aligned} \tag{28}$$

An upper boundary of the switching loss reduction can be found for low output voltage values, i.e. negligible times $T_\mathrm{f,u}$, thus the switching loss reduction lies in the range of

$$P_\mathrm{Sw,loss,Np} = \frac{P_\mathrm{Sw,loss,1}}{N_\mathrm{p}} \ldots \frac{P_\mathrm{Sw,loss,1}}{N_\mathrm{p}^2} \tag{29}$$

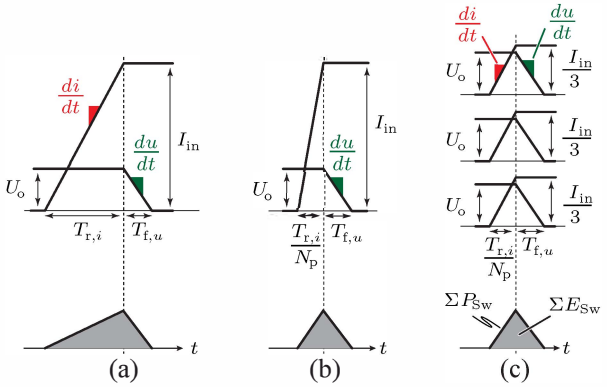


**Fig. 10:** Comparison of switching losses between a single boost converter (a) and parallel-interleaved boost convertes (c) for the same rates of $\mathrm{d}u/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$. The single boost converter can only reach the same level of switching losses as the parallel-interleaved converter, if the rate of $\mathrm{d}i/\mathrm{d}t$ is increased by a factor of $N_\mathrm{p}$ (b).

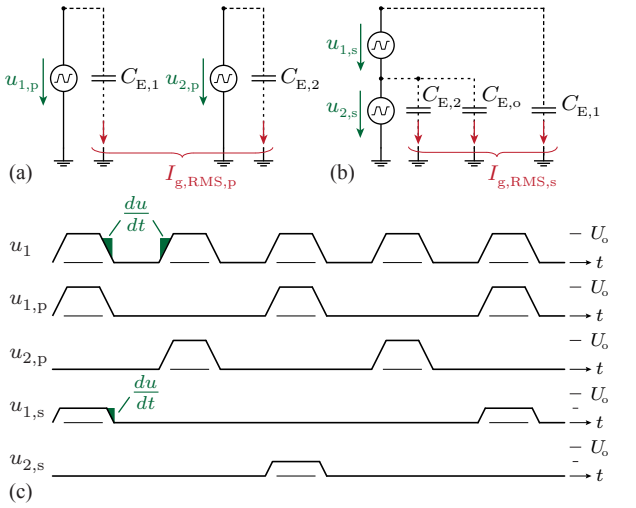


**Fig. 11:** Equivalent circuit model for ground currents of (a) the parallel-interleaved boost converter and (b) the series interleaved boost converter. The waveforms of the switch-node voltages of the parallel-interleaved system ($u_{1,p}$, $u_{2,p}$) and series-interleaved system ($u_{1,s}$, $u_{2,s}$) are compared to those of a single boost converter ($u_1$) in (c) under the assumption of same $du/dt$ in all systems.

*Switching losses (Option 2):* The calculation of the switching losses based on the energy stored in the parasitic transistor and diode capacitances yields for the system with parallel-interleaved boost converters

$$\begin{aligned} P_{\text{Sw,loss,Np}} &= N_\text{p} \cdot E_{\text{on,Np}} \cdot \frac{f_{\text{sw,1}}}{N_\text{p}} \\ &= \frac{1}{2} \cdot C_{\text{eff,Np}}(U_\text{o}) \cdot U_\text{o}^2 \cdot f_{\text{sw,1}} \end{aligned} \tag{30}$$

and/or

$$P_{\text{Sw,loss,Np}} = \frac{C_{\text{eff,Np}}(U_\text{o})}{C_{\text{eff,1}}(U_\text{o})} \cdot P_{\text{Sw,loss,1}} \ . \tag{31}$$

Since the switches and diodes in the parallel-interleaved boost converters have to be rated for the same voltage but for a lower current than the switch in the single boost converter, the employed Silicon area can be smaller and thus also the parasitic capacitances will be smaller and the capacitive switching losses will decrease.

## V. Ground Capacitances

The parasitic ground capacitances at the switch-nodes of the converters are a source for unwanted common mode currents which necessitate the application of common-mode filters, e.g. in PFC boost rectifiers, that substantially increase the volume of the converter. The voltage of the switch-node can be modeled with a trapezoidal wave voltage source that exhibits a certain $\mathrm{d}u/\mathrm{d}t$, as shown in **Fig. 11(a)** for the parallel-interleaved boost converter and in **Fig. 11(b)** for the series-interleaved boost converter with parasitic capacitances as defined in **Fig. 1**. A comparison of the voltage waveforms between the single boost converter ($u_1$), the parallel-interleaved ($u_{1,p}$, $u_{2,p}$) and the series-interleaved boost converter ($u_{1,s}$, $u_{2,s}$) is depicted in **Fig. 11(c)**. Based on the fundamental relationship of $I_\text{C} = C \cdot \mathrm{d}u/\mathrm{d}t$ the RMS value of the ground current of a single boost converter system through capacitor $C_\text{E}$ can be calculated as

$$I_{\text{g,RMS,1}} = \sqrt{2k} \cdot C_\text{E} \cdot \frac{\mathrm{d}u}{\mathrm{d}t} \text{ with } k = \frac{U_\text{o} \cdot f_\text{sw}}{\frac{du}{dt}} \ . \tag{32}$$

The switching frequency of the parallel-interleaved boost converters can be reduced by $1/2$ (for $N_\text{p} = 2$) for an equal current ripple amplitude (cf. (26)) leading to

$$k_\text{p} = \frac{U_\text{o} \cdot f_\text{sw}}{\frac{\mathrm{d}u}{\mathrm{d}t} \cdot 2} = \frac{k}{2} \ . \tag{33}$$

Under the assumption of $C_{\text{E,1}} = C_{\text{E,2}} = C_\text{E}$ the RMS value of the ground current can be found as

$$I_{\text{g,RMS,p}} = \sqrt{2} \cdot \sqrt{2k_\text{p}} \cdot C_\text{E} \cdot \frac{\mathrm{d}u}{\mathrm{d}t} = \sqrt{2k} \cdot C_\text{E} \cdot \frac{\mathrm{d}u}{\mathrm{d}t} \ . \tag{34}$$

For the series-interleaved system the switching frequency can be reduced by $1/4$ (for $N_\text{s} = 2$) for an equal current ripple amplitude (cf. (4)) and in combination with an voltage amplitude of only $U_\text{o}/2$ for each equivalent source results

$$k_\text{s} = \frac{\frac{U}{2} \cdot f_\text{sw}}{\frac{\mathrm{d}u}{\mathrm{d}t} \cdot 4} = \frac{k}{8} \ . \tag{35}$$

By super-position and again assuming $C_{\text{E,1}} = C_{\text{E,2}} = C_\text{E}$ the equation for the ground current yields

$$\begin{aligned} I_{\text{g,RMS,s}} &= \sqrt{2k_\text{s} \cdot \left((C_{\text{E,o}} + 2C_\text{E})\frac{\mathrm{d}u}{\mathrm{d}t}\right)^2 + 2k_\text{s} \cdot \left(C_\text{E}\frac{\mathrm{d}u}{\mathrm{d}t}\right)^2} \\ &= \frac{1}{2} \cdot \sqrt{k} \cdot \sqrt{(C_{\text{E,o}} + 2 \cdot C_\text{E})^2 + C_\text{E}^2} \cdot \frac{\mathrm{d}u}{\mathrm{d}t} \ . \end{aligned} \tag{36}$$

By relating the ground currents of multi-cell systems to the single boost converter it can be found that

$$\frac{I_{\text{g,RMS,p}}}{I_{\text{g,RMS,1}}} = 1 \tag{37}$$

$$\frac{I_{\text{g,RMS,s}}}{I_{\text{g,RMS,1}}} = \frac{1}{2\sqrt{2}} \sqrt{\left(2 + \frac{C_{\text{E,o}}}{C_\text{E}}\right)^2 + 1} \ . \tag{38}$$

This means that the RMS ground current of the series-interleaved system can only reach the same value as the parallel-interleaved system (and thus as the single boost converter) if $C_{\text{E,o}} = (\sqrt{7} - 2) \cdot C_\text{E} \approx 0.64 \cdot C_\text{E}$. This is rather unlikely since capacitance $C_{\text{E,o}}$ denotes the capacitance of the entire "upper" converter cell to ground, which is amongst others defined by the physical size of the entire converter cell. Thus, the series-interleaved boost converter system will potentially exhibit larger RMS ground currents.

The RMS value of the ground currents does not allow to extract any information about the frequency and the amplitude of the ground currents. Thus, in order to draw any conclusions for the design and volume of a common mode filter a more in depth analysis of the ground currents becomes indispensable, including a Fourier analysis to obtain the current spectrum for the different converter concepts. This will be investigated in a future publication in a more detailed and comprehensive way.

## VI. Conclusion

Based on the investigation of the scaling laws it can be summarized that both the series-interleaved as well as the parallel-interleaved approach offer considerable advantages in terms of conduction losses, switching losses and/or harmonic distortion compared to a single converter system. The parallel-interleaved concept also shows the same RMS values of the parasitic ground currents as the single converter. The series-interleaved converter,

however, exhibits most likely larger ground currents (depending on $C_{\mathrm{E,o}}$) since the converter cells are stacked and thus their potential referenced to ground also depends on the switching states of the lower converter cells in the converter stack.

The analysis of voltage and/or current balancing in multi-cell systems reveals that a common-duty cycle operation of all converter cells is applicable to ISOP and IPOS converters due to their self-balancing capabilities. For ISOS and IPOP converters the input voltage or input current sharing, respectively, needs to be ensured by an additional controller.

In conclusion, this paper has demonstrated that splitting a power electronic converter into multiple converter cells which share the system power equally can increase the overall system efficiency and power density. The benefits of multi-cell systems can be leveraged in many dimension e.g. to improve the harmonic spectrum of the converters and/or to obtain a reduction of the switching and conduction losses, depending on the choice of switching frequency of the individual cells compared to the switching frequency of the single converter. Since standard components with lower voltage and/or current ratings can be employed, the costs for a multi-cell system also decreases.

## APPENDIX A
## DERIVATION OF GENERAL SCALING LAWS

The efficiency of a power electronic system with input power $P_1$, output power $P$ and losses $P_{\mathrm{L}}$ is defined as

$$\eta = \frac{P}{P_1} = \frac{P}{P + P_{\mathrm{L}}} \Rightarrow P_{\mathrm{L}} = \frac{1-\eta}{\eta} P \ . \tag{39}$$

In the most simplified approach the power electronic system is considered to be a cube with surface $A$ which scales with the volume $V$ of the cube by $A = 6V^{2/3}$. The heat dissipation capability $p_{\mathrm{L}}$ of a system can be defined by relating the losses of a system to its surface area,

$$p_{\mathrm{L}} = \frac{P_{\mathrm{L}}}{A} = \frac{1-\eta}{\eta} \cdot \frac{P}{6V^{2/3}} \ . \tag{40}$$

This allows to derive fundamental scaling laws since any scaled system needs to have the same value of $p_{\mathrm{L}}$ as the reference system (denoted by subscript "$_0$"),

$$\frac{1-\eta}{\eta} \cdot \frac{P}{6V^{2/3}} = \frac{1-\eta_0}{\eta_0} \cdot \frac{P_0}{6V_0^{2/3}} \ . \tag{41}$$

Rearranging this equation yields

$$\frac{P}{P_0} = \frac{(1-\eta_0)}{(1-\eta)} \cdot \frac{\eta}{\eta_0} \cdot \left(\frac{V}{V_0}\right)^{2/3} \ . \tag{42}$$

By assuming a constant efficiency, i.e. $\eta = \eta_0$, the relation

$$\frac{V}{V_0} = \left(\frac{P}{P_0}\right)^{3/2} \tag{43}$$

can be found, whereas the condition of a constant power density, i.e. $\rho = P/V = \rho_0 = P_0/V_0$, leads to

$$\eta = \frac{\eta_0 \left(\frac{P}{P_0}\right)^{1/3}}{1 + \eta_0 \left(\left(\frac{P}{P_0}\right)^{1/3} - 1\right)} \ . \tag{44}$$

## REFERENCES


[1] S. Waffler and J. Kolar, "Comparative Evaluation of Soft-Switching Concepts for Bi-Directional Buck+Boost DC-DC Converters," in *Proc. of the International Power Electronics Conference (IPEC)*, pp. 1856–1865, 2010.

[2] IEC TR 62380, "Reliability data handbook - Universal model for reliability prediction of electronics components, PCBs and equipment," IEC, Tech. Rep., 2004.

[3] R. Giri, V. Choudhary, R. Ayyanar, and N. Mohan, "Common-Duty-Ratio Control of Input-Series Connected Modular DC-DC Converters with Active Input Voltage and Load-Current Sharing," *IEEE Trans. Ind. Appl.*, vol. 42, no. 4, pp. 1101–1111, 2006.

[4] W. van der Merwe and T. Mouton, "Natural Balancing of the Two-Cell Back-to-Back Multilevel Converter with specific Application to the Solid-State Transformer Concept," in *Proc. of the 4th IEEE Conf. on Industrial Electronics and Applications (ICIEA)*, pp. 2955–2960, 2009.

[5] H. Mouton, J. Enslin, and H. Akagi, "Natural Balancing of Series-Stacked Power Quality Conditioners," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 198–207, 2003.

[6] J. van der Merwe and H. du T Mouton, "An Investigation of the Natural Balancing Mechanisms of Modular Input-Series-Output-Series DC-DC Converters," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 817–822, 2010.

[7] W. Chen, X. Ruan, H. Yan, and C. Tse, "DC/DC Conversion Systems Consisting of Multiple Converter Modules: Stability, Control, and Experimental Verifications," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1463–1474, 2009.

[8] R. Ayyanar, R. Giri, and N. Mohan, "Active Input-Voltage and Load-Current Sharing in Input-Series and Output-Parallel Connected Modular DC-DC Converters Using Dynamic Input-Voltage Reference Scheme," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1462–1473, 2004.

[9] I. Batarseh, K. Siri, and H. Lee, "Investigation of the Output Droop Characteristics of Parallel-Connnected DC-DC Converters," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, pp. 1342–1351, 1994.

[10] S. Luo, Z. Ye, R.-L. Lin, and F. Lee, "A Classification and Evaluation of Paralleling Methods for Power Supply Modules," in *Proc. of the 30th IEEE Power Electronics Specialists Conference (PESC)*, vol. 2, pp. 901–908, 1999.

[11] M. Li, C. Tse, H. Iu, and X. Ma, "Unified Equivalent Modeling for Stability Analysis of Parallel-Connected DC/DC Converters," *IEEE Trans. Circuits Syst. II*, vol. 57, no. 11, pp. 898–902, 2010.

[12] Y. Huang, C. Tse, and X. Ruan, "General Control Considerations for Input-Series Connected DC/DC Converters," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 6, pp. 1286–1296, 2009.

[13] J. Huber and J. Kolar, "Optimum Number of Cascaded Cells for High-Power Medium-Voltage Multilevel Converters," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, pp. 359–366, 2013.

[14] F. Udrea, "Future and Expected Applications of Si Power Devices," in *ECPE Workshop Future Trends for Power Semiconductors, Zurich*, 2012.

[15] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. W. De Doncker, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Springer, 2011.

[16] J. Kolar, "What are the Big Challenges in Power Electronics," in *Proc. of 8th International Conference on Integrated Power Electronic Systems (CIPS) Keynote presentation*, 2014.

[17] M. Henini and M. Razeghi, *Optoelectronic Devices: III Nitrides*. Elsevier Science & Technology, 2004.

[18] F. Krismer, "Modeling and Optimization of Bidirectional Dual Active Bridge DC-DC Converter Topologies," Ph.D. dissertation, Power Electronic Systems Laboratory, ETH Zurich, 2008.

[19] S. Utz and J. Pforr, "Current-Balancing Controller Requirements of Automotive Multi-Phase Converters with Coupled Inductors," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 372–379, 2012.

[20] R. Burkart, H. Uemura, and J. W. Kolar, "Optimal Inductor Design for 3-Phase PWM Converters Considering Different Magnetic Materials and a Wide Switching Frequency Range," in *Proc. of the International Power Electronics Conference (IPEC)*, 2014.