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***Abstract*—Single-phase inverters and rectifiers in $230\,\mathrm{V_{rms}}$ applications, with a DC-side voltage of $400\,\mathrm{V}$, achieve ultra-high-efficiency with a simple 2-level topology. These single-phase designs typically utilize a line-frequency unfolder stage, which has very low losses and essentially doubles the peak-to-peak voltage that can be generated on the AC-side for a given DC-link voltage. For certain applications, however, such as higher-power grid-connected photovoltaic inverters, electric vehicle chargers and machine drives, three-phase converters are needed. Due to the three-phase characteristic of the system, unfolders cannot be similarly used, leading to a higher minimum DC-link voltage of the three-phase line-to-line voltage amplitude, which is typically set to $800\,\mathrm{V}$ for $230\,\mathrm{V_{rms}}$ phase voltage systems. Previous demonstrations indicate that significantly more levels – and the associated higher cost and complexity – are required for ultra-high-efficiency three-phase converters relative to their single-phase counterparts. In this work, we seek to determine the fundamental reason for the performance difference between three-phase, $800\,\mathrm{V}$ DC-link and single-phase, $400\,\mathrm{V}$ converters. First, we build a $2.2\,\mathrm{kW}$ DC/AC hardware demonstrator to confirm the necessity of higher-complexity converters, showing a simultaneous reduction in efficiency and power density between a 2-level, $400\,\mathrm{V}$ benchmark ($99.2\,\%$ peak efficiency at $18.0\,\mathrm{kW/l}$) and a 3-level, $800\,\mathrm{V}$ inverter phase-leg ($98.8\,\%$, $9.1\,\mathrm{kW/l}$). With the motivation confirmed, we derive general scaling laws for bridge-leg losses across number of levels and DC-link voltage, finding the efficiency-optimal chip area and the minimum semiconductor losses. With commercially-available Si or GaN power semiconductors, the scaling laws indicate that 6 or more levels would be required for an $800\,\mathrm{V}$, three-phase AC/DC converter to meet or exceed the bridge-leg efficiency of a 2-level, $400\,\mathrm{V}$ GaN benchmark for a fixed output filter. With a complete Pareto optimization, we find that at least 7-levels are necessary to recover the efficiency of the 2-level, $400\,\mathrm{V}$ benchmark, and we validate this theory with a 7-level, $800\,\mathrm{V}$, $2.2\,\mathrm{kW}$ hardware prototype with a power density of $15.8\,\mathrm{kW/l}$ and a peak efficiency of $99.03\,\%$. Finally, two practical solutions that make use of the benefits of unfolder bridges familiar in single-phase systems are identified for three-phase systems.**

***Index Terms*— AC/DC power converters, Three-phase electric power, Single-phase electric power, Scaling laws, Flying capacitor multilevel (FCML), Gallium Nitride (GaN).**

I. Introduction

Ultra-efficient and power-dense AC/DC and DC/AC power converters are critical for a broad range of emerging applications, from renewable energy converters [1] to more-electric aircraft motor drives [2], [3] to power-factor-correction (PFC) rectifiers [4], [5]. Single-phase inverters and rectifiers, such as the bridgeless totem-pole PFC rectifier shown in **Fig. 1a**, typically include an unfolder bridge-leg to provide a return path for the current, that operates at line-frequency ($50\,\mathrm{Hz} - 60\,\mathrm{Hz}$) and can therefore be designed for very low conduction losses [6]. This unfolder essentially doubles the "effective" output voltage from the DC-link voltage, U_{dc}, to $2U_{\mathrm{dc}}$ without increasing the semiconductor or capacitor voltage stresses, allowing single-phase designs for $230\,\mathrm{V_{rms}} - 240\,\mathrm{V_{rms}}$ lines to operate with DC-link voltages near $400\,\mathrm{V} - 450\,\mathrm{V}$ (with around $20\,\%$ voltage margin), as shown in **Fig. 1b**.

These single-phase systems, however, are limited by $16\,\mathrm{A_{rms}}$ feeds to $3.7\,\mathrm{kW}$, and by the less-common $32\,\mathrm{A_{rms}}$ outlets to $7.4\,\mathrm{kW}$ [7]. Therefore, for applications that require higher power ratings such as residential photovoltaic (PV) inverters, electric vehicle (EV) chargers and machine drives, a three-phase $230\,\mathrm{V_{rms}} - 240\,\mathrm{V_{rms}}$ (line-to-neutral) interface is required, where oftentimes the power that each one of the three phases processes is similar to that of single-phase systems [7]–[9]. In contrast to single-phase systems, however, three-phase inverters and rectifiers (**Fig. 1c**) cannot straightforwardly utilize a similar unfolding technique, given that the current that is generated in one of the phases is returned through the other two phases. In these systems, the DC-link voltage must be doubled to near $720\,\mathrm{V} - 800\,\mathrm{V}$ [10], as shown in **Fig. 1d**, as the AC voltage is generated against the DC-link midpoint. For the same AC power and phase voltage, then, three-phase systems will have lower DC current but at the penalty of doubled voltage stresses on the key components, as the high-frequency bridge-leg must generate both the positive- and negative-polarity AC cycles.

For $400\,\mathrm{V}$ DC-link voltage single-phase systems (used, for example, in data center power supply modules or solar inverters), a literature review finds that a simple "2-level" half-bridge (**Fig. 2a**) can deliver efficiencies above $99\,\%$ [5], [6], [11] and as high as $99.1\,\%$ [12]. Designs with more levels and/or interleaved stages – a preferred approach in the Google Little Box Challenge [13] – achieve higher power densities through output filter size reduction [2], [4], [14]–[18], but these higher-complexity designs generally do not improve upon the efficiency of a 2-level design.

Ultra-high-efficiency three-phase $800\,\mathrm{V}$ DC-link voltage inverters and rectifiers shown in literature, however, feature much higher complexities. In [19], a 5-level E-type converter reaches a peak efficiency of $98.3\,\%$. Similarly, in Ref. [20], 13-levels are used to achieve $98.3\,\%$ peak efficiency with low-voltage GaN devices. Ref. [21] utilizes a 5-level T-type inverter with $1200\,\mathrm{V}$ SiC devices for $99.2\,\%$ peak AC/DC efficiency at $720\,\mathrm{V}$ input voltage, and an all-Silicon, 7-level design in [22] peaks at $99.3\,\%$ efficiency at the same $720\,\mathrm{V}$ input voltage.

The interest naturally arises, then, to assess the fundamental reason behind the performance difference between simple 2-level single-phase systems, which can operate with $400\,\mathrm{V}$ DC-links due to the (nearly lossless [5], [23]) unfolder stage, and three-phase systems, where the required DC-link voltage is near $800\,\mathrm{V}$ and the ultra-high-efficiency converters presented in literature feature a more complex multi-level structure (to the authors' knowledge, the only $800\,\mathrm{V}$ DC-link systems that exceed $99\,\%$ efficiency feature five or more levels). Hence, our goal is to assess if 3-levels are "enough" for an $800\,\mathrm{V}$ DC-link voltage system to recover the performance of a $400\,\mathrm{V}$ DC-link voltage system, or if this can only be achieved by using a

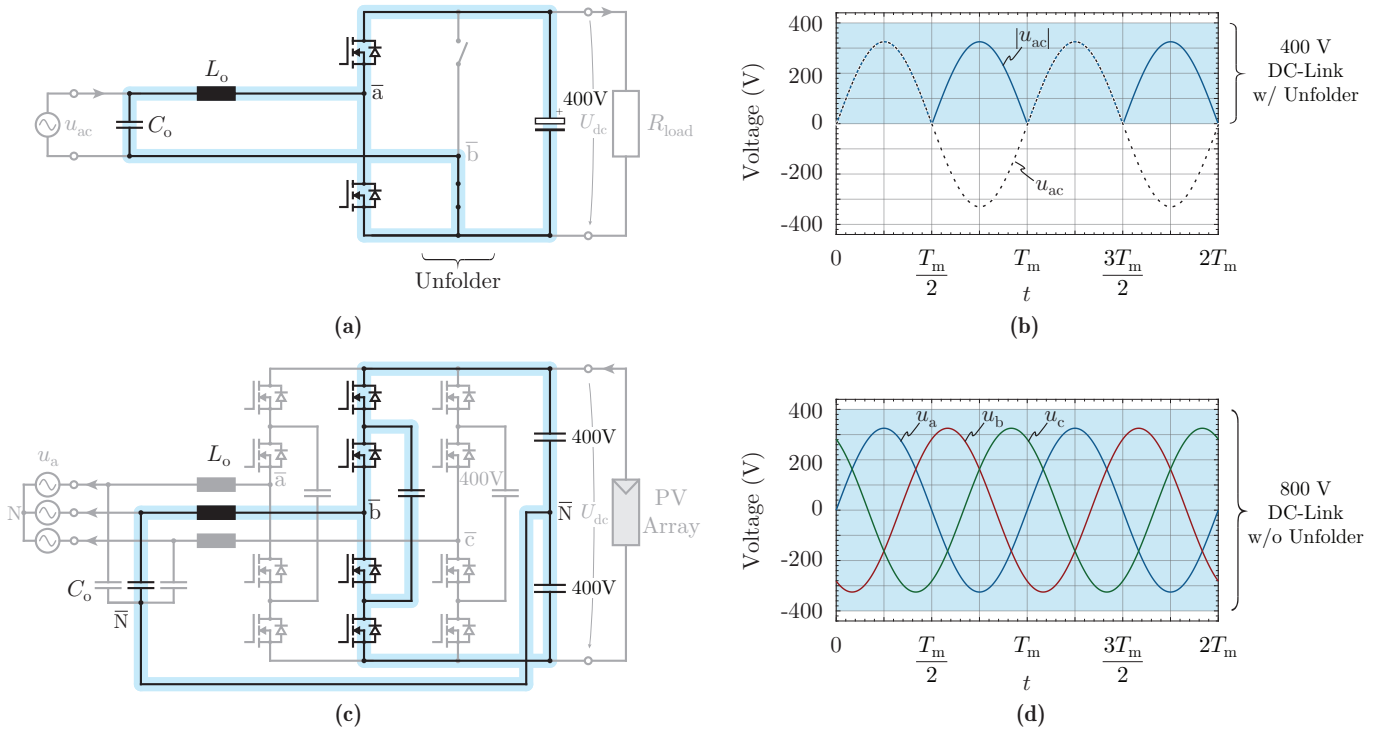


Fig. 1: Comparison between high-frequency bridge-legs in single-phase and three-phase grid-tied converter systems. **(a)** Single-phase, 2-level, totem-pole, power-factor-correction (PFC) rectifier, with a high-frequency bridge-leg (highlighted) and a line-frequency unfolder (which is typically implemented with Si-SJ MOSFETs and is only conceptually indicated) used to generate a bipolar output. Output capacitance must be sized to provide power pulsation buffering. **(b)** Typical voltage waveforms (for two line periods T_m) of a 230 V_{rms} single-phase PFC rectifier like in **(a)**, where the continuous line represents the rectified sinusoidal voltage $|\ u_{ac}\ |$ and the dashed line represents the single-phase grid voltage u_{ac}. The unfolder permits operation with a 400 V − 450 V DC-link for a 230 V_{rms} phase voltage. **(c)** Three-phase grid-tied flying capacitor multi-level (FCML) inverter with three levels, shown for a solar photovoltaic (PV) application, with one of the three high-frequency bridge-legs highlighted. With a 3-level configuration, identical semiconductors with > 400 V voltage ratings can be used in **(c)** as in **(a)**. The DC-link capacitor does not need to provide power pulsation buffering due to the overall constant power flow of three-phase systems. **(d)** Typical voltage waveforms of a 230 V_{rms} line-to-neutral three-phase PFC rectifier like in **(c)**, where the three-phase grid voltages u_a, u_b and u_c are shown. For the three-phase system case, a 720 V − 800 V DC-link is required to generate the 230 V_{rms} phase voltages.

higher number of levels. For this, we center our comparison on multi-level converters, and in particular on the flying capacitor multi-level (FCML) topology (**Fig. 1c**) [15], [24], [25], which is capable of generating DC outputs and is gaining interest in both single- and three-phase systems to achieve ultra-high-efficiency and/or power density. Compared to a conventional half-bridge (**Fig. 1a**), multi-level converters:

- increase the effective frequency (f_{eff}) at the output filter for a given switching frequency (f_{sw}), reducing the passive component size [26],
- decrease the voltage applied to the filter inductor, lowering the applied volt-seconds and further reducing the filter size, and
- enable the use of lower-voltage power semiconductors, which are inherently less lossy than a higher-voltage counterpart [27].

It is important to note that increasing the level of converter designs to improve efficiency may carry, for particular applications, penalties in power density, cost, and/or reliability and maintenance [10], [28]. In all power electronics designs, these requirements are in competition, with the respective weight given to each determined by the application. However, there is a broad trend towards ultra-high-efficiency in emerging applications, including solar PV and data center power supplies, where efficiency ranks highest amongst the key performance metrics and decreasing losses can result in lower overall life cycle cost [29]. Ultra-high-efficiency multi-level designs may, further, improve reliability through the elimination of active cooling components and overall lower operating temperatures [22], and the increasing integration of gate drives with power semiconductors will reduce a significant complexity penalty in current designs [30], [31]. This work, overall, seeks efficiency-optimized designs in the analytical derivation (before adding power density during a Pareto optimization) with a target towards these critical efficiency-maximized applications.

To more deeply analyze the performance difference between the single-phase 400 V DC-link voltage and the three-phase 800 V DC-link voltage cases presented in **Fig. 1a-c**, we start by analyzing the individual bridge-legs, shown in **Fig. 2a-b**, respectively. When moving from a 400 V DC-link to an 800 V DC-link for a three-phase system, as a first step towards a multi-level approach, we can add a third level to mitigate the component stress increase and reuse the same power switches and output filter (**Fig. 2b**) [32]. With f_{sw} halved and all other components kept the same, the output filter waveforms (f_{eff} and current ripple magnitude, Δi_L, and voltage ripple magnitude, Δu_{ac}) are identical (**Figs. 2c-d**), and therefore the filter losses and performance do not change (assuming the filter capacitor star point is connected to the DC-link midpoint [33], as shown in **Fig. 2b**). Output current now flows through two devices instead of one, doubling the conduction losses, and the hard-switching losses are kept constant (since the switched current is the same in both cases across all switching cycles). Due to the 2× higher conduction losses and additional components, the 800 V, 3-level design must have lower efficiency and lower power density than a 400 V, 2-level bridge-leg. With the chip area re-optimized (and increased) for the 3-level design, the increase in losses is slightly smaller than the increase in this case of identical switches, but the 400 V, 2-level bridge-leg

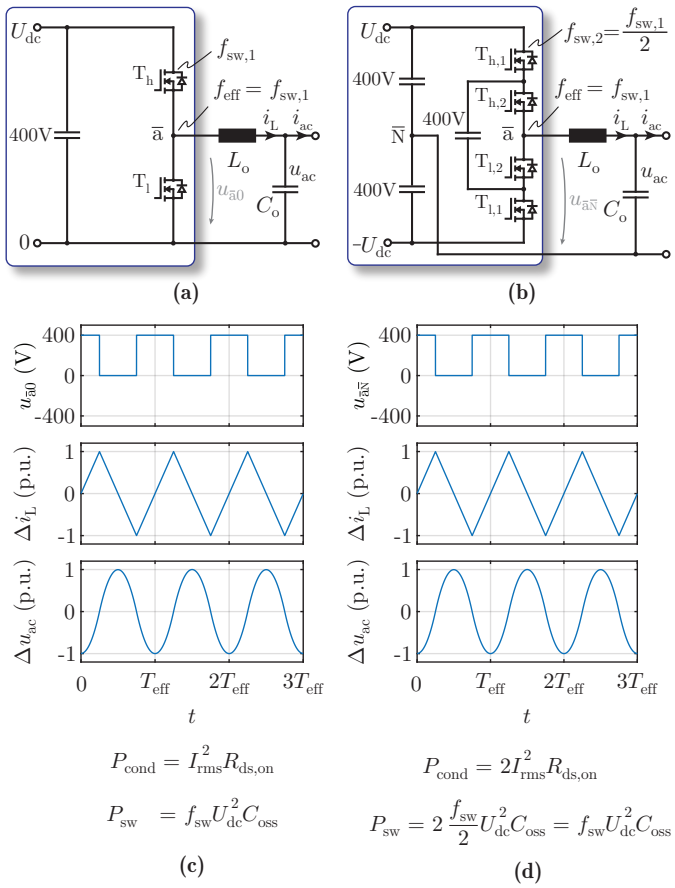


Fig. 2: Comparison of power circuits and key waveforms between 400 V DC-link, 2-level and 800 V DC-link, 3-level FCML designs. **(a)** 2-level, 400 V DC-link converter circuit, with the line-frequency unfolder in **Fig. 1a** removed to highlight the high-frequency bridge-leg comparison. **(b)** 3-level, 800 V DC-link FCML converter circuit, with the switching frequency (f_{sw}) halved to keep the same output frequency, inductor current ripple, and capacitor voltage ripple. **(c)** Key normalized waveforms and semiconductor losses for the 2-level, 400 V benchmark. **(d)** Key normalized waveforms and semiconductor losses for the 3-level, 800 V design, referenced to the DC-link midpoint $\overline{\text{N}}$. With the same power devices, conduction losses double and capacitive switching losses remain the same when moving to the 800 V DC-link in three-phase converters.

will still outperform the 800 V, 3-level design, as we show in detail later in the paper. In this analysis, and for the remainder of the paper, we ignore the losses in any unfolder stages. This approximation is valid because the unfolder stages switch at line frequency, hundreds or thousands of times slower than the bridge-leg semiconductors, and therefore incur negligible switching losses. Without switching losses as a tradeoff, the die area of the unfolder power semiconductors can be increased to nearly eliminate conduction losses and therefore any unfolder-stage cooling requirements. A more detailed justification of neglecting the unfolder stage losses is included in **Section II** and Ref. [23].

While our simple analysis in **Fig. 2** shows that three-levels are clearly not enough for ultra-high-efficiency at 800 V, the number of levels for a given efficiency target is not known from existing literature. Refs. [26], [34] aim to keep the semiconductor losses constant and optimize the output filter, and general design criteria for multi-level converters are included in [24], [25], [35], [36]. Here, we instead fix the output filter and optimize an FCML bridge leg across DC-link voltage (U_{dc}), number of levels ($N+1$), semiconductor die area (A_{die}), and device technology (GaN, SiC, or Si), analytically deriving simple scaling laws to elucidate the key tradeoffs and to find the required number of levels for an ultra-high-efficiency 800 V system.

In **Section II**, we build and characterize 2-level, 400 V and 3-level, 800 V DC/AC converters to verify the intuition that three levels are indeed "not enough," motivating the remainder of the work. In **Section III**, we derive scaling laws for FCML converters with a fixed output filter, highlighting tradeoffs in input voltage, complexity, efficiency, and semiconductor technology. **Section IV** discusses the correct output filter constraints and stresses for a fair comparison, including adhering to electromagnetic interference (EMI) regulations. **Section V** uses an efficiency versus power density Pareto optimization to ascertain the required number of levels for ultra-high-efficiency 800 V FCML converters, and in **Section VI** we build and characterize a Pareto-optimized 7-level, 800 V inverter to validate that the theorized 7-levels are "enough" to regain the efficiency of the 2-level, 400 V benchmark. **Section VII** highlights paths forward for ultra-high-efficiency three-phase inverters and rectifiers through a system-wide lens.

II. Hardware Validation: 3 Levels are Not Enough

To validate the intuition that 3-levels are indeed not enough for an 800 V DC-link bridge-leg to recover the efficiency (or power density) of a 2-level, 400 V benchmark, we construct a loss-optimized 2.2 kW DC/AC converter shown in **Fig. 3c** which can be used for the 3-level 800 V (**Fig. 3b**) as well as for the 2-level 400 V (cf., **Fig. 3a**, operation limited to cyclic repetition of the positive half-cycle of an actual single-phase PFC rectifier system). The design details are shown in **Table I**. These inverters utilize 35 mΩ, 600 V GaN-on-Si HEMTs and film capacitors. Note that using for the converter in **Fig. 3c** the ceramic capacitors utilized in **Section VI**, the volume of the flying capacitors could be decreased by approximately a factor ×3 at a ×10 higher cost, but would not change the key bridge-leg comparison. The 3-level design operates with half the switching frequency ($f_{\text{sw}} = 35$ kHz) of the 2-level design ($f_{\text{sw}} = 70$ kHz, selected to be similar to previous literature and existing commercial designs, e.g. [12]), keeping in **Fig. 3** identical output filter waveforms as described in **Fig. 2**.

The measured DC/AC efficiencies for each design are reported in **Fig. 4a**, and, as expected, the three-level, 800 V design has both lower efficiency and, because of the extra semiconductor stage for the 3-level characteristic and the flying capacitor, lower power density (see **Table I**). Efficiencies are measured with the *Yokogawa WT3000* precision power analyzer, which is shown in [22] to have excellent agreement with calorimetric techniques in this efficiency and output power range. The peak efficiency for the 2-level, 400 V inverter is 99.2 %, and the peak efficiency for the 3-level, 800 V inverter is 98.8 %. Both efficiencies are relatively flat from 40 % to 120 % load. The power pulsation buffer capacitors and unfolder stage necessary for single-phase conversion are both excluded from the efficiency measurements and reported power densities, as the goal of this study is to compare the bridge-legs in single-phase and three-phase systems. The exclusion of the unfolder can be justified considering two aspects: losses and costs. A typical single-phase 400 V power supply features a high switching frequency bridge-leg realized with GaN devices, and a low-frequency (mains frequency) unfolder bridge-leg implemented with Silicon Superjunction (Si-SJ) devices to save costs [12]. Taking as example for the unfolder realization the lowest $R_{\text{ds,on}}$ class Si-SJ devices available in the market (34 mΩ devices at a junction temperature of $T_{\text{j}} = 125\,^{\circ}\text{C}$ [37], [38]), the losses would be around 3.8 W, incurring a 0.19 % efficiency penalty at 2.0 kW, cf.,

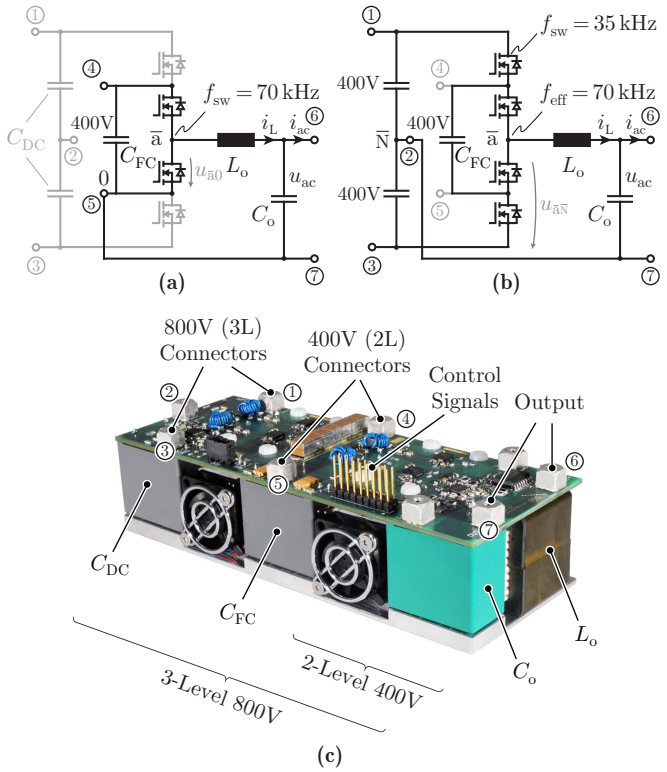


Fig. 3: **(a)** 2-level ("2L") 400 V and **(b)** 3-level ("3L") 800 V hardware connection schematics of the **(c)** loss-optimized 2.2 kW DC/AC inverter used for experimental 2L, 400 V and 3L, 800 V comparison (cf., **Fig. 2**). 2-level inverter operates at $f_{sw} = 70\,\text{kHz}$ and 3-level inverter operates at $f_{sw} = 35\,\text{kHz}$ to maintain the same f_{eff}. 2-level size is $61\,\text{mm} \times 59\,\text{mm} \times 34\,\text{mm}$ ($18.0\,\text{kW/l}$), and 3-level size is $121\,\text{mm} \times 59\,\text{mm} \times 34\,\text{mm}$ ($9.1\,\text{kW/l}$).

Fig. 4a. To analyze the cost of the unfolder bridge-leg, an electrical conductance related cost can be defined as

$$\sigma_G = \frac{\frac{Cost}{A_{die}}}{\frac{G_{ds}}{A_{die}}} = \frac{Cost}{G_{ds}} \left[\frac{\$}{\text{m}\Omega^{-1}}\right] = Cost \cdot R_{ds}\,[\$ \cdot \text{m}\Omega]\ , \qquad (1)$$

where $G_{ds} = R_{ds}^{-1}$ is the electrical on-state conductance in $[\text{m}\Omega^{-1}]$, A_{die} is the die area of a given device, and diea area proportional costs are assumed. Taking the aforementioned $34\,\text{m}\Omega$ (at $T_j = 125\,^\circ\text{C}$) Si-SJ devices [37], $\sigma_{G,\text{Si-SJ}} = 439$ \$·mΩ, whereas the $110\,\text{m}\Omega$ (at $T_j = 125\,^\circ\text{C}$) GaN devices [39] feature $\sigma_{G,\text{GaN}} = 1694$ \$·mΩ, indicating for the current state-of-the-art a factor $\times 3.9$ cost advantage of the Si-SJ technology (cost data obtained from [38] for a MOQ of 1000 pcs.).

The key measured waveforms are shown in **Fig. 5**, where we highlight the naturally balanced flying capacitor [40] in the 3-level design and identical output waveforms in each design, ignoring the unipolar current in the 2-level design due to the excluded unfolder stage.

We can compare the measured efficiency difference between the designs to that predicted by the simple, intuitive model of **Fig. 2**, and the predicted loss breakdown for each design is shown in **Fig. 4b-c**. We measure 15.5 W of total losses in the 2-level design at 2 kW of output power, a deviation of only 1.1 W from the predicted losses. In the 3-level design, the measured losses (24.2 W) are 3.7 W higher than the modeled losses, an efficiency error of 0.19 %. These additional losses are partially attributed to the increased parasitic capacitance that arises by having the flying capacitors and the switch pair closest to the switch node $u_{\bar{a}0}$ ($T_{h,2}$, $T_{l,2}$ in **Fig. 2b**) jumping in potential with respect ground. This parasitic capacitance was measured to be 70 pF, which besides increasing the hard-switching losses, extends the partial (or incomplete) soft-switching regime to higher currents [41], and degrades the efficiency across the line cycle. This hardware demonstration, at its core, validates our intuition that 3-levels are "not enough" for inverters and rectifiers in three-phase, 800 V DC-link applications to match the performance of single-phase bridge-legs in 400 V DC-link applications. With a fixed output filter, the 3-level bridge-leg efficiency will always be less than the 2-level, 400 V design due to the increased conduction losses. With the motivating intuition validated, we move to the defining question of the work - how many levels are enough for an 800 V DC-link bridge-leg to recover the efficiency of a 400 V, 2-level benchmark? To answer this question, we first derive the key bridge-leg scaling laws for an arbitrary number of levels, DC-link voltage, and power semiconductor.

TABLE I: Components, key values, and performance metrics for the constructed DC/AC inverters of **Figs. 4** and **5**. Component labels reference **Fig. 2**.

Parameter	400 V, 2-Level	800 V, 3-Level
U_{dc}	400 V	800 V
f_{sw}	70 kHz	35 kHz
P_o	2.2 kW	
Power semicond.	35 mΩ 600 V IGOT60R035D1, *Infineon*	
Gate driver	1EDF5673K, *Infineon*	
Filter inductor, L_o	58 µH N87 3x Stacked E32x16x9 Litz Wire 630x71 µm, 16 turns	
Filter capacitor, C_o	4.7 µF (film) F861FR475M310ZLH0J	
Flying capacitors	–	4x10 µF (film) C4AEGBU5100A1YJ
Fan	1x ⌀25 mm, 0.6 W	2x ⌀25 mm, 0.6 W
Heatsink	1x $(25 \times 28 \times 42)\,\text{mm}^3$	2x $(25 \times 28 \times 42)\,\text{mm}^3$
Power density	18.0 kW/l	9.1 kW/l
Peak efficiency	99.2 %	98.8 %

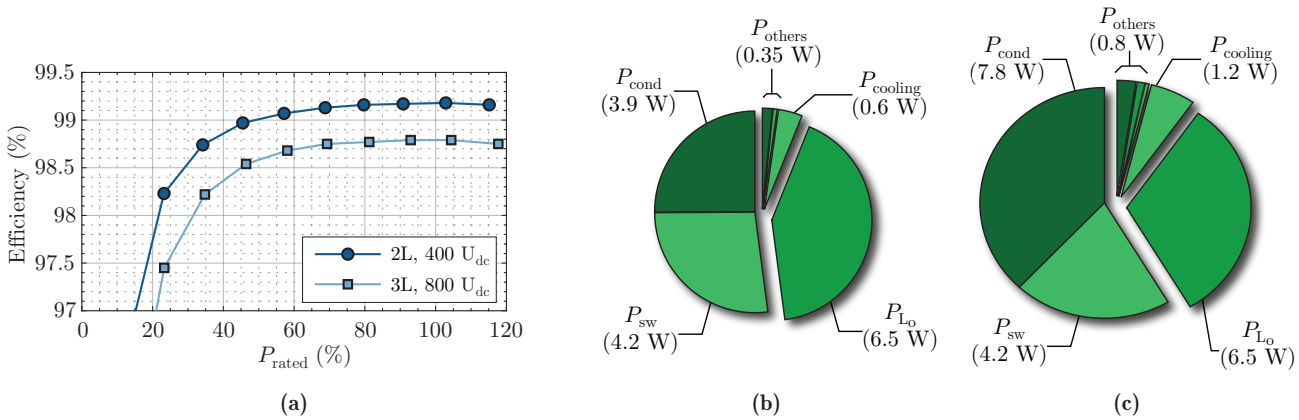
III. Efficiency-Optimized Bridge-Leg Scaling Laws

As shown in **Fig. 2**, the losses in the semiconductors in a hard-switched two-level converter are [4]:

$$P_{semi} = I_{rms,ac}^2 \frac{R'_{ds}(U_{dc})}{A_{die}} + f_{sw} U_{dc}^2 C'_Q(U_{dc}) A_{die}, \qquad (2)$$

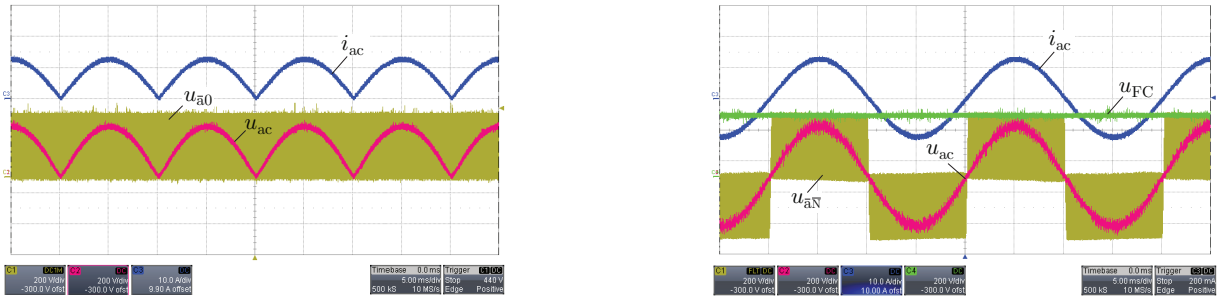
with $R'_{ds}(U_{dc})$ the specific on-resistance at blocking voltage rating U_{dc}, $C'_Q(U_{dc})$ the specific charge-equivalent capacitance at the same voltage rating, and f_{sw} the switching frequency of an individual transistor.. U_{dc} is the DC-link voltage and $I_{rms,ac}$ is the RMS output current. The charge-equivalent capacitance is the correct linear equivalent to evaluate the capacitive switching losses, since Ref. [41] shows that the minimum switching losses $E_{sw,min}$ occurring during hard-switching are related to the output capacitance charge Q_{oss} by $E_{sw,min} = U_{dc} Q_{oss}(U_{dc}) = U_{dc}^2 C_Q(U_{dc})$. These losses accurately coincide with the zero current switching losses [41]–[43]. Note that both Q_{oss} and C_Q are voltage-dependent due to the non-linearity of the output capacitance C_{oss} [41]. Eqn. (2), then, provides a first approximation to find the optimal chip area, with losses from the voltage-current overlap period during hard-switching and reverse-recovery losses both ignored. These are valid approximations for wide-bandgap devices, which have very fast switching speeds and zero (GaN HEMTs) or nearly negligible (SiC MOSFETs) reverse-recovery charge, particularly for currents much smaller than the rated current of the devices [4]. Gate driving losses are safely ignored as negligible.

For an $(N+1)$-level converter ($2N$ identical switches per bridge-leg), the losses are:



(a) (b) (c)

Fig. 4: **(a)** Measured DC/AC efficiency for the 2-level, 400 V and 3-level, 800 V inverters from 20 % – 120 % load. Efficiency measurements include fan and gate drive power and exclude losses in power pulsation buffer capacitors to emphasize the bridge-leg comparison between single- and three-phase systems. Peak efficiency for the 2-level, 400 V inverter is 99.2 % at 2.25 kW. Peak efficiency for the 3-level, 800 V inverter is 98.8 % at 2.25 kW. Expected loss breakdown at 90 % load (2 kW) for the **(b)** 2-level, 400 V U_{dc} inverter (predicted losses: 15.5 W, measured losses: 16.6 W) and the **(c)** 3-level, 800 V U_{dc} inverter (predicted losses: 20.5 W, measured losses: 24.2 W). P_{others} includes gate driver, output capacitor (C_{o}), and flying capacitor losses. P_{cooling} is fan power consumption. The 3-level, 800 V U_{dc} conduction losses are 2× higher than the 2-level conduction losses, and the switching losses are identical.



(a) (b)

Fig. 5: **a)** Key measured waveforms at 90 % load (2 kW) for the 2-level, 400 V inverter. **b)** Key measured waveforms at 90 % load (2 kW) for the 3-level, 800 V inverter. Labels are referenced to **Fig. 2**. The output waveforms are identical with the exception of an unfolder for the 2-level inverter. Without a bipolar output, one switch in the 2-level design will hard-switch more often than its bridge-leg counterpart, while in the 3-level design, the hard- and soft-switching periods will be symmetric. This asymmetry has a negligible effect on device heating and, therefore, also a negligible effect on measured efficiency.

$$P_{\text{semi}} = I_{\text{rms,ac}}^2 N \frac{R'_{\text{ds}}\left(\frac{U_{\text{dc}}}{N}\right)}{A_{\text{die}}} + N f_{\text{sw}} \left(\frac{U_{\text{dc}}}{N}\right)^2 C'_{\text{Q}}\left(\frac{U_{\text{dc}}}{N}\right) A_{\text{die}}. \quad (3)$$

A known advantage of multi-level converters is the use of lower voltage switches, and we highlight the reduction of blocking voltage from U_{dc} to U_{dc}/N. From **Appendix A**, the functions of capacitance and resistance can be rewritten as:

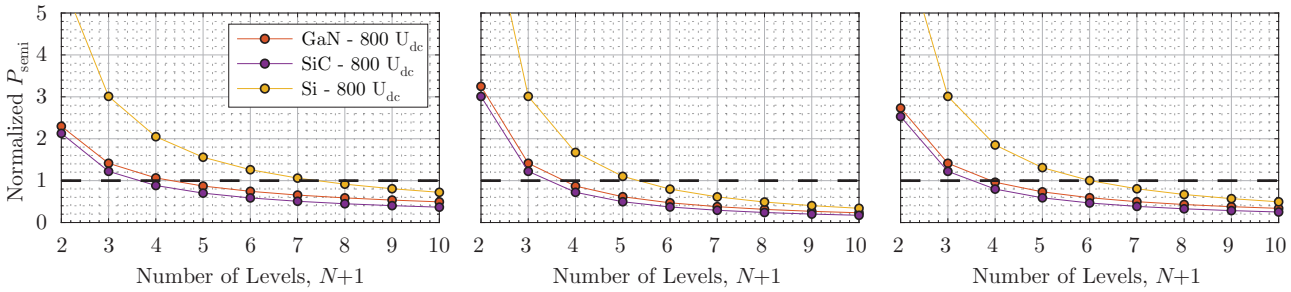
$$R'_{\text{ds}}\left(\frac{U_{\text{dc}}}{N}\right) = \frac{R'_{\text{ds}}(U_{\text{dc}})}{N^{\alpha_{\text{R}}}} \quad (4)$$

$$C'_{\text{Q}}\left(\frac{U_{\text{dc}}}{N}\right) = \frac{C'_{\text{Q}}(U_{\text{dc}})}{N^{\alpha_{\text{C}}}}. \quad (5)$$

α_{r} and α_{c} are exponential scaling factors of, respectively, R'_{ds} and C'_{Q}, with rated blocking voltage. These are empirically fit for candidate technologies – GaN-on-Si HEMTs, SiC MOSFETs, and Si MOSFETs – in **Fig. 17** and reported in **Table V**. For silicon power devices, MOSFETs are preferred to IGBTs for the considered ultra-high-efficiency applications in this switching frequency range, as these unipolar devices have much lower switching losses than IGBTs due to the elimination of the dominant current-tailing effect [44]. Further, inverter circuits that utilize IGBTs require additional anti-parallel diodes, while MOSFETs inherently include this reverse conduction characteristic and therefore achieve overall smaller footprints. Previous work on optimization ignores the scaling of C'_{Q} with voltage [26], [34], [35], but the increase of C'_{Q} at lower breakdown voltages is non-negligible and influential. For now, we assume that the semiconductor voltage rating can be precisely chosen as U_{dc}/N, although this constraint is relaxed later for a practical implementation with the discrete blocking voltages available in commercial devices.

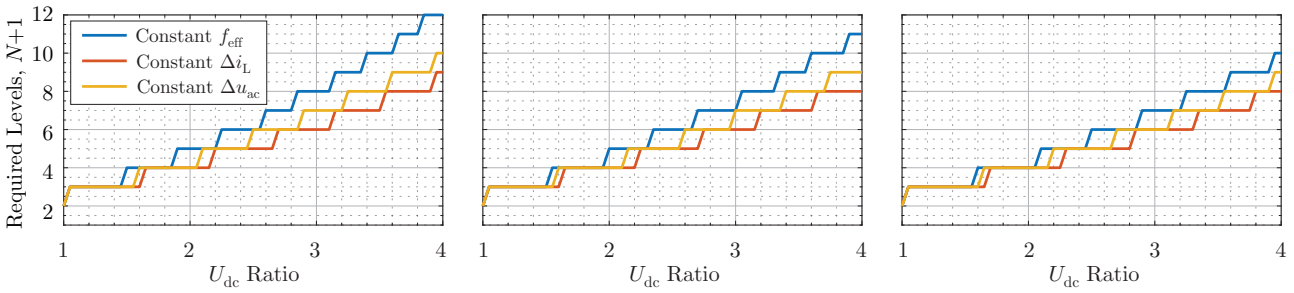
The assumptions underlying the subsequent derivation – many of which are explicitly relaxed later – are summarized as:

- Switching losses are equal to the minimum hard-switching losses of $U_{\text{dc}}Q_{\text{oss}}$, with losses from the voltage-current overlap period ignored [41], [45],
- Reverse-recovery losses are ignored,
- Gate driving power is considered negligible for the power levels and switching frequencies evaluated here,
- Power semiconductors are used to their full voltage rating; that is, there is no voltage safety margin,
- Power semiconductors can be selected at any voltage for any technology, and
- The empirical scalings of R'_{ds} and C'_{Q} derived in **Appendix A** describe the correct voltage relationship for current power semiconductor technologies.



(a) Fixed f_{sw} (b) Fixed Δi_L (c) Fixed Δu_{ac}

Fig. 6: Normalized semiconductor power dissipation for chip area-optimized FCML converters with a given power rating, the same output filter, and three output filter constraints (compared to a 2-level, 400 V GaN benchmark). Theoretical comparison assumes that semiconductor devices that can be selected for any desired voltage blocking rating, an assumption that is relaxed later for a more accurate assessment with respect to device-specific technologies. For any filter constraint, 3-level, 800 V designs are more lossy than the 2-level, 400 V GaN benchmark, shown with a dashed line. GaN refers to GaN-on-Si HEMTs and Si/SiC refers to Si/SiC MOSFETs, respectively.



(a) GaN (b) SiC (c) Si

Fig. 7: Scaling of levels for *fixed power rating and power dissipation of the bridge-leg* with increasing DC-link voltage, U_{dc}, for area-optimized FCML converters across three output constraints with a fixed filter, based on **Table II**. Each plot selects the number of levels to keep the same bridge-leg losses as the 2-level, $U_{dc} = 1$ (normalized) design for the respective semiconductor technology. Discrete steps are required to fix the number of levels to an integer value. For a given U_{dc} ratio, the filter constraint affects the required number of levels through the different f_{sw} scalings. The different number of levels for different device technologies (i.e. comparing GaN, SiC, and Si at the same U_{dc} ratio) is due to the voltage-scaling parameters (α_R and α_C) fit in **Appendix A**. We continue to assume that any desired voltage rating can be selected for all semiconductor devices. GaN refers to GaN-on-Si HEMTs and Si/SiC refers to Si/SiC MOSFETs, respectively.

Substituting the voltage scaling fits back into Eqn. (3):

$$P_{semi} = I_{rms,ac}^2 N^{(1-\alpha_R)} \frac{R'_{ds}(U_{dc})}{A_{die}} + N^{-(1+\alpha_C)} f_{sw} U_{dc}^2 C'_Q(U_{dc}) A_{die}. \tag{6}$$

We solve for the optimal semiconductor area to minimize the device losses ($dP_{semi}/dA_{die} = 0$), with a loss-minimized device area of:

$$A_{die,opt} = \frac{I_{rms,ac} N^{(2-\alpha_R+\alpha_C)/2}}{U_{dc}} \sqrt{\frac{R'_{ds}(U_{dc})}{f_{sw} C'_Q(U_{dc})}} \tag{7}$$

The total loss-optimized semiconductor area ($A_{die,opt,tot}$) for the bridge-leg is $2NA_{die,opt}$, which for a given DC-link voltage, depends on the power rating through the factor $I_{rms,ac}$.
We find the minimum semiconductor losses P_{semi} using the loss-optimal semiconductor area $A_{die,opt}$ for an $(N+1)$-level FCML converter as:

$$P_{semi} = \frac{2 I_{rms,ac} U_{dc}}{N^{(\alpha_R+\alpha_C)/2}} \sqrt{R'_{ds}(U_{dc}) C'_Q(U_{dc}) f_{sw}}. \tag{8}$$

The optimal semiconductor losses are linearly dependent on the power rating of the bridge-leg, since the product of $I_{rms,ac}U_{dc}$ can be related, assuming a lossless power transfer, to the input power P_{in} by $I_{rms,ac}U_{dc} = P_{in}\frac{2\sqrt{2}}{M(U_{dc})}$, where $M(U_{dc})$ is the DC-link voltage dependent modulation index, $M(U_{dc}) = \frac{U_{pk,ac}}{U_{dc}/2} = \frac{\sqrt{2}U_{rms,ac}}{U_{dc}/2}$.
Only considering the optimal semiconductor losses P_{semi} of **(8)**, the efficiency of the system can be calculated as:

$$\eta = \frac{P_{in} - P_{semi}}{P_{in}} = 1 - \frac{P_{semi}}{P_{in}}\ , \tag{9}$$

where we identify P_{semi}/P_{in} as the efficiency penalty incurred by the semiconductor losses. Substituting (8) in (9), we can rewrite the efficiency as:

$$\eta = 1 - \frac{4\sqrt{2}}{M(U_{dc}) \cdot N^{(\alpha_R+\alpha_C)/2}} \sqrt{R'_{ds}(U_{dc}) C'_Q(U_{dc}) f_{sw}}\ . \tag{10}$$

Since the loss-optimum semiconductor area $A_{die,opt}$ is always employed (larger die area for larger power and/or current, as given by (7)), the semiconductor losses scale linearly with the rated power, and the efficiency therefore does not depend on the power rating. This derivation, then, allows to compare, for any selected power rating, the semiconductor losses of a bridge-leg between different number of levels and DC-link voltages. Further, we can compare the efficiency penalty of the semiconductor losses across different power ratings, since the efficiency penalty depends on the semiconductor technology, number of levels, DC-link voltage, switching frequency, and modulation index, but not on the power rating.

IV. Output Filter

To isolate the relative bridge-leg performance from the filter stage, f_{sw} must be adjusted to keep the same output filter stress as N and/or U_{dc} are varied. Filter stress, however, is not a straightforward

TABLE II: Efficiency-optimized scaling laws with N and U_{dc} for FCML converters with three output filter constraints (fixed device technology, fixed $I_{\text{rms,ac}}$).

	Fixed f_{eff}	**Fixed Δi_{L}**	**Fixed Δu_{ac}**
$f_{\text{sw,2}}/f_{\text{sw,1}}$	$\frac{N_1}{N_2}$	$\frac{U_{\text{dc,2}}}{U_{\text{dc,1}}}\left(\frac{N_1}{N_2}\right)^2$	$\sqrt{\frac{U_{\text{dc,2}}}{U_{\text{dc,1}}}}\left(\frac{N_1}{N_2}\right)^3$
$A_{\text{die,opt,2}}/A_{\text{die,opt,1}}$	$\sqrt{\frac{N_2}{N_1}}\left(\frac{N_2U_{\text{dc,1}}}{N_1U_{\text{dc,2}}}\right)^{(2-\alpha_{\text{R}}+\alpha_{\text{C}})/2}$	$\sqrt{\frac{N_2}{N_1}}\left(\frac{N_2U_{\text{dc,1}}}{N_1U_{\text{dc,2}}}\right)^{(3-\alpha_{\text{R}}+\alpha_{\text{C}})/2}$	$\sqrt{\frac{N_2}{N_1}}\left(\frac{N_2U_{\text{dc,1}}}{N_1U_{\text{dc,2}}}\right)^{(5-2\alpha_{\text{R}}+2\alpha_{\text{C}})/4}$
$P_{\text{semi,2}}/P_{\text{semi,1}}$	$\sqrt{\frac{U_{\text{dc,2}}}{U_{\text{dc,1}}}}\left(\frac{N_1U_{\text{dc,2}}}{N_2U_{\text{dc,1}}}\right)^{(1+\alpha_{\text{R}}+\alpha_{\text{C}})/2}$	$\sqrt{\frac{U_{\text{dc,2}}}{U_{\text{dc,1}}}}\left(\frac{N_1U_{\text{dc,2}}}{N_2U_{\text{dc,1}}}\right)^{(2+\alpha_{\text{R}}+\alpha_{\text{C}})/2}$	$\sqrt{\frac{U_{\text{dc,2}}}{U_{\text{dc,1}}}}\left(\frac{N_1U_{\text{dc,2}}}{N_2U_{\text{dc,1}}}\right)^{(3+2\alpha_{\text{R}}+2\alpha_{\text{C}})/4}$
$f_{\text{eff,2}}/f_{\text{eff,1}}$	1	$\frac{U_{\text{dc,2}}N_1}{U_{\text{dc,1}}N_2}$	$\sqrt{\frac{U_{\text{dc,2}}N_1}{U_{\text{dc,1}}N_2}}$
$\Delta i_{\text{L,2}}/\Delta i_{\text{L,1}}$	$\frac{U_{\text{dc,2}}N_1}{U_{\text{dc,1}}N_2}$	1	$\sqrt{\frac{U_{\text{dc,2}}N_1}{U_{\text{dc,1}}N_2}}$
$\Delta u_{\text{ac,2}}/\Delta u_{\text{ac,1}}$	$\frac{U_{\text{dc,2}}N_1}{U_{\text{dc,1}}N_2}$	$\frac{U_{\text{dc,1}}N_2}{U_{\text{dc,2}}N_1}$	1

parameter, and this section discusses different output filter metrics, with a special focus on losses and EMI performance, to determine the correct constraint.

A. Output Filter Constraint Options

There are three potential filter stress constraints that could be fixed: effective switching frequency (f_{eff}), inductor current ripple magnitude (Δi_{L}), or output capacitor voltage ripple magnitude (Δu_{ac}). Fixing any one of these would drive filter losses, volume, and required performance in different ways [46], [47], and we need to determine the correct change in f_{sw} ("f_{sw} scaling") that is required to keep an individual filter constraint constant with varying N and/or U_{dc}.

The worst-case peak-to-peak current ripple in the inductor occurs at $50\,\%$ duty cycle and can be derived as:

$$\Delta i_{\text{L}} = \frac{U_{\text{dc}}}{4N^2 f_{\text{sw}} L_{\text{o}}}, \tag{11}$$

with the worst-case peak-to-peak output voltage ripple (assuming all ripple current flows into the capacitor [46]) occurring at the same duty cycle:

$$\Delta u_{\text{ac}} = \frac{U_{\text{dc}}}{32N^3 f_{\text{sw}}^2 L_{\text{o}} C_{\text{o}}}. \tag{12}$$

For multi-level converters, we define $50\,\%$ duty cycle as the midpoint output voltage that lies between two adjacent voltage levels.

The f_{sw} scalings to maintain the respective fixed output filter stresses can be determined from these equations as:

(I) The effective switching frequency, f_{eff}, remains constant if the switching frequency, f_{sw}, is reduced by a factor of $1/N$.

(II) The worst-case inductor current ripple, Δi_{L}, is kept constant if f_{sw} is scaled by U_{dc}/N^2, cf. Eqn. (11), from increased f_{eff} ($1/N$ factor) and decreased voltage ripple magnitude (U_{dc}/N). Δi_{L} is typically set between $20\,\% - 40\,\%$ of the peak nominal output current as a compromise between inductance magnitude, inductor losses, and ease of control of i_{L} [46]. Fixed Δi_{L} may be required to meet a given loss budget in the filter inductor or to maintain a control bandwidth with a fixed current sampling rate.

(III) Fixing the worst-case output capacitor voltage ripple, Δu_{ac}, adds a further $1/N$ factor to the Δi_{L} constraint from the reduction in capacitor impedance with higher f_{eff}, for a fixed output voltage ripple f_{sw} scaling of $\sqrt{U_{\text{dc}}/N^3}$, cf. Eqn. (12) (assuming all ripple current flows into the capacitor [46]). Δu_{ac} determines the total harmonic distortion (THD) of the AC waveform. For motor drives, higher THD results in higher winding losses. For grid-tied applications, THD must be less than a certain value to meet regulations (e.g., CISPR 11 [48]).

These scalings of f_{sw} for two bridge-legs with different U_{dc} and N are listed in the first line of **Table II**. Within a particular device technology, we can substitute the f_{sw} scalings into Eqns. (7) and (8) to find the area and loss relationship between two designs with an arbitrary DC-link voltage ratio ($U_{\text{dc,2}}/U_{\text{dc,1}}$) and number of levels ($N_2/N_1$). These loss and area relationships are summarized in the next two rows of **Table II**.

The relative semiconductor losses for three device technologies and these three fixed output filter stresses (at a given power rating) are then plotted in **Fig. 6**, with the losses normalized for a benchmark 2-level, $400\,\text{V}$ DC-link GaN-based design. 3-levels are indeed "not enough" for an $800\,\text{V}$ DC-link bridge-leg (cf., $2U_{\text{dc}}$ in **Fig. 7**) – for any semiconductor or output filter constraint, these scaling laws indicate that more than 4 levels are necessary to recover the bridge-leg efficiency degradation from the $2\times$ increase in U_{dc} between single-phase and 3-phase systems, even assuming that we can select devices with any voltage rating.

For a more tangible comparison, let's assume a benchmark 2-level, $400\,\text{V}$, $2.2\,\text{kW}$ AC/DC converter with $230\,\text{V}_{\text{rms}}$ u_{ac} that operates with $f_{\text{sw}} = 70\,\text{kHz}$ (similar to the hardware demonstrator of **Section II**). With no voltage margin and any choice of voltage rating, $400\,\text{V}$ GaN switches would, based on the scalings in **Appendix A**, have $R'_{\text{ds}} = 176\,\text{m}\Omega\,\text{mm}^2$ and $C'_{\text{Q}} = 28\,\text{pF/mm}^2$. Using (7), the loss-minimized device area is $7.2\,\text{mm}^2$ and, by (8), the semiconductor power dissipation is $4.5\,\text{W}$.

An $800\,\text{V}$, 3-level design is the special case that all three output filter stresses are identical with $f_{\text{sw}} = 35\,\text{kHz}$ (see **Fig. 2**). The loss-minimized area per device increases by $\sqrt{2}$ to $10.2\,\text{mm}^2$. The increase in area reduces the per-device power dissipation by $\sqrt{2}$, but with double the number of devices, the overall power dissipation increases by the same $\sqrt{2}$ ratio to $6.3\,\text{W}$. Because the semiconductor area is re-optimized when moving to 3-levels, the increase over the 2-level losses is smaller than that shown in **Fig. 2**, where the devices are kept the same, but the semiconductor losses still increase with a factor $\sqrt{2}$.

If we scale to a 7-level design with the same Δi_{L}, we can use $133\,\text{V}$ GaN switches (assuming any voltage rating can be selected and zero voltage margin, the assumptions for now), f_{sw} decreases to $3.9\,\text{kHz}$, the area per device is $33.8\,\text{mm}^2$, and the device power dissipation is driven down to $1.7\,\text{W}$, $2.6\times$ smaller than the $400\,\text{V}$, 2-level design and $3.7\times$ better than the 3-level design at $800\,\text{V}$. The penalties for recovering the efficiency at higher U_{dc} are increased complexity, lower reliability due to higher part count, significantly more semiconductor area, and additional volume for flying capacitors.

An alternate way to look at these scaling laws is to consider the required levels for constant overall bridge-leg semiconductor loss

as the U_{dc} ratio is increased, which is plotted in **Fig. 7** with each plot normalized to a 2-level design with the respective semiconductor technology and the same power rating. Only integer numbers of levels are allowed, accounting for the staircase-like shape of the plotting functions. At U_{dc} ratios of 2, these results again indicate that at least 4-levels are required for any filter constraint. In **Fig. 7a**, for example, an increase in U_{dc} of 2× (the 400 V to 800 V increase between single-phase and three-phase systems) could require 4 or 5 levels for the same bridge-leg efficiency as the 2-level, 400 V design, with the exact value depending on the selected output filter constraint. At very large U_{dc} ratios, we observe significant differences in the required number of levels based on the voltage-scaling parameters (α_R and α_C from **Appendix A**) of the particular technologies.

Fixing the correct output constraint, then, is absolutely critical in determining the levels required for an ultra-high-efficiency bridge-leg. Accordingly, the next section focuses on these constraints in the full AC/DC converter context.

B. Output Filter Constraint Selection

The scaling of f_{sw} with U_{dc} and N plays a critical role in the optimal semiconductor area, efficiency, and number of levels, as we found in the previous section. For a fixed output filter – and we emphasize that we are focused on comparing bridge-leg efficiencies without changing the filter – this factor is determined by the filter constraint (fixed f_{eff}, fixed Δi_L, or fixed Δu_{ac}) that is held constant. Here, we investigate these three proposed constraints to judge the most appropriate.

The filter is assumed to be second-order (see **Fig. 2**) with the corner frequency well below f_{sw} for the 2-level, 400 V DC-link base case. We assume that *a)* the base case converter meets the EMI regulation with no margin, *b)* all of the current ripple, Δi_L, flows into the output capacitor, C_o [46], and *c)* over a switching cycle, the output voltage (u_{ac}) is constant. The worst-case inductor current ripple and capacitor voltage ripple are respectively given in Eqns. (11) and (12).

Fig. 8 revisits the three numerical examples introduced in **Section III**, and plots the key filter metrics with f_{sw} scaled by the values in **Table II** to fix the appropriate metric. The three N-U_{dc} combinations are: **1)** the 2-level, 400 V base case, **2)** a 3-level, 800 V design that is the special case of identical filter stresses, and **3)** a 7-level, 800 V design. **Figs. 8.i.a-c** show the simulated switch node voltage ($u_{\bar{a}0}$), where we observe that a fixed magnitude of Δi_L or Δu_{ac} necessarily shifts f_{eff}. Similarly, we highlight the variation of inductor (**Figs. 8.ii.a-c**) and capacitor (**Figs. 8.iii.a-c**) ripple with duty cycle, and we again observe that fixing one worst-case ripple magnitude necessarily shifts f_{eff} and the other ripple magnitude. The exact worst-case ripple magnitude and effective frequency changes across U_{dc} and N are derived in the bottom half of **Table II**.

To determine the most appropriate filter metric to fix when comparing bridge-legs, we consider filter efficiency and adherence to EMI regulations.

C. Filter Efficiency

The losses in the 2nd-order filter will be driven by the inductor, and the capacitor losses can be ignored [50]. Assuming equal output power, the same inductor, the low-frequency asymptote for litz wire (valid up to a few MHz) [51], [52], and ignoring DC bias effects on core losses, the high-frequency inductor losses can be written as (under the Generalized Steinmetz Equation):

$$P_L = V_c k_c f_{eff}^{\alpha} B^{\beta} + R_{dc} a f_{eff}^2 \Delta i_L^2, \tag{13}$$

where V_c is the core volume, α and β are the Steinmetz parameters, a is the AC to DC resistance ratio, R_{dc} is the DC resistance, and B is the magnitude of the high-frequency flux density. With B proportional to Δi_L, the relative core losses (P_C) are:

$$\frac{P_{C,2}}{P_{C,1}} = \left(\frac{\Delta i_{L,2}}{\Delta i_{L,1}}\right)^{\beta} \left(\frac{f_{eff,2}}{f_{eff,1}}\right)^{\alpha}, \tag{14}$$

and the relative winding losses (P_W) are:

$$\frac{P_{W,2}}{P_{W,1}} = \left(\frac{\Delta i_{L,2}}{\Delta i_{L,1}}\right)^{2} \left(\frac{f_{eff,2}}{f_{eff,1}}\right)^{2}. \tag{15}$$

TABLE III: Output filter constraint evaluation for losses in the output filter inductor for FCML converters with three output filter constraints (fixed device technology, fixed $I_{rms,ac}$). Output filter components (L_o, C_o) are fixed. Total relative inductor filter losses ($P_{L,2}/P_{L,1}$) assume the rough approximation of Steinmetz parameters of $\alpha = \beta = 2$ [47], [53]. The exact values of α and β are material-dependent.

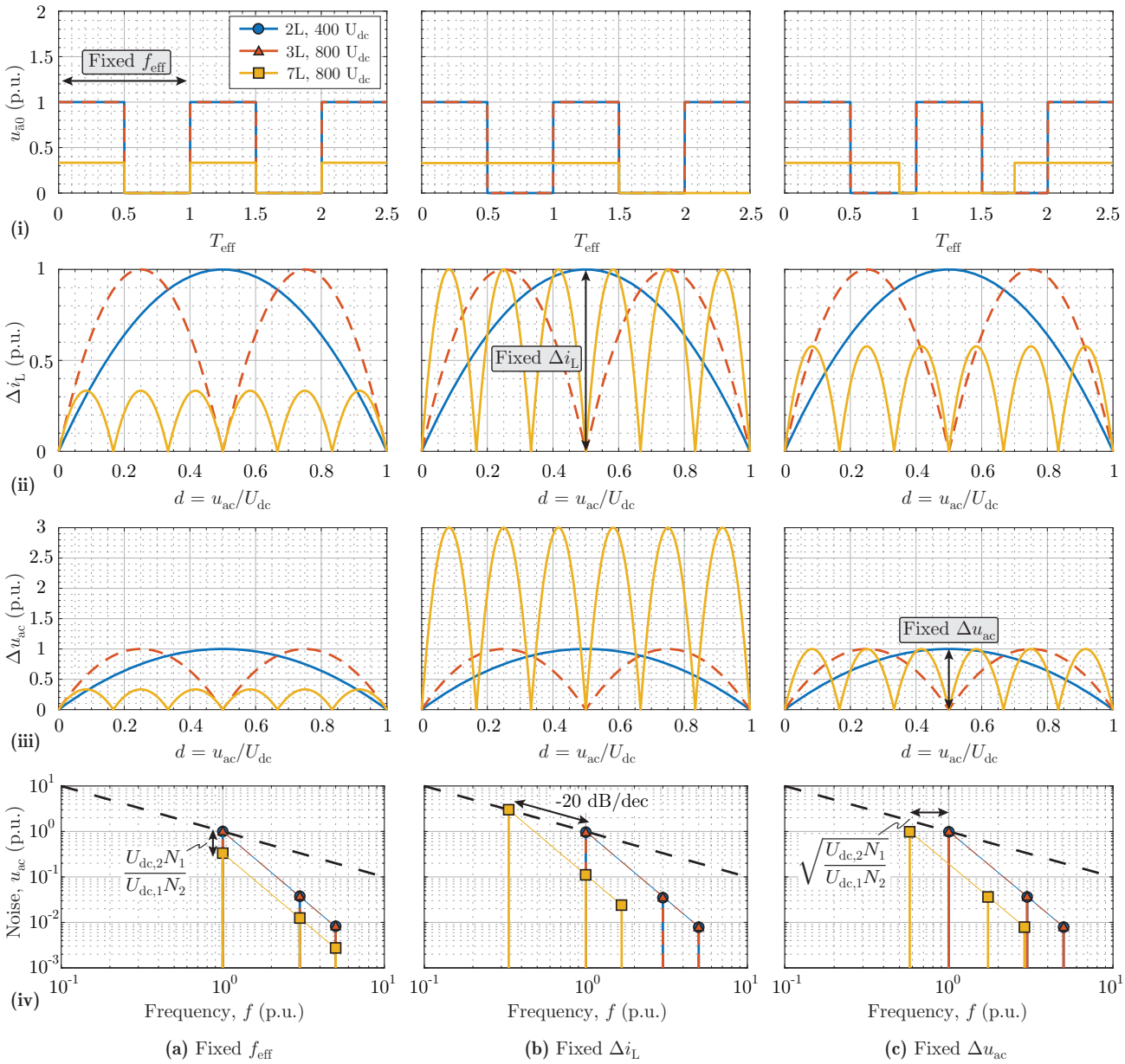
	Fixed f_{eff}	**Fixed Δi_L**	**Fixed Δu_{ac}**
$P_{C,2}/P_{C,1}$	$\left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{\beta}$	$\left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{\alpha}$	$\left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{(\alpha+\beta)/2}$
$P_{W,2}/P_{W,1}$	$\left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{2}$	$\left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{2}$	$\left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{2}$
$P_{L,2}/P_{L,1}$	$\approx \left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{2}$	$\approx \left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{2}$	$\approx \left(\frac{N_1 U_{dc,2}}{N_2 U_{dc,1}}\right)^{2}$

The core and winding AC loss ratios are reported for each constraint in **Table III** with the appropriate f_{eff} and Δi_L relative scalings from **Table II**. As expected, the core losses are related to the Steinmetz coefficients, with the key parameter depending on the applied output filter constraint. With f_{eff} held constant, the ripple magnitude varies, and the core losses will therefore depend on the flux density Steinmetz parameter, β. In contrast, if the ripple magnitude, Δi_L, is held constant, the ripple frequency will vary, and the core losses will only depend on the frequency Steinmetz parameter, α. Fixing Δu_{ac} changes the current ripple magnitude and frequency (see **Fig. 8.ii.c**), and the core losses must therefore depend on both Steinmetz parameters.

With the approximations here, the winding losses simply scale as the square of the U_{dc}/N ratio for all three cases. If we approximate the Steinmetz parameters $\alpha = \beta = 2$ [47], [53], then, we find that – for the same output filter – the inductor losses scale identically for all three constraints as the square of the U_{dc} and N ratios (see **Table III**). The particular Steinmetz parameters, we want to be clear, are highly materially-dependent, and this rough approximation of $\alpha = \beta = 2$ is used to consider the relative scaling of filter losses. The result of this approximation, where we find roughly equal filter losses across all three constraints, indicates that the constraint selection will have little effect on filter losses, and we can compare bridge-leg efficiencies directly under any of the three proposed output filter constraints. If, instead, the inductor design is constrained by saturation limits from the low-frequency output current with very minor AC losses [53], the output filter constraint will again have no effect on the filter efficiency. Confident that the choice of constraint, then, will have a minor impact on filter efficiency, we move to evaluate the effect of the filter constraint on EMI.

D. Conducted EMI Performance

To compare bridge-legs across U_{dc} and N, we must also verify that the system continues to meet the relevant EMI regulations. With this work focused in part on grid-interfaced inverters and rectifiers, we seek to meet the CISPR 11 [48], IEEE 519 [54], IEEE 1547.1 [55], and "BDEW" [56] standards. Ref. [49] proposes a unification of the CISPR 11 and BDEW limits to address the 9 kHz – 150 kHz gap for individual converters that is poorly addressed by IEEE 519/1547 (which target, respectively, systems at the point of common coupling



(a) Fixed f_{eff} **(b)** Fixed Δi_{L} **(c)** Fixed Δu_{ac}

Fig. 8: Key simulated waveforms and mappings for test cases: the 2-level, 400 V benchmark ("2L, 400 U_{dc}"), a 3-level, 800 V bridge-leg ("3L, 800 U_{dc}"), and a 7-level, 800 V bridge-leg ("7L, 800 U_{dc}"). **(a)** Fixed f_{eff}. **(b)** Fixed Δi_{L}. **(c)** Fixed Δu_{ac}. **(i)** Simulated switch-node voltage ($u_{\bar{a}0}$) at 50 % output duty cycle. **(ii)** Inductor current ripple magnitude (Δi_{L}) vs. duty cycle (d), defined as $d = u_{\text{ac}}/U_{\text{dc}}$, and calculated with Eqn. (11). **(iii)** Capacitor voltage ripple magnitude (Δu_{ac}) vs. duty cycle (d), and calculated with Eqn. (12). **(iv)** Spectrum at u_{ac} for worst-case Δu_{ac} operating point to evaluate compliance with EMI regulations, with a $-20\,\text{dB}$ per decade noise ceiling valid in the $9\,\text{kHz} - 500\,\text{kHz}$ frequency range [49]. All $u_{\bar{a}0}$ are referenced to zero (ignoring any DC bias at different levels), we assume that u_{ac} is constant over the switching cycle, and all plots are normalized to the 2-level, 400 V benchmark.

and legacy thyristor-based converters). The most stringent expected-future EMI regulation at each frequency from $9\,\text{kHz} - 500\,\text{kHz}$, then, obeys a $-20\,\text{dB}$ per decade slope for this entire range [4].

The fundamental frequency component at the bridge-leg output, f_{eff}, for most kW-scale FCML converters falls into this range, although select recent papers push f_{eff} beyond 500 kHz to improve power density (e.g. [2] at 800 kHz and 98.0 % peak efficiency, [3] at 960 kHz and 98.6 %, and [20] at 1.44 MHz and 98.3 %). Up to 5 MHz – which has not been exceeded for f_{eff} in this class, to our knowledge – the most stringent relevant conducted EMI regulation is CISPR 11, with a flat (frequency-independent) noise ceiling. With only a minor loss of generality, we can then consider two cases: a noise ceiling with a $-20\,\text{dB}$ per decade slope (valid for most FCML designs, from $9\,\text{kHz} - 500\,\text{kHz}$) and a flat ceiling, which is valid for f_{eff} between $500\,\text{kHz} - 5\,\text{MHz}$.

We compare the harmonic content in the output waveform for the three output constraints, normalized to the 2-level, 400 V base case that we assume to *just* meet the relevant EMI specification. We reiterate here that the filter itself does not change between the different designs. The harmonic content is the product of the harmonic magnitude at the switch node, $u_{\bar{a}0}$ in **Fig. 2**, and the filter performance at the relevant frequency, and these must each be considered to understand the performance across U_{dc} and N.

For any constraint, the output frequency shifts by:

$$\frac{f_{\text{eff},2}}{f_{\text{eff},1}} = \frac{f_{\text{sw},2} N_2}{f_{\text{sw},1} N_1}, \tag{16}$$

and the EMI-relevant voltage ripple magnitude, Δu_{ac}, changes by:

$$\frac{\Delta u_{\text{ac},2}}{\Delta u_{\text{ac},1}} = \frac{U_{\text{dc},2}}{U_{\text{dc},1}} \left(\frac{N_1}{N_2}\right)^3 \left(\frac{f_{\text{sw},1}}{f_{\text{sw},2}}\right)^2. \tag{17}$$

For each constraint, we substitute the previously-derived f_{sw} ratios (top line in **Table II**) into (16) and (17) to quantitatively understand the effect on EMI, which is shown in **Figs. 8.iv.a-c** for each constraint.
For fixed f_{eff} (**Fig. 8.iv.a**), the magnitude of each u_{sw} harmonic increases by $U_{\text{dc},2}N_1/U_{\text{dc},1}N_2$ with the frequency unchanged by the constraint definition. If $U_{\text{dc},2}N_1/U_{\text{dc},1}N_2 > 1$, designs under this constraint will violate EMI regulations (under the assumption that the base case just meets the limit).
With the magnitude of Δi_{L} held constant (**Fig. 8.iv.b**), the frequency of each harmonic is shifted by $U_{\text{dc},2}N_1/U_{\text{dc},1}N_2$. Intuitively, this change in frequency can be thought of as a change in capacitor impedance that affects the voltage ripple magnitude for the fixed current ripple magnitude (Δi_{L}) flowing into C_{o}. Each harmonic magnitude scales by $U_{\text{dc},2}N_1/U_{\text{dc},1}N_2$ at $u_{\bar{a}0}$, the same ratio as the frequency shift, resulting in a slope of exactly $20\,\text{dB}$ per decade (see **Fig. 8.iv.b**). Conveniently, then, if the base design meets an EMI regulation with a $-20\,\text{dB}$ per decade slope, any other bridge-leg with the same output filter will also meet the EMI regulation under this constraint, regardless of U_{dc} or N. From an EMI perspective, the Δi_{L} constraint is therefore preferred for the frequency range $9\,\text{kHz} - 500\,\text{kHz}$.
By definition, the fixed Δu_{ac} constraint (**Fig. 8.iv.c**) guarantees identical harmonic magnitudes at the output, u_{ac}. The harmonics are each shifted in frequency by a factor $\sqrt{U_{\text{dc},2}N_1/U_{\text{dc},1}N_2}$. If $U_{\text{dc},2}N_1/U_{\text{dc},1}N_2 > 1$, the harmonic content will be higher in frequency but at the same magnitude, violating an EMI regulation with a $-20\,\text{dB}$ per decade slope (again, under the assumption that the base case just meets the limit). With fixed Δu_{ac}, however, we are guaranteed to meet regulations in a flat frequency band since the harmonic magnitude is held constant. The Δu_{ac} constraint may therefore be preferred for frequencies from $500\,\text{kHz} - 5\,\text{MHz}$.
In summary, we find that fixing either Δi_{L} ($f_{\text{eff}} < 500\,\text{kHz}$) or Δu_{ac} ($500\,\text{kHz} < f_{\text{eff}} < 5\,\text{MHz}$) could meet the relevant EMI regulation with a fixed output filter. Ultra-high-efficiency converters, our focus, will likely operate with $f_{\text{eff}} < 500\,\text{kHz}$, leaving fixed Δi_{L} as the preferred constraint. We also reiterate that – for a given filter design – the selected output constraint has little effect on filter losses with the assumptions considered here.

V. Pareto Optimization

The first assumption that is relaxed for the loss modeling (not yet considering power density) is the use of arbitrary semiconductor voltage ratings, which has a significant effect on how many levels are "enough." We introduce discretized device ratings based on those that are commercially-available, a voltage utilization of $2/3$, and the appropriate penalty on C'_{Q} for underutilized devices. At the time of writing, GaN-on-Si HEMTs are commercially-available at ratings of $[100, 120, 150, 200, 600/650, 900]\,\text{V}$, ignoring lower-voltage devices that cannot be used at the maximum number of considered levels (10) with an $800\,\text{V}$ DC-link. SiC MOSFETs are not commercially-available below $650\,\text{V}$, and Si MOSFETs are available at a broad range of voltages.
Fig. 9 shows the relative semiconductor efficiency (fixed Δi_{L}) for a given power rating with these discretized voltage ratings and realistic voltage margin, with the results indicating that a higher-order multi-level design (6- or 7-levels) now necessary to recover the benchmark $400\,\text{V}$ efficiency at $800\,\text{V}$ (a large change over **Fig. 7**, where 4-levels were sufficient). The 6-level, $800\,\text{V}$ GaN design has approximately the same modelled semiconductor losses as the benchmark, and once other unavoidable losses are included (e.g. gate driver and flying capacitor losses), we predict that 7 or more levels will be required to reach the efficiency of the benchmark. At 7-levels, we can transition from $600\,\text{V}$ to $200\,\text{V}$ GaN devices, accounting for the dramatic improvement in efficiency when stepping from 6 to 7-levels. Because SiC MOSFETs are not available at voltage ratings below $650\,\text{V}$, SiC-based bridge-legs do not materially lower their losses with level counts higher than 3. In summary, then, a high level count (much higher than the academia- and industry-standard of 3) is necessary for a three-phase bridge-leg to meet or exceed the efficiency of a single-phase bridge-leg with the same output filter.

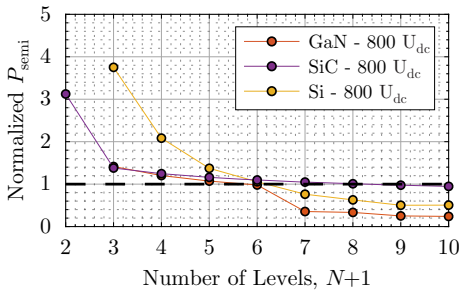


Fig. 9: Normalized semiconductor power dissipation for chip area-optimized FCML converters with a given power rating, fixed peak Δi_{L} and a fixed output filter, using commercially-available device voltage ratings (compared to a 2-level, $400\,\text{V}$ DC-link GaN benchmark). GaN refers to GaN-on-Si HEMTs and Si/SiC refers to Si/SiC MOSFETs, respectively. With commercially-available device voltage ratings, our analysis indicates that, with an $800\,\text{V}$ DC-link, only a multi-level converter with more than 6-levels will approach the semiconductor efficiency of the 2-level, $400\,\text{V}$ DC-link benchmark, which is shown with a dashed line.

To this point, we have derived scaling laws for relative comparisons of multi-level converters at arbitrary ratios of input voltage, U_{dc}. The validity of these scaling laws is independent of the base f_{sw}, the filter design, or the precise input voltage. With our focus on ultra-high-efficiency, we have thus far ignored the power density improvements for the filter stage with increasing f_{eff}, and have not considered the optimal f_{sw} to balance efficiency and power density. More tangibly, with the $70\,\text{kHz}$ operating frequency of the 2-level, $400\,\text{V}$ benchmark, the 7-level design with the assumptions of **Fig. 9** would operate with a switching frequency of only $3.9\,\text{kHz}$, an unrealistically low selection that would sacrifice available gains in power density. At this stage, we introduce specificity to find optimized designs, with the ultimate goal of finding the required number of levels and associated power density sacrifices necessary to recover the efficiency of a 2-level, $400\,\text{V}$ DC-link benchmark for an $800\,\text{V}$ DC-link.
With this guidance, we move to a full efficiency vs. power density optimization to include the tradeoff between filter size and bridge-leg efficiency with switching frequency, where for the $800\,\text{V}$ DC-link case, 3-level and the 7-level bridge-legs are chosen for the comparison. To this point, the analysis only examines *relative* bridge-leg efficiencies with a fixed output filter; here, we optimize the full bridge-leg, i.e., the semiconductors, the cooling system, the L_{o}-C_{o} filter, and the flying capacitors, if applicable, for each evaluated design to find *absolute* power density and inverter efficiency across switching frequency. The electrolytic DC buffer capacitor for power

pulsation, any additional EMI filter outside of L_o-C_o, and unfolder stages are excluded to equitably compare single- and three-phase systems, aiming for a fundamental understanding of the underlying difference between 400 V and 800 V DC-link voltage systems. We revisit the exclusion of these components in **Section VII**, but proceed here with the bridge-leg focus.

The Pareto front is generated for three bridge-leg configurations: **1)** the 2-level, 400 V base case, **2)** a 3-level, 800 V design with identical filter stresses of f_{eff}, Δi_{L}, and Δu_{ac}, and **3)** a 7-level, 800 V design. The selected power rating of the bridge-leg is 2.2 kW, which is similar to the 99.1 % data center power supply presented in [12] and derived from the motivation of this work: to ascertain why single-phase systems with a 400 V DC-link voltage in the 2.2 kW – 3.3 kW power range (like [12]) outperform three-phase systems with a 800 V DC-link voltage power rating of 6.6 kW – 10 kW [22], even though each of the three phases processes the same power, ac voltage, and ac current as the single-phase system.

Commercially-available GaN HEMT devices are selected for the semiconductor stage, where voltage ratings are used with a maximum applied voltage of 2/3 of the rating (i.e. 200 V GaN HEMTs may be used up to 133 V). For the 2-level 400 V and 3-level 800 V bridge-legs, the 600 V GaN HEMT device suite of *Infineon* [57] are considered for the optimization, and for the 7-level 800 V bridge-leg, the 200 V EPC 2034C GaN HEMT devices from *EPC Co.* are used. For a comprehensive and accurate Pareto front optimization, switching losses including the V-I overlap [45] improve the accuracy over including only the capacitive switching losses ($Q_{\text{oss}}U_{\text{dc}}$). For this purpose, calorimetrically-measured switching losses are employed for the Pareto optimization routine. The switching losses for the 600 V, 70 mΩ GaN devices from *Infineon* (IGOT60R070D1) are taken from [58], and the switching losses from [59] for the 200 V, EPC 2047 7 mΩ GaN devices of *EPC Co.* are scaled proportionally by Q_{oss} to model the 200 V, 6 mΩ EPC 2034C GaN devices that are used in this work. To model the dynamic on-state resistance of the GaN devices, data is taken from [60]. Paralleled devices are allowed to support the optimized selection of semiconductor area.

For the cooling system of the 2-level, 400 V and 3-level, 800 V designs, an extruded fin-fan heat sink is assumed with a Cooling System Performance Index (CSPI) of 20 $^{\text{W}}/_{\text{K l}}$ (this value is measured from the hardware demonstrator used for the measurements shown in **Section II**) and a temperature difference between heat sink and ambient of 20 °C. With the low losses of the 7-level topology and the fact that the losses are distributed among several switches (which additionally reduces the overall junction-to-PCB thermal resistance due to the heat spreading effect [61]), the 7-level converter can be designed with natural convection. For example: if 10.9 W of total semiconductor losses (the case for the built hardware in **Fig. 13(b)**) are distributed among 24 semiconductor devices with a junction-to-ambient thermal resistance of 45 $^{\text{K}}/_{\text{W}}$ [62], the temperature rise is only 20.5 °C. Contrarily, natural convection would not be possible for the 2-level, 400 V and 3-level, 800 V designs – at a measured 4 W of losses per device (**Fig. 4b** at 2 kW output power), the measured case temperature with natural convection exceeds 150 °C. The on-state resistance dependence of the semiconductors on the junction temperature is taken into account, and the maximum junction temperature of all semiconductor models is limited to 130 °C. Fan and gate driver power and size are included in the optimization.

To design the output filter, the filter design space [46] is constrained in such a way that the output voltage ripple is guaranteed to be below 1% of the peak output voltage amplitude that occurs at a modulation index of $M = 0.81$, and the maximum reactive power consumption

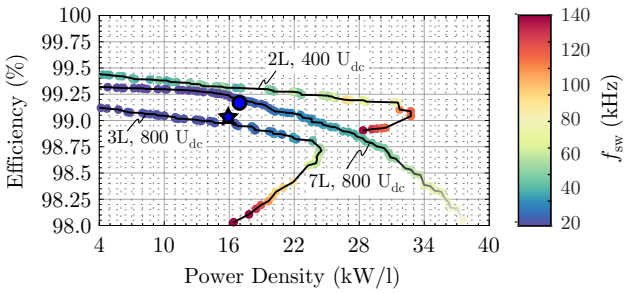


Fig. 10: Pareto fronts for efficiency vs. power density for 2.2 kW DC/AC inverters with different level counts and input voltages. All fronts are shown for commercially-available GaN HEMTs. Gate driver and fan losses are included, and the volume is calculated as the summed component box volume with a 30 % overhead for air and PCB height. Power densities and efficiencies exclude the power pulsation buffer capacitors and unfolder stages for a direct comparison between bridge-legs. The '●' is the selected design for the hardware demonstrator in **Section VI**, and the '★' indicates measured efficiency and power density.

of the L_o-C_o filter is limited to 3 %. The inductor modelling for L_o follows the guidelines presented in [53]. The considered core material is N87 ferrite featuring E, ELP, and ETD core geometries of different sizes, and the considered wire types are round and litz wires.

The flying capacitor dimensioning follows the guidelines presented in [15], where the capacitance value of the flying capacitors is chosen to limit the voltage ripple of the flying capacitors to 5 % of the blocking voltage of each switch (400 V for the 3-level case, and 133 V for the 7-level case). For the flying capacitors, X6S ceramic capacitors of the C5750X6S series of *TDK* are chosen. Although the Ceralink capacitor family from *TDK* feature lower losses than the selected X6S capacitors [63], these losses are negligible (in the tens of mW) and the X6S capacitors are selected for the 2× increase in capacitance density and 3× decrease in price relative to the Ceralink capacitors. For C_o, C0G type ceramic capacitors are preferred to the X6S type. Although C0G capacitors feature a lower capacitance density than the X6S, the DC voltage bias has no effect on their capacitance, i.e., they don't have a capacitance derating, and they can safely be assumed to be lossless, which is not the case for X6S capacitors with a large-signal 50 Hz excitation [64]–[66].

Finally, the volume is calculated as the summed box volume of each component with a 30 % overhead for air and PCB height. Each of the considered designs are evaluated for a base switching frequency of f_{sw} in the range of 20 kHz-140 kHz [4], [12] and for an inductor peak-to-peak ripple ratio r in the range of 2 % and 200 %, where $r = \Delta i_{\text{L,pp,max}}/I_{\text{ac,pk}}$, with $\Delta i_{\text{L,pp,max}}$ as the maximum peak-to-peak inductor current ripple.

The Pareto fronts for the evaluated designs are shown in **Fig. 10**. The tradeoff between power density and efficiency for ultra-high-efficiency FCML converters can now be clearly understood in the full design space, with a few takeaways that merit highlighting:

- Relative to the 2-level, 400 V DC-link benchmark, a 3-level 800 V design that sought to maintain the same efficiency (say, 99.1 %) will incur a 7× penalty in power density. Our previous analysis showed that the same efficiency cannot be achieved with a fixed filter, so efficiency can only be held constant through a large reduction in f_{sw} and the filter inductor will grow in size and value accordingly. The 3-level design must further add volume for the flying capacitors and additional switching stage.
- Relative to the 2-level, 400 V DC-link benchmark, a 3-level 800 V design that sought to maintain the same power density (e.g. 12 $^{\text{kW}}/_{\text{l}}$) will feature around 50 % higher losses. A fixed

TABLE IV: Components, key values, and performance metrics for the 7-level inverter of **Fig. 11b-c**. Component labels reference **Fig. 11a**.

Parameter	800 V, 7-Level
U_{dc}	800 V
f_{sw}	30 kHz (eff. 180 kHz)
P_o	2.2 kW
Power semicond.	6 mΩ 200 V EPC 2034C, *EPC Co.*
Gate driver	2EDF7275K, *Infineon*
Filter inductor, L_o	28 µH N87 2x Stacked ELP 32x6x20 Litz Wire 630x71 µm, 6 turns
Flying capacitors	12.2 µF (C5750X6S2W225K250KA)
Filter capacitor, C_o	2.0 µF (C5750C0G2J104J280KC)
Power density	15.8 kW/l
Peak efficiency	99.03 %

power density must increase f_{eff} to counterbalance the power density reduction from adding flying capacitors and having to cool more switches, so the real increase in losses with a fixed power density is even larger than our fixed output filter analysis found in the preceding sections.

- For an 800 V DC-link, 7-levels nearly recover the efficiency of the 400 V, 2-level benchmark, but with a power density reduction. Our previous analysis only considered efficiency; with power density included, we more clearly see the large volume penalty of the large PCB area determined by the switch cells and the flying capacitors. In **Section VI**, we build and characterize this Pareto-optimized 7-level design that is predicted to meet the efficiency of the 400 V, 2-level benchmark.
- 7-level inverters achieve a higher overall efficiency and power density than the 3-level inverter at the same input voltage. The main reason for this is that the 7-level bridge-leg does not require active cooling because of the lower semiconductor losses and larger chip area to spread these losses. Since the 3-level design needs active cooling, the power density is also limited by the amount of heat that has to be extracted from the switches – as f_{sw} starts to increase, the decrease in magnetics size outweighs the cooling system size increase, but, at a certain f_{sw}, this balance tips and increasing f_{sw} brings only a small benefit in inductor size but a large penalty in cooling system size due to the increased switching losses.

VI. Hardware Validation: 7-Levels Are (Nearly) Enough

To confirm the Pareto optimization finding that a 7-level, 800 V DC-link bridge-leg can (nearly) recuperate the efficiency of the 2-level, 400 V benchmark, a 7-level FCML bridge-leg hardware prototype is constructed (cf., **Fig. 11**) with the component details in **Table IV**. The measured 7-level characteristic waveforms are shown in **Fig. 12**, where the multi-level output waveform is a result of naturally balanced flying capacitors [15], [22], [40].

The design of the hardware follows the switch cell design principle first used in medium voltage drives [25] and then adopted and optimized for lower voltage applications [15], [20], [67], where flying capacitor switch cells (cf., **Fig. 11a-b**) are implemented such that two adjacent switch pairs are housed in each individual cell. To enable high efficiency, each switch utilizes two paralleled EPC 2034C GaN devices from *EPC Co.* Because of the high efficiency and the increased switch count and area, a heatsink-less design can be realized that relies solely on passive convective cooling. Each pair of adjacent switches are driven with the 2EDF7275K gate driver from *Infineon*. To limit the voltage ripple across each flying capacitor to less than 5 % of the blocking voltage of the switches, an *effective* capacitance

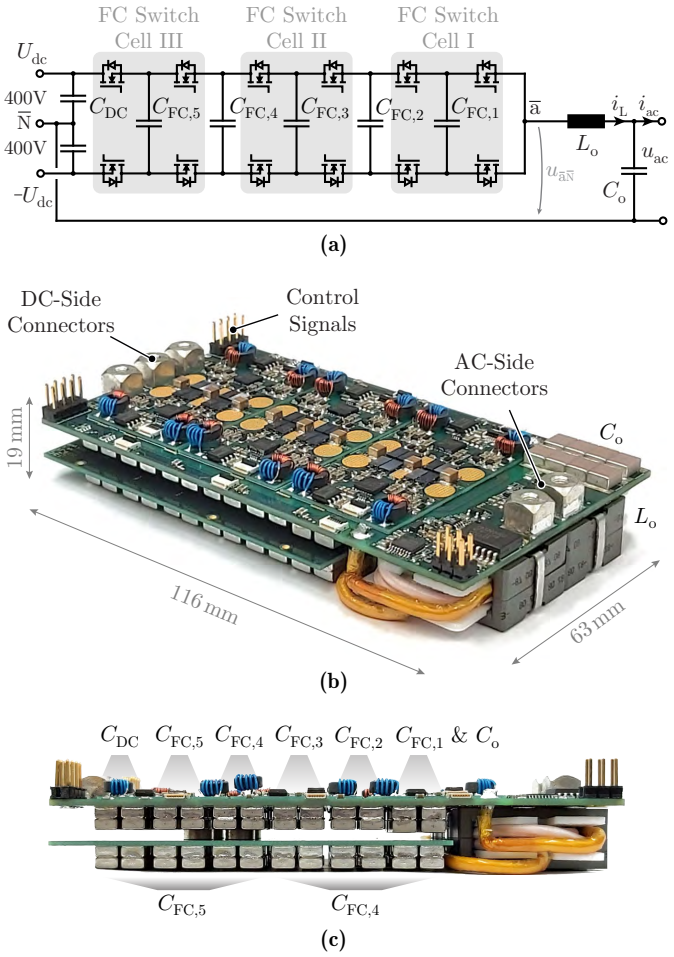


Fig. 11: **(a)** 7-Level FCML bridge-leg circuit schematic. **(b)** Hardware implementation of the 7-level FCML bridge leg, featuring a boxed volume of 116 mm × 63 mm × 19 mm. **(c)** Side-view of the implemented hardware with a detailed annotation of the capacitor placement.

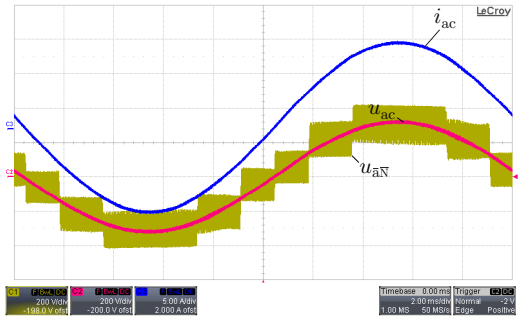


Fig. 12: Key measured waveforms at 2 kW for the 7-level, 800 V inverter, where labels are referenced to **Fig. 11(a)**.

of 12 µF is required for each flying capacitor. These capacitors are implemented with the C5750X6S ceramic capacitor series by *TDK*, which are rated for 450 V and feature a nominal capacitance of 2.2 µF at zero DC bias voltage. Since the capacitance of these X6S capacitors decreases with DC bias voltage – reducing up to 20 % of the nominal capacitance value at 400 V for a capacitance of only 0.44 µF – a different number of capacitors has to be placed for each one of the five flying capacitors $C_{FC,i}$. For $C_{FC,4}$ (DC bias: 533 V) and $C_{FC,5}$ (DC bias: 666 V), the situation is aggravated by the 450 V capacitor rating, which requires a series-connection of

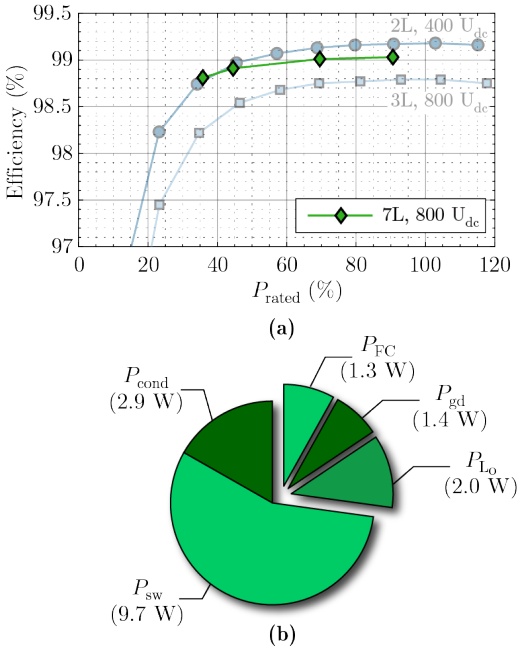


Fig. 13: (a) Measured DC/AC efficiency for the 7-level, 800 V inverter. Efficiency measurements include gate drive power and exclude losses in power pulsation buffer capacitors. Peak efficiency for the inverter is 99.03 %. **(b)** Expected loss breakdown at 2.0 kW (predicted losses: 17.3 W, measured losses: 19.4 W).

multiple capacitors and an additional parallel resistive divider to ensure a continuously-balanced voltage across the capacitors [68]. This leads to a large mismatch in the number of capacitors between, for example, $C_{\text{FC},1}$, which requires at least 11 discrete capacitors to achieve 12 µF at 133 V DC bias voltage, and $C_{\text{FC},5}$ which requires at least 99 discrete capacitors to feature 12 µF at 666 V DC bias voltage. The resistive divider is implemented with 1.6 MΩ resistors, leading to total losses of 1.3 W, cf., **Fig. 13b**. To accommodate all of these capacitors in a power-dense configuration, a second PCB is connected to the main PCB through screw connectors that allow the series and/or parallel connection of additional capacitors, as shown in **Fig. 11c**.

The efficiency measurements (measured with the *Yokogawa WT3000* precision power analyzer) and calculated loss breakdown are shown in **Fig. 13**. The efficiency of the 7-level, 800 V DC-link design is higher than the 3-level, 800 V DC-link design and reaches the efficiency of the 2-level, 400 V baseline case, particularly near around 40 % of rated load. The flattening of the efficiency curve of the 7-level prototype for higher loads can be attributed to two reasons: firstly, since the semiconductor losses increase at higher load (higher conduction and switching losses), the junction temperature increases more relative to the 2-level and 3-level designs that feature forced-air cooling, and conduction losses further increase due to the positive temperature coefficient of the GaN on-state resistance. Secondly, in order to limit the switching transient overshoot across the semiconductors to ≈ 10 % (150 V maximum at a nominal switched voltage of 133 V), the gate resistance is increased to 30 Ω per device. Unless the power stage design is further optimized (as in [3]), where power semiconductors are soldered on both sides of the PCB to reduce the commutation loop inductance and therefore the transient overshoot, the only way of reducing these overvoltages is to increase the turn-on gate resistance to slow the switching transient speed. The slow transition, though, increases switching losses (more tangibly, [3] shows that increasing the gate resistance from 10 Ω to 30 Ω for the EPC2034 devices more than halves the dv/dt of the switch transition). In sum, we measure 99.03 % peak efficiency in the hardware prototype, close to the predicted 99.15 % peak efficiency of the Pareto-optimized design and with the degradation explained by the two drivers above (with some additional contributions from unmodelled losses, e.g., conduction losses in PCB traces and additional parasitic capacitance at the switch nodes).

Despite this flat efficiency curve, the 7-level, 800 V DC-link inverter matches the efficiency of the 2-level, 400 V baseline. Increasing the number of levels of a bridge-leg enables higher efficiency, recovering the loss penalty associated with increasing the DC-link voltage from 400 V to 800 V for the same ac output voltage. Confirming our analysis, we show that a minimum of 7-levels are required for a three-phase bridge-leg to meet the efficiency of a single-phase bridge leg, which benefits immensely from an unfolder (see **Fig. 1b**). In the final section of this paper, we discuss the ramifications of this crucial finding on three-phase grid and motor drive applications, and propose different system architectures that can halve the DC-link voltage, enabling higher efficiency.

VII. Conclusion

Through the scaling laws and hardware demonstrations in this work, we show that three-levels are indeed "not enough" for high-efficiency AC/DC and DC/AC converters in three-phase applications featuring an 800 V DC-link voltage to recover the performance of a single-phase converter that, thanks to an unfolder bridge leg, can feature a 400 V DC-link voltage to generate the same 230 V_{rms} − 240 V_{rms} ac voltage. Our hardware demonstrators validate this prediction, with the 800 V DC-link, 3-level FCML inverter featuring 50 % higher measured losses and 2× lower power density than our 400 V DC-link, 2-level design. With idealized power semiconductor voltage ratings, a minimum of 4-levels are required to recover the efficiency of a 2-level, single-phase design at the 800 V DC-links required for three-phase conversion, and with currently-available device voltage ratings, an even higher numbers of levels are required. With a complete Pareto optimization, we find that a 7-level, 800 V DC-link inverter will nearly reach the efficiency of the 400 V DC-link, 2-level benchmark at full load, and we validate this theory with a 7-level, 2.2 kW hardware prototype with a power density of 15.8 $^{\text{kW}}/_{\text{l}}$ and a peak efficiency of 99.03 % that reaches the same partial load efficiency as the 2-level, 400 V benchmark, however, at a slightly lower power density.

The increase in DC-link voltage between single-phase and three-phase systems can be fundamentally attributed to the unavailability of a line-frequency unfolder in three-phase systems. In single-phase systems, these unfolders essentially double the AC voltage generation capability without increasing voltage stresses or power semiconductor losses [23], allowing the use of low-voltage semiconductors at low overall complexity. The fundamental advantage of a line-frequency unfolder is also immediately understandable by comparing the instantaneous power flow $\overline{p}$ (averaged over a switching cycle) which is processed by a bridge-leg for a single-phase and a three-phase PFC rectifier system (cf. **Figs. 14a-b**). Characteristic waveforms for same global (related to a mains period) average power P_{phase} are depicted in **Figs. 14c-d**. The three-phase system shows a heavily uneven distribution of $\overline{p}$ over the mains period which reaches twice the maximum value of the single-phase converter. Moreover, for the three-phase system in **Fig. 14b**, the processed power is (slightly) negative for negative phase voltages $u < 0$, i.e., the DC-link is

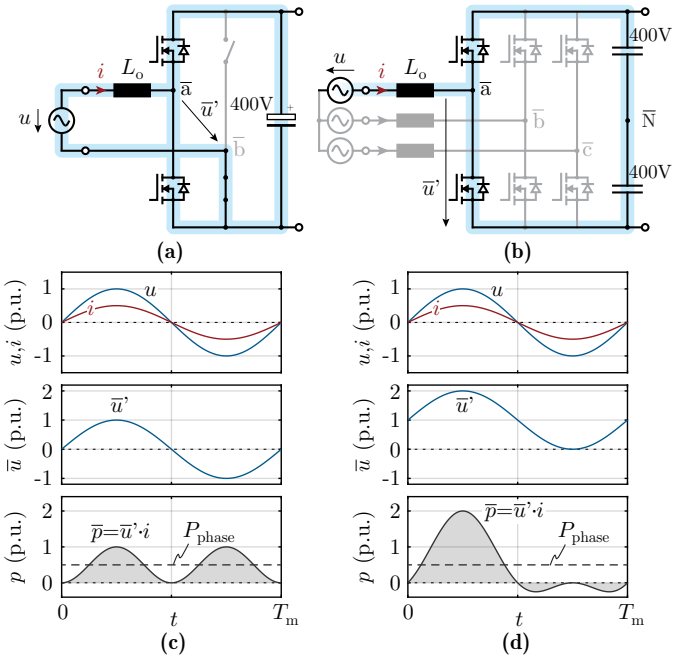


Fig. 14: Instantaneous power flow considerations for a **(a)** single-phase 2-level PFC rectifier, with the conduction path highlighted for $u > 0$ (the return path of the current via the unfolder bridge-leg, which is typically implemented with Si-SJ MOSFETs is only conceptually indicated), and a **(b)** three-phase 2-level PFC rectifier, with the conduction path of one of the three high-frequency bridge-legs highlighted (phase current returns through the other two phases). **(c-d)** Typical input phase voltage, current and power waveforms for a single mains period (T_m) shown per unit (p.u.), for the converters in **(a-b)**, respectively. For the same input voltage u and global average phase power P_phase, the power $\overline{p}$ processed by a bridge-leg of the three-phase system shows twice the maximum instantaneous peak power of the single-phase system and includes intervals of (slightly) negative instantaneous power.

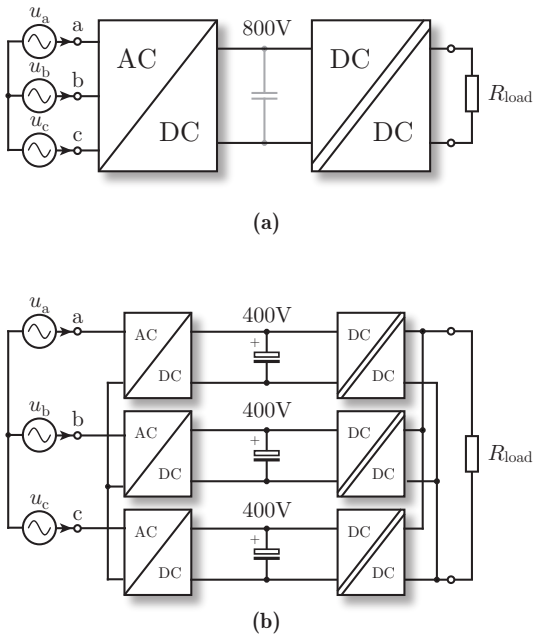


Fig. 15: Three-phase grid-connected converter block diagrams with an isolated DC/DC stage to provide galvanic isolation for safety and/or large voltage conversion ratios. **(a)** Monolithic three-phase conversion stage, with a single three-phase converter and isolated DC/DC converter. In this case, the AC/DC bridge-legs must be rated for the full 800 V DC-link (cf. **Fig. 1d**) but the output power is constant, reducing the DC-link capacitor size (cf. **Fig. 1d**). The AC/DC converter may include an unfolder-like structure for three-phase capabilities, such as an input voltage selector [71], [72]. **(b)** Phase-modular three-phase system, where each phase has a single-phase AC/DC stage (cf. **Fig. 1a**) and an isolated DC/DC converter [76]. In this architecture, the AC/DC bridge-legs can operate with low complexity and ultra-high-efficiency due to the low DC-link voltage, but the DC-link capacitor must be sized for power pulsation buffering (cf., **Fig. 1b**).

instantaneously sourcing power back to the grid for the considered phase (although the sum of the instantaneous powers of the three individual phases for a balanced three-phase system is constant at any point in time) [69], an issue which is also known from single-phase class-D amplifier circuits that feature a half-bridge instead of a full-bridge power circuit structure [70]. It follows directly, then, that three-phase applications should seek to, where possible, replicate the reduced-voltage benefit of single-phase designs, and we briefly discuss two use cases that may accomplish this goal. These two sample cases that are identified utilize the same unfolder concept used in single-phase systems and extend it to systems which require a three-phase solution, thereby halving the DC-link voltage requirement and leading to a performance increase of the three-phase semiconductor stage.

• *Three-phase grid-connected converters:* These often include an isolated DC/DC stage for safety and/or large voltage ratio conversion, as shown in **Fig. 15a**. The AC/DC conversion stage can be implemented as a monolithic three-phase converter (like the one shown in **Fig. 1b**), where the DC-link capacitor is small due to the constant three-phase power (cf., **Fig. 1d**) but the DC-link voltage must be high, with the associated penalties that we detail in this work. In this application, unfolder-like three-phase techniques that can reduce the semiconductor blocking voltage requirements are especially valuable, including input voltage selectors [71], [72] or novel modulation schemes [73]–[75].
Alternatively, the single-phase bridge-leg benefits can be recovered by adopting a phase-modular approach (**Fig. 15b**), where each of the three phases has a separate, isolated powertrain connected in parallel at the DC output [76], [77]. The DC-link capacitance requirement of the AC/DC stage is increased substantially, as each phase block must include power pulsation energy storage, but each AC/DC stage can be implemented with the low complexity and ultra-high-efficiency 2-level configuration of **Fig. 1a**. In this configuration, the summation of the phase power (shown in **Fig. 1d**) is performed by the parallel electric connection at the combined DC-link. High-efficiency monolithic (**Fig. 15a**) configurations (e.g., used for 10 kW EV chargers) typically feature a 3-level (for example, a VIENNA configuration) rectifier, where a midpoint DC-link connection is used to series-connect two DC/DC modules [78]. This enables the use of 600/650 V-rated semiconductors in the DC/DC stage of the monolithic approach, where each DC/DC module processes half of the input power (5 kW). Similarly, the DC/DC stage of the phase-modular (**Fig. 15b**) approach can be realized with 600/650 V-rated semiconductors, given the reduction to a 400 V DC-link, and requires the power rating of each module to be 3.3 kW, or one-third of the rated power. Hence, assuming the DC/DC modules for both the monolithic and phase-modular approaches can be realized with similar efficiencies (the only difference being a minor difference in power rating), one can safely conclude that the main efficiency difference lies in the front-end AC/DC stage.

• *Three-phase motor drive systems:* As seen in (**Fig. 16a**), three-phase motor drives require a higher DC-link voltage than a "phase-modular" counterpart (**Fig. 16b**). If the virtual star-point formed at the capacitor connection is not connected to the DC-link midpoint, as shown in **Fig. 16a**, discontinuous PWM schemes could improve semiconductor

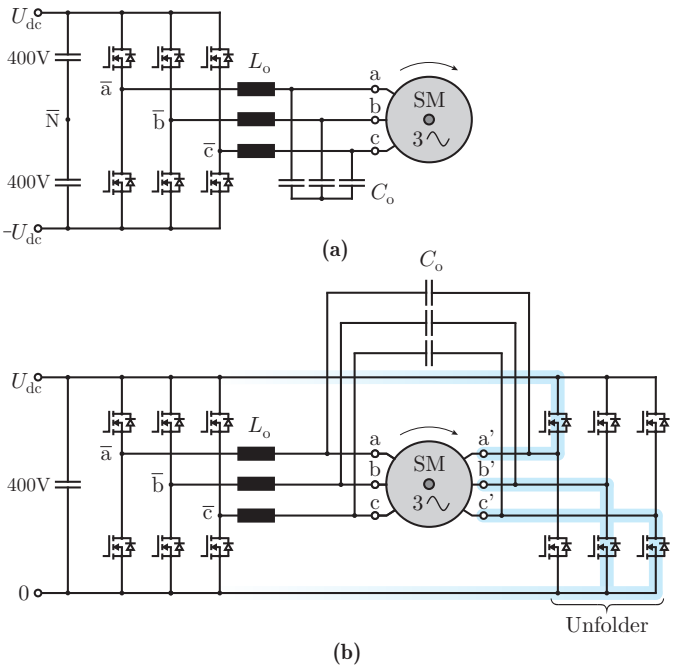


Fig. 16: Three-phase motor drive inverter systems. **(a)** Conventional three-phase motor drive system, where the motor windings are terminated in a star or delta configuration. The three-phase drive must operate with a high DC-link voltage because the winding terminations cannot be individually accessed, decreasing the bridge-leg efficiency. **(b)** Open-winding motor configuration, with both terminals on the individual windings accessible. The individual unfolder stages (highlighted) reduce the required DC-link voltage by a factor of ≈ 2 (as shown in **Fig. 1**), improving the efficiency of the bridge-legs [9], [80], [81].

losses and change the optimal area [79]; these considerations are kept outside the scope of this work to maintain the focus on the bridge-leg comparison. The advantages of moving to a single-phase architecture, then, can be realized with an open-winding configuration, with an unfolder for each stage placed at the winding terminal opposite the high-frequency bridge [9], [80], [81]. In motor drives, the summation of the individual phase powers is performed in the rotor, and the DC-link capacitor does not need to provide power pulsation capability. In this case, the only penalty for the higher-efficiency bridge leg is the addition of three motor terminals, but with the accelerating adoption of integrated motor drives, these additional connections will decrease in importance.

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Appendix A
Voltage Scaling for Power Semiconductors

A common motivation for the FCML architecture is the ability to use lower-voltage power semiconductor devices, which have lower specific on-resistance (R'_{ds}) than a higher-voltage counterpart [82]. One-dimensional, unipolar device scaling laws [27] provide a theoretical foundation for the relationship between breakdown voltage and R'_{ds}; these laws, however, do not **a)** account for the current state-of-the-art in power semiconductors, with some technologies far from the theoretical limits (e.g. low-voltage SiC) or using a structure that is poorly modeled by a 1-D drift region (GaN-on-Si HEMTs), **b)** include devices that break these theoretical limits (ReSURF / "superjunction" structures) [83], and

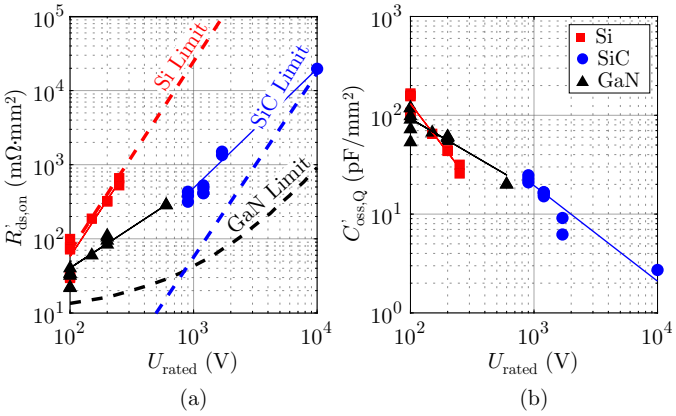

Fig. 17: Survey of candidate commercially-available semiconductors with voltage ratings above 100 V, with **(a)** specific on-resistance (R'_{ds}) and **(b)** specific charge-equivalent capacitance (C'_Q) determined from known die areas. GaN refers to GaN-on-Si HEMTs and Si/SiC refers to Si/SiC MOSFETs, respectively.

TABLE V: Blocking voltage scaling factors for R'_{ds} and C'_Q.

	R'_{ds}	C'_Q	α_R	α_C
Si	$300\,\mathrm{m\Omega\,mm^2}$ @ 200 V	$40\,\mathrm{pF/mm^2}$ @ 200 V	2.5	-1.6
SiC	$300\,\mathrm{m\Omega\,mm^2}$ @ 900 V	$20\,\mathrm{pF/mm^2}$ @ 900 V	1.6	-1.0
GaN	$300\,\mathrm{m\Omega\,mm^2}$ @ 650 V	$20\,\mathrm{pF/mm^2}$ @ 650 V	1.1	-0.7

c) provide a scaling of specific charge-equivalent capacitance (C'_Q) with voltage, leaving a gap in determining switching losses [41].

A complete understanding and justification of these scaling factors lies outside the scope of this work, and is the focus of an upcoming paper. Here, we survey the commercially-available state-of-the-art, as shown in **Fig. 17**, and empirically fit exponential scaling factors such that $R'_{ds} \propto U_{dc}^{\alpha_R}$ and $C'_Q \propto U_{dc}^{\alpha_C}$ (see **Table V**). This survey, which includes a broad range of manufacturers, provides benchmark scaling values that are representative of the current state-of-the-art for each technology node, a more indicative value than either the theoretical limit or a value from a single manufacturer. These exponential scaling factors are derived for GaN-on-Si HEMTs, SiC MOSFETs, and Si MOSFETs.

To determine C'_Q, we assume that the applied voltage is $2/3$ of the voltage rating. With discrete device voltage ratings (e.g. GaN-on-Si HEMTs are currently not available between 200 V or 600 V, and SiC MOSFETs are not available below 650 V), a lower voltage utilization factor may occur for certain designs, and the associated penalty of an increase in C'_Q is included in **Section V**.

These scalings capture the gains (lower R'_{ds}) and penalties (higher C'_Q) from lower-voltage power semiconductors, enabling the scaling laws developed for multi-level architectures. As semiconductor technologies evolve, the terms in **Table V** can be updated or expanded without affecting the validity of the analysis developed in this work.

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