

PwrSoC 2014 - Granular Power Management

Title:

Deep trench capacitor based on-chip switched capacitor voltage regulators for micro-processor power delivery

Abstract:

On-chip (or monolithic) switched capacitor DC-DC voltage regulators are currently being investigated as a promising candidate for granular power delivery and power management for future many-core exascale computing systems. To fit into such an application, it is critical for the switched capacitor voltage regulator to simultaneously achieve 1) high efficiency, 2) high power density, 3) react fast to transient load changes, and 4) deliver high power. This talk treats how the above four specifications can be met using smart circuit techniques and by leveraging on advanced deep submicron technologies that include the high-density deep trench capacitor.

We include measurement results of an on-chip switched capacitor voltage regulator demonstrator implemented in IBM's 32nm SOI CMOS technology which features fast switching transistors and deep trench capacitors. A peak efficiency of 90% at $3.7\text{W}/\text{mm}^2$ is demonstrated with 1.8V input voltage and 0.7V to 1.1V regulated output voltage, and the maximum output power is 850mW. The digital controller compares the output voltage with a reference voltage at a sampling frequency of 4GHz, resulting in a control loop that reacts to line and load variations with only 250ps maximum latency. With 16 interleaved converter phases, no dedicated output decoupling, and only very limited input decoupling, the output voltage droop is 11% of the DC output voltage under worst-case transient load step conditions.

Finally, we will present our latest chip (which is in production at the time of writing). This chip features an on-chip switched capacitor converter designed to deliver more than 10W of output power. This design furthermore incorporates a novel control concept that achieves droopless transient response without excessive decoupling.

Bio:

Toke Meyer Andersen received the B.Sc. and M.Sc. degrees from the Technical University of Denmark (DTU) in 2008 and 2010, respectively. He is currently pursuing the Ph.D. degree at the Power Electronic Systems Laboratory (PES) at the Swiss Federal Institute of Technology (ETH) in Switzerland. The Ph.D. degree is carried out in collaboration with IBM Research Zurich in Switzerland. His research area covers the analysis, design, implementation, and optimization of on-chip power converters in deep submicron CMOS technologies for future many-core exascale computing systems.