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Optimal Level Number and Performance Evaluation of Si/GaN Multi-Level Flying Capacitor Inverter for Variable Speed Drive Systems

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***Abstract*—This paper analyzes the optimal number of voltage levels concerning power density for a motor-integrated Multi-Level Flying Capacitor inverter (ML FCi) with $800\,\mathrm{V}$ DC-link driving a $7.5\,\mathrm{kW}$ Permanent Magnet Synchronous Motor (PMSM). The analysis is performed for an ML FCi, as it enables high efficiency and power density required for motor integration on the one hand and decreases the output filter volume with increasing output voltage level numbers N on the other hand. General scaling laws of the ML FCi are derived analytically and a Pareto optimization based on real hardware dimensions is performed to determine which number of levels is optimal in terms of power density and efficiency and which system performance is achieved for employing Si or GaN power transistors.**

I. Introduction

Today's variable speed drive systems are typically composed of a three-phase inverter and a separate motor connected via a motor cable. This distributed drive system allows high flexibility in the choice and combination of individual components, but results in relatively high complexity and requires a large installation space. Therefore, a trend has developed in recent years towards drive systems with motor-integrated inverters, which largely eliminate the need for complex wiring and thus enable simple installation of the drive system [1].

Motor-integrated drive systems rely on power electronics that on the one hand enables high power density ρ and/or high compactness, and on the other hand ensures high efficiency η to avoid further stressing the electronic components considering the already high temperature in the immediate vicinity of the motor. To accomplish these two objectives, fast-switching and low on-state resistance WBG power semiconductors are an attractive alternative to the established Si IGBTs, facilitating low switching and conduction losses. However, the fast switching transients are causing increased (radiated) EMI emissions as well as motor bearing currents and potentially result in reflections on motor cables and/or motor terminal over voltages, i.e. excessive stress on the motor winding insulation [2].

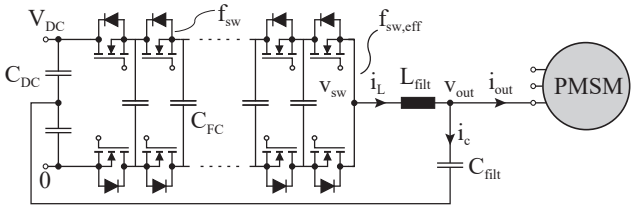

Fig. 1: Single bridge-leg of a three-phase Multi-Level (N-Level) Flying Capacitor inverter (ML FCi) with full sine wave LC output filter driving a three-phase PMSM.

One possible measure to protect the motor and reduce EMI emissions, is to use a DC-link referenced full sine wave LC filter between the inverter and the motor [3]. It also eliminates HF losses in the motor, resulting in an even higher overall system efficiency, and prevents low-frequency common-mode resonances in the motor windings, which can also occur in a motor-integrated system without long motor cables and regardless of the switching speed [4]. Advantageously, the LC filter cutoff frequency can be selected relatively high for WBG devices, which already ensures a low filter volume.

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TABLE I: Motor-integrated inverter specifications.

Parameter		Value
DC-Link Voltage	V_{DC}	$800\,\mathrm{V}$
Nominal Output Power	P_{nom}	$3 \times 2.5\,\mathrm{kW}$
Nominal Phase Current Peak Amplitude	$i_{\mathrm{out,nom}}$	$15\,\mathrm{A}$
Ambient Temperature	T_{amb}	$90\,^{\circ}\mathrm{C}$
Minimum Nominal Inverter Efficiency	$\eta_{\mathrm{nom,min}}$	$99\,\%$

Nevertheless, the filter volume still represents a significant share fo the overall inverter volume and limits the achievable power density.

In addition to the advantages gained at the device level, a modification on the topology level, i.e. the use of a *Multi-Level* (ML) instead of a 2L inverter concept further reduces the output filter volume, as it offers a multiplication of the individual device switching frequency and multiple output voltage levels allowing a closer approximation of the ideally sinusoidal output voltage waveform. Moreover, ML inverters benefit on the device level from the fact that low-voltage semiconductors with an improved Figure-of-Merit (FOM) can be used, further increasing system efficiency [5], [6]. Hence, ML inverters are ideally suited for motor integration.

In the literature, various ML inverter typologies such as the Cascaded H-Bridge (CHB), Neutral-Point Clamped (NPC) and Flying Capacitor (FC) inverter have been studied considering 3L, 5L, 7L, 9L, 10L or even 13L arrangements and different applications [7], [8]. However, it still has to be clarified which number of levels is ideal for motor integration in terms of efficiency η and power density ρ, as different to the aforementioned volume reduction of the output filter, a higher number of levels results in higher complexity, i.e. a higher number of switches, gate drivers, flying capacitors, measurement and control circuits and accordingly in a potentially larger converter volume as also shown in [9].
In this paper, the optimal number of levels is determined for a motor-integrated ML FC inverter (ML FCi) (cf. **Fig. 1**), which also offers DC operation capability to generate a motor standstill torque, first in a general form based on scaling laws and then using the example of an $800\,\mathrm{V}$ DC-link $7.5\,\mathrm{kW}$ variable speed drive system with specifications as given in **Table I**.
In **Section II** the general scaling of the power transistors, the Flying Capacitors (FC) and the LC output filter is derived for an ML FCi as a function of the number of levels N. In a first step, N-independent constant total semiconductor losses $P_{\mathrm{semi,tot}}$ are assumed, which are equally divided into conduction losses $P_{\mathrm{cond,tot}}$ and switching losses $P_{\mathrm{sw,tot}}$. The analysis could also be performed for an arbitrary loss distribution, i.e. $P_{\mathrm{cond,tot}} = s \cdot P_{\mathrm{semi,tot}}$ where $s = [0...1]$. In **Section III**, these assumptions are withdrawn and, based on the specifications of **Table I**, a Pareto optimization is performed for an ML FCi with respect to achievable efficiency η and (volumetric) power density ρ for different numbers of levels N. It is also investigated which N is optimal for realization of the ML FCi based on Si MOSFETs and GaN power transistors, whereby an implementation with discrete components and a fully integrated, chip-based realization are considered. Finally, **Section IV** concludes the paper.

TABLE II: Power semiconductor technology fitting parameters given such that all quantities concerned (e.g. R_{dson}, A_{die}, V_{rated}, $C_{\mathrm{oss,Q}}$, FOM) result in SI units.

Parameter	Si	GaN
k_{R}	$4.8 \cdot 10^{-13}$	$0.26 \cdot 10^{-9}$
α_{R}	2.5	1.1
k_{C}	$2.4 \cdot 10^{-1}$	$2.7 \cdot 10^{-3}$
α_{C}	-1.6	-0.7
k_{FOM}	$8.68 \cdot 10^{12}$	$1.42 \cdot 10^{12}$
α_{FOM}	-0.9	-0.4

II. Multi-Level Component Scaling

A. Power semiconductors

Compared to a 2L inverter, the DC-link voltage in an N-level inverter is divided equally among $(N-1)$ power semiconductors connected in series. Thus, as the number of levels N increases, the voltage V_{B} to be blocked by each semiconductor decreases with $1/(N-1)$, i.e. $V_{\mathrm{B}}(N) = V_{\mathrm{DC}}/(N-1)$. Depending on the application, V_{B} is typically set to about $50-70\,\%$ of the specified device blocking voltage V_{rated}. In the following analysis, for V_{B} a safety factor of $k_{\mathrm{s}} = 3/2$ is assumed, which results in a required N-dependent maximum voltage blocking capability V_{rated} (cf. **Fig. 3 (a)**) as

$$V_{\mathrm{rated}}(N) = k_{\mathrm{s}} \cdot V_{\mathrm{B}}(N) = k_{\mathrm{s}} \cdot \frac{V_{\mathrm{DC}}}{N-1}. \tag{1}$$

However, due to the series connection of the $(N-1)$ semiconductors, the total on-state resistance of one bridge-leg and/or phase $R_{\mathrm{dson,tot}}$ increases proportionally with the on-state resistance of a single switch R_{dson} and with the increasing level number N as $R_{\mathrm{dson,tot}}(N) = (N-1) \cdot R_{\mathrm{dson}}$. Under the above mentioned assumption of constant and N-independent semiconductor losses $P_{\mathrm{semi,tot}}$ (and equal partitioning into conduction and switching losses), this means that for constant conduction losses per bridge leg ($P_{\mathrm{cond,tot}} = R_{\mathrm{dson,tot}} \cdot I^2_{\mathrm{out,eff}}$), the same total on-state resistance $R_{\mathrm{dson,tot}}$ must be achieved in an N-level inverter as in a 2L inverter. Thus in an N-level inverter the on-state resistance per switch R_{dson} to be achieved (cf. **Fig. 3 (a)**) must decrease with increasing number of levels N by factor of $1/(N-1)$,

$$R_{\mathrm{dson}}(N) = \frac{R_{\mathrm{dson,tot}}}{(N-1)}. \tag{2}$$

This on-state resistance R_{dson} must be achieved at nominal junction temperature T_{j}, which according to **Table I** for the underlying application at least equals the ambient temperature $T_{\mathrm{j}} = T_{\mathrm{amb}} = 90\,^{\circ}\mathrm{C}$. Consequently, the R_{dson} typically specified in datasheets at $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$ must be selected even smaller. For the considered case of $90\,^{\circ}\mathrm{C}$, the on-state resistance of Si and GaN increases according to $R_{\mathrm{dson}}(90\,^{\circ}\mathrm{C}) = k_{\mathrm{T}} \cdot R_{\mathrm{dson}}(25\,^{\circ}\mathrm{C})$ approximately by a factor of $k_{\mathrm{T}} = 1.5$.

Furthermore, assuming that semiconductor technology and blocking voltage capability of the used devices remain unchanged, a reduction in on-state resistance $R_{\mathrm{dson}}(N)$ according to (2) would require the die area A_{die} of each switch to increase linearly with N. However, the required blocking voltage V_{rated} decreases according to (1) with $1/(N-1)$, which results in a lower on-state resistance R_{dson} for the same die area A_{die} as derived in [5]. The on-state resistance R_{dson} at $25\,^{\circ}\mathrm{C}$ of a single switch scales with rated voltage as

$$R_{\mathrm{dson}} = \frac{k_{\mathrm{R}} \cdot V_{\mathrm{rated}}^{\alpha_{\mathrm{R}}}}{A_{\mathrm{die}}}, \tag{3}$$

where the technology-specific constant k_{R} and the voltage-scaling factor α_{R} represent material parameters and are listed in **Table II** for Si and GaN power transistors.

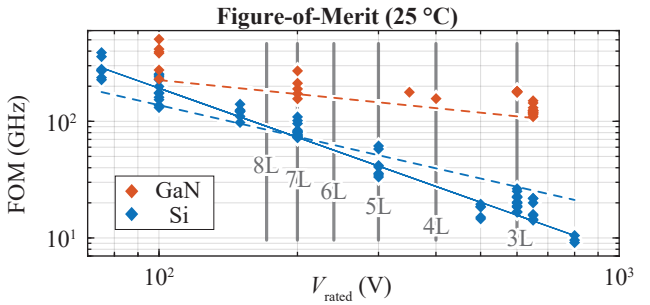

Fig. 2: FOM for latest commercially available Si and GaN power transistors for the R_{dson} at $25\,^{\circ}\mathrm{C}$ and $C_{\mathrm{oss,Q}}$ at $1/k_{\mathrm{s}} = 2/3$ of the rated voltage V_{rated}. Dashed trend lines are derived with (8) using the parameters given in **Table II**. For Si an alternative solid trend line is proposed for later use in the Pareto optimization. This helps not to overestimate devices with higher voltage ratings, as these additionally suffer from high Q_{rr} losses compared to the lower voltage semiconductors, an effect not captured by the FOM. The thick gray lines indicate the minimum semiconductor blocking voltage $V_{\mathrm{rated}}(N)$ required for the different numbers of levels N considering $k_{\mathrm{s}} = 3/2$ as safety factor.

As a result, $\alpha_{\mathrm{R}} >> 1$ implies that for a constant A_{die} the on-state resistance R_{dson} decreases even more than with $1/(N-1)$ as required in (2), which is e.g. the case for Si devices. Conversely, by substituting (2) into (3), the required chip area per switch A_{die} or the total chip area of a bridge-leg and/or phase of the inverter $A_{\mathrm{die,tot}}$ can be calculated as

$$A_{\mathrm{die}}(N) = \frac{k_{\mathrm{R}} \cdot V_{\mathrm{rated}}(N)^{\alpha_{\mathrm{R}}}}{R_{\mathrm{dson}}(N)} \propto (N-1)^{1-\alpha_{\mathrm{R}}} \tag{4}$$

and

$$A_{\mathrm{die,tot}}(N) = 2(N-1) \cdot A_{\mathrm{die}}(N) \propto (N-1)^{2-\alpha_{\mathrm{R}}}. \tag{5}$$

It can be seen that for a Si inverter and constant total on-state resistance $R_{\mathrm{dson,tot}}$, the chip area per switch A_{die} as well as the total chip area of the Si inverter $A_{\mathrm{die,tot}}$ decrease with increasing level number N (cf. **Fig. 3 (b)** and **(c)**). For GaN with $\alpha_{\mathrm{R}} = 1.1 \approx 1$, however, although A_{die} decreases slightly with increasing N, $A_{\mathrm{die,tot}}$ of the GaN inverter increases quasi linearly with N. When assuming constant costs per chip area [$\$/\mathrm{cm}^2$], a proportional scaling of the semiconductor costs with $A_{\mathrm{die,tot}}$ results. Thus for a Si inverter the costs decrease with increasing N, but are increasing for a GaN-based realization. If it is additionally considered that the costs per chip area decrease with lower blocking voltages V_{rated}, then the costs again scale proportionally with A_{die}, i.e. for Si a strong cost reduction with increasing N can be expected, while the costs for GaN remain almost constant or only slightly decrease with N.

One would also expect the charge-equivalent output capacitance of a switch $C_{\mathrm{oss,Q}}$ to decrease with a smaller A_{die}. However, since the semiconductor can be designed for a lower rated voltage V_{rated}, the expected $C_{\mathrm{oss,Q}}$ increases with lower V_{rated} or with increasing level number N (cf. **Fig. 3 (d)**) as

$$\begin{aligned} C_{\mathrm{oss,Q}}(N) &= k_{\mathrm{C}} \cdot V_{\mathrm{rated}}(N)^{\alpha_{\mathrm{C}}} \cdot A_{\mathrm{die}}(N) \\ &\propto (N-1)^{1-\alpha_{\mathrm{R}}-\alpha_{\mathrm{C}}} = (N-1)^{1+\alpha_{\mathrm{FOM}}}. \end{aligned} \tag{6}$$

The technology-specific constant k_{C} and the voltage-scaling factor α_{C} listed in **Table II** were determined empirically in [5] considering $C_{\mathrm{oss,Q}}$ at 2/3 V_{rated}.

The voltage-dependent $C_{\mathrm{oss,Q}}$ is an important parameter for the choice of semiconductors, because while the on-state resistance R_{dson} determines the conduction losses P_{cond}, $C_{\mathrm{oss,Q}}$ together with the switching frequency f_{sw} defines the minimum hard-switching losses

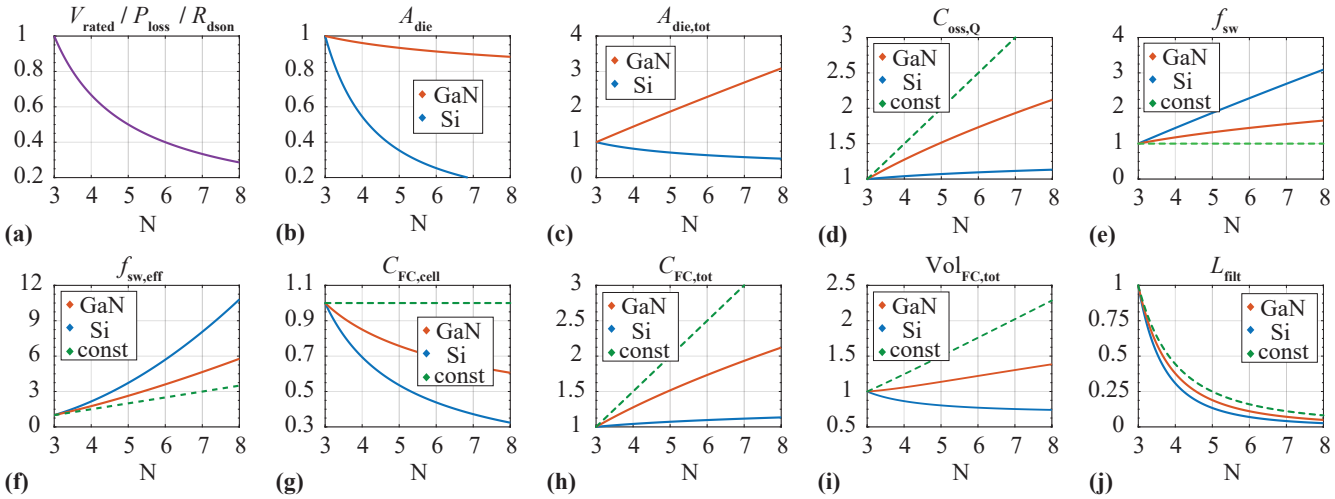

Fig. 3: Scaling of the different characteristic quantities in an ML FCi as a function of the number of levels N according to (1) to (15) for Si and GaN. The green dashed lines labeled with "const", emulate a semiconductor technology with a constant FOM ($\alpha_{\mathrm{FOM}} = 0$), where all semiconductors feature the same and blocking voltage independent FOM as a 600 V power transistor. This illustrates how much the FOM-dependent quantities of an FCi are affected by the topology itself and how much they are influenced by the choice of semiconductor technology. All plots are normalized with the corresponding values of an $N = 3$ design.

For a 99 % semiconductor efficiency at the nominal power and current specified in **Table I** and with equal partitioning in conduction and switching losses for $N = 3$, this results in an R_{dson} of 55.6 mΩ for both semiconductor technologies. The required die area for the same R_{dson} is larger for Si than for GaN with $A_{\mathrm{die,Si}} = 114\,\mathrm{mm}^2$ and $A_{\mathrm{die,GaN}} = 7.98\,\mathrm{mm}^2$. The respective charge equivalent output capacitance $C_{\mathrm{oss,Q,Si}} = 984\,\mathrm{pF}$ is also larger than $C_{\mathrm{oss,Q,GaN}} = 245\,\mathrm{pF}$, which results in a lower possible switching frequency for Si than for GaN with the same switching losses, i.e., $f_{\mathrm{sw,Si}} = 40\,\mathrm{kHz}$ and $f_{\mathrm{sw,GaN}} = 159\,\mathrm{kHz}$.

for zero-current switching (ZCS) according to

$$P_{\mathrm{semi,tot}}(N) = P_{\mathrm{cond,tot}} + P_{\mathrm{sw,tot}} = (N-1)\cdot(R_{\mathrm{dson}}\cdot I^2_{\mathrm{out,rms}} + f_{\mathrm{sw}}\cdot C_{\mathrm{oss,Q}}\cdot V_{\mathrm{B}}^2), \quad (7)$$

which along with the smaller current-dependent loss components (V-I overlap losses) - especially for fast current/voltage transitions - account for the largest part of the total switching losses. Therefore, to achieve high efficiencies and/or high switching frequencies, semiconductors with low R_{dson} and $C_{\mathrm{oss,Q}}$ are advantageously used.

In order to compare semiconductors with different on-state resistances R_{dson}, output capacitances $C_{\mathrm{oss,Q}}$, rated voltages V_{rated} and technologies (Si, GaN, SiC), various FOMs have been derived [5], [6], [10], where the simplest FOM is only defined by two mentioned quantities R_{dson} (cf. (3)) and $C_{\mathrm{oss,Q}}$ (cf. (6)) as

$$\mathrm{FOM} = \frac{1}{R_{\mathrm{dson}}\cdot C_{\mathrm{oss,Q}}} = k_{\mathrm{FOM}}\cdot V_{\mathrm{rated}}^{\alpha_{\mathrm{FOM}}}, \quad (8)$$

with $k_{\mathrm{FOM}} = 1/(k_{\mathrm{R}}\cdot k_{\mathrm{C}})$ and $\alpha_{\mathrm{FOM}} = -(\alpha_{\mathrm{R}} + \alpha_{\mathrm{C}})$ defined in [5]. Thus, a high FOM value corresponds to a low $R_{\mathrm{dson}}C_{\mathrm{oss,Q}}$-product or lower semiconductor losses. FOM values of commercially available Si and GaN semiconductor devices are shown in **Fig. 2** as a function of rated blocking voltage V_{rated}. In addition, the trend line given by (8) is indicated. As already shown in e.g. [5], for Si and GaN power semiconductors, the FOM increases with smaller blocking voltage V_{rated}, i.e., the semiconductor performance increases at lower blocking voltages, especially for Si due to a steeper slope (i.e. more negative α_{FOM}), motivating the choice of a high level number N. Furthermore, the minimum semiconductor blocking voltages $V_{\mathrm{rated}}(N)$ required for the different numbers of levels N are shown with thick gray lines in **Fig. 2**. It can be noted that the distances between the indicated lines of V_{rated} become narrower with increasing N, and thus the benefit in terms of improved semiconductor properties also decreases with increasing N. Especially for GaN featuring a relatively flat FOM over V_{rated}, a higher level number reduces the semiconductor losses less effectively.

Nevertheless, neglecting the current-dependent switching losses as in (7) for given total switching losses $P_{\mathrm{sw,tot}}$, the maximum possible switching frequency f_{sw} of one switching cell can be determined directly from $C_{\mathrm{oss,Q}}$ according to

$$f_{\mathrm{sw}}(N) = \frac{P_{\mathrm{sw,tot}}}{(N-1)\cdot C_{\mathrm{oss,Q}}(N)\cdot V_{\mathrm{B}}(N)^2} \propto (N-1)^{-\alpha_{\mathrm{FOM}}}. \quad (9)$$

As shown in **Fig. 3 (e)**, the switching frequency of each switching cell f_{sw} can be increased as the number of levels N increases, but the increase of f_{sw} becomes less and less for higher N, similar to the FOM. However, the effective switching frequency (cf. **Fig. 3 (f)**)

$$f_{\mathrm{sw,eff}}(N) = (N-1)\cdot f_{\mathrm{sw}}(N) \propto (N-1)^{1-\alpha_{\mathrm{FOM}}} \quad (10)$$

measurable at the switch node still increases with more than $(N-1)$, which is advantageous especially with regard to the LC output filter volume, as will be discussed in *Section II-C*.

B. Flying Capacitors

As thoroughly described in [11] for phase-shifted PWM, the Flying Capacitors (FC) of each FC cell, which here also include the DC-Link capacitors for high frequency currents, are sequentially charged and discharged with the load current i_{out}, whereas the duration of the charge and discharge interval actually depends on the converter operating condition. For phase-shifted PWM the worst case charge/discharge duration is found as $\delta T(N) = 1/f_{\mathrm{sw,eff}}(N) = 1/((N-1)\cdot f_{\mathrm{sw}}(N))$, leading to a worst case change in charge of $\delta Q_{\mathrm{FC}}(N) = i_{\mathrm{out,max}}/f_{\mathrm{sw,eff}}(N)$. The resulting peak-to-peak FC voltage ripple $\Delta V_{\mathrm{FC,pp}}(N) = \delta Q_{\mathrm{FC}}(N)/C_{\mathrm{FC,cell}}$ is either limited by the semiconductor blocking voltage V_{rated} and typically fixed at a certain percentage of $V_{\mathrm{B}}(N)$, i.e., $\Delta V_{\mathrm{FC,pp}}(N) = V_{\mathrm{B}}(N)\cdot k_{\mathrm{FC}}$ with k_{FC} in the range of $k_{\mathrm{FC}} = [0\ldots0.2]$, or is limited thermally by the maximum allowed RMS current in the flying capacitors. Neglecting the latter, the required capacitance per FC cell $C_{\mathrm{FC,cell}}$ is given with

$$C_{\mathrm{FC,cell}}(N) = \frac{i_{\mathrm{out,max}}}{\Delta V_{\mathrm{FC,pp}}(N)\cdot f_{\mathrm{eff}}(N)} \propto (N-1)^{\alpha_{\mathrm{FOM}}}. \quad (11)$$

Neglecting the advantage of increasing the switching frequency $f_{\mathrm{sw}}(N)$ due to better semiconductor FOM with increasing N, i.e. considering $\alpha_{\mathrm{FOM}} = 0$ and thus $f_{\mathrm{sw}}(N) = \text{const.}$, the required capacitance per cell $C_{\mathrm{FC,cell}}$ remains constant regardless of the chosen N, as derived in [8] and also indicated in **Fig. 3 (g)** with the green dashed line. However, considering the actual FOMs of Si and GaN, it can be noted that the required capacitance per cell even decreases with N. Accordingly, since for each cell the same capacitance $C_{\mathrm{FC,cell}}(N)$ is required, the total capacitance of a single phase $C_{\mathrm{FC,tot}}(N)$ is found as

$$C_{\mathrm{FC,tot}}(N) = (N-1) \cdot C_{\mathrm{FC,cell}} \propto (N-1)^{1+\alpha_{\mathrm{FOM}}}. \quad (12)$$

As shown in **Fig. 3 (h)**, $C_{\mathrm{FC,tot}}(N)$ increases linearly when $\alpha_{\mathrm{FOM}} = 0$, i.e., $f_{\mathrm{sw}}(N) = \text{const.}$ (green dashed line), however, when the actual FOMs are taken into account, the increase in total capacitance is much smaller, especially for Si.

For the calculation of the corresponding capacitor volume $\mathrm{Vol}_{\mathrm{FC,tot}}(N)$, it must be considered that the FCs of the different cells are operated with different bias voltages, i.e. $V_{\mathrm{FC,n}}(N) = V_{\mathrm{DC}}/(N-1) \cdot n$ with $n = [1...(N-1)]$ (cf. **Fig. 1**)). As the capacitor voltage rating increases, the dielectric layer thickness increases linearly [12], causing the volumetric capacitance density ρ_{cap} [F/m^3] to decrease. The corresponding scaling can be found under the simple assumption that for a given type of capacitor and a bias voltage doubling, two capacitors are connected in series in order to double the dielectric strength and two in parallel because of the required capacitance, and thus the capacitance density ρ_{cap} decreases quadratically with the rated capacitor voltage $V_{\mathrm{cap,rated}}$, i.e. with the stored energy, as

$$\rho_{\mathrm{cap}} = \frac{k_{\mathrm{cap}}}{V_{\mathrm{cap,rated}}^2}, \quad (13)$$

where a certain capacitor technology performance factor k_{cap} is considered. This scaling is verified by analyzing the capacitor density of commercially available ceramic and film capacitor series. The analysis also reveals that the X6S series from TDK shows one of the highest capacitance densities at zero voltage bias, with the empirically fitted value of $k_{\mathrm{cap}} = 6.24 \cdot 10^6$ FV^2/m^3. However, it has to be taken into account that the capacitance of Class II type ferroelectric ceramics strongly decays with increasing bias voltage. For example, the capacitance of the 450 V X6S capacitor (C5750X6S2W225K250KA) drops at rated voltage below $d = 20\,\%$ compared to the rated capacitance measured at zero voltage, thus in this case a five times larger capacitance must be installed compared to (12) if all capacitors were biased at the rated voltage (i.e. $V_{\mathrm{FC,n}}(N) = V_{\mathrm{cap,rated}}$). Nevertheless, even with derating, X6S capacitors still feature a higher capacitance density than bias-independent C0G ceramics or film capacitors, and are thus considered for the further analysis.

Consequently, in addition to the voltage-dependent nominal capacitance density according to (13), a bias-dependent capacitance derating d must also be taken into account when calculating the total FC volume of a single bridge-leg

$$\mathrm{Vol}_{\mathrm{FC,tot}}(N) = \sum_{n=1}^{N-1} \frac{C_{\mathrm{FC,cell}}(N) \cdot V_{\mathrm{FC,n}}(N)^2}{k_{\mathrm{cap}}} \cdot 1/d \propto (N-1)^{\alpha_{\mathrm{FOM}}-1} \cdot N \cdot (2N-1). \quad (14)$$

Assuming again a constant and N-independent switching frequency $f_{\mathrm{sw}}(N)$, the FC volume would increase sharply with N, as shown in **Fig. 3 (i)** (green dashed line). However, thanks to the improving FOM with increasing N, the increase in FC volume is weakened for GaN or the FC volume can even be reduced for Si.

C. Output Filter

The dimensioning of the output filter depends directly on $f_{\mathrm{sw,eff}}(N)$ and the voltage step amplitude $V_{\mathrm{DC}}/(N-1)$ measurable at the switch node of the ML FCi, since these directly define the necessary filter inductance for a desired maximum peak-to-peak current ripple $\Delta i_{\mathrm{L,pp}}$ as

$$L_{\mathrm{filt}}(N) = \frac{V_{\mathrm{DC}}/(N-1)}{4 \cdot f_{\mathrm{sw,eff}}(N) \cdot \Delta i_{\mathrm{L,pp}}} \propto (N-1)^{2-\alpha_{\mathrm{FOM}}}. \quad (15)$$

The corresponding scaling of the output filter inductor $L_{\mathrm{filt}}(N)$ assuming a constant current ripple is shown in **Fig. 3 (j)** for Si, GaN, and $f_{\mathrm{sw}}(N) = \text{const.}$. Consequently, selecting a certain current ripple, the output filter inductance $L_{\mathrm{filt}}(N)$ is directly defined. Subsequently, the output filter capacitance $C_{\mathrm{filt}}(N)$ is determined based on the required LC filter attenuation, e.g., to ensure a minimum output voltage quality. However, the choice of L and C is restricted to the following limits:

1) L_{min}: Maximum allowed current ripple $\Delta i_{\mathrm{L,pp}}$.
2) L_{max}: Maximum allowed voltage drop v_{L} across L_{filt} at maximum electrical output frequency $f_{\mathrm{out,max}}$.
3) $C_{\mathrm{min},1}$: Maximum allowed voltage ripple at the output Δv_{out}.
4) $C_{\mathrm{min},2}$: Minimum required filter attenuation at $f_{\mathrm{sw,eff}}$, such that $f_{\mathrm{sw,eff}}$ and the filter resonance frequency f_{LC} are well separated.
5) $C_{\mathrm{max},1}$: Minimal allowed f_{LC} such that $f_{\mathrm{out,max}}$ is not attenuated.
6) $C_{\mathrm{max},2}$: Maximum reactive current i_{C} for $f_{\mathrm{out,max}}$.

From this, the design with the smallest filter volume can be chosen, which generally coincides with the lowest possible inductance L_{filt}, since the volume of the filter capacitors is negligible in comparison.

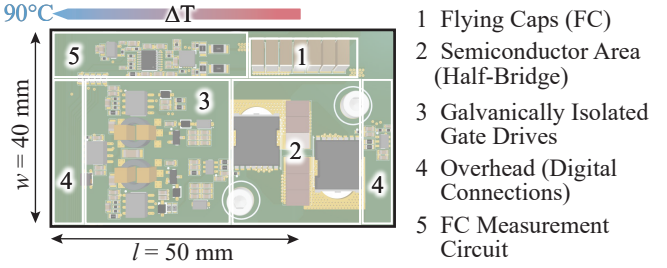

Fig. 4: Rendered 3D CAD image of the layout of a FC cell of the motor-integrated 7L FCi prototype power stage with labeling of the main components whose volume is considered in the Pareto optimization. It is assumed that the FC cell is mounted on a copper plate which is laterally attached to the 90°C motor housing. Thus, the heat is extracted from the semiconductor area (main loss source) to the housing with a maximum allowed $\Delta T = 8\,^{\circ}\mathrm{C}$ along the copper plate.

III. Pareto Analysis and Performance Evaluation

From the simplified analysis conducted up to this point, Si will benefit from a higher number of levels N in terms of power density since the total chip area $A_{\mathrm{die,tot}}$ as well as the filter inductance L_{filt} decrease and the required total flying capacitance $C_{\mathrm{FC,tot}}$ remains almost constant. However, for GaN the trend is not so obvious, since $A_{\mathrm{die,tot}}$ and $C_{\mathrm{FC,tot}}$ increase strongly and only L_{filt} becomes smaller. In order to evaluate the optimal N and achievable system performance over all efficiencies based on physical components and layouts, a $\eta\rho$-Pareto optimization is performed, considering a Si and a GaN based realization of the bridge-legs of the motor-integrated ML FCi with the specifications given in **Table I**. For this purpose, following assumptions were made:

- The optimization considers a peak-to-peak inductor current ripple $\Delta i_{\mathrm{L,pp}}$ of 80 % from the nominal peak output current $i_{\mathrm{out,nom}}$. The peak-to-peak FC voltage ripple $\Delta V_{\mathrm{FC,pp}}$ is limited to 15 % of $V_{\mathrm{B}}(N)$.
- Additional volumes for e.g. gate drivers, measurement circuits and electrical signal connections are taken into account accord-

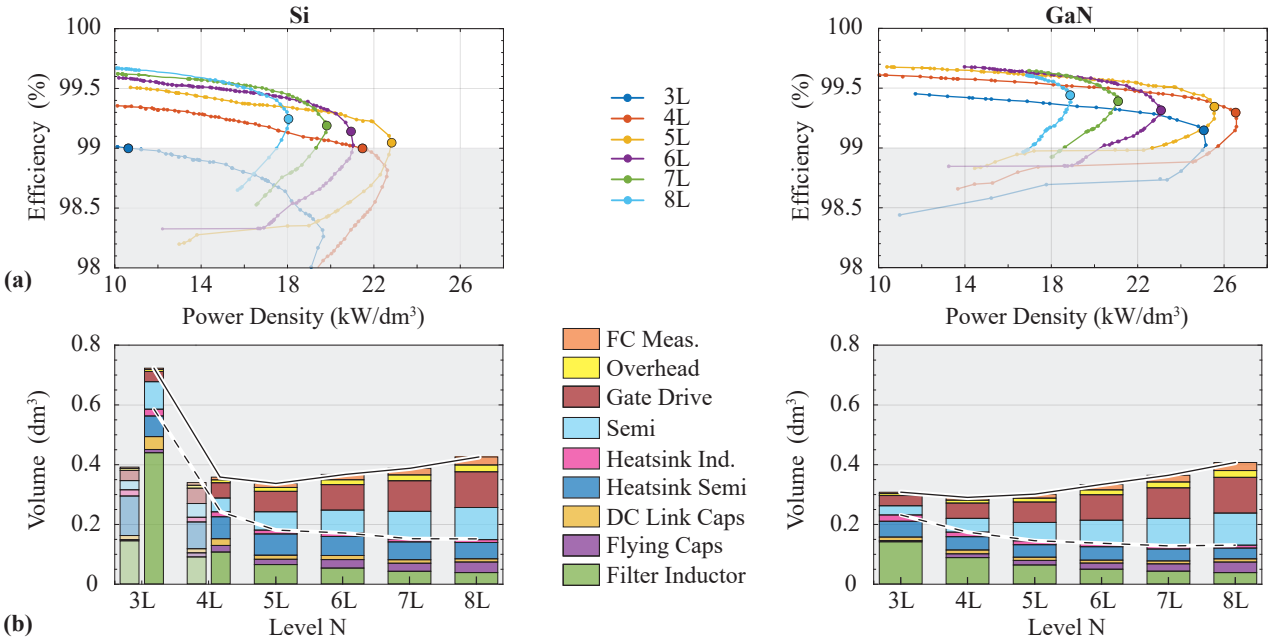

Fig. 5: (a) Pareto fronts of 7.5 kW 3L-8L FCis employing virtual FOM-based semiconductors with appropriate voltage rating $V_{\mathrm{rated}} = 3/2\ V_{\mathrm{B}}$ in either Si or GaN technology. **(b)** Overall volume distribution of Pareto-optimal designs with maximum power densities and efficiencies higher than 99 % (dots) considering a hardware realization with discrete components. The semitransparent volume bars for Si show the volume distribution for the Pareto-optimal designs with maximum power densities which do not reach the 99 % efficiency target. In addition, the dashed line indicates the overall volume obtained for the adoption of a fully integrated design, where the semiconductors, gate drives and measurement circuits are housed in a single package with negligible volume and/or integrated directly in the PCB.

ing to the layout of a 7L FCi cell shown in **Fig. 4** for a motor-integrated prototype with 200 V Si switches. The required heatsink volume is calculated based on the assumption that a single FCi cell is mounted on a copper plate, which is laterally attached to the 90 °C motor housing. As the width w and length l of the copper plate are given by the FCi cell layout, the thickness of the copper plate with a thermal conductivity of $\lambda = 394\,\mathrm{W/mK}$ is adjusted to achieve a maximum temperature difference of $\Delta T = 8\,^{\circ}\mathrm{C}$ along the plate up to the semiconductor area, where the majority of the losses originate (cf. **Fig. 4**). Any additional mechanical structures for mounting are not considered in the optimization.

- The FCs (including the high frequency DC link capacitors) are realized with the already mentioned 450 V X6S capacitors. Additionally, the losses of the FCs are calculated from the RMS current as proposed in [13] and in case the maximum rated capacitor operating temperature would be exceeded, the capacitance value is increased accordingly.
- The volume and losses of the output filter inductor L_{filt} are calculated with a design script that uses toroidal powder cores with soft saturation characteristics and low losses at high frequencies (KoolMu HF from Magnetics [14]).

The resulting Pareto fronts for a 3L to 8L FCi employing either Si or GaN semiconductors and featuring the FOMs discussed in *Section II-A* are shown in **Fig. 5 (a)**. It is noted that for both semiconductor technologies, the efficiency increases with higher numbers of levels because low-voltage semiconductors with an improved FOM can be used, resulting in lower switching and conduction losses. Furthermore, regardless of the selected number of levels, the power density can be increased by selecting a higher switching frequency f_{sw}, since the volumes of passive components (FCs and output filter) are reduced. However, due to higher switching losses, this comes at the cost of lower efficiency, even though the Pareto optimization tries to counteract this increase by selecting semiconductors with smaller die areas, i.e. smaller $C_{\mathrm{oss,Q}}$, because at the same time this leads to larger conduction losses due to a larger R_{dson}.

Higher switching frequency also results in a larger heat sink volume (thicker copper plate), which compensates the volume reduction of the passive components at the maximum achievable power density. In addition, the volume reduction of the inductor stagnates at this point, since it is limited either thermally by a higher core loss density or mechanically by e.g. a minimum wall thickness of 3 mm.

The Pareto-optimal designs with the highest power density at a minimum efficiency of 99 % (dots in **Fig. 5 (a)**) are compared in terms of volume **Fig. 5 (b)** for different numbers of levels N. The semitransparent volume bars for Si show the volume distribution of the Pareto-optimal designs with maximum power density, which however do not reach the 99 % efficiency level.

For both semiconductor technologies, it can be seen that the efficiency achieved for the Pareto-optimal design with maximum power density increases with the number of levels N. However, apart from a Si 3L design, this efficiency improvement leads to an almost constantly increasing total FCi volume, i.e., with a Si 5L FCi and a GaN 4L FCi the highest power density is achieved if a realization with discrete devices and components is considered. For GaN, it can be further observed that already for the GaN 3L FCi a high power density and a similar overall volume as for the 4L FCi is obtained. This can be explained by the fact that for GaN already at $N = 3$ a high switching frequency can be selected, resulting in an inductor volume that is already smaller than the volume occupied by the half-bridges, gate drives and measurement circuits. Thus, as N is further increased, these volumes increase more than what can be saved with a smaller inductor volume, resulting in an overall optimal 4L FCi design for GaN.

In contrast, for Si and considering the 99 % efficiency target, the inductor volume strongly dominates the overall FCi volume for $N = 3$. Therefore, with a higher number of levels N, this dominant volume fraction is greatly reduced and the total volume reaches its minimum at $N = 5$. For higher N, the volume shares of the half-bridges, gate drivers and measuring circuits start to dominate and the

total volume increases accordingly.
Nevertheless, considering now a suitable realization of the optimal 4L GaN FCi, it is found that there are no commercially available $400\,\mathrm{V}$ GaN switches which would be required for an $N = 4$ design. Therefore, the same semiconductors as for an $N = 3$ would have to be used (e.g. blocking voltages around $600\,\mathrm{V}$/$650\,\mathrm{V}$), which would shift the Pareto front to lower efficiencies and power densities. For the same reason, a strong shift of the Pareto fronts for $N = 5$ and 6 can be observed for GaN, where currently only $200\,\mathrm{V}$ and $600\,\mathrm{V}$/$650\,\mathrm{V}$ switches are available on the market which also offer a greater variety of R_{dson} values. With these considerations, the optimal feasible design for GaN results in a 3L FCi.
If semiconductor availability is also considered for Si, $300\,\mathrm{V}$ Si switches are available for the optimal Si design with N = 5, but the current $300\,\mathrm{V}$ Si switches suffer from large reverse recovery losses (Q_{rr} losses), which are not included in the selected FOM[1]. The same is true for N = 6, so a 7L Si FCi with competitive $200\,\mathrm{V}$ semiconductors emerges as a feasible design for Si when discrete devices and components are used.
In general, however, it can be seen in **Fig. 5 (b)** that for ML FCis with a higher number of levels, a large part of the total FCi volume consists of gate drivers, semiconductors, measurement circuits and additional volume, e.g. for signal tracks on the PCB (cf. layout in **Fig. 4**), if discrete components are used. These volumes are highly dependent on the available IC packages and the designer's circuit choice, as one can, for example, choose between bootstrap circuitry or galvanic isolation [15] to power the gate drives, or choose a more integrated gate driver option [16], which is becoming more popular due to reduced complexity and improved switching performance. Theoretically, a customized solution is also possible where these functions are fully integrated into a single chip or even into the PCB. To account for this degree of freedom of realization, the dashed line in **Fig. 5 (b)** shows the trend of a "fully integrated ML FCi realization, where only the volumes of the filter inductor, the capacitors, the heat sink and the semiconductors are considered. This solution now shows the other extreme and the truth for the fully integrated system lies somewhere between the solid and dashed lines of **Fig. 5 (b)**. Basically, however, it can be stated that for the given specifications of the motor-integrated converter, even a fully integrated design with more than $N = 6 - 8$ cannot significantly increase the power density anymore.

IV. Conclusions

In this paper, the optimal number of voltage levels for a motor-integrated $7.5\,\mathrm{kW}$ flying capacitor inverter with LC full sine wave output filter is investigated with respect to the selected semiconductor technology (Si/GaN). Based on derived scaling laws and subsequently performed comprehensive $\eta\rho$-Pareto optimizations it is shown that higher numbers of levels N are especially useful for semiconductor technologies whose Figure-of-Merit (FOM) strongly depends on the power semiconductor voltage blocking capability, i.e. show a large negative α_{FOM}, as given for Si power transistors. WBG power semiconductors show a significantly better, but rather flat FOM characteristic, which means that already with a low number of voltage levels a high efficiency and a high power density are achieved, but with increasing number of levels this performance cannot be enhanced significantly anymore.
Taking into account the discrete blocking voltage levels of commercially available semiconductors and, especially for Si, the additional reverse recovery losses occurring for hard switching, the *7L Si FCi* as well as the *3L GaN FCi* achieve the highest (volumetric) power densities in the Pareto optimizations for a design with discrete components (power transistors, gate drives, isolated gate drive power supplies, etc.) and a minimum required efficiency of $99\,\%$. The comparison between the two implementations shows that compared to the 7L Si FCi, with the 3L GaN FCi the inverter volume can be reduced by another $20\,\%$ with considerably less complexity.
Moreover, the study reveals that with the trend towards fully integrated implementations, in which the required volume for gate drivers, measurement and control circuits is largely eliminated, the optimal number of levels shifts to higher values, but the benefit in power density decreases significantly for level numbers beyond $N = 6 - 8$.

[1]The reverse recovery losses could be considered as shown in [6], if manufacturers would specify the required information in the datasheet.

References

[1] T. M. Jahns and B. Sarlioglu, "The Incredible Shrinking Motor Drive: Accelerating the Transition to Integrated Motor Drives," *IEEE Power Electronics Magazine*, vol. 7, no. 3, pp. 18–27, Sep. 2020.
[2] J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "Effect of PWM Inverters on AC Motor Bearing Currents and Shaft Voltages," *IEEE Transactions on Industry Applications*, vol. 32, no. 2, pp. 250–259, Mar. 1996.
[3] M. Antivachis, P. Niklaus, D. Bortis, and J. W. Kolar, "Input/Output EMI Filter Design for Three-Phase Ultra-High Speed Motor Drive GaN Inverter Stage," *CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 1, pp. 74–92, Mar. 2021.
[4] S. Sundeep, J. Wang, A. Griffo, and F. Alvarez-Gonzalez, "Anti-resonance Phenomenon and Peak Voltage Stress within PWM Inverter Fed Stator Winding," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2021.
[5] J. Azurza Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020.
[6] D. Cittanti, E. Vico, and I. R. Bojoi, "New FOM-Based Performance Evaluation of 600/650 V SiC and GaN Semiconductors for Next-Generation EV Drives," *IEEE Access*, vol. 10, pp. 51 693–51 707, 2022.
[7] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, and R. P. Aguilera, "Modular Multilevel Converters: Recent Achievements and Challenges," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 224–239, 2021.
[8] C. B. Barth, P. Assem, T. Foulkes, W. H. Chung, T. Modeer, Y. Lei, and R. C. N. Pilawa-Podgurski, "Design and Control of a GaN-Based, 13-Level, Flying Capacitor Multilevel Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2179–2191, Sep. 2020.
[9] J. Wu, Y. Qi, F. Muhammad, and X. Wu, "A Unified Switch Loss Model and Design Consideration for Multilevel Boost PFC with GaN Devices," *CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 4, pp. 349–358, Dec. 2021.
[10] M. Guacci, J. Azurza Anderson, K. L. Pally, D. Bortis, J. W. Kolar, M. J. Kasper, J. Sanchez, and G. Deboy, "Experimental Characterization of Silicon and Gallium Nitride 200 V Power Semiconductors for Modular/Multi-Level Converters Using Advanced Measurement Techniques," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2238–2254, Sep. 2020.
[11] C. B. Barth, P. Assem, T. Foulkes, W. H. Chung, T. Modeer, Y. Lei, and R. C. N. Pilawa-Podgurski, "Design and Control of a GaN-Based, 13-Level, Flying Capacitor Multilevel Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2179–2191, Sep. 2020.
[12] M.-J. Pan and C. A. Randall, "A brief introduction to ceramic capacitors," *IEEE Electrical Insulation Magazine*, vol. 26, no. 3, pp. 44–50, May 2010.
[13] S. Coday and R. C. Pilawa-Podgurski, "High Accuracy Calorimetric Measurements and Modeling of Ceramic Capacitor Losses Under Large Ripple Operation," in *Proc. of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans (LA), Mar. 2020, pp. 188–194.
[14] Magnetics, "Magnetics - Kool Mu HF Cores," https://www.mag-inc.com/Kool-Mu-HF-Cores, Jul. 2022.
[15] Z. Ye and R. C. N. Pilawa-Podgurski, "A Power Supply Circuit for Gate Driver of GaN-Based Flying Capacitor Multi-Level Converters," in *Proc. of the 4th IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov. 2016, pp. 53–58.
[16] A. Lidow, "Gallium Nitride Integration: Breaking Down Technical Barriers Quickly," *IEEE Power Electronics Magazine*, vol. 7, no. 1, pp. 56–63, Mar. 2020.