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Electrical and Thermal Characterization of an Inductor-Based ANPC-Type Buck Converter in 14 nm CMOS Technology for Microprocessor Applications

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ABSTRACT Integrated Voltage Regulators (IVRs) are attractive substitutes for conventional voltage regulators located on the motherboards, due to outstanding dynamic performances and superior power densities. IVRs operate with switching frequencies in the range of 100 MHz and are assembled in highly compact packages close to the microprocessor load. This paper presents a comprehensive characterization of a PCB- and inductor-based four-phase ANPC-type IVR that uses a Power Management IC (PMIC) implemented in a 14 nm CMOS technology node. The characterization is based on the results of electrical measurements, thermal inspections of the chip surface, and simulations, which enables the separation of the total losses into on-chip and off-chip loss components and the allocation of important loss components inside the chip. The investigated IVR achieves a maximum efficiency of 84.1% at an output power of $P_{\text{out}} = 640\,\text{mW}$ and a switching frequency of $f_{\text{s}} = 50\,\text{MHz}$. The thermal measurements reveal that the maximum efficiency of the PMIC itself is between 88 % and 90 % at $f_{\text{s}} = 50\,\text{MHz}$ and $P_{\text{out}} \in [500\,\text{mW},\ 600\,\text{mW}]$; at $P_{\text{out}} = 890\,\text{mW}$, a chip current density of $24.7\,\text{A/mm}^2$ is achieved. The findings in particular point out that the losses in the chip-internal interconnections, i.e., the conductors of the Power Distribution Network (PDN) and the twelve stacked metal layers below the PDN, have a substantial contribution to the total losses. Furthermore, the combination of Cadence post-layout simulations with impedance networks obtained from an appropriate software tool, e.g., FastHenry, is found to establish a suitable toolbox for estimating losses in IVRs.

INDEX TERMS 14 nm technology, ANPC, CMOS, half-bridge, IVR, multi-phase, PMIC, stacked transistors, thermal electrical characterization.

I. INTRODUCTION

Cloud computing in data-centers, internet-of-things devices, as well as applications related to mobile communication, automotive, and artificial intelligence drive the needs for increased data processing capabilities of modern microprocessors, which, today, operate at clock frequencies up to 5 GHz [1] and have tens of cores in their more advanced versions [1]–[3]. Increased computational power of microprocessors has been achieved by reducing the transistors' gate widths to below 22 nm in recent technology nodes, leading to breakdown voltages of less than 1 V. However, the performance increase comes at the cost of increased power consumption, exceeding 150 W per device [4], and is accompanied by high supply currents reaching values close to 100 A considering a typical package voltage of 1.8 V [5]. In this regard, the concepts of independent Voltage Domains (VDs) for different cores or

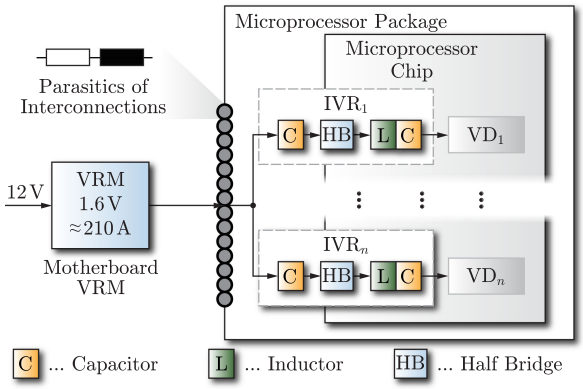

FIG. 1. Granular power delivery of a modern microprocessor system, where a single external voltage regulator provides power to multiple IVRs.

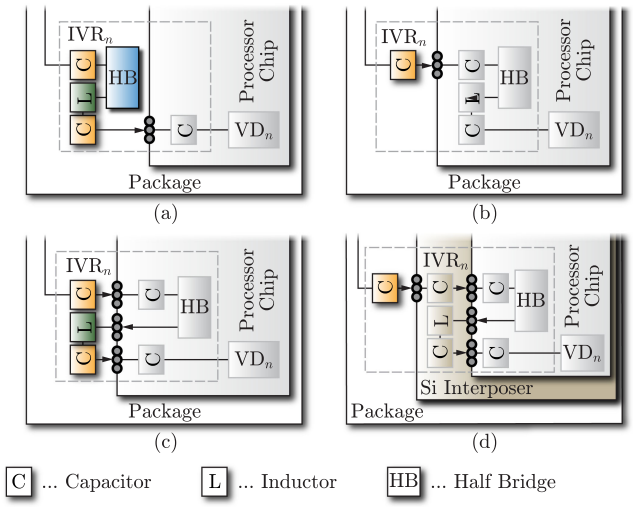

FIG. 2. Packaging solutions of IVRs providing granular power delivery in modern microprocessors. (a) Fully on-package IVR [6]; (b) fully on-die IVR [7]–[9]; (c) and (d) hybrid IVRs where the half-bridges are on the microprocessor die and the main passive components (inductors and capacitors) integrated into the package [10]–[12] or the silicon interposer [13]–[15].

parts of the core and Dynamic Voltage and Frequency Scaling (DVFS) are effective countermeasures to reduce the power demands of microprocessors, since each core can be separately operated according to its workload. This is achieved with a granular power delivery system that uses several independent Integrated Voltage Regulators (IVRs) for the different VDs, cf. Fig. 1.

Literature reveals numerous different realizations of IVRs, ranging from on-package implementations to fully chip-integrated solutions. In case of on-package implementations, a common package accommodates all components of the IVRs and the microprocessor, however, the IVRs do not reside in the microprocessor die itself (off-die), cf. Fig. 2(a) [6]. On-package IVRs allow for reduced parasitics of the supply lines (resistances, lead inductances), as compared to conventional (off-package) voltage regulators, however, they are still too large to be suitable for microprocessor applications that require very thin cases and tens of VDs, e.g., mobile phones, laptop computers, and tablets. By contrast, in case of fully chip-integrated (on-die) IVRs, all components reside on the microprocessor die, as shown in Fig. 2(b). Fully integrated IVRs realize very low parasitics of the supply lines and enable a reduction of the number of supply connections between the package and the microprocessor die, due to the reduced total input current. However, these benefits come at the cost of substantial chip area being sacrificed for the IVRs' components [7], [8] and / or highly challenging realization of chip-integrated inductors, e.g., due to the need of complex Through Silicon Vias (TSVs) [9] and additional Back End Of Line (BEOL) post-processing steps [8]. In addition, the chip technology node used for the microprocessor defines stringent design constraints, which considerably limit the flexibility of the converter design.

In an alternative approach, denoted as hybrid IVRs in this paper, only the active switching stages of the IVRs and necessary parts of the dc capacitors reside on-die and the remaining passive components, in particular the inductors in case of buck-type solutions, are located in the package or in a lower-cost second chip (silicon interposer), as shown in Fig. 2(c), (d). Hybrid IVRs can operate at very high switching frequencies of more than 100 MHz, due to the low switching losses of the microprocessor's transistors, and benefit from increased flexibilities for designing the passive components that reside in the package [10]–[12] or on the silicon interposer [13]–[16]. Compared to fully chip-integrated IVRs, hybrid solutions feature a reduction of the occupied microprocessor chip area and / or the use of less challenging connections between on-die and off-die components, at the cost of an increased number of connections to and from the microprocessor die. For both, package-based and interposer-based hybrid IVRs, high inductor and chip current densities, e.g., 3.2 A/mm^2 and 10.8 A/mm^2 respectively in [15], and efficiencies around 90 % have been reported [10], [13].

All realizations of IVRs have in common that the converter design is not straightforward, since technically reasonable realizations are feasible within relatively wide ranges of values for different design variables, e.g., switching frequency and inductor current ripple in case of a buck converter. However, the chosen values have an impact on the finally achieved efficiency. Accordingly, a systematic converter design approach, using model-based optimization, is commonly conducted [17]. In this regard, a continuous verification and refinement as well as the identification of eventually present deficiencies of the used models is important, in particular in case of emerging technologies, to gain a better understanding of the technology and to improve the accuracies of subsequent optimizations. According to a literature research, most related work focuses on electrical or thermal characterizations of selected on-package and chip-integrated components. With regard to electrical characterization, references [12], [18]–[20], for example, present measured impedance characteristics of

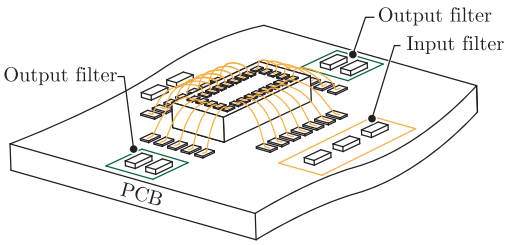

FIG. 3. Illustration of the investigated setup: the active switching stage resides in the Power Management IC (PMIC), the passive components (capacitors, inductors) on the PCB, and bond wires provide the electrical connections.

on-package conventional and coupled inductors, without and with magnetic core, or examine parasitic resistances and capacitances of key components in Through Silicon Interposers, i.e., metal layers for BEOL interconnects, TSVs, redistribution layer, and micro-bumps. In case of thermal characterizations, related publications typically focus on the identification of peak chip temperatures in order to determine measures to prevent overheating, e.g., observations of chip temperatures under different load conditions [21], [22] and thermal characterization of a microprocessor to derive guidelines for on-line thermal management [23], [24]. Only few publications discuss complete models of IVRs and provide experimental results for verification, e.g., [15], [25] for the realization of a buck-type IVR realized in 45 nm CMOS technology.

Common topologies for IVRs are Switched Capacitor (SC) and buck converters. Since SC converters have been analyzed in detail in a previous investigation [26], the authors intentionally decided to focus on a buck converter, with the aim of this paper being the identification and allocation of the loss components in a four-phase buck-type hybrid IVR, which employs a switching stage realized in 14 nm CMOS technology. Electrical and thermal measurements are conducted in order to enable a separation of on-chip losses (e.g., due to conduction and switching) and off-chip losses (e.g., in the inductors), which requires a physical separation of the chip and the inductors. The investigated IVR employs discrete inductors and capacitors that reside on a Printed Circuit Board (PCB); bond wires provide the electrical connections between chip and PCB, which is illustrated in Fig. 3. To begin with, **Section II** details the implemented Power Management IC (PMIC), i.e., converter specifications, main schematic diagram of the semiconductor power stage, chip lithograpy, and gate signal generation unit. **Section III** describes the conducted thermal and electrical characterization procedures that serve for the separation of the total losses into on-chip and off-chip components and discusses the obtained results, which reveal that the losses in the metal layers and the Power Distribution Network (PDN) of the PMIC have a substantial contribution to the total losses. The complete IVR achieves a maximum efficiency of 84.1 % and a full-load efficiency of 83.0 % and a corresponding chip current density of 24.7 W/mm^2. The maximum efficiency of the PMIC itself, which is subject to increased uncertainty due to the measurement with thermal camera, is between 88% to 90% for output power levels between 500 mW and 600 mW.

TABLE I Specifications of the Investigated four-phase IVR.

Parameters	Symbol	Value
Input voltage	V_{in}	1.6 V
Output voltage range	V_{out}	0.8 V to 1.2 V
Output power	P_{out}	800 mW
Max. input voltage ripple	$\Delta V_{\text{in,pp}}$	$V_{\text{in}} \cdot 1.2\% = 19.2$ mV
Min. output voltage	$V_{\text{out,min}}$	0.6 V

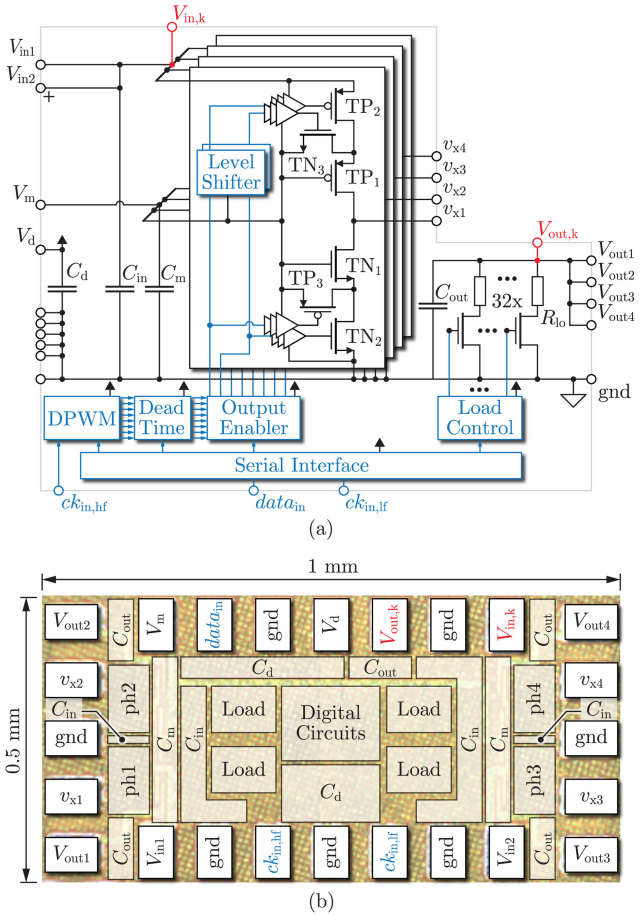

FIG. 4. (a) Simplified schematics of the PMIC containing the four-phase CMOS ANPC HBs. (b) Chip micrography of the implemented PMIC with the pads according to (a); 'ph1' to 'ph4' denote the locations of the HBs of the four converter phases; 'C_{in},' 'C_{m},' 'C_{out},' and 'C_{d}' refer to the positions of the corresponding capacitances realized with MOS technology; loads and gate signal generation unit are located toward the center of the PMIC.

II. PMIC IN 14 NM CMOS TECHNOLOGY

Table I lists the specifications of the investigated IVR, which is a prototype of an IVR intended for providing power to a VD of a CPU core, and Fig. 4(a) depicts the schematics of the implemented PMIC. Since the input voltage of 1.6 V exceeds the transistors' maximum drain-source voltage of a short channel device of the technology, each switch of the

realized buck converter is composed of the two stacked transistors. Furthermore, TN_3 and TP_3 in Fig. 4(a) realize an Active Neutral Point Clamping (ANPC) circuit in order to avoid unbalanced voltages across the main power transistors during or after switching, to improve efficiency and reliability [27].[1] The chip consists of four CMOS Half-Bridges (HBs) with ANPC, an open-loop logic circuitry to generate the switches' gate signals, and a configurable internal resistive load.

The chip requires three supply voltages. The main supply is connected to the $V_{\text{in}\{1,2\}}$-pads, which share the converter input current. An auxiliary voltage is provided at the V_{m}-pad, to define the gate bias voltages for TP_1 and TN_1 and the source potentials of the clamping switches TN_3 and TP_3. There, the applied voltage needs to be controlled to half of the input voltage, $V_{\text{m}} = V_{\text{in}}/2$, to avoid additional leakage currents.

The voltage supply of the auxiliary analog and digital circuits (open-loop logic circuitry, load control circuitry, serial interface, and flash memory) is connected to the V_{d}-pad. A two-wire unidirectional serial interface (pads $data_{\text{in}}$ and $ck_{\text{in,lf}}$ for data and clock inputs, respectively) serves for the configuration of gate signal generation unit and on-chip load; an on-chip flash memory stores the current configuration.

The signal provided at the $ck_{\text{in,hf}}$-pad controls the switching frequency of the CMOS ANPC HBs. The frequency of the given clock signal is divided by 16, e.g., a clock signal with a frequency of 1.6 GHz at the $ck_{\text{in,hf}}$-pad results in a switching frequency of 100 MHz. The switched output voltages are present at the $v_{\text{x}\{1,2,3,4\}}$-pads and applied to the external filter inductors. The filtered output voltages are connected back to the PMIC at the $V_{\text{out}\{1,2,3,4\}}$-pads, to utilize the chip-integrated configurable load. The chip includes two Kelvin pads, $V_{\text{in,k}}$ and $V_{\text{out,k}}$, to allow for accurate four-point voltage measurements of the input and output voltages, respectively. Seven ground pads are used in parallel to reduce the converter losses and provide a stable reference for the internal chip circuits.

Fig. 4(b) shows the micrography of the realized PMIC in 14 nm CMOS technology. The total chip area is 0.5 mm^2, from which 0.032 mm^2 are dedicated to the HBs of the four-phase converter [ph{1,2,3,4} in Fig. 4(b)], 0.027 mm^2 to the digital circuits, and 0.052 mm^2 to the four chip-internal loads. The power stages are placed at the edges of the chip, to achieve a layout that features short paths to the respective input and output pads, e.g., $V_{\text{in,1}}$ and $v_{\text{x,1}}$ in case of phase 1, in order to avoid excessive conduction losses in the Power Distribution Network (PDN) of the chip, as further detailed in Section III. Chip-integrated buffering of the supply voltages V_{in}, V_{m}, and V_{d} and the voltage provided to the load, V_{out}, is realized with a combination of Metal-Oxide-Semiconductor (MOS) and Metal-Insulator-Metal (MIM) capacitors. The MOS capacitors are placed in the Front End Of Line (FEOL) areas marked in Fig. 4(b) and MIM capacitors are placed in the entire BEOL area of the chip excluding the pads. Fig. 5(c) illustrates a cross-sectional drawing of the power stage, revealing FEOL, BEOL, and the general locations of MIM and MOS capacitors.

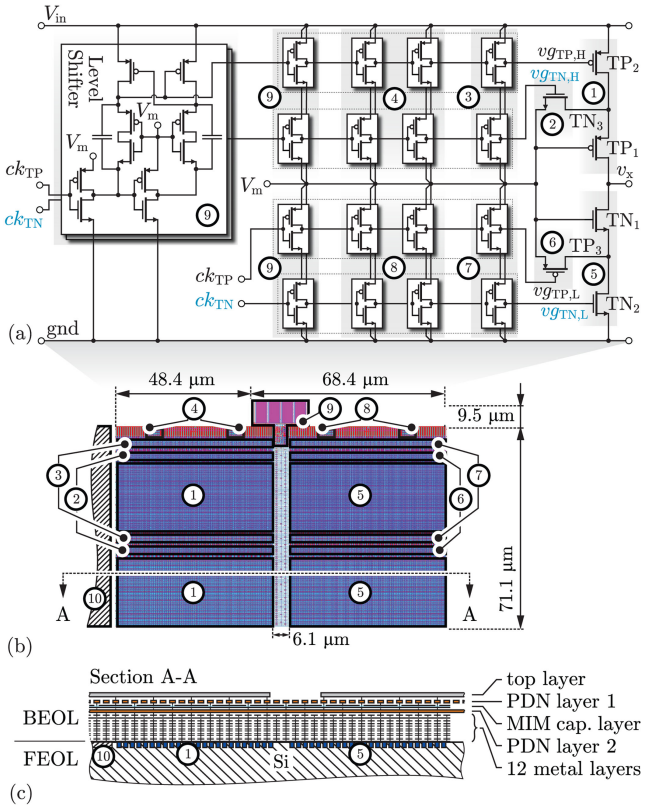

FIG. 5. (a) Schematics of a single converter phase of the CMOS ANPC HB; (b) Layout picture of the designed CMOS ANPC HB corresponding to the schematics of Fig. 5(a)). The two clamping switches, two independent gate drivers, and one level shifter increase the chip FEOL area by approximately 14% as compared to a conventional CMOS HB with stacked transistors.

A. POWER STAGE

Fig. 5(a) depicts a detailed schematic drawing of a single CMOS ANPC HB phase of the implemented PMIC. The output stage is composed of the main transistors (①: TP_1, TP_2; ⑤: TN_1, TN_2) and the clamping transistors (②: TN_3 and ⑥: TP_3). Four gate drivers, ③, ④, ⑦, ⑧, ⑨, are used for the main switches and the clamping switches, where each gate driver is composed of four inverter stages that are connected in series. Two level-shifters ⑨ adjust the voltages of the input signals in order to be suitable for the high-side gate drivers.

Fig. 5(b) presents the layout of a single converter phase corresponding to the schematics of Fig. 5(a) and Fig. 5(c) depicts a drawing of the cross section of the chip, revealing the top metal layer (contains the pads), the two layers of the PDN with the MIM capacitor layer in between, and the 12 metal layers. The FEOL area of the complete power stage is 0.0081 mm^2. All main transistors (① and ⑤) are of same size, each clamping transistor (② and ⑥) and the final inverter stage of each gate driver (③ and ⑦) require 1/10 of the area of

[1] According to [27] the ANPC topology is expected to achieve an increase of the efficiency by up to 2% at a switching frequency of 250 MHz.

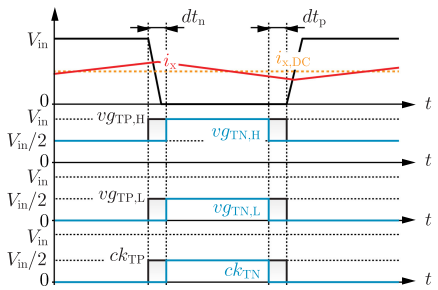

FIG. 6. Clock and gate signals of a single CMOS ANPC HB [27].

one main transistor, and the second and third stages of each gate driver (④ and ⑧) together need 1/50 of the area of one main transistor. The two additional gate drivers for the clamping transistors and the additional level shifter increase the total chip FEOL area by approximately 14% as compared to a conventional CMOS HB with stacked transistors. The remaining FEOL area is used to realize MOS capacitors (⑩).

B. GENERATION OF GATE SIGNALS

Each phase of the CMOS ANPC HB uses the gate signals depicted in Fig. 6 to generate a rectangular voltage with its main transistors at the respective output node, i.e., $v_{x,i} = 0$ or $v_{x,i} = V_{in}$ for $i \in \{1, 2, 3, 4\}$, and to balance the voltages across the stacked main transistors with the clamping transistors. The shown sequence is based on two complementary signals with dead time, ck_{TP} and ck_{TN}, and uses separate dead times, dt_n and dt_p, for the falling and rising edges of the rectangular output voltage.[2] The durations of both dead times, dt_n and dt_p, are programmable in order to enable the operating-point dependent optimization of the switching losses. Further details related to the operation of the CMOS ANPC HB are presented in [27].

Fig. 7 shows the simplified schematics of the open-loop circuitry that is used to generate $ck_{TP\{1,\ldots4\}}$ and $ck_{TN\{1,\ldots4\}}$ and $ck_{TN\{1,\ldots4\}}$ for all four converter phases. The combination of four-bit counter, four-bit comparator, and RS latch is used to generate a PWM signal with a frequency equal to $f_{ck}/16$ and a programmable duty cycle that can be adjusted with a resolution of $\Delta T = 1/f_{ck}$. Three shift registers further process the PWM signal in order to generate gate signals that are phase shifted by 90°, 180°, and 270°; from this, a configurable phase angle selector block redirects selected PWM signals, with or without phase shift, to the dead time generation units of the four converter phases. Finally, phase-enabling circuits allow for a proper deactivation of all transistors of a selected output stage, which enables the implementation of phase-shedding to achieve increased part-load efficiency.

[2]Please note that TP_1, TP_2, and TP_3 are p-type transistors, e.g., $vg_{TP,L} = 0$ turns TP_3 on and $vg_{TP,L} = V_{in}/2$ turns TP_3 off. Accordingly, the gate drivers ensure that TN_2, TP_2, TN_3, and TP_3 are turned off during both dead times.

TABLE II Accuracies of DAU34970 (voltage) and N6781A (current).

Equipment	Measurement error	
	δ	ϵ
DAU34970	±0.0035 %	±50 µV
N6781A	±0.03 %	±250 µA

III. CHARACTERIZATION OF THE BUCK CONVERTER

The employed procedure to characterize the converter losses takes calculated and simulated results as well as experimental results from electrical and thermal measurements into account, to accurately identify the different loss components of the investigated converter. The procedure comprises of the steps listed below.

1) Numerical estimation of the dc resistances of the power transistors' channels, the metal layers, the converter interconnections, and the PDN using numerical software tools (Cadence post-layout simulation, FastHenry).
2) Electrical measurement of the converter's dc resistances and comparison to the numerical estimations in order to clarify whether all important contributions to the dc losses are considered.
3) Use of the chip-internal configurable resistive load to characterize the temperature rise of the chip with respect to on-chip power dissipation, which enables a separation of the converter's ac and dc losses.
4) Experimental evaluation at different operating points, using an external electronic load (chip-internal load is disabled): electrical measurements of input and output power levels and thermal measurement of the chip temperature. This enables a separation of on-chip and off-chip losses of the IVR.

Steps 1 and 2 are further detailed in Section III-A, step 3 in Section III-B, and step 4 in Section III-C.

Fig. 8 depicts the employed experimental setup with a schematic overview in Fig. 8(a), the realization of the hybrid PCB-based four-phase IVR in Fig. 8(b), and a magnified view of the IVR in Fig. 8(c). The investigated IVR utilizes the PMIC of Fig. 4. High Temperature Silicon Capacitors (HTSC) with low series equivalent inductance (manufactured by IPDiA) realize the dc capacitors, $C_{in1} = 43$ nF, $C_{d1} = 10$ nF, $C_{m1} = 10$ nF, and $C_{out\{1,2,3,4\}} = 10$ nF. Solenoidal inductors with magnetic cores (PFL1005-36NMR, manufactured by Coilcraft) with $L_{\{1,2,3,4\}} = 36$ nH form the output inductors. All measurements are conducted with the high-accuracy equipment listed below.

- *N6781A:* two-quadrant source/measure unit, provides the supply voltages and the load current.
- *DAU34970:* data acquisition unit resistances of the PMIC arising used for all voltage measurements.
- *SC5000:* thermal camera to monitor the temperature distribution on the chip. The camera is equipped with the microscopic zoom lens L0808X5 (1.9 × 1.4 mm).

Table II lists the specified relative and absolute measurement uncertainties, δ and ϵ, that apply for a certain value, X,

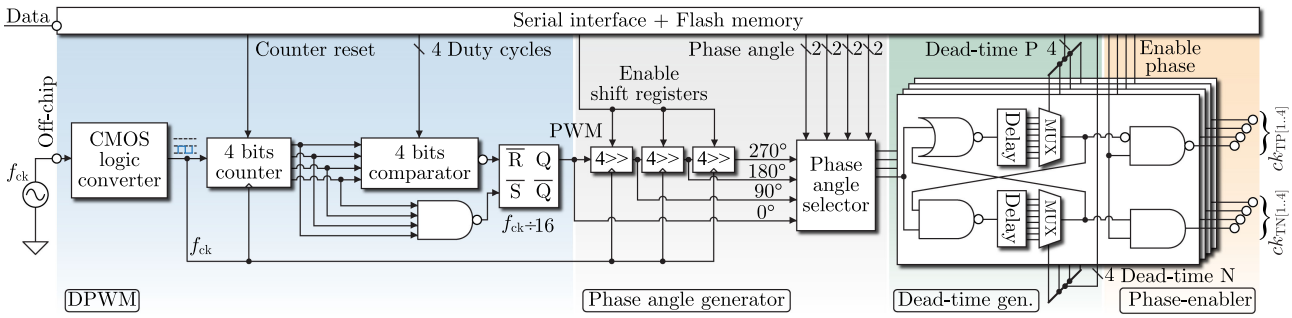

FIG. 7. Simplified schematics of the open-loop circuitry used to generate the gate signals of the converter HBs. This circuit generates the 16 required signals to operate the 4 CMOS ANPC HBs of the PMIC of Fig. 4(a).

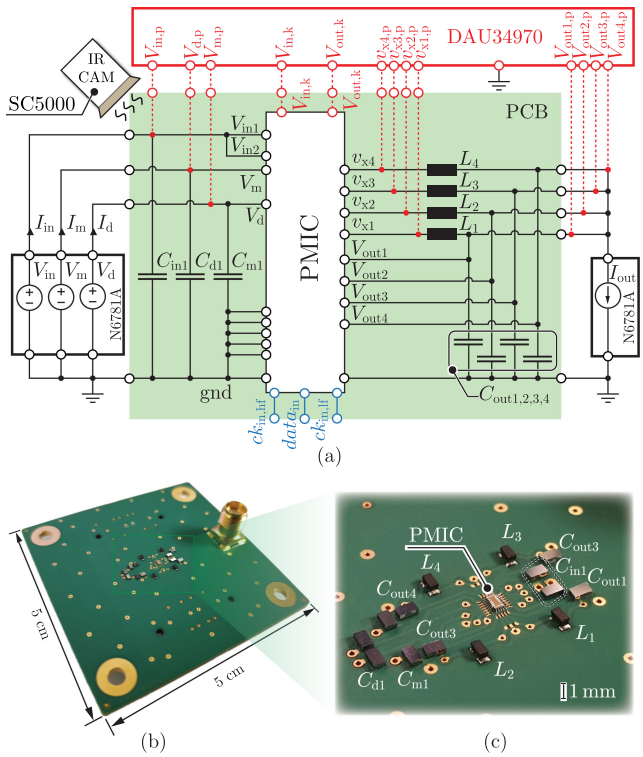

FIG. 8. (a) Measurement setup used to for the loss characterization and the efficiency measurements. Aluminum bond wires are used to connect the PMIC to the PCB substrate; SMA connectors with coaxial cables provide the connections between PCB, measurement devices, and power supplies. (b) Picture of the corresponding assembled PCB-based IVR. (c) Magnified view of the center of the IVR with the PMIC in the middle.

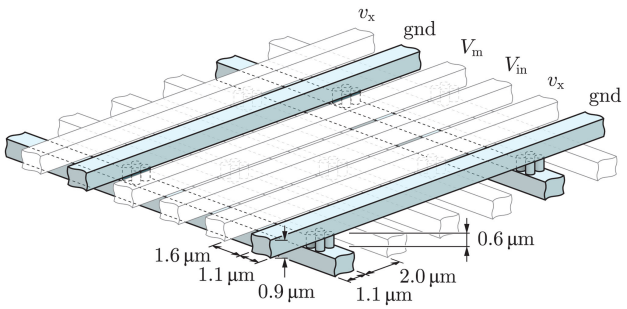

FIG. 9. The Power Distribution Network (PDN) consists of horizontal and vertical conductors; four vias connect the conductors at each crossing. The PDN alternately provides connections for V_{in}, V_m, gnd, and v_x, where v_x denotes the switched voltage of the connected converter phase, e.g., $v_x = v_{x1}$ applies in case of the PDN for converter phase 1. A detailed description of the PDN is provided in [28].

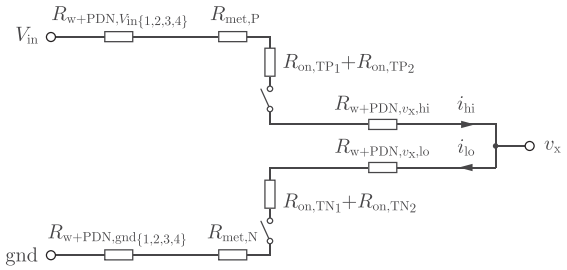

FIG. 10. Internal resistances of the PMIC arising from bond wires and PDN ($R_{w+PDN,V_{in}\{1,2,3,4\}}$, $R_{w+PDN,GND_{\{1,2,3,4\}}}$, $R_{w+PDN,v_x,hi}$, $R_{w+PDN,v_x,lo}$), metal layers stack and vias ($R_{met,P}$, $R_{met,N}$), and MOSFET channels ($R_{on,TP_{\{1,2\}}}$, $R_{on,TN_{\{1,2\}}}$).

for a corresponding measured value, X_{meas},

$$X \in [X_{meas}(1-\delta)-\epsilon,\ X_{meas}(1+\delta)+\epsilon]. \qquad (1)$$

For all experiments, $V_{in,k} = 1.6\,V$ and $V_m = 0.8\,V$ apply.

A. DC RESISTANCES

The dc losses substantially contribute to the total converter losses, which is partly due to the MOSFETs' on-state resistances. However, also the PDN is prone to increased losses in the 14 nm CMOS technology, due to very thin layers of metallization, and needs to be taken into account. Fig. 9 illustrates the layout of the PDN, which realizes an interleaved structure of the required power conductors (e.g., V_{in}, V_m, gnd, and, in case of converter phase 1, v_{x1}). It consists of horizontal conductors on a first layer, vertical the required power conductors on a second layer, and vias at the crossings to connect the two layers to each other [28].

Fig. 10 depicts the network of the internal resistances of the PMIC, which arise from bond wires and

TABLE III Computed Values of the Resistances shown in Fig. 10.

Parameters	Symbol	Value (mΩ)
Values obtained from Cadence simulations		
PMOS channel at $T_j = 85°C$	$R_{on,TP_{\{1,2\}}}$	115/2
PMOS, metal layers stack	$R_{met,P}$	18
NMOS channel at $T_j = 85°C$	$R_{on,TN_{\{1,2\}}}$	103/2
NMOS, metal layers stack	$R_{met,N}$	25
Values obtained from FastHenry computations		
Bond wires + PDN of V_{in} (converter phases 1 to 4)	$R_{w+PDN,V_{in\{1,2,3,4\}}}$	{145, 185, 145, 182}
Bond wires + PDN of v_x, high-side on (same for all phases)	$R_{w+PDN,v_x,hi}$	139
Bond wires + PDN of v_x, low-side on (same for all phases)	$R_{w+PDN,v_x,lo}$	100
Bond wires + PDN of gnd (converter phases 1 to 4)	$R_{w+PDN,gnd_{\{1,2,3,4\}}}$	{159, 197, 155, 155}

PDN (R_{w+PDN}, $V_{in,\{1,2,3,4\}}$, R_{w+PDN}, $v_{x,hi}$, R_{w+PDN}, $v_{x,lo}$, and $R_{w+PDN,gnd_{\{1,2,3,4\}}}$), metal layers stack and vias ($R_{met,P}$ and $R_{met,N}$), and MOSFET channels ($R_{on,TP_{\{1,2\}}}$ and $R_{on,TN_{\{1,2\}}}$), metal layers stack and vias ($R_{met,P}$ and $R_{met,N}$), and MOSFET channels ($R_{on,TP_{\{1,2\}}}$ and $R_{on,TN_{\{1,2\}}}$). FastHenry has been used to compute the resistances of the PDN and Cadence post-layout simulations to determine the resistances of metal layers stack, vias, and MOSFETs; Table III lists the respective results. According to this result, the resistances of the metal layers stacks are comparably small, however, the effective resistances of the PDN are more than twice of the on-state resistances of two series-connected MOSFETs, e.g., in case of the high-side conduction path of phase 1, $R_{w+PDN,V_{in\{1,2,3,4\}}} + R_{w+PDN,v_x,hi} = 284\ m\Omega$ and $R_{on,TP_1} + R_{on,TP_2} = 115\ m\Omega$ apply, even though, the maximum conductor density possible with the given design rules has been utilized. Table III also reveals that $R_{w+PDN,V_{in\{2,4\}}}$ are substantially larger than $R_{w+PDN,V_{in\{1,3\}}}$, which is due to longer conduction paths, since the supply pads, V_{in1} and V_{in2} in Fig. 4, are located close to phases 1 and 3. Similarly, the increased resistance of R_{w+PDN,gnd_2}, as compared to $R_{w+PDN,gnd_{\{1,3,4\}}}$, can be explained based on the arrangement of the ground pads, because, due to layout-specific restrictions, the top-side pad sequence is V_m – *dat* – gnd instead of V_m – gnd – *dat*, which causes a disturbance of the symmetry.

The subsequent measurement of the dc resistances is conducted with the setup shown in Fig. 11, which allows for an experimental characterization of the high-side and low-side conduction paths, depending on whether $TP_{\{1,2\}}$ or $TN_{\{1,2\}}$ conduct. Accordingly,

$$R_{dc,hi,\{1,2,3,4\}} \in \left[\frac{\min\left(V_{in,p} - v_{x\{1,2,3,4\}}\right)}{\max\left(I_{out}\right)}\right] \text{ and} \quad (2)$$

$$R_{dc,lo,\{1,2,3,4\}} \in \left[\frac{\min\left(v_{x\{1,2,3,4\}}\right)}{\max\left(-I_{out}\right)}\right] \quad (3)$$

result for the high-side and low-side conduction paths, respectively. Fig. 12 depicts calculated and measured dc resistances (measured at an output current of 200 mA). Due to chip-internal leakage currents, which cause losses between 10 mW and 11 mW, slightly different dc resistances of the high-side conduction paths result, depending on whether the input or the output currents are used for the calculation. Calculated and measured resistances match well, which confirms the significant contribution of the PDN identified above.

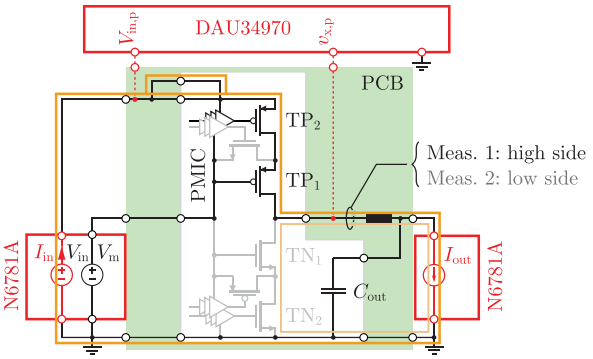

FIG. 11. Setup used to measure the dc resistances of high side and low side of a single converter phase; $v_{x,p}$ is the switching node of the measured phase, e.g., $v_{x1,p}$ in case of phase 1.

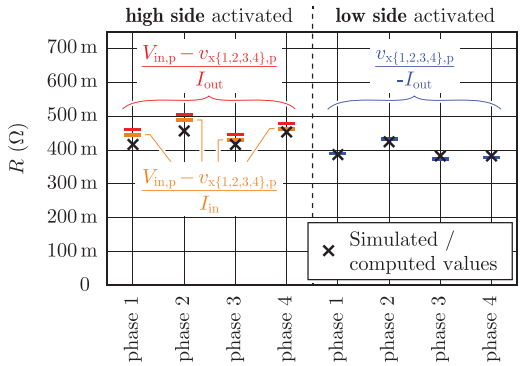

FIG. 12. Calculated and measured dc resistances of the four converter phases (measured at I_{out} = 200 mA and T_{amb} = 20°C); left: high-side resistances according to Fig. 11(a), right: low-side resistances according to Fig. 11(b). The high-side resistances are determined for input and output currents, revealing minor differences due to chip-internal leakage currents.

B. THERMAL CHARACTERIZATION

The relatively large resistance values of the chip-internal load enable an accurate electrical measurement of the losses. Therefore, this load is utilized for the experimental characterization of the dependency of the chip temperature on the losses dissipated in the chip, using the measurement setup depicted in Fig. 13. During the thermal characterization, the transistors of the PMIC are turned off. All four loads have been utilized separately (not simultaneously).

Main measurement uncertainties are related to measurement accuracy and losses in the bond wires, because it is unclear, to what extent the losses in the bond wires contribute to heating up the chip. Accordingly, the respective power is within

$$P_{heat} \in \left[P_{total} - I_{out}^2 R_{bw,eff},\ P_{total}\right], \quad (4)$$

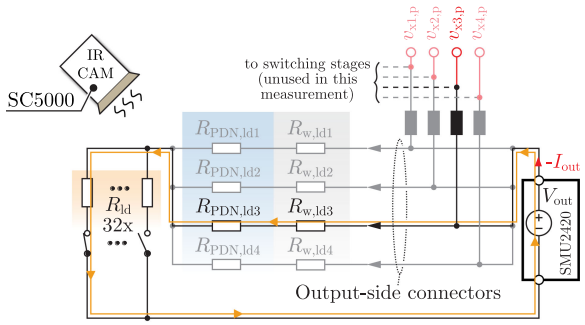

FIG. 13. Simplified equivalent circuit of the measurement setup used to identify the characteristic of power dissipation versus chip temperature for the example of a measurement at the load assigned to converter phase 3. The voltage at the switching node of the corresponding converter phase, i.e., v_{x3} in the depicted example, reveals the voltage that is present just outside the chip (similar to a Kelvin measurement).

since only the current to the load, I_{out}, generates substantial losses in the bond wires; the implications of the losses in the bond wires due to the other currents, e.g., input and supply currents, are negligible. The total power includes the power levels at all ports (input, mid-point, output, supply of chip-internal digital components) and is determined with

$$P_{total} = V_{in,p} I_{in} + V_{m,p} I_m + V_{d,p} I_d + v_{x,p} I_{out}, \tag{5}$$

where $v_{x,p}$ denotes the voltage at the output node of the converter phase that corresponds to the tested internal load (e.g., $v_{x1,p}$ if load 1 is currently under test), since this node yields the most accurate measurement of the load voltage close to the PMIC (similar to a Kelvin pad). Aluminum wires with a length of 500 μm and a diameter of 20 μm realize the bond wires leading to a resistance of 42 mΩ. The input to every internal load is connected to the PCB via a single bond wire. The ground connection uses seven bond wires in parallel, however, due to the large resistance of the PDN, only a single bond wire may carry most of the return current through ground. Accordingly, based on a worst case assumption, the effective bond wire resistance may be up to

$$R_{bw,eff} = 2 \times 42\,\text{m}\Omega = 84\,\text{m}\Omega. \tag{6}$$

Still, the uncertainty remains small, e.g., $\pm$2.6 mW at a dissipated power of 170 mW and a load current of 250 mA.

With regard to the thermal measurements, the chip has been painted with high-emissivity black paint to achieve accurate results. In steady-state, the distributions of the surface temperatures are found to be similar for all considered excitations. Fig. 14 presents a thermal image of the chip that results if the load dissipates a power of 180 mW. The observed local areas of increased or reduced temperatures are linked to the layouts of top layer and PDN, e.g., reduced temperatures result at the pads. Further temperature gradients are found close to the edges of the chip, which, however, are far from the investigated chip-internal converter parts. The obtained result is different to what is found for chips used in high-power modules, where large temperature gradients may occur on the

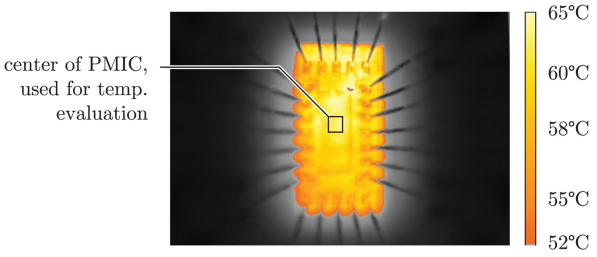

FIG. 14. Example of a thermal measurement of the load at a dissipated power of 178 mW. The temperature used for chip characterization is the mean value of the temperatures of 3 × 3 pixels in the center of the PMIC.

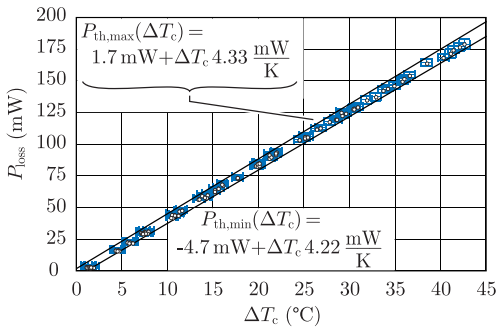

FIG. 15. Identified power dissipation characteristic with respect to chip temperature.

surface, e.g. in IGBTs as presented in [29], and is due to the comparably small chip volume and the placement of the chip on the PCB, providing thermal insulation. Due to these reasons and because the control circuitry, which generates only negligible losses, resides at the center of the chip, it is assumed that the losses in the on-chip load resistors and the converter phases have similar implications on the chip temperature at the center. Thus, the average temperature of 3 × 3 pixels in the middle of the chip is used as chip surface temperature, T_c, cf. Fig. 14. In the considered temperature range, the employed thermal camera, SC5000 (Flir), has an absolute accuracy of ± 1°C. However, the presented setup uses the same camera and the same setup to identify the dependency of the chip temperature on the losses in a first step and to estimate the on-chip losses based on the chip temperature in a second setup that is conducted shortly after. Therefore, systematic errors are removed and only noise remains as a source of uncertainty for which an uncertainty equal to the standard deviation of ± 0.3°C, typically found in the measurements, has been considered.

Fig. 15 depicts the experimental results for the power dissipation with respect to the difference between chip surface temperature and ambient temperature,

$$\Delta T_c = T_c - T_{amb}, \tag{7}$$

where the ambient temperature has been measured at the center of the chip prior to the load measurements and with no supply voltages being provided to the PMIC. The shown

results have been obtained for different voltages at the load, ranging from 0.5 V to 0.85 V, and for each of the four load phases; the result reveals same temperature characteristics for all phases. With the known uncertainties of thermal and electrical measurements, the characteristics of upper and lower boundaries of the on-chip losses, which are found to be almost linear with respect to temperature, can be estimated using the bottom-right and the top-left corners of the uncertainty ranges of each measurement result. In this regard, a subsequent least mean square optimization yields

$$P_{\mathrm{th,min}} = 4.22\frac{\mathrm{mW}}{\mathrm{K}}\Delta T_{\mathrm{c}} - 4.7\,\mathrm{mW}, \tag{8}$$

$$P_{\mathrm{th,max}} = 4.33\frac{\mathrm{mW}}{\mathrm{K}}\Delta T_{\mathrm{c}} + 1.7\,\mathrm{mW}. \tag{9}$$

C. EFFICIENCY MEASUREMENTS AND LOSS BREAKDOWN

With all four phases being operated, the IVR yields the losses and efficiencies presented in Fig. 16 for a voltage conversion ratio of

$$M = \frac{V_{\mathrm{out,k}}}{V_{\mathrm{in,k}}} = \frac{V_{\mathrm{out,k}}}{1.6\,\mathrm{V}} \approx 0.7 \tag{10}$$

and for three switching frequencies (50 MHz, 100 MHz, and 150 MHz). The total efficiency and the total losses,

$$\eta_{\mathrm{IVR}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}}, \qquad P_{\mathrm{loss,el}} = P_{\mathrm{in}} - P_{\mathrm{out}}, \tag{11}$$

are directly determined from the input and output power levels of the IVR measured with the setup of Fig. 8,

$$P_{\mathrm{in}} = V_{\mathrm{in,p}} I_{\mathrm{in}}, \qquad P_{\mathrm{out}} = V_{\mathrm{out,k}} I_{\mathrm{out}}. \tag{12}$$

At the gaps observed in Fig. 16, e.g., at $P_{\mathrm{out}} \approx 350\,\mathrm{mW}$ in Fig. 16(a), the duty cycle is changed from 75 % (= 12/16) to 81 % (= 13/16) such that M remains close to 0.7.

The PMIC itself generates only a part of the total losses, which is determined from the chip temperature using (8), (9), cf. Fig. 15. Similar to Section III-B, the uncertainty of the temperature measurement is set equal to the standard deviation found for the thermal measurements, which is $\pm 0.3^{\circ}\mathrm{C}$,

$$P_{\mathrm{loss,th}} \in \left[P_{\mathrm{th,min}}(T_{\mathrm{c}} - 0.3^{\circ}\mathrm{C}), P_{\mathrm{th,max}}(T_{\mathrm{c}} + 0.3^{\circ}\mathrm{C})\right]. \tag{13}$$

The depicted efficiency of the PMIC itself is calculated with

$$\eta_{\mathrm{PMIC}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{loss,th}}}. \tag{14}$$

The on-chip losses, $P_{\mathrm{loss,th}}$, can be further separated into a resistive loss component, $P_{\mathrm{loss},R}$, and an additional loss component, $P_{\mathrm{loss,add}}$, using the resistor network of Fig. 10 and the previously identified resistance values, cf. Section III-A,

$$P_{\mathrm{loss,th}} = P_{\mathrm{loss},R} + P_{\mathrm{loss,add}}, \tag{15}$$

where $P_{\mathrm{loss},R}$ is calculated with the dc resistances, (2) and (3), and the currents through the high-side and low-side paths for all enabled converter phases, N (e.g., $N = 4$ applies in Fig. 16 and Fig. 17),

$$P_{\mathrm{loss},R} = \sum_{n=1}^{N} \left(R_{\mathrm{dc,hi},n} I_{\mathrm{hi,rms}}^2 + R_{\mathrm{dc,lo},n} I_{\mathrm{lo,rms}}^2\right); \tag{16}$$

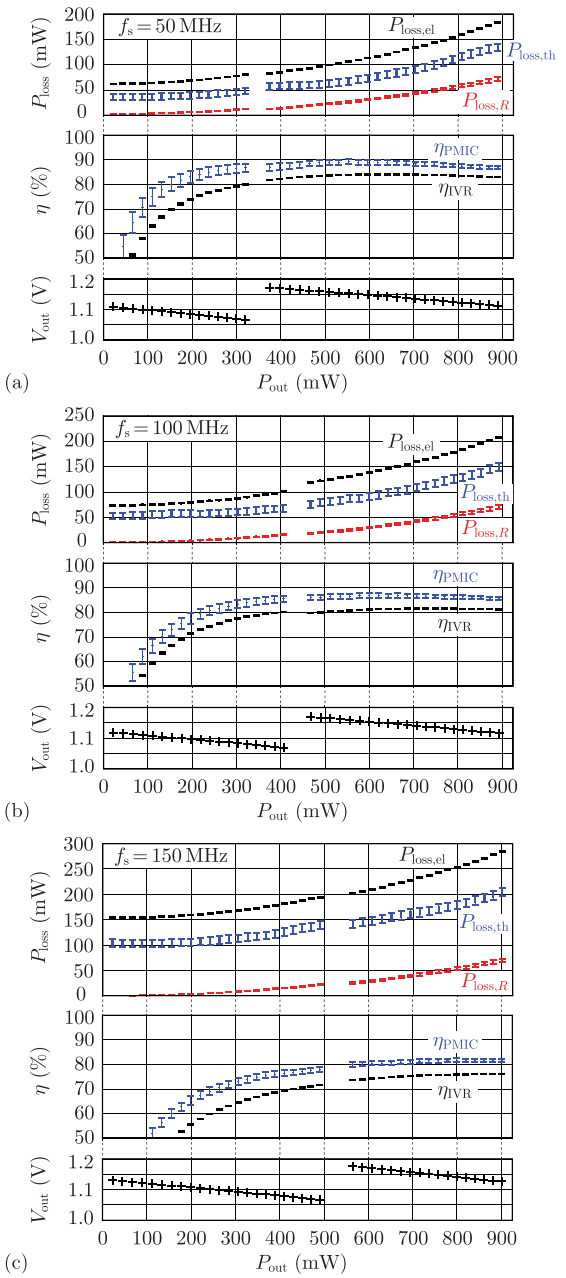

FIG. 16. Losses and efficiencies for $M = 0.7$ and two different switching frequencies: (a) $f_s = 50$ MHz, (b) $f_s = 100$ MHz, and (c) $f_s = 150$ MHz; $P_{\mathrm{loss,el}}$ and $P_{\mathrm{loss,th}}$ denote the losses determined with electrical and thermal measurements, $P_{\mathrm{loss},R}$ refers to the resistive on-chip losses determined for the measured resistances of the PMIC's high-side and low-side current paths. The shown gap results due to a step of the duty cycle, which is needed to maintain V_{out} close to $0.7 \times 1.6\,\mathrm{V} = 1.12\,\mathrm{V}$.

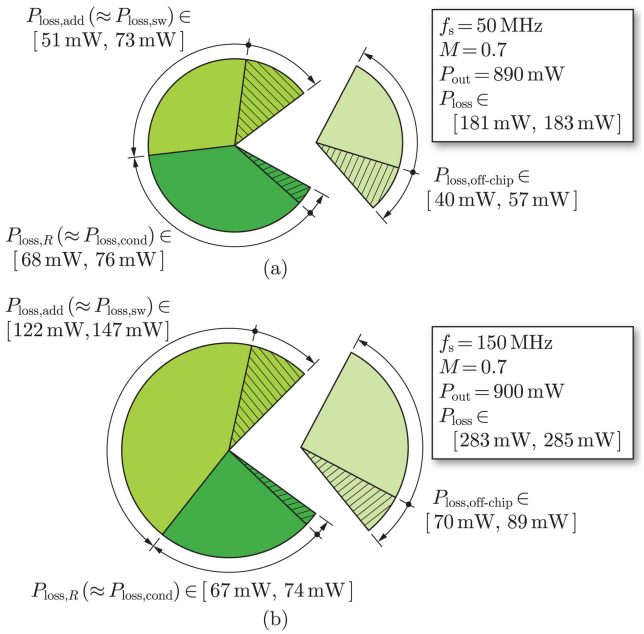

FIG. 17. Breakdown of the losses of the IVR for two different switching frequencies based on the data shown in Fig. 16, for an output power of 0.9 W, and two different switching frequencies: (a) $f_s = 50$ MHz, (b) $f_s = 150$ MHz; $P_{\text{loss,ac}} = P_{\text{loss,th}} - P_{\text{loss,dc}}$ and $P_{\text{loss,off-chip}} = P_{\text{loss,el}} - P_{\text{loss,th}}$ apply. The result reveals that an increase of the switching frequency leads to increased ac losses on the chip (switching losses, ac conduction losses) and increased off-chip losses (e.g., in the inductor).

$I_{\text{hi,rms}}$ and $I_{\text{lo,rms}}$ are determined based on inductor rms current, $I_{L,\text{rms}}$, and duty cycle, D,

$$I_{\text{hi,rms}} = I_{L,\text{rms}}\sqrt{D}, \quad I_{\text{lo,rms}} = I_{L,\text{rms}}\sqrt{1-D}, \tag{17}$$

using

$$I_{L,\text{rms}}^2 = \left(\frac{I_{\text{out}}}{N}\right)^2 + \left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2 \Delta I_L = \frac{V_{\text{out,k}}(1-D)}{f_s L}. \tag{18}$$

The additional loss component, $P_{\text{loss,add}}$, is the sum of switching losses, losses due to leakage currents, increased losses due to eddy current effects inside the chip (Skin and Proximity effects), and power dissipation in the digital control circuitry. The calculation of the ac resistances of the PDN with FastHenry gives a negligible increase at the considered switching frequencies, due to the small physical dimensions, the losses due to leakage identified in Section III-A are in the range of 10 mW, and the power demand of the control circuitry is approximately 1 mW. For these reasons, it can be assumed that the resistive losses and the additional losses mainly resemble the conduction losses and the switching losses, respectively,

$$P_{\text{loss,cond}} \approx P_{\text{loss},R}, \qquad P_{\text{loss,sw}} \approx P_{\text{loss,add}}, \tag{19}$$

The results reveal that the losses in the PMIC typically contribute to more than two thirds of the total losses of the IVR and that the additional loss component increases if the switching frequency is increased, which confirms (19). In addition, also the off-chip losses,

$$P_{\text{loss,off-chip}} = P_{\text{loss,el}} - P_{\text{loss,th}}, \tag{20}$$

which contain the losses of inductor and PCB,[3] increase for increasing switching frequencies. At $f_s = 50$ MHz, the IVR achieves a maximum efficiency of 84.1 % at $P_{\text{out}} = 640$ mW. With respect to the active chip area of the power stages of all four phases (0.0324 mm^2), this efficiency is achieved at a chip current density of 17.3 A/mm^2. At full load, $P_{\text{out}} = 890$ mW (corresponding to a chip current density of 24.7 A/mm^2), the efficiency is 83.0 %. The maximum efficiency of the PMIC is in the range $\eta_{\text{PMIC,max}} \in [88\,\%,\ 90\,\%]$ at $f_s = 50$ MHz and output power levels between 500 mW and 600 mW; the corresponding full-load efficiency of the PMIC is between 86.3 % and 87.6 %. Please note that an increased range of uncertainty results for $\eta_{\text{PMIC,max}}$, compared to the electrically measured efficiency, due to the increased uncertainty of the thermal measurement.

Fig. 17 depicts the ranges of conduction losses, switching losses, and off-chip losses for full-load operation with $P_{\text{out}} = 0.9$ W, $M \approx 0.7$, and two different switching frequencies, i.e., $f_s = 50$ MHz in Fig. 17(a) and 150 MHz in Fig. 17(b), in order to provide a more detailed view on the three loss components. The shaded areas denote the uncertainty ranges that result for the available measurement data at the considered operating points, cf. Fig. 16. For $f_s = 50$ MHz, the range of the resistive losses, $P_{\text{loss},R} \in [68\text{ mW},\ 76\text{ mW}]$, is similar to the range of the additional losses, $P_{\text{loss,add}} \in [51\text{ mW},\ 73\text{ mW}]$. In contrast, for $f_s = 150$ MHz, the additional losses, $P_{\text{loss,add}} \in [122\text{ mW},\ 147\text{ mW}]$, are approximately twice the resistive losses ($P_{\text{loss},R} \in 67\text{ mW},\ 74\text{ mW}$]).

In order to clarify the origin of the additional losses, a detailed simulation has been realized for converter phase 1. This simulation includes the parasitic components of metal layers 1 to 10 and models the parasitics of PDN and PCB with the simplified network depicted in Fig. 18, cf. [28].

The values of the presented parasitic inductances and resistances of PDN and PCB have been computed with FastHenry. Fig. 19 depicts the waveforms of the chip-internal input voltage of the half bridge of converter phase 1, V_{dd}, and the voltage at the corresponding chip-internal switching node, v_{x1}, determined with the detailed simulations and for three different switching frequencies of 50 MHz, 100 MHz, and 150 MHz. According to the obtained results, the additional parasitic components lead to several unwanted effects, e.g., increased turn-on and turn-off times and oscillations superimposed on supply voltages, output voltages, and output currents. Compared to the results of simplified Cadence simulations that do not take the output current ripple and the parasitic components introduced by metal layers, PDN, bond wires, and PCB into account [27], these parasitic components are indeed

[3] A separation of the off-chip losses into the losses of inductor and PCB would require a detailed characterization of the high-frequency inductor losses in presence of DC bias; however, this information is currently not available.

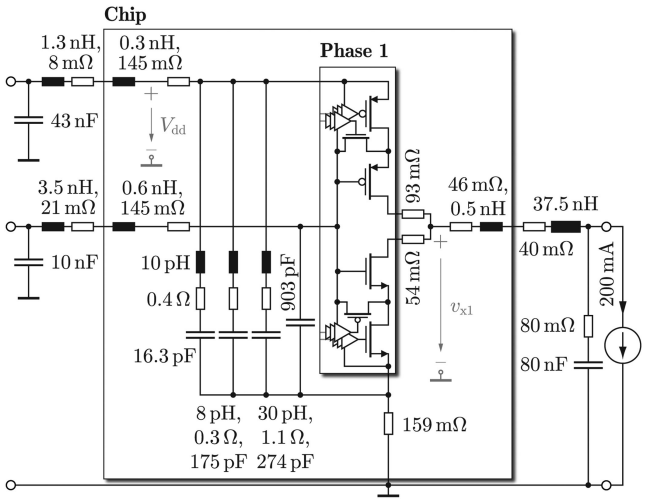

FIG. 18. **Network used to model the parasitic components of PCB, bond wires, and PDN for the detailed simulation of converter phase 1. The framed block 'Phase 1' refers to a detailed simulation model that takes further parasitic components introduced by metal layers 1 to 10 into account.**

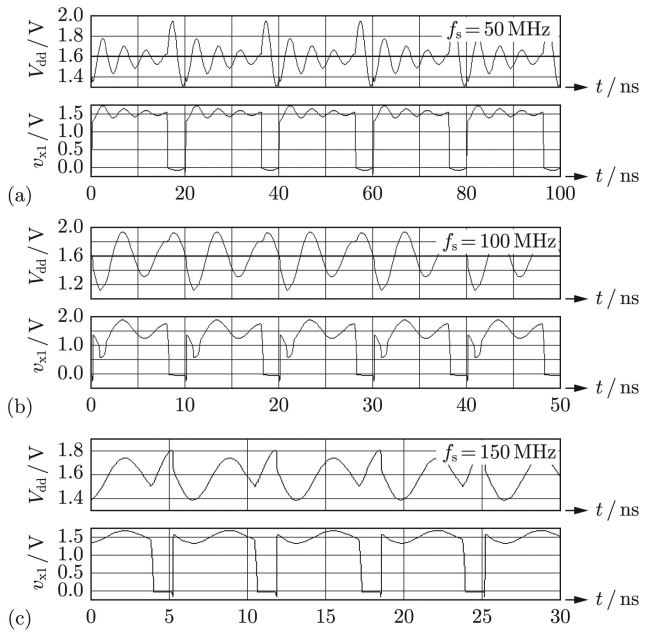

FIG. 19. **Waveforms of the supply voltage and the voltage at the switching node of converter phase 1, V_{dd} and v_{x1}, cf. Fig. 18, obtained from a detailed Cadence simulation and for different switching frequencies: (a) $f_s = 50$ MHz, (b) $f_s = 100$ MHz, (c) $f_s = 150$ MHz.**

the main reason for the increased losses, in particular at high output currents, cf. Fig. 20. Remaining differences between simulated and measured losses are of relatively low value and may be reproduced by even more detailed simulations, e.g., the measured losses at $f_s = 50$ MHz are found to be larger than expected, which may originate from additional resonance effects in PCB and PDN.

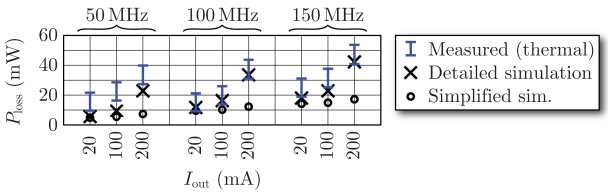

FIG. 20. **Comparison of the losses of converter phase 1, determined with simplified and detailed simulations, to the measured on-chip losses. In contrast to the detailed simulation, cf. Fig. 18, the simplified simulation does not take parasitic components into account (e.g., due to metal layers, PDN, etc.) [27]. The depicted outcome reveals a substantial contribution of these parasitic components on the obtained losses; especially at high output currents, e.g., $I_{out} = 200$ mA, these are mainly responsible for the differences between the results determined with simplified simulations and measurements.**

IV. CONCLUSION

This paper presents a detailed characterization of an inductor-based four-phase buck converter featuring CMOS APNC HBs, which is supported by the results of profound simulations and extensive experiments. The investigated converter uses a PMIC assembled in a 14 nm CMOS technology node and allows for operation with switching frequencies between 50 MHz and 150 MHz. Its implemented open-loop circuitry allows for configurable dead times, to optimize switching losses, and realizes output stages that are capable of being deactivated, in order to facilitate phase-shedding, i.e., operation of a reduced number of converter phases, to increase the achieved efficiency at lower output power levels. With a FEOL chip area of only 0.0081 mm^2 for each phase of the four-phase converter, a very compact design has been achieved, consuming only a small amount of valuable chip area.

The process of realizing an optimized chip-integrated IVR is highly challenging, mainly due to the aspects listed below.

1) Limited possibility to fabricate several different chips to conduct a redesign as it is commonly done in power electronics, since chip design is bound to high costs and high time requirements.
2) Since it is not possible to measure voltages and currents inside the chip, the chip designer needs to fully trust the simulation results, e.g., also in case of switching losses. For the purpose of verification, specific test chips could be planned and realized to investigate a particular effect, which, however, is in contradiction to aspect 1). In this regard, Fig. 21 shows the layout of a more advanced version of the presented PMIC including a high-speed Analog-to-Digital Converter (ADC) to electrically measure the voltage at the v_{x3} node on the chip. In the course of a comparison against simulated waveforms, this will allow for further insights with respect to similarities and differences between the simulated and the real processes, e.g., to clarify if the network assumed for the PDN needs to be further refined.
3) The design tools for most recent CMOS technologies are of limited extent, i.e., only a certain part of the chip can be simulated; accordingly, important interactions

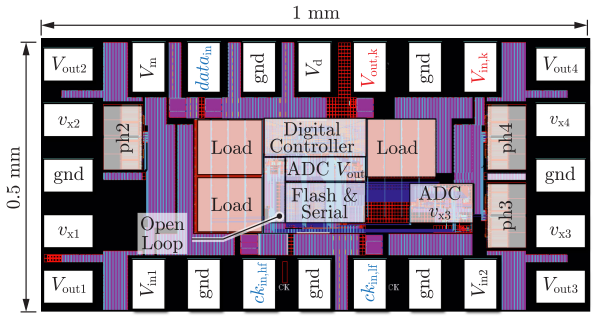

FIG. 21. Layout image of a more advanced generation of the designed PMIC including ADCs for digital output voltage control and v_{x3} voltage measurement. The high impedance voltage measurement at the v_{x3} node will allow for experimental verification of its switching waveform and output power.

between different parts of a complete IVR are not identified.

In order to still gain detailed insights into the investigated IVR, the presented converter characterization consolidates the results of electrical measurements, thermal inspections of the chip surface, and simulations, which enables the separation of the total losses into on-chip and off-chip loss components as well as the allocation of important loss components inside the chip. In summary, the IVR achieves a maximum efficiency of 84.1% at $P_{out} = 640\,\text{mW}$ and $f_s = 50\,\text{MHz}$ and a maximum full-load efficiency of 83.0% at $P_{out} = 890\,\text{mW}$ with a corresponding chip current density of $24.7\,\text{A/mm}^2$. The maximum efficiency of the PMIC itself is between 88% and 90% for $P_{out} \in [500\,\text{mW},\ 600\,\text{mW}]$. The obtained results reveal that PDN and metal layers cause a considerable increase of the total losses, e.g., a simulation of the PMIC without PDN and metal layers reveals losses of only 30 mW at $f_s = 100\,\text{MHz}$ and $P_{out} = 0.9\,\text{W}$; however, the corresponding measured losses of the PMIC are in the range between 140 mW and 156 mW, which can be reproduced with detailed simulations. Furthermore, the measured experimental results confirm that the combination of appropriate software tools, e.g., Cadence to conduct detailed post-layout circuit simulations and FastHenry to identify the impedances of PDN and PCB, enables a prediction of the expected losses with reasonable accuracy.

Table IV lists the performance and design values of the realized ANPC IVR and provides a comparison to previously presented results. The achieved maximum current density of the realized PMIC is amongst the highest documented values, however, the peak efficiency of 84.1% is below the maximum documented efficiency of 91.5%. According to Table IV, the efficiency of the IVR can be increased with advanced packaging technologies, e.g., flip-chip bonding the PMIC on an interposer that provides the inductors and the capacitors. In addition, this Table indicates a trend that more mature CMOS technology nodes, e.g., 22 nm, 40 nm, enable the realization of more efficient IVRs. This trend matches to the results of prior realizations with more mature CMOS nodes, where the losses

TABLE IV Performance and Design Values of the Investigated ANPC HB IVR in Comparison to Previously Presented Converters.

	This work	C. Schaef et al. [11]	H. K. Krishnamurty et al. [8]	H. K. Krishnamurty et al. [9]	E. A. Burton et al. [10]	F. Neveu et al. [13]	N. Sturcken et al. [15]
Techn. node PMIC (nm)	**14**	14	14	14	22	40	45
Peak efficiency (%)	**84.1**	88	84 (for on-die induct.)	80	90	91.5	75
Max. curr. density (A/mm^2)*	**24.7**	10.7	–	–	31	6.3	22.7
Input voltage (V)	**1.6**	1.6	1.5	1.2	1.7	3.3	1.8
Conv. ratio M at peak efficiency	**0.7**	0.75	0.77	0.77	0.62	0.73	0.67
HB topology	**ANPC**	stacked transist.	stacked transist.	stacked transist.	stacked transist.	stacked transist.	single transist.
Switching freq. (MHz)	**50**	70	100	90	140	100	up to 200
Inductor value L (nH)	**36**	2.5	1.5 or 22**	4.8	–	60	12.5
Inductor technology	**discrete**	on-package	on-die or ext.	on-die	on-package	discrete	silicon interp.
Inductor packaging	**bond-wire**	flip-chip	– / on-probe	–	flip-chip	flip-chip	flip-chip
Number of phases	**4**	1	2	2	16	1	8

* Defined as the maximum output current of the IVR divided by the area of the enabled power switches, gate-drivers, and level shifters. This value was calculated using information found in the corresponding publications.
** Two realizations are presented, with on-die and external inductor.

in PDN and metal layers have been relatively low, and the findings of this paper, which reveal substantial losses, there, due to the small values of maximum widths and thicknesses defined by the design rules. Therefore, even higher losses in the PDN and the metal layers would be expected in case of higher-integrated, e.g., 7 nm, CMOS nodes [30]. Accordingly, future research will also focus on alternative solutions that do not require a direct integration of the PMIC on the CPU die, e.g., 3D realizations using chiplets [31], which extends the current design space with respect to system complexity, efficiency, and costs.

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