Power Electronic Systems
Laboratory



Proceedings of the 28th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD 2016), Prague, Czech Republic, June 12-16, 2016

## The Ideal Switch is Not Enough

J. W. Kolar,
D. Bortis,
D. Neumayr



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

# The Ideal Switch is Not Enough

J. W. Kolar, D. Bortis, and D. Neumayr
Power Electronic Systems Laboratory, ETH Zurich, Switzerland.
Email: kolar@lem.ee.ethz.ch

***Abstract*—There is an ongoing demand for increased power density and efficiency along with lower costs of converter systems and shorter development time for specific applications in the field of power electronics. In order to expedite the technology development Google and IEEE initiated the Google Little Box Challenge (GLBC) including $1 million prize money. Aim of the GLBC was to build the worldwide smallest $2\,\mathrm{kVA}/400...450\,\mathrm{V_{DC}}/230\,\mathrm{V_{AC}}$ single-phase converter with $\eta > 95\,\%$ efficiency and an air-cooled case temperature of less than $60\,^{\circ}\mathrm{C}$ by using latest semiconductor technology and innovative topological concepts. Out of 2000+ applications 18 finalists have been selected, whose converter systems exhibited power densities mostly in the range of $120...220\,\mathrm{W/in^3}$. With this, a clear performance increase compared to the state of the art ($\rho < 50\,\mathrm{W/in^3}$) was achieved, but in the end it represented only a limited performance improvement. In this work, a high power density DC/AC converter system, developed by a team of the ETH Zurich, the Fraunhofer Institute for Reliability and Microintegration (IZM) and the Fraza company and presented at the GLBC finale in Golden, Colorado, will be described and further optimized. Given the converter system, it will be clarified which components and technologies are finally limiting an increase in performance. In a first step, the optimum solution will be identified by means of a $\eta\rho$-Pareto front obtained from a multi-objective optimization. The analysis will be based on detailed loss and volume models of the utilized GaN GIT power switches, inductors and capacitors as well as on component stresses, resulting for advanced modulation and control techniques. Thereafter, the models of the power semiconductors will be gradually idealized by means of reducing the switching and conduction losses. The resulting shift of the Pareto front reveals the sensitivity of the system performance with respect to the semiconductor technology and ultimately leads to an 'absolute' performance limit imposed by the passive components and the cooling system. It is shown that for fully idealized semiconductors a maximum possible performance increase of $50\,\%$ regarding power density or losses is feasible, whereby the switching frequencies are limited to $\approx 1\,\mathrm{MHz}$ due to the losses in the magnetic components. Thus, for the realization of highly compact systems, high frequency core materials and winding concepts of the magnetic components, new heat management concepts and 3D-packaging will gain further importance in future along with the ongoing improvement of semiconductor technologies.**

## I. Introduction

During the last decades, the advances in power semiconductors and microelectronics have been – besides innovative topology, modulation and control concepts – the driving force for the development of new power electronic converters towards higher compactness/power density, efficiency and cost reduction [1]. In particular, wide bandgap power semiconductors are expected to bring a significant improvement of the performance of converter systems. Following this idea, Google and IEEE launched the Google Little Box Challenge (GLBC) in 2015 aiming for a massive enhancement of the power density (factor of 10) of a $2\,\mathrm{kVA}$ single-phase DC/AC converter system compared to state-of-the-art technology advertizing $1 million prize money. As minimum requirements a power density of $\rho > 50\,\mathrm{W/in^3}$, an efficiency of $\eta > 95\,\%$, a system case temperature of $T_c < 60\,^{\circ}\mathrm{C}$ and a minimal lifetime of $t_{\mathrm{L}} > 100\,\mathrm{h}$ were set. Additionally, the system should comply with the EMC standards according to CISPR11 Class B and should only show a voltage ripple less than $3\,\%$ of the nominal voltage across the DC bus. Meeting the ripple voltage specification demands to include an energy storage in the converter in order to buffer the fluctuating power at the AC side intrinsic to single-phase power conversion systems.

The challenging specifications and the attractive prize money created a remarkable interest in the power electronics community, which led to the application of 2000+ teams – companies, research institutes and universities – for the GLBC. Finally, 100+ teams submitted technical descriptions of realized systems. Out of these applications, 18 finalists were selected, whereby the achieved power densities were mainly in the range of $120$ ... $220\,\mathrm{W/in^3}$. With this, a distinctly higher performance compared to the minimum specification of $50\,\mathrm{W/in^3}$ according to the state of the art was achieved. However, despite the use of latest GaN or SiC semiconductor technologies, soft-switching topologies and appropriate modulation techniques, clear performance limits became visible. This raises the question, which components are responsible for these performance limits and which contribution can be made by an advancement of the power semiconductors for a further performance increase.

In this work, this aspect shall be analyzed for the system which has been realized by a team of the ETH Zurich, the Fraunhofer (FH) Institute for Reliability and Microintegration (IZM) and the Fraza company and which has been presented at the finals. It was the target of ETH, FH-IZM and Fraza to employ several new technologies, but also to realize an industry-type solution without sophisticated 3D-packaging, which could be implemented as a product directly in a next step. The chosen approach is based on a full-bridge DC/AC converter structure (cf. Fig. 1) which is operated with triangular output currents (TCM operation, [2], [3]) and therefore ensures soft-switching of the GaN GITs employed as power switches at switching frequencies in the range of $200\,\mathrm{kHz}$ to $1\,\mathrm{MHz}$ (depending on output voltage and power) without additional circuitry. New gate drivers [4] with high $\frac{\mathrm{d}v}{\mathrm{d}t}$-immunity ($500\,\mathrm{kV/\mu s}$)and extremely low delay time ($< 20\,\mathrm{ns}$ delay from FPGA output to gate) have been developed for the power transistors. Moreover, innovative foil winding inductors with multiple air-gaps (Fraza, [6], [7]) and low high frequency losses have been employed as well as an ultra-compact heat sink with a Cooling System Performance Index (CSPI, [8]) of $25\,\mathrm{W/(dm^3\,K)}$. A fully digital DSP/FPGA-based control facilitated to operate two parallel bridge legs per AC output phase in interleaved mode which ensured a relatively smooth output current and allowed to achieve a small EMI filter size. The double-line frequency power fluctuation occurring at the AC side, intrinsic to single-phase converter systems, was buffered by means of an active Power Pulsation Buffer (PPB, [5]) equipped with high energy density ceramic capacitors (CeraLink), leading to a higher power density compared to a conventional passive buffering with electrolytic capacitors. A prototype of the system is depicted in Fig. 2 and characteristic voltage and current waveforms are shown in Fig. 3.

The component values and the switching frequency of the system have been selected based on engineering experience and findings from former research projects, clearly leaving some room for future improvements. Therefore, in the following in a first step, the actually optimum solution will be identified in the form of a $\eta\rho$-Pareto front obtained by means of a multi-objective optimization presented in Section II. The performed optimization will be based on detailed loss and volume models of the utilized GaN GIT power devices, inductors and capacitors. It will become apparent that an alternative

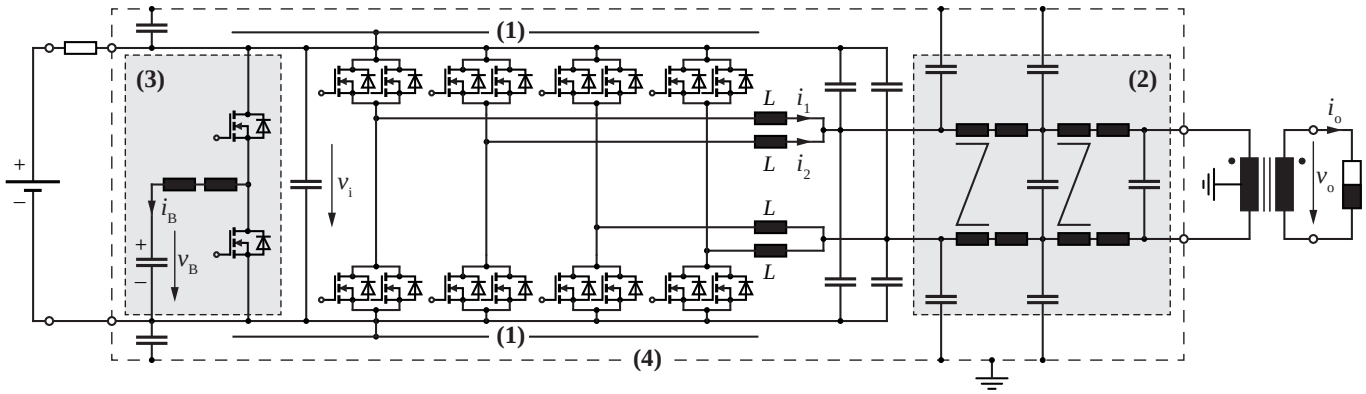



Fig. 1. Topology of the DC/AC converter system designed for the Google Little Box Challenge (GLBC). Each output phase is comprised of two interleaved bridge-legs, each switch is comprised of two parallel connected GaN GIT [4]. The two-stage EMI filter at the AC output ensures to meet CISPR 11, Class B EMI standards. In order to buffer the double-line frequency power pulsation, a buck-type Power Pulsation Buffer (PPB, [5]) equipped with high energy density ceramic capacitors (CeraLink) is installed at the DC input of the converter.

capacitor technology - which at the time of the realization has not been available with the required high component values - would have allowed to reduce the losses of the PPB and increase the power density of the converter due to the resulting lower cooling effort. The introductory question, in which way future semiconductor technology improvements might enable a further performance increase, is then answered in Section III based on the optimally designed system. Hereby, the models of the power semiconductors are stepwise idealized by reduction of the switching and conduction losses and the resulting shift of the $\eta\rho$-Pareto front is calculated. This clearly shows the sensitivity of the system performance with respect to the semiconductor technology and ultimately leads for completely ideal power semiconductors (without switching, conduction and gate driver losses) to an 'absolute' performance limit, which is imposed by the passive components and the cooling system. In order to clarify the influence of the TCM operation mode on the obtained optimization result, in a next step the operation of the converter with conventional pulse width modulation (PWM) is analyzed in an analogous manner, whereby similar conclusions result. Subsequently it is shown in Section IV, how a variety of design parameter combinations eventually leads to similar $\eta\rho$-performance. Hence, there exists a large variety of solutions and/or design space diversity that can only be narrowed down by considering another performance criterion, e.g. costs [11]. Section V summarizes the main conclusions and gives an outlook on the technologies that have to be developed for a further performance increase in the future.

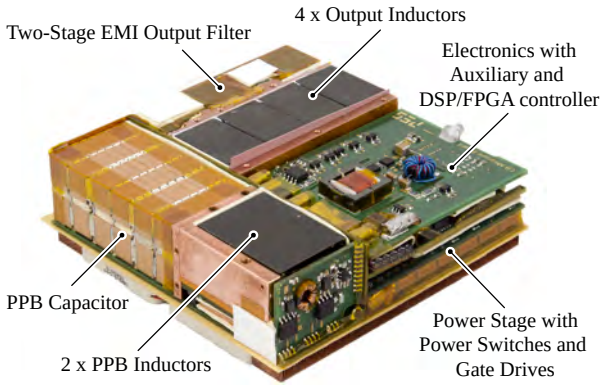



Fig. 2. Realized prototype presented by a team of ETH Zurich, FH-IZM, and Fraza company, at the finals of the Google Little Box Challenge [9].

## II. $\eta\rho$-Performance Evaluation and Optimization

Since the system parameters and component values of the constructed converter system depicted in Fig. 2 were chosen based on engineering experience and findings from former research projects, a comprehensive design optimization will potentially lead to a significant improvement in performance. Since a minimum converter efficiency of $95\,\%$ must be ensured, a multi-objective, i.e. $\eta\rho$-performance optimization, has to be carried out also considering system efficiency $\eta$ besides power density $\rho$. Based on the imposed system specifications and selected design parameter values, the component stresses and the required attenuation to comply with conducted EMI standards are calculated. Having comprehensive volume and loss models of the main converter components at hand, and considering the thermal coupling between these components, the total converter volume and total power density are calculated [11]. These calculations are performed in large number, each iteration with modified design variables, in order to find the best possible trade-off between efficiency and power density. After exploring the entire design space, those designs with best efficiency / power density combination define the $\eta\rho$-Pareto front in the $\eta\rho$-performance space. A comprehensive description of the employed models and optimization routine is given in [12] and is omitted herein for the sake of brevity. The results of the employed optimization routine are shown in Fig. 4, wherein the performance of the DC/AC converter specifically designed for the GLBC (cf. Fig. 2) is denoted with (a). The results of the optimization indicate the possibility of a significant improvement of the actually built system ((b) in Fig. 4), which could be achieved by using only a single bridge-leg per output phase as a detailed analysis reveals. Employing low-loss class II X6S capacitors for the buffer capacitor in the PPB ( [5], for (a) and (b) in Fig. 4 CeraLink capacitors are used), a further significant performance improvement can be achieved (cf. (c) in Fig. 4). According to the latest available technology and the chosen system-, operation-, and packaging-concept (cf. Fig. 1 & Fig. 2), this best performing solution (c) is chosen as a basis for predicting potential future performance improvements due to advances in power semiconductor technology.

## III. Multi-Objective Optimization for Idealized Power Semiconductors

Based on the optimal design determined in Section II which employs only best state-of-the-art components ((c) in Fig. 4), it should now be analyzed which performance improvements could be expected from future advances in the semiconductor technology, and/or which

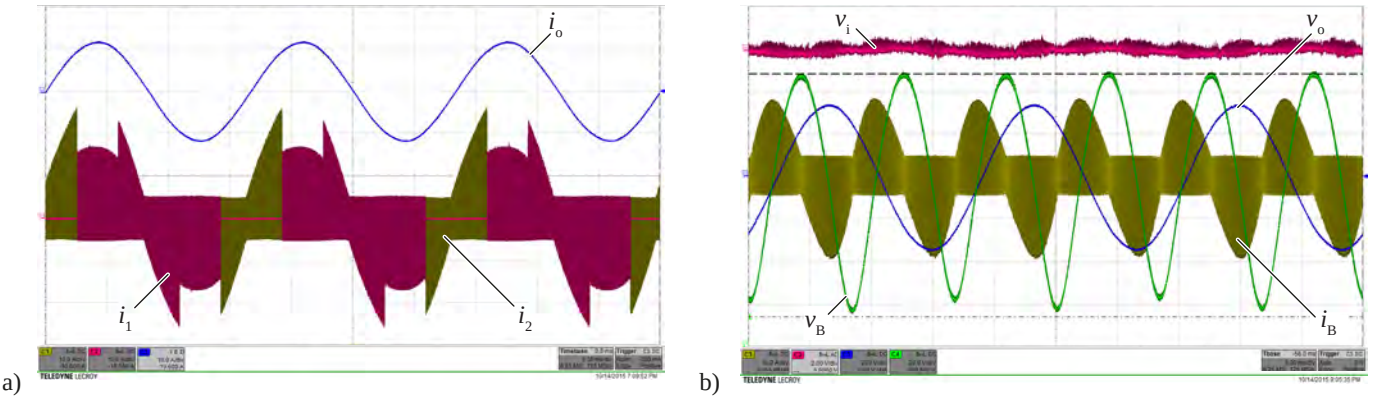



Fig. 3. (a) Current in one of the output phases $i_o$ (10 A/div) according to Fig. 1 and corresponding triangular switching-frequency currents $i_1$, $i_2$ (10 A/div)in the inductors of the interleaved bridge-legs. For maximal efficiency, both bridge-legs are operated simultaneously only around the current amplitudes; in the vicinity of the current zero-crossings only a single bridge-leg is operated alternatingly (4D-Interleaving [10]). (b) DC input voltage $v_i$ (2 V/div, AC-coupled), generated AC voltage $v_o$ (200 V/div) and buffer capacitor voltage $v_B$ (20 V/div) of the employed Power Pulsation Buffer (PPB), as well as the TCM current $i_B$ (10 A/div) in the PPB inductor.

shifting of the $\eta\rho$-Pareto front towards higher power densities and/or efficiencies could be achieved. Consequently, a comprehensive sensitivity analysis of the system performance depending on different key properties of the semiconductor devices has to be carried out. Therefore, as shown in Fig. 5, a step-by-step idealization of the power transistors is performed; $k_c$ and $k_s$ represent the weighting factors of the conduction and switching losses respectively, where $(k_c = 1, k_s = 1)$ characterizes the real switches and $(k_c = 0, k_s = 0)$ denotes the fully idealized switches without any conduction and switching losses.

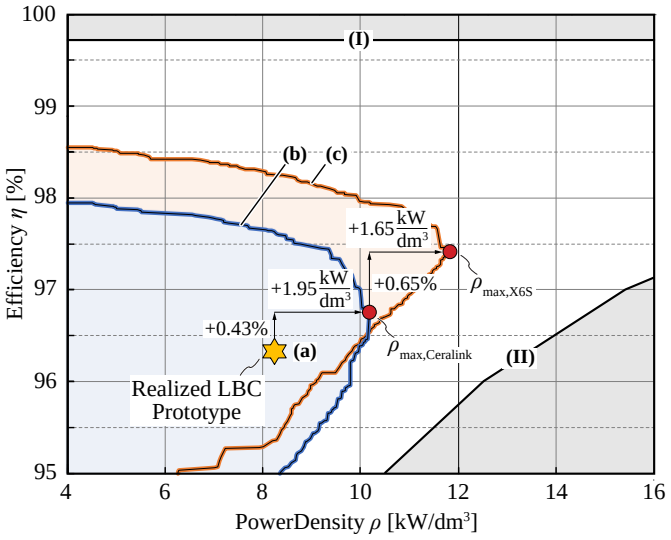



Fig. 4. Results of the multi-objective optimization of the converter concept in Fig. 1. (a) Performance of the converter system realized based on engineering experience without preceding design optimization (cf. Fig. 2). (b) results from the multi-objective optimization revealing that a single bridge-leg per phase is optimal. (c) Optimization results for employing a ceramic capacitor technology with lower losses in the Power Pulsation Buffer (PPB) (class II, X6S [5]), resulting in an improvement in efficiency and power density (reduced heat sink volume). This design is used in Section III as basis for further analysis. Note: (a) refers to a specific design point, i.e. the design of the system shown in Fig. 2, (b) and (c) refers to the $\eta\rho$-Pareto fronts. The grey shaded areas are indicating fundamental performance limits resulting from the power consumption of auxiliary circuits (measurements, control, i.e. DSP and FPGA, etc.) and from the power density of the cooling system which is directly defined by the relative losses $(1 - \eta)$ assuming a defined Cooling System Performance Index (CSPI, [8]) and a given temperature difference between heatsink and ambient.

It should be noted that, independently from the degree of idealization, the constant losses generated by the measurement, control and auxiliary circuits already define a maximum achievable efficiency (cf. (I) in Fig. 6). A further fundamental limit (II) is given by the efficiency dependent volume of the cooling system – characterized by the Cooling System Performance Index (CSPI, [8]) - and the storage capacitor volume of the Power Pulsation Buffer (PPB, [5]) as well as the constant volumes needed for the interconnections, the measurement and control circuits. Theoretically, even if the volume of all other components would be vanishing small, the sum of these volumes cannot be undercut [13].

In order to get a deeper insight into the optimal system designs calculated for the different weighting factor combinations ($k_c$, $k_s$), besides the resulting $\eta\rho$-Pareto fronts in Fig. 6 also the volume and loss distributions, the optimal inductance values and corresponding switching frequencies are given for the power density of $\rho = 6\,\mathrm{kW/dm^3}$ ($98.3\,\mathrm{W/in^3}$) as well as $\rho = 11.9\,\mathrm{kW/dm^3}$ ($195\,\mathrm{W/in^3}$), which is the maximum power density that can be achieved with a real system operated with Triangular Current Mode (TCM). The relatively low power density of $6\,\mathrm{kW/dm^3}$ can already be achieved with low switching frequencies, which due to the TCM operation corresponds to a relatively large inductance value. Accordingly, based on the Pareto optimization, the inductors consume the largest share of the overall system volume (cf. Fig. 6), since in

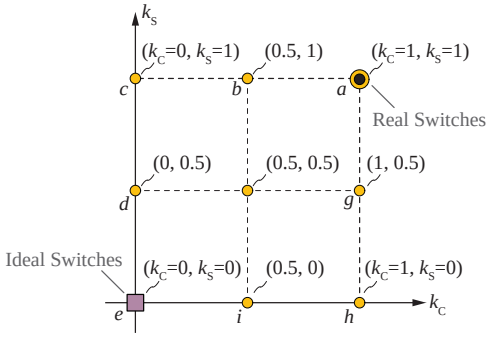



Fig. 5. Scaling factors $k_c \in [0, 1]$ and $k_s \in [0, 1]$ of the conduction and switching losses, respectively, used to gradually idealize the power semiconductor properties; $(k_c = 1, k_s = 1)$ represents the real switches (GaN GIT), $(k_c = 0, k_s = 0)$ represents ideal switches without any conduction and switching losses. The $\eta\rho$-Pareto fronts associated with the inscribed coordinates $(k_c, k_s)$ are shown in Fig. 6 for Triangular Current Mode (TCM) opertion and in Fig. 7 for PWM operation of the converter bridge-legs.

general the inductor losses decrease with larger construction volume and lower switching frequencies [13]. Furthermore, due to the low switching frequency the semiconductor losses are dominated by the conduction losses, thus a complete elimination of the switching losses $k_\mathrm{s} = 1 \rightarrow k_\mathrm{s} = 0$ results in a relatively low efficiency improvement. On the other hand, the elimination of the conduction losses $k_\mathrm{c} = 1 \rightarrow k_\mathrm{c} = 0$ shifts the $\eta\rho$-Pareto front by $\approx 0.5\,\%$ upwards. Consequently, this also results in a heat sink volume reduction (besides the effective component volume, the volumes given in Fig. 6 also include the corresponding heat sink volume, which is needed to dissipate the heat generated in the respective component), however, compared to the inductor volume the gained volume is small and thus the inductance value remains unchanged. In order to achieve a power density of $11.9\,\mathrm{kW/dm^3}$, which means that the inductance volume has to be strongly decreased, a much higher switching frequency is needed. Hence, again starting from $(k_\mathrm{c} = 1, k_\mathrm{s} = 1)$, with the elimination of the switching losses $k_\mathrm{s} = 1 \rightarrow k_\mathrm{s} = 0$ higher efficiency gains are achieved compared to $6\,\mathrm{kW/dm^3}$. The volume gained due to the volume reduction of the heat sink is now occupied by the inductors. Furthermore, compared to $(k_\mathrm{c} = 1, k_\mathrm{s} = 1)$, the inductance value is increased resulting in a lower switching frequency and/or in lower high-frequency (HF) inductor losses and thus in a higher system efficiency. A similar change in the design also occurs for $(k_\mathrm{c} = 0, k_\mathrm{s} = 1)$, however,

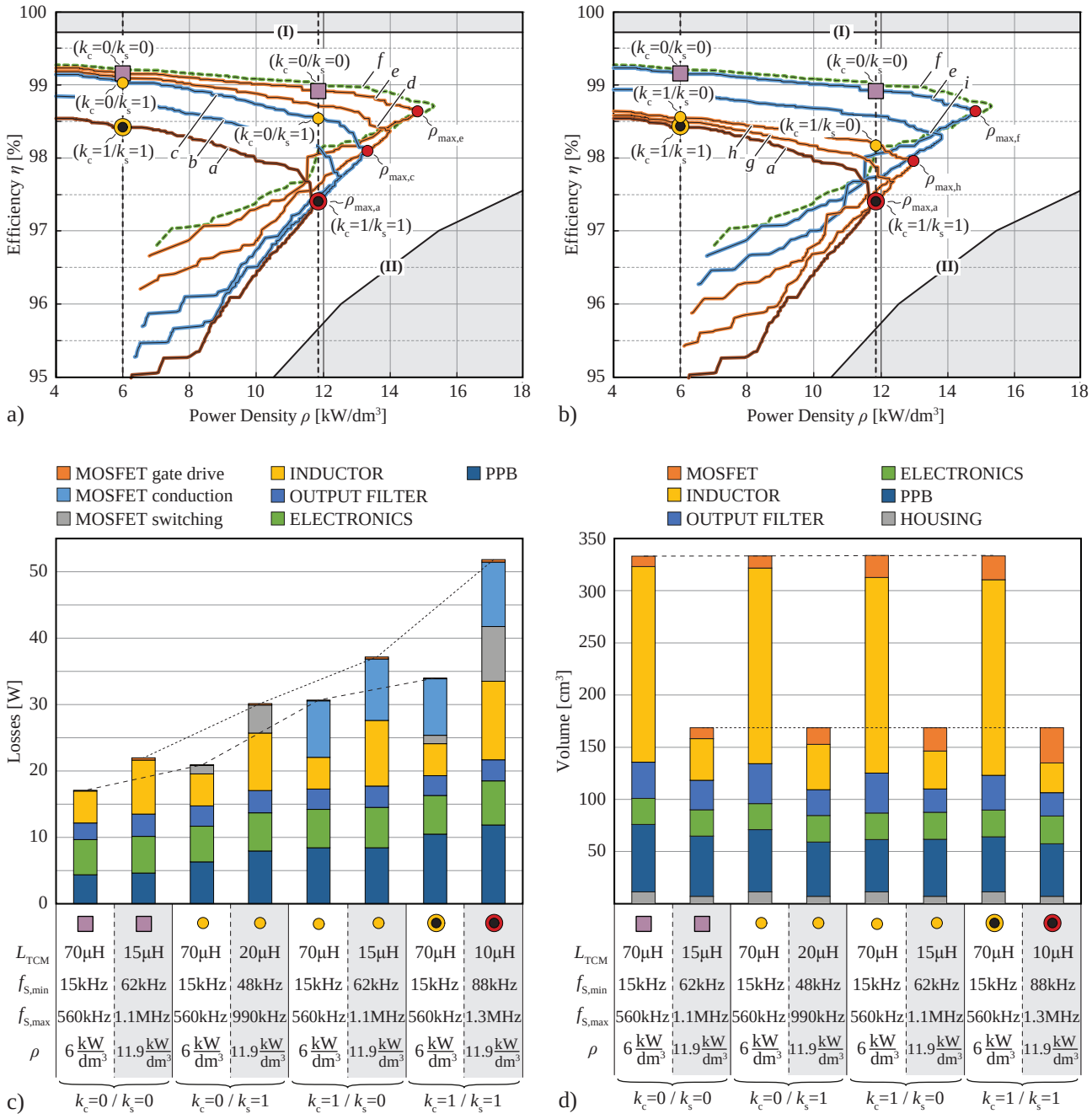



Fig. 6. (a) and (b): $\eta\rho$-Pareto fronts obtained for Triangular Current Mode (TCM) operation of the bridge-legs of each output phase ((c) in Fig. 4) for gradual idealization of the semiconductor properties according to Fig. 5. Furthermore, volume and loss balance, and component values for systems with a power density of $6\,\mathrm{kW/dm^3}$ ($98.3\,\mathrm{W/in^3}$) and $11.9\,\mathrm{kW/dm^3}$ ($195\,\mathrm{W/in^3}$) are depicted in (c) and (d), respectively. The latter represents the maximal power density achievable when employing real GaN GIT power semiconductor, i.e. $\rho_\mathrm{max}$ for $(k_c = 1,\ k_s = 1)$. The grey shaded areas are indicating fundamental performance limits (cf. Fig. 4).

since the conduction losses still represent the largest share of the semiconductor losses, compared to $(k_c = 1, k_s = 0)$ with the elimination of the conduction losses a smaller heat sink volume is needed, which in the optimization results in an even higher inductance value. In each case and independent of the degree of idealization, it can be noted that the maximum achievable power density $\rho_{max}$ as well as the resulting switching frequencies are still limited to reasonable values and/or compared to the optimal design for the real power semiconductors, the power density can (only) be improved by $\approx 20\,\%$. This can ultimately be related to the strongly switching frequency dependent HF-losses of the magnetic components and their cooling. A closer analysis shows that in all design points with maximum power densities $\rho_{max}$ the inductors are designed at their thermal limit. Consequently, a further enhancement of the power density (under the acceptance of decreasing efficiency) could only be achieved with an improved cooling system performance. Independent from the load conditions, the so far considered TCM modulation scheme enables soft-switching (ZVS) over the whole output period. On the other hand, the inductor current exhibits a high RMS current value with a large HF-current component, which in particular leads to notable HF-losses in the magnetic components at high switching frequencies. Furthermore, in spite of ZVS the high current ripple results in considerable switching losses during the turn-off transients [4]. Finally, the optimization is significantly restricted by the direct relation between selected inductance value and resulting switching frequency range which is inherent to TCM. It is therefore obvious that besides the TCM modulation also the conventional pulse width modulation (PWM) should be analyzed,

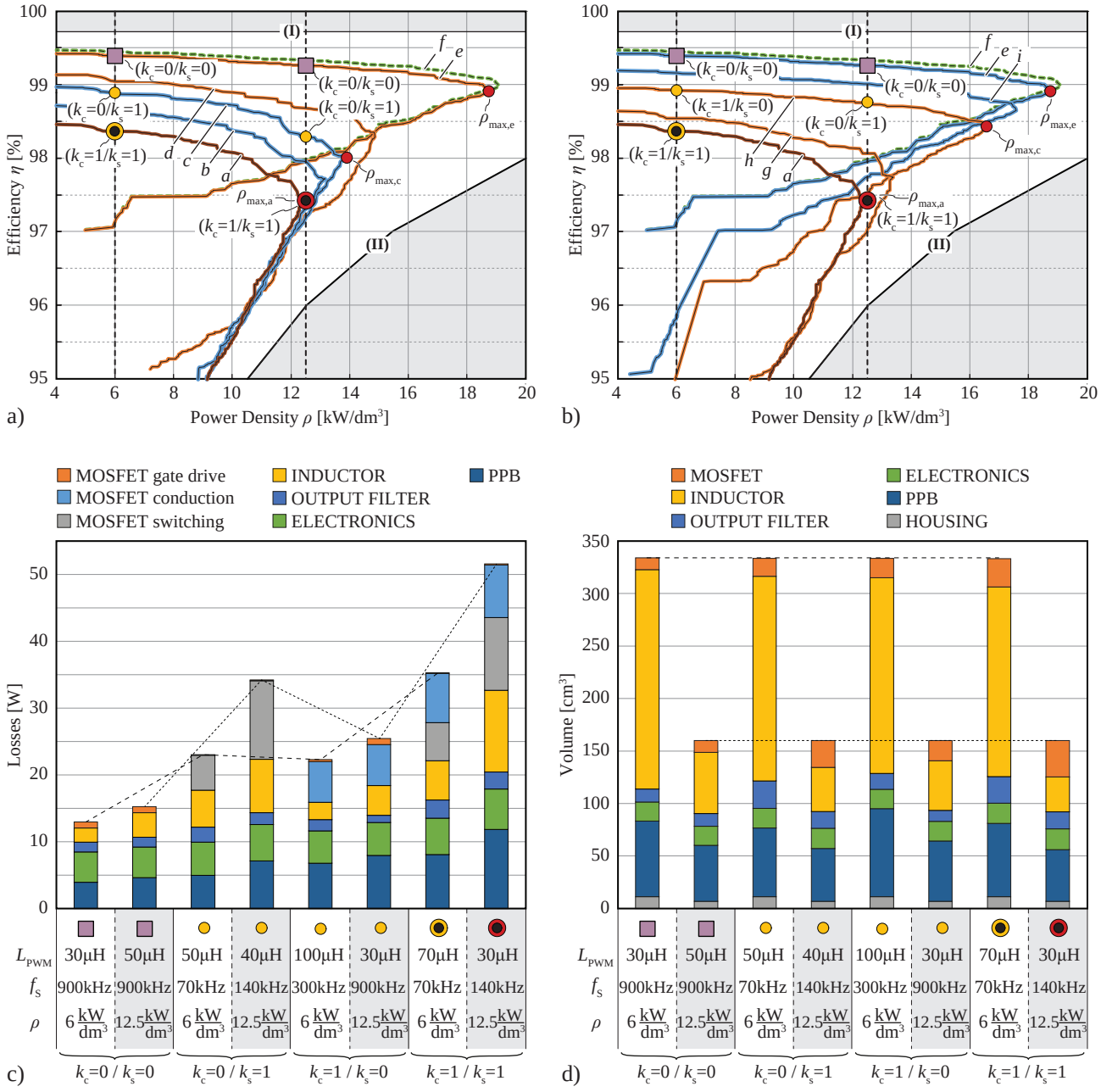



Fig. 7. (a) and (b): $\eta\rho$-Pareto fronts obtained for PWM operation of the bridge-legs of each output phase with constant switching frequency ((c) in Fig. 4) for gradual idealization of the semiconductor properties according to Fig. 5. Furthermore, volume and loss balance, and component values for systems with a power density of $6\,\mathrm{kW/dm^3}$ ($98.3\,\mathrm{W/in^3}$) and $12.5\,\mathrm{kW/dm^3}$ ($204.8\,\mathrm{W/in^3}$) are depicted in (c) and (d), respectively. The latter represents the maximal power density achievable when employing real GaN GIT power semiconductor. The grey shaded areas are indicating fundamental performance limits (cf. Fig. 4).

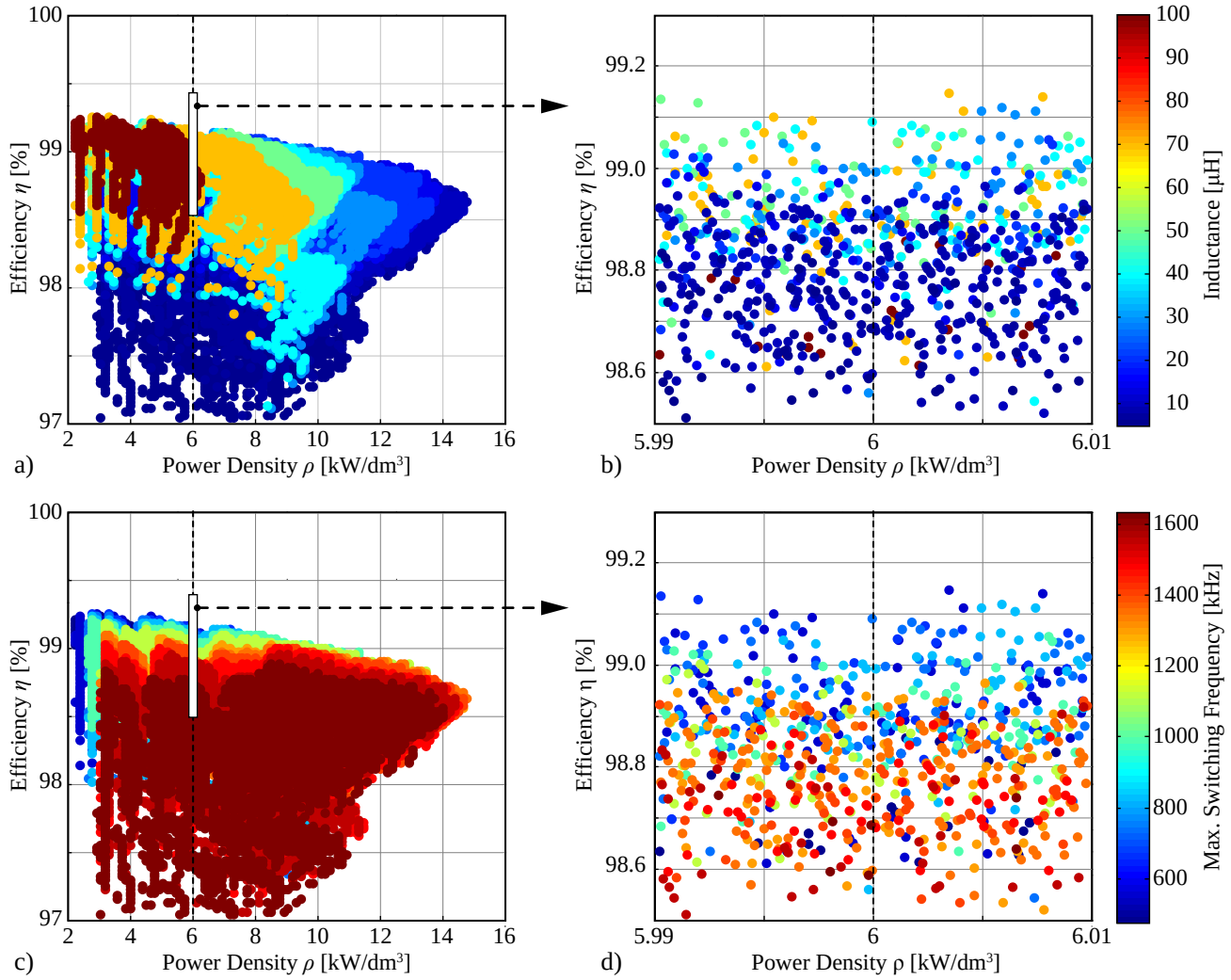



Fig. 8. (a) and (c): Results of the system optimization in the $\eta\rho$-performance space for fully idealized power semiconductors ($k_\mathrm{c} = 0$, $k_\mathrm{s} = 0$) and TCM operation. The colors are indicating the inductance value (cf. (a)) or maximum switching frequency (cf. (c)) used for the different designs. (b) and (d): Enlarged section of the performance space clearly showing the high design space diversity.

for which the inductance value can be selected independent from the (constant) switching frequency providing an additional degree of freedom. At a given switching frequency, for example, the HF-current ripple can be adjusted by the inductance value. While on the one hand, a small current ripple results in lower HF-losses in the magnetic components, with a higher current ripple the hard-switching turn-on losses can be decreased, which around the current zero crossings even turns into ZVS. High switching frequencies, however, which are e.g. typically achieved with TCM modulation around the zero crossings of the phase output currents, are beneficially avoided with PWM modulation saving again HF-losses. Furthermore, the switching frequency can also be selected as $f_\mathrm{PWM} < 150\,\mathrm{kHz}$, which is below the lower frequency limit of the EMI directives relevant frequency range.

In analogy to the optimization results shown in Fig. 6 for TCM modulation, in Fig. 7 the optimization results for PWM are given. The system parameters determined for $6\,\mathrm{kW/dm^3}$ and $12.5\,\mathrm{kW/dm^3}$ (which is the maximum achievable power density for the PWM system employing real switches), can be explained again with similar reasons as for TCM in Fig. 6. For the sake of brevity a detailed explanation is omitted here and the authors would like to refer to [12] for a comprehensive discussion. It only should be emphasized that the possibility of an independent selection of the switching frequency and the inductance value provides a better utilization of the design space and compared to $(k_\mathrm{c} = 1, k_\mathrm{s} = 1)$ with the ideal switch the power density can be increased by $\approx 50\,\%$ at a similar efficiency as achieved with TCM.

## IV. Analysis of Design Space Diversity

The parameter values (inductor values $L_\mathrm{TCM}/L_\mathrm{PWM}$ and switching frequencies $f_\mathrm{PWM}$) determined for the different system designs $(k_\mathrm{c} = 1, k_\mathrm{s} = 1), \ldots, (k_\mathrm{c} = 0, k_\mathrm{s} = 0)$, which are given in Fig. 6 and Fig. 7, cannot always be explained immediately, since there is no clear tendency for component values, such as a steady decrease of the inductance $L$ or increase of the switching frequency $f_\mathrm{PWM}$, even if the power switches are more and more idealized. In general, one would expect that the system designs found for the real and the ideal power switches represent extreme design points which also provide corresponding extreme parameter values and consequently, in case of a partial switch idealization, the values for the inductance $L_\mathrm{TCM}/L_\mathrm{PWM}$ and switching frequency $f_\mathrm{PWM}$ would be within the range defined by the extreme values. Considering all design points listed in Fig. 6 and Fig. 7, with PWM operation this is totally true for the switching frequency $f_\mathrm{PWM}$ and also applies for almost all inductance values $L_\mathrm{TCM}/L_\mathrm{PWM}$. For both modulation schemes, TCM and PWM, only one design point with a partial idealization of the power

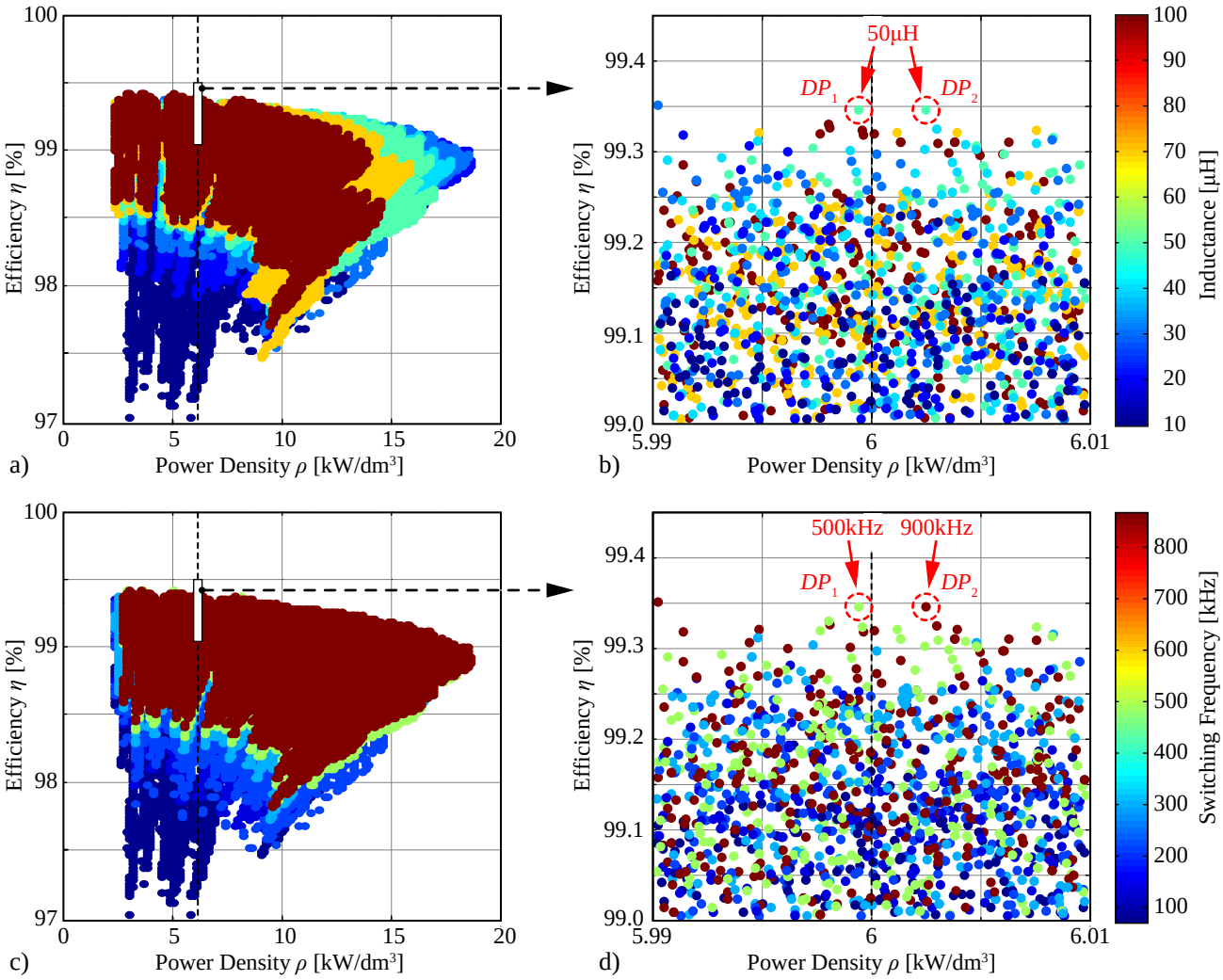



Fig. 9. As Fig. 8 but for PWM operation of the bridge legs. Two designs achieving nearly the same $\eta\rho$-performance with same inductance values but substantially different PWM switching frequency are indicated in (b) and (d), again underlining a high degree of design diversity.

switch is outside the extreme value range, e.g. at the power density of $6\,\mathrm{kW/dm^3}$ and PWM, for the design point without conduction losses ($k_\mathrm{c}=1, k_\mathrm{s}=0$), the inductance value $L_\mathrm{PWM}=100\,\mu\mathrm{H}$ is far outside the extreme values of $L_\mathrm{PWM}=30\,\mu\mathrm{H}$ ($k_\mathrm{c}=1, k_\mathrm{s}=1$) and $L_\mathrm{PWM}=50\,\mu\mathrm{H}$ ($k_\mathrm{c}=0, k_\mathrm{s}=0$) (cf. Fig. 7). This broad parameter spread (also outside the extreme value range) can be explained based on the design space diversity shown in Fig. 8 for TCM and in Fig. 9 for PWM, where the color of all calculated design points is selected depending on the determined inductance value $L_\mathrm{TCM}/L_\mathrm{PWM}$ or switching frequency $f_\mathrm{PWM}$. By limiting the power density to only $6\,\mathrm{kW/dm^3}\pm0.01\,\mathrm{kW/dm^3}$ and the efficiency for TCM to $\eta>98.5\,\%$ and for PWM to $\eta>99\,\%$, it becomes clear that on the one hand, a large number of different design points results in the same or quite similar performance and on the other hand, the design points feature a wide variety of parameter values (inductor value $L_\mathrm{TCM}/L_\mathrm{PWM}$ and switching frequency $f_\mathrm{PWM}$), thus underlining the broad design space diversity. This can be justified by the fact that despite a totally different design point selection certain effects concerning losses and volume are compensating each other either within the same single component (e.g. LF and HF-losses in the inductor) or between different components (e.g. inductors and power switches). This is illustrated using the example of two design points, $DP_1$ and $DP_2$, marked in Fig. 9. Both design points $DP_1$ and $DP_2$ have an inductance value of $L_\mathrm{PWM}=50\,\mu\mathrm{H}$, however, the switching frequencies differ almost by a factor of two ($f_\mathrm{PWM,DP1}=500\,\mathrm{kHz}$ and $f_\mathrm{PWM,DP2}=900\,\mathrm{kHz}$), but still both designs lead to quasi identical performance concerning volume and efficiency. By analyzing the volume and loss distribution for $DP_1$ and $DP_2$, it can be noticed that the inductors are constructed identically, i.e. the same core type and the same litz wire and the same number of turns is used. Consequently, for both designs the effective inductor volume (without corresponding heat sink volume) is the same. However, due to the different switching frequencies, the generated inductor losses and accordingly also the corresponding heat sink volumes are different. Considering the loss distribution in the inductor, it can be noticed that compared to $DP_1$ with the higher switching frequency in design point $DP_2$ the core losses can be reduced by $\Delta P_\mathrm{core}=P_\mathrm{core,DP2}-P_\mathrm{core,DP1}=-400\,\mathrm{mW}$. This gain in efficiency can be explained by the fact that the Steinmetz parameters in this frequency range exhibit a stronger dependency of the core losses on the flux density $\Delta B_\mathrm{HF}$ than on the switching frequency $f_\mathrm{PWM}$, and thus the higher switching frequency leads to a smaller current ripple $\Delta I_\mathrm{L,HF}$ and accordingly to a lower flux density excitation $\Delta B_\mathrm{HF}$ in the core material. In contrast, however, due to the higher switching frequency, in $DP_2$ the gate drive losses (still considered despite the idealization of the conduction and switching

losses) are increased by $\Delta P_{\mathrm{gd}} = P_{\mathrm{gd,DP2}} - P_{\mathrm{gd,DP1}} = 400\,\mathrm{mW}$ compared to $DP_1$. Hence, the gains in efficiency due to the lower core losses $\Delta P_{\mathrm{core}}$ are again compensated by the additional losses $\Delta P_{\mathrm{gd}}$ in the gate drive, which means that there exists a compensation effect between different components and thus, in spite of a different design of the components the overall efficiency stays constant. As already mentioned, for both design points the effective inductor and gate drive volume stays constant and only the heat sink volumes are changing. However, since for both components the heat sink volume is calculated based on the same CSPI, not only the losses but also the volumes of the two components compensate each other, which means that also the performance concerning power density stays constant. Furthermore, the different switching frequencies used in $DP_1$ and $DP_2$ not only causes different core losses but also different winding losses. It becomes evident that with the higher switching frequency in $DP_2$ the HF-winding losses increase by $\Delta P_{\mathrm{wind,HF}} = P_{\mathrm{wind,HF,DP2}} - P_{\mathrm{wind,HF,DP1}} = 200\,\mathrm{mW}$ and on the contrary, due to the lower RMS-current (lower HF-current ripple), the low-frequency (LF)-winding losses (60 Hz) are dropping by the same amount ($\Delta P_{\mathrm{wind,LF}} = P_{\mathrm{wind,LF,DP2}} - P_{\mathrm{wind,LF,DP1}} = -200\,\mathrm{mW}$). Hence, also two other effects are compensating each other within the same component. As a consequence, already the comparison of these two design points exemplifies, that it is nearly impossible to keep an overview of the large design diversity shown in Fig. 8 and Fig. 9 without an optimization as performed in this paper. Finally, for the realization of the system, a certain design point has to be selected from the wide variety of possible designs. As it is also done for the design points given in Fig. 8 and Fig. 9, for a given power density ($6\,\mathrm{kW/dm^3} \pm 0.01\,\mathrm{kW/dm^3}$) one could simply choose the design with the highest efficiency, which based on the $\eta\rho$-analysis provides the best performance. However, this design probably features a large inductance and/or demands a large semiconductor area which results in high system costs, or the selected design parameters are not allowing a highly dynamic control of the system. Therefore, besides the $\eta\rho$-analysis, additional design criteria such as costs ($\$/\mathrm{kW}$), realization effort, control performance, thermal aspects, etc. have to be considered in order to support/simplify the decision making process and to filter out the actually optimal design for the underlying application.

## V. Conclusion

As shown in this work, an increase of the power density of state-of-the-art air-cooled single-phase DC/AC converters with higher power rating is possible by a factor of $2\ldots3$ until $\approx 15\,\mathrm{kW/dm^3}$ ($250\,\mathrm{W/in^3}$) by further improvements of the power semiconductor technology. Furthermore, the losses can be reduced by a factor of $\approx 2$ compared to the state of the art, and efficiency values of nearly $99\,\%$ can be achieved at high power density values. The reason for the limitation of the power density increase - even if ideal power semiconductors are considered - is the fact that an energy storage has to be necessarily employed for the DC/AC conversion given that an approximately constant DC input current is required. This size of the energy storage could only be decreased by new dielectric materials (ceramics) with higher energy density. On the other hand, the switching frequency that is derived by a multi-objective optimization stays even for theoretically ideal power semiconductors in the range of $\approx$ 1...1.5 MHz. This is mainly due to the ferrite materials that are used today and due to the high-frequency inductor losses that are increasing with higher switching frequencies. Furthermore, when reducing the size of the magnetic components, finally a thermal limit is reached, which can only be shifted by novel cooling concepts. Thus, research focus has to be primarily put on magnetic components and advanced cooling methods besides the ongoing improvement of the performance of wide-bandgap semiconductors and their applicability through 3D-packaging, the integration of the semiconductors with gate drivers, monitoring, sensing and protection circuits to intelligent, low-inductive and electromagnetically quiet modules, as well as through digital control ICs with high clock frequency and time resolution, respectively, and low power consumption. Some examples are high frequency magnet materials with low permeability, new winding techniques and arrangements, new magnetic circuit geometries [14], [15], electrically isolating materials with high thermal conductivity being used as heat spreaders and extractors, and double-sided cooling as well as corresponding advanced design tools. All this could allow overcoming the switching frequency barrier at approximately 1 MHz for non-modular systems in the kilowatt range with two-level bridge legs while maintaining acceptable losses and realization costs and advancing towards even higher power densities due to the reduction of the EMI filter size.

## References


[1] J. W. Kolar, F. Krismer, and H. P. Nee, "What are the "Big Challenges" in Power Electronics?" *Pres. at the 8th IEEE Int. Conf. Integr. Power Electron. Syst. (CIPS)*, pp. 1–20, 2014.

[2] C. P. Henze, H. C. Martin, and D. W. Parsley, "Zero-voltage Switching in High Frequency Power Converters using Pulse Width Modulation," in *Proc. of the 3rd IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1988, pp. 33–40.

[3] C. Marxgut, J. Biela, and J. W. Kolar, "Interleaved Triangular Current Mode (TCM) Resonant Transition, Single-Phase PFC Rectifier with High Efficiency and High Power Density," in *Proc. of the IEEE Int. Power Electron. Conf. (ECCE Asia, IPEC)*, 2010, pp. 1725–1732.

[4] D. Bortis, D. Neumayr, O. Knecht, and J. W. Kolar, "Comprehensive Evaluation of GaN GIT in Low- and High-Frequency Bridge Leg Applications," in *Proc. of the IEEE Energy Convers. Congr. Expo. (ECCE Asia) [Accepted for Publication]*, 2016.

[5] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-Compact Power Pulsation Buffer for Single-Phase DC/AC Converter Systems," in *Proc. of the IEEE Energy Convers. Congr. Expo. (ECCE Asia) [Accepted for Publication]*, 2016.

[6] F. Zajc, "Flat Band Winding for an Inductor Core," US Patent (pending).

[7] ——, "Multi Gap Inductor Core, Multi Gap Inductor, Transformer and Corresponding Manufacturing Method," Patent EP 2 528 069 B1, December 18, 2013.

[8] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM Converter Power Density Barriers," in *Proc. of the 4th IEEE Power Conversion Conference (PCC)*, 2007, pp. 9–29.

[9] J. W. Kolar, D. Bortis, D. Neumayr, Y. Lobsiger, O. Knecht, and F. Krismer, "Approaches to Overcome the Google/IEEE Little-Box Challenges," *Keynote Presentation at the 37th IEEE International Telecommunications Energy Conference (INTELEC)*, 2015.

[10] M. Kasper, M. Antivachis, D. Bortis, J. W. Kolar, and G. Deboy, "4D-Interleaving of Isolated ISOP Multi-Cell Converter Systems for Single-Phase AC/DC Conversion," in *Proc. of the IEEE Intern. Exhibit. and Conf. for Power Electron., Intel. Motion, Renew. Energy and Energy Managem. (PCIM)*, 2016.

[11] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance Trends and Limitations of Power Electronic Systems," in *Proc. of the 6th IEEE Int. Conf. Integr. Power Electron. Syst. (CIPS)*, 2010, pp. 1–20.

[12] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$ -Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the Google Little Box Challenge," in *Proc. of the 17th IEEE Workshop on Control Model. Power Electron. (COMPEL) [Submitted for Publication]*, 2016.

[13] J. W. Kolar, J. Biela, and J. Miniböck, "Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2% Efficiency vs. $7\,\mathrm{kW/dm^3}$ Power Density," in *Proc. of the 6th IEEE Int. Power Electron. Motion Control Conf. (ECCE Asia, IPEMC)*, 2009, pp. 1–21.

[14] A. J. Hanson, J. A. Belk, S. Lim, D. J. Perreault, and C. R. Sullivan, "Measurements and Performance Factor Comparisons of Magnetic Materials at High Frequency," in *Proc. of the IEEE Energy Convers. Congr. Expo. (ECCE)*, 2015, pp. 5657–5666.

[15] C. R. Sullivan, "Prospects for Advances in Power Magnetics," in *Proc. of the 9th IEEE International Conference on Integrated Power Electronics Systems (CIPS)*, 2016.

ETH zürich

# The Ideal Switch Is Not Enough ?

007

**Johann W. Kolar et al.**

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

ETH zürich

# The World Is Not Enough !

007

**Johann W. Kolar, D. Bortis, D. Neumayr**

Swiss Federal Institute of Technology (ETH) Zurich
Power Electronic Systems Laboratory
www.pes.ee.ethz.ch

# Outline

- The Google Little Box Challenge
- *Little Box 1.0*
- *ηρ - Pareto Optimization*
- *ηρ - Pareto Limits for Ideal Switches*
- *Little Box 2.0 - Alternative Topologies*
- *Little Box 3.0 - HF Magnetics, etc.*
- Conclusions

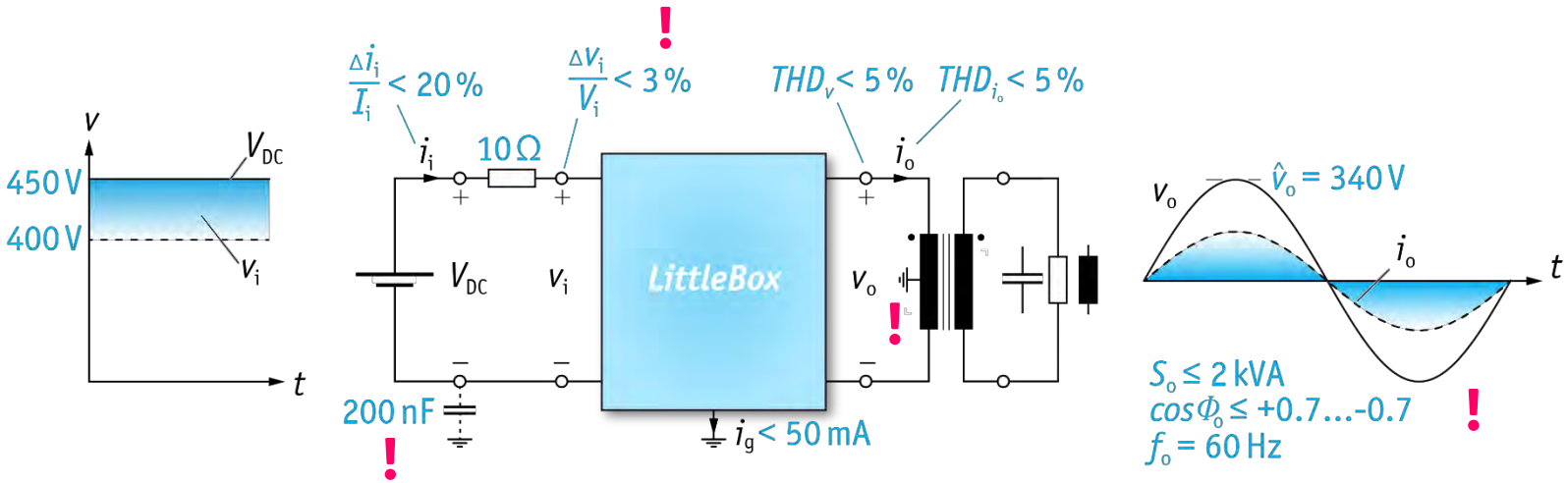
# Google Little Box Challenge

Requirements
The Grand Prize
Team Members

# LiTTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B




■ Push the Forefront of New Technologies in R&D of High Power Density Inverters

# LiTTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-Φ Solar Inverter with the Highest Power Density in the World
- **Power Density > 3kW/dm³ (50W/in³)**
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B

■ **Push the Forefront of New Technologies in R&D of High Power Density Inverters**

# The Grand Prize

Google | IEEE

- Highest Power Density (> 50W/in$^3$)
- Highest Level of Innovation

**$1,000,000**

- Timeline
  - Challenge Announced in Summer 2014
  - 2000+ Teams Registered Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - 18 Finalists (3 No-Shows)

# Inverter

- **Multi-National Team**
  - Switzerland
  - Germany
  - Slovenia

ETH zürich ... Topologies, Circuits, Control, Software, System Testing, etc.

Fraunhofer IZM ... Packaging, Embedding, EMI, etc.

Fraza d.o.o. ... HF Inductor Technology

- **Acknowledgment**
  - Components
  - Academic Award (10)
  - Donation (6)

Infineon EPCOS TDK

Google

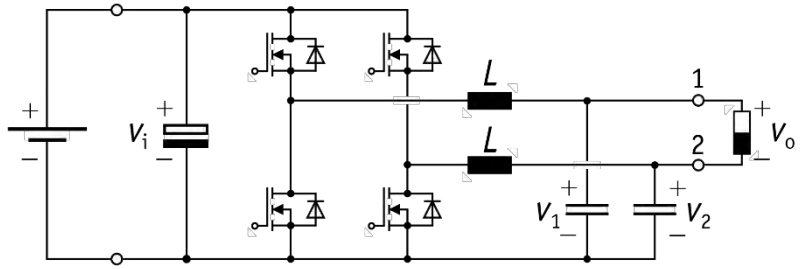
ECPE

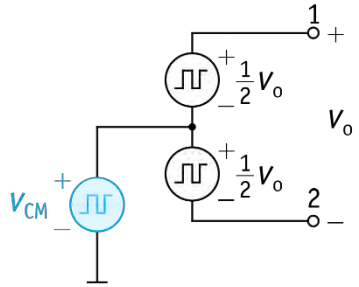
# Little Box 1.0

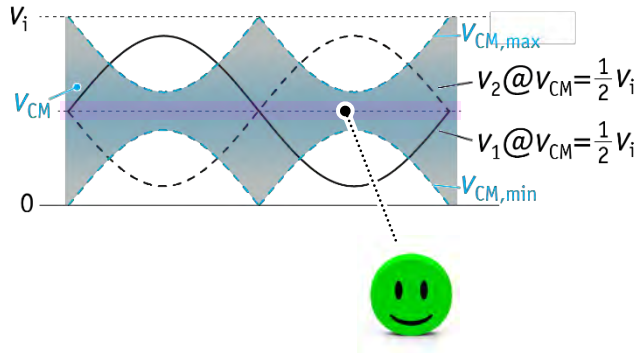
Converter Topology
ZVS Modulation Scheme
GaN GIT Gate Drive
Hardware Demonstrator

# Selected Converter Topology

- Full-Bridge Output Stage
- Modulation of Both Bridge Legs



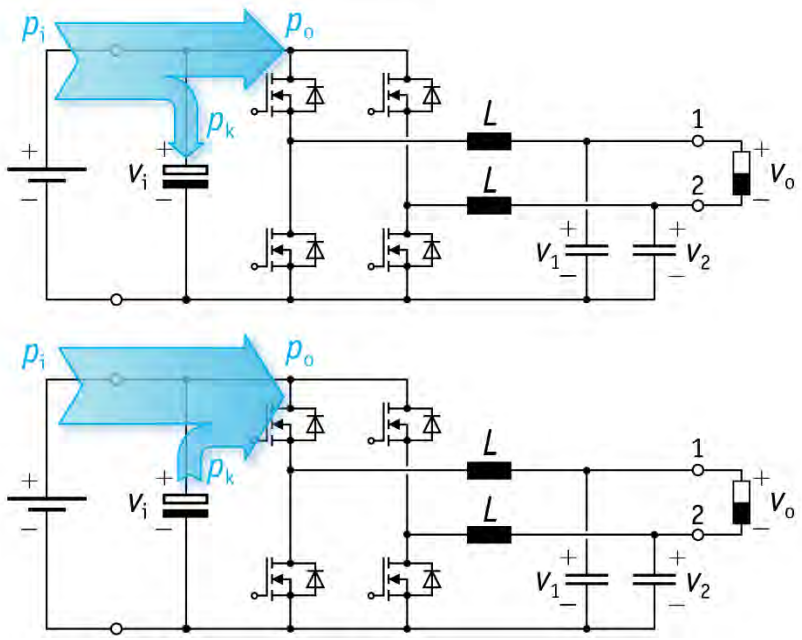



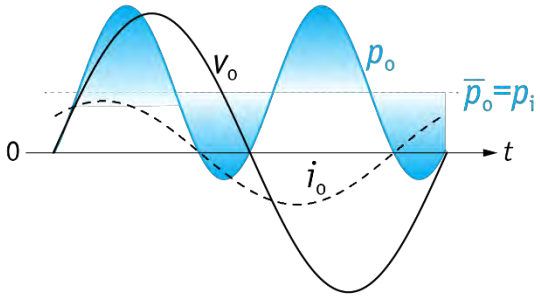




- DM Component of $u_1$ and $u_2$ Defines Output Voltage $u_0$
- No Low-Frequency CM Component of $u_1$ and $u_2$ (Different to e.g. 1-Φ PFC Rectifier Systems !)

# DC-Side Power Pulsation Buffering

- Compensation of 120Hz Output Power AC Component → Constant DC Supply Current

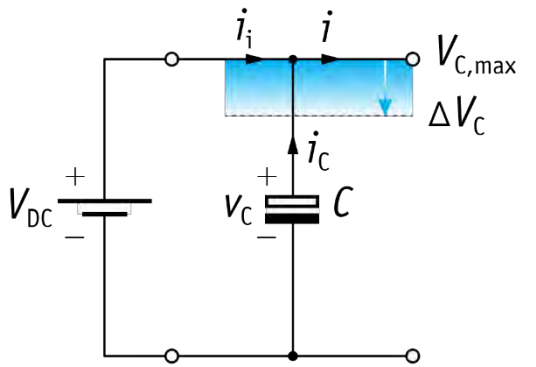


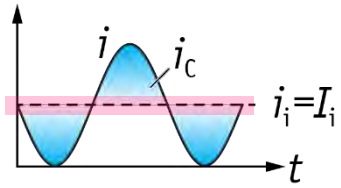



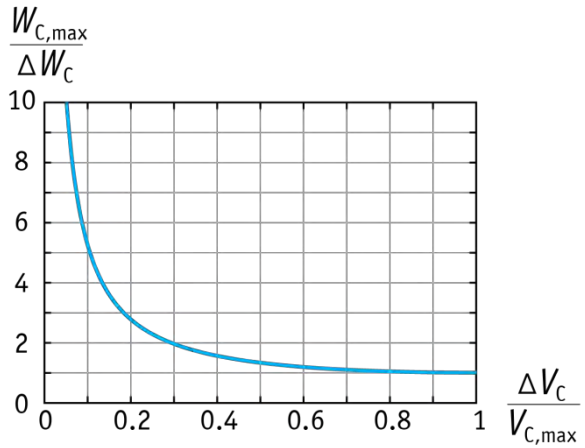

- Parallel or Series / Passive or Active Buffer Concepts
- Parallel Approach for Limiting Voltage Stress on Full-Bridge Semiconductors

# DC-Side Passive Power Pulsation Buffer

- Electrolytic Capacitor



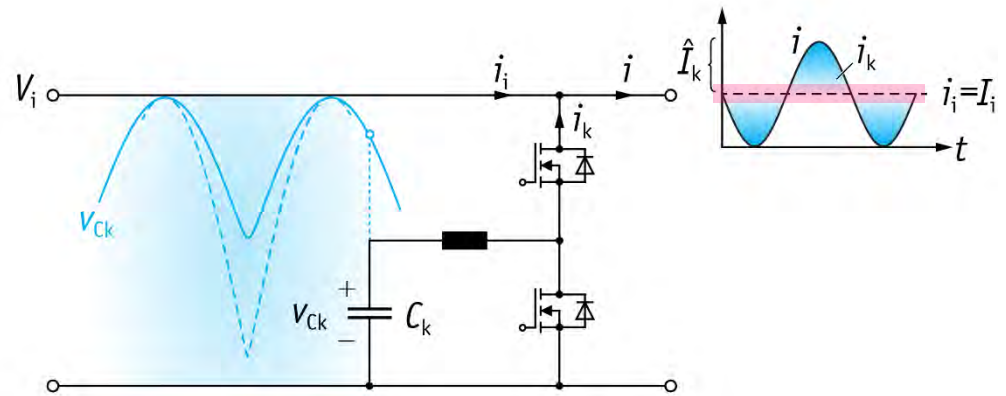




$S_0$ = 2.0 kVA
cos $\Phi_0$ = 0.7
$V_{C,max}$ = 450 V
$\Delta V_C / V_{C,max}$=3 %

- C > 2.2mF / 166 cm$^3$ → Consumes 1/4 of Allowed Total Allowed Volume !

# DC-Side Active Power Pulsation Buffer

- Large Voltage Fluctuation Foil or Ceramic Capacitor
- Buck-Type (Lower Voltage Levels) or Boost-Type DC/DC Interface Converter



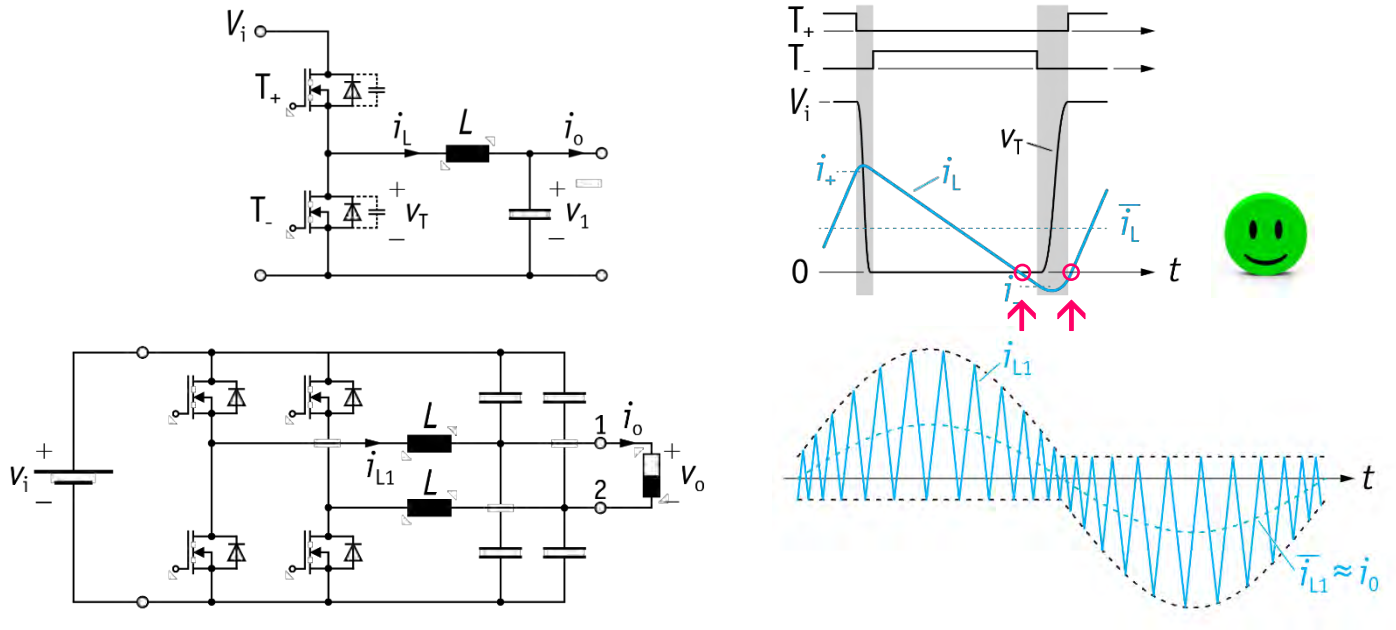

CeraLink TDK

108 x 1.2µF /400 V
$C_k \approx 140\mu F$
$V_{Ck} = 23.7cm^3$

- Significantly Lower Overall Volume Compared to Electrolytic Capacitor

# Triangular Current Mode (TCM) ZVS Operation

- TCM Operation for Resonant Voltage Transition @ Turn-On/Turn-Off

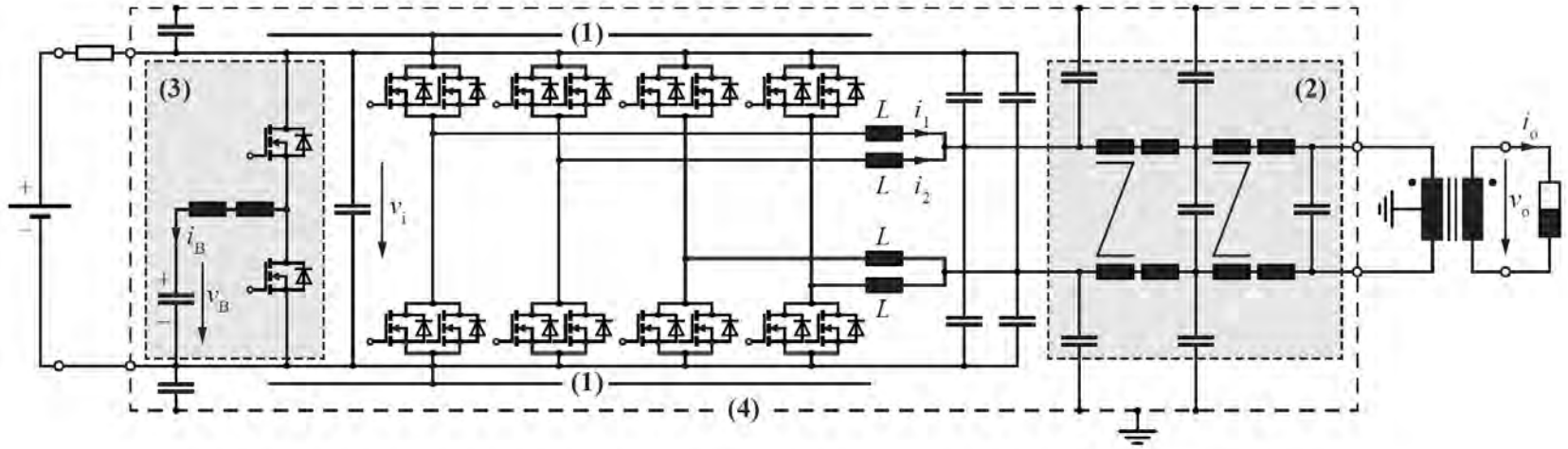



- Requires Only Measurement of Current Zero Crossings, $i = 0$
- High $f_S$ Around $i = 0$ Challenging for Digital Control
- Variable Sw. Freq. $f_S$ Lowers EMI

# Final Converter Topology

- Interleaving of 2 Bridge Legs per Phase
- Active DC-Side Buck-Type Power Pulsation Buffer
- 2-Stage EMI AC Output Filter

(2) EMI Filter
(3) Power Pulsation Buffer

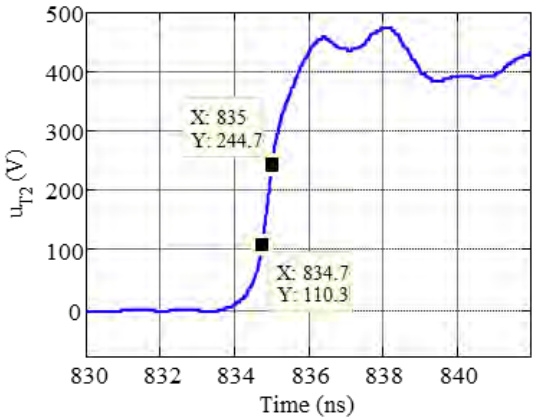



- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range (4D-TCM-Interleaving)
- Heatsinks Connected to DC Bus / Shield to Prevent Cap. Coupling to Grounded Enclosure

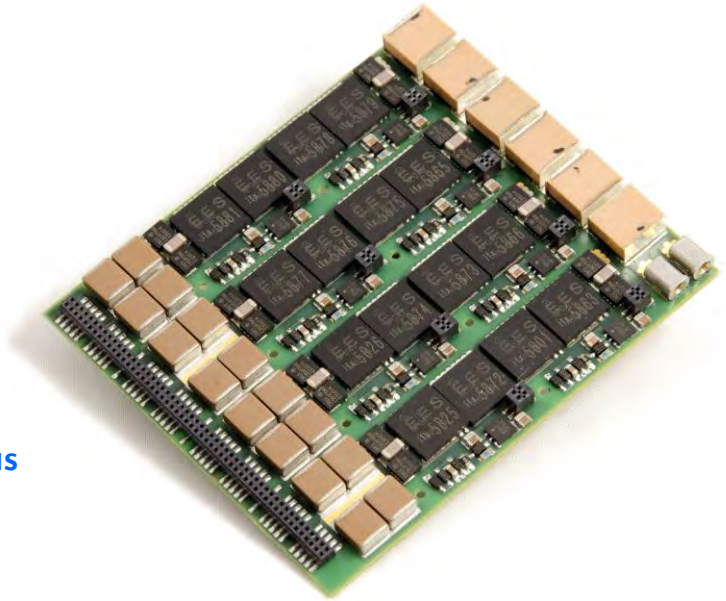
# Power Semiconductors

- 600V IFX Normally-Off GaN GIT - ThinPAK8x8
- 2 Parallel Transistors / Switch
- Antiparallel CREE SiC Schottky Diodes

- 1.2V typ. Gate Threshold Voltage
- 55 mΩ $R_{DS,on}$ @ 25°C, 120mΩ @ 150°C
- 5Ω Internal Gate Resistance



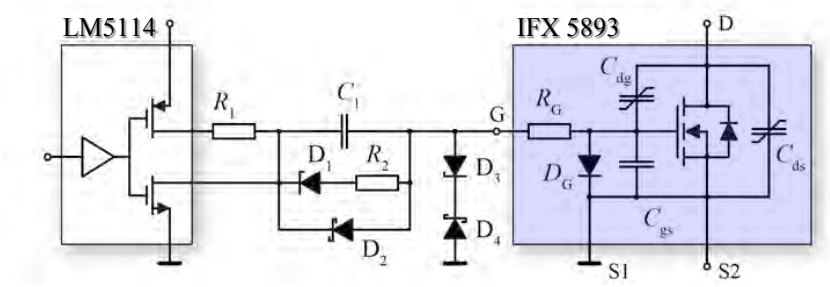

dv/dt = 500kV/µs

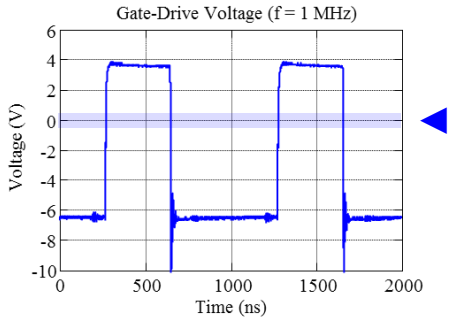


- CeraLink Capacitors for DC Voltage Buffering

# Advanced Gate Drive

- Fixed Negative Turn-off Gate Voltage - Independent of Sw. Frequency and Duty Cycle
- Extreme dv/dt Immunity (500kV/µs) - Due to CM Choke at Signal Isolator Input

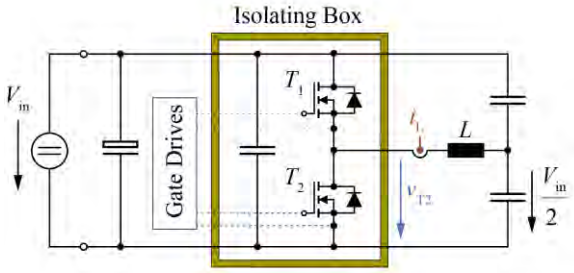


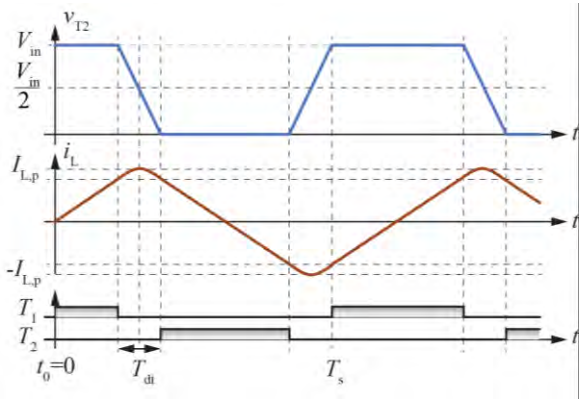



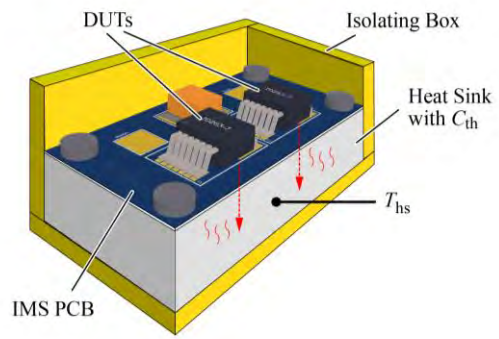

- Total Prop. Delay < 30ns incl. Signal Isolator, Gate Drive, and Switch Turn-On Delay

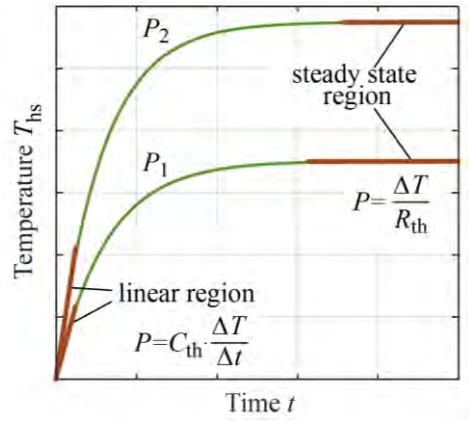
# Remark: Accurate ZVS Sw. Loss Measurement

- Accurate Measurement by Calorimetric Approach
- High Sw. Frequency for Large Ratio of Sw. and Conduction Losses



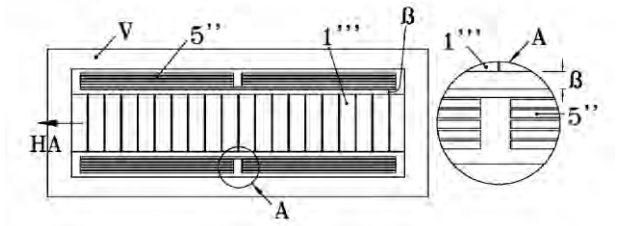

- Direct Measurement of the Sum of Sw. and Conduction Losses
- Subtraction of the Conduction Losses Known from Calibration
- Fast Measurement by $C_{th}.\Delta T/\Delta t$ Evaluation

# High Frequency Inductors (1)

- Multi-Airgap Inductor with Patented Multi-Layer Foil Winding Minimizing Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza (2012)

- L= 10.5µH
- 2 x 8 Turns
- 24 x 80µm Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 µm Copper Foil / 4 in Parallel
- 7 µm Kapton Layer Isolation
- 20mΩ Winding Resistance / Q=800
- Terminals in No-Leakage Flux Area

■ Dimensions - 14.5 x 14.5 x 22mm³



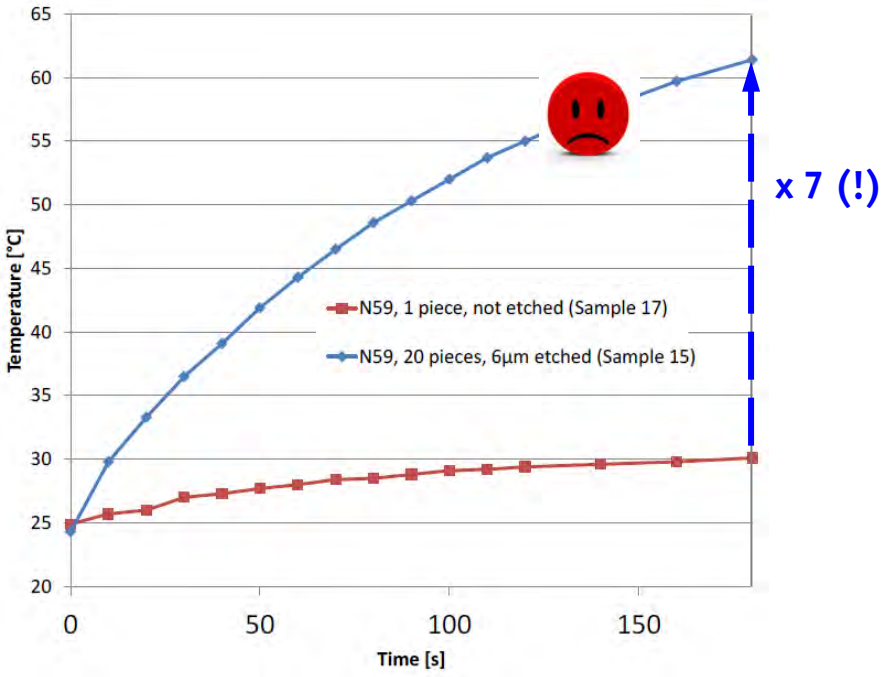

# High Frequency Inductors (2)

IEEE TRANSACTIONS ON MAGNETICS, VOL. MAG-11, NO. 1, JANUARY 1975 ←

**The Origin of the Increase in Magnetic Loss Induced by Machining Ferrites**

JOHN E. KNOWLES

- Cutting of Ferrite Introduces Mechanical Stress in the Surface (5µm Layer)
- Significant Increase of the Loss Factor
- Reduction by Polishing / Etching




- Comparison of Temp. Increase of a Bulk and a Sliced Sample @ 70mT / 800kHz

# Little-Box 1.0 Prototype

- **Specifications**

- 8.2 kW/dm$^3$
- 8.9cm x 8.8cm x 3.1cm
- **96,3% Efficiency @ 2kW**
- **$T_c$=58°C @ 2kW**

- $\Delta u_{DC}$= 1.1%
- $\Delta i_{DC}$= 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%


- **Compliant to All *Original* Specifications (!)**

- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

# Little-Box 1.0 Prototype

- **Specifications**

- 8.2 kW/dm$^3$
- 8.9cm x 8.8cm x 3.1cm
- **96,3% Efficiency @ 2kW**
- **$T_c$=58°C @ 2kW**

- $\Delta u_{DC}$= 1.1%
- $\Delta i_{DC}$= 2.8%
- $THD+N_U$ = 2.6%
- $THD+N_I$ = 1.9%

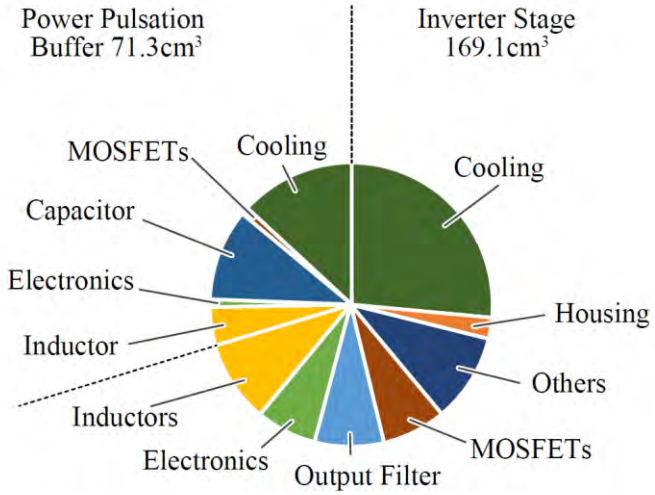
★ **135 W/in$^3$**

- **Compliant to All *Original* Specifications (!)**

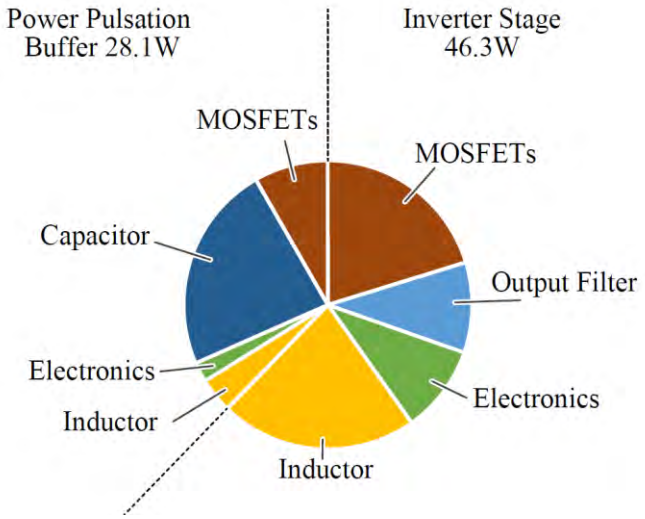
- No Low-Frequ. CM Output Voltage Component
- No Overstressing of Components
- All Own IP / Patents

# Evaluation / Optimization Potential

- **Volume Distribution (240cm³)**




- **Loss Distribution (75W)**



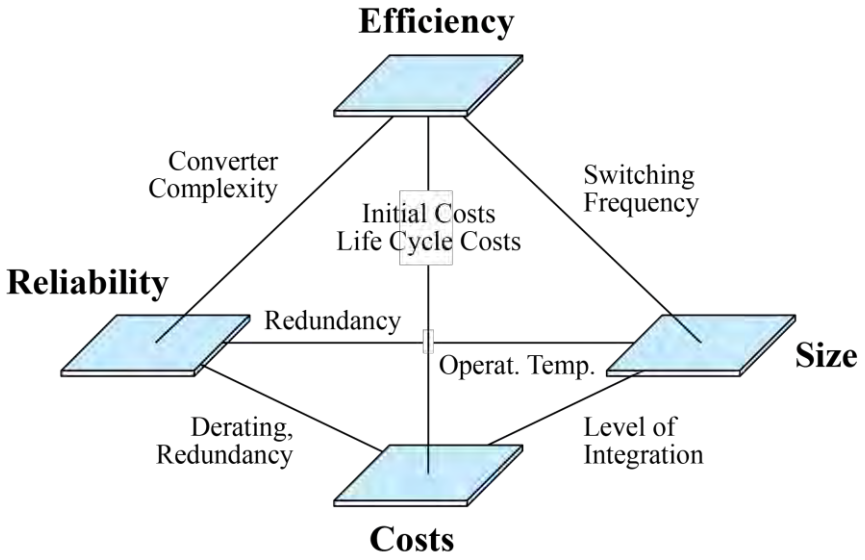

- Large Heatsink (incl. Heat Conduction Cu Interfaces)
- Large Losses in Power Fluctuation Buffer Capacitor (!)
- TCM Causes Relatively High Conduction & Switching Losses @ Low Power
- Relatively Low Switching Frequency @ High Power – Determines EMI Filter Volume

# $\eta\rho$-Pareto Optimization

Design Space / Performance Space
Pareto Front / Design Space Diversity
New Power Pulsation Buffer Capacitor Technology
Optimization of Little Box 1.0

# Multi-Objective Design Challenge

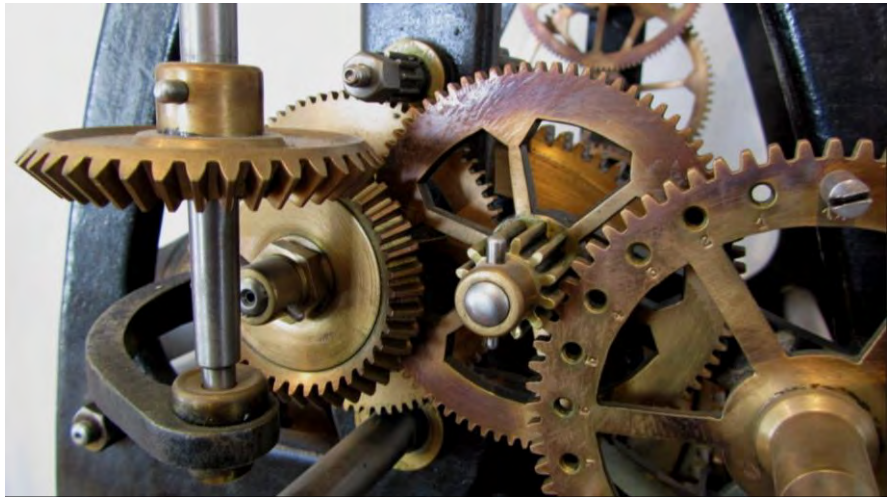
- Mutual Coupling of Performance Indices - Trade-Offs
- Counteracting Effects of Key Design Parameters




→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

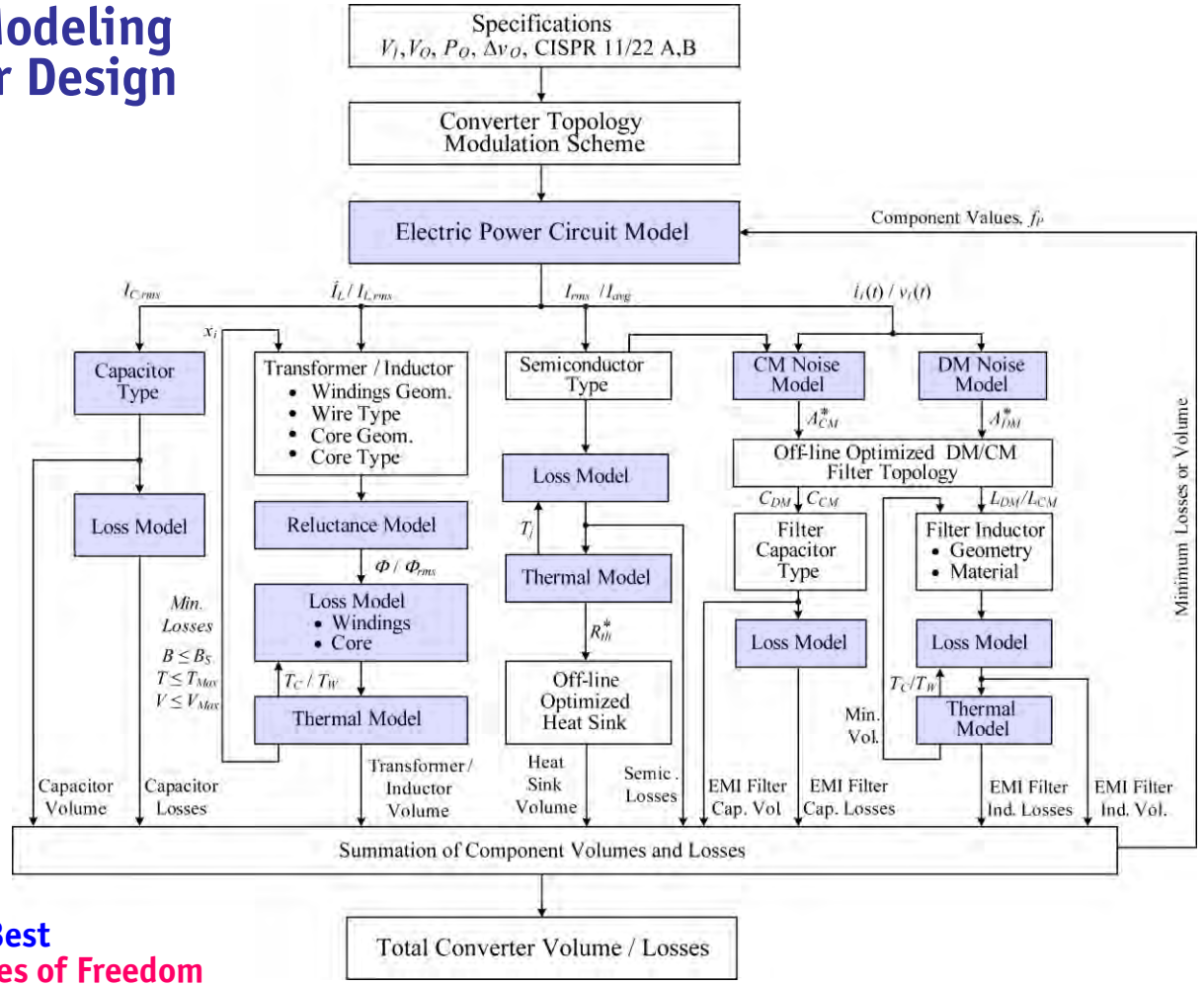
# Multi-Objective Design Challenge

- Mutual Coupling of Performance Indices / Trade-Offs
- Counteracting Effects of Key Design Parameters



→ Large Number of Degrees of Freedom / Multi-Dimensional Design Space
→ Full Utilization of Design Space only Guaranteed by Multi-Objective Optimization

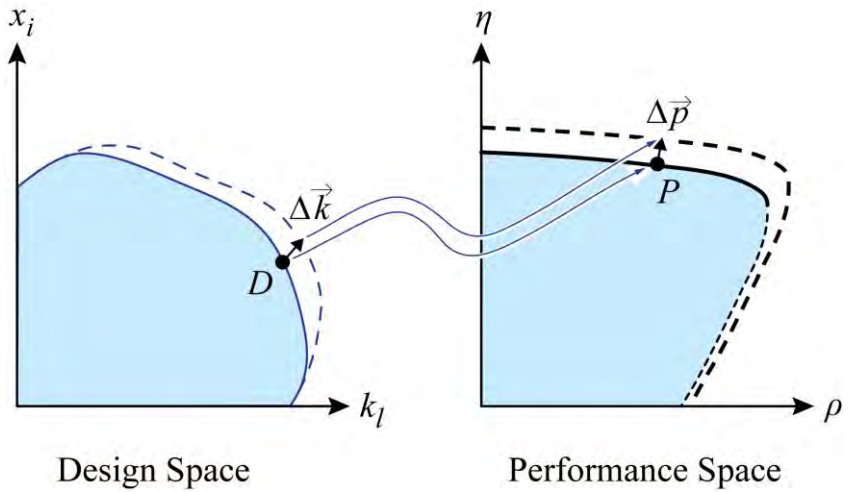
# Mathematical Modeling of the Converter Design

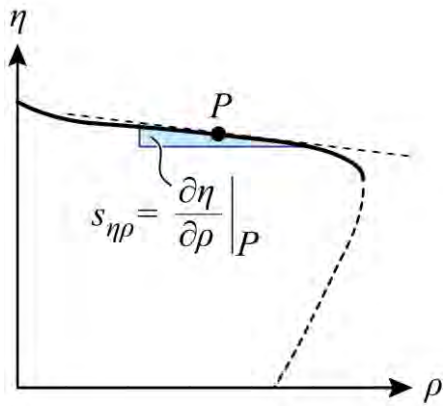



→ **Optimization Ensures Best Utilization of All Degrees of Freedom**

# Multi-Objective Optimization (1)

- Ensures Optimal Mapping of the "Design Space" into the "Performance Space"
- Identifies Absolute Performance Limits → Pareto Front / Surface

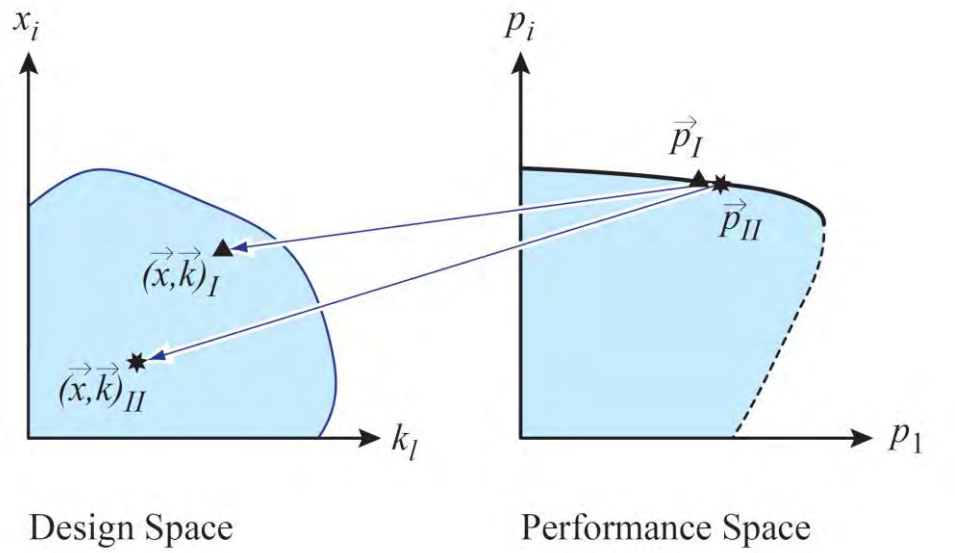



→ Sensitivities to Technology Advancements (Example: ηρ-Pareto Front)
→ Trade-off Analysis

# Multi-Objective Optimization (2)

- Mutual Compensation of Volume and Loss Contributions (e.g. Cond. vs. Sw. Losses)
- Equal Performance for Largely Different Sets of Design Parameters

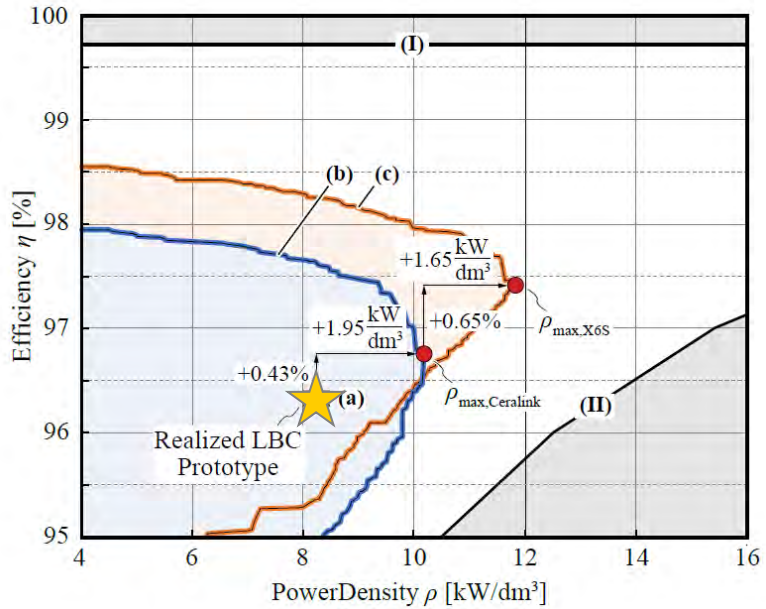



→ Design Space Diversity
→ Allows Optimization for Further Performance Index (e.g. Costs)

- ηρ-Optimization of Little Box 1.0 →

# Little Box 1.0 ηρ-Performance Limits

- Multi-Objective Optimization of Little-Box 1.0 (incl. CeraLink → X6S)
- Absolute Performance Limits (I) - DSP/FPGA Power Consumption
  (II) - Heatsink Volume @ (1-η)



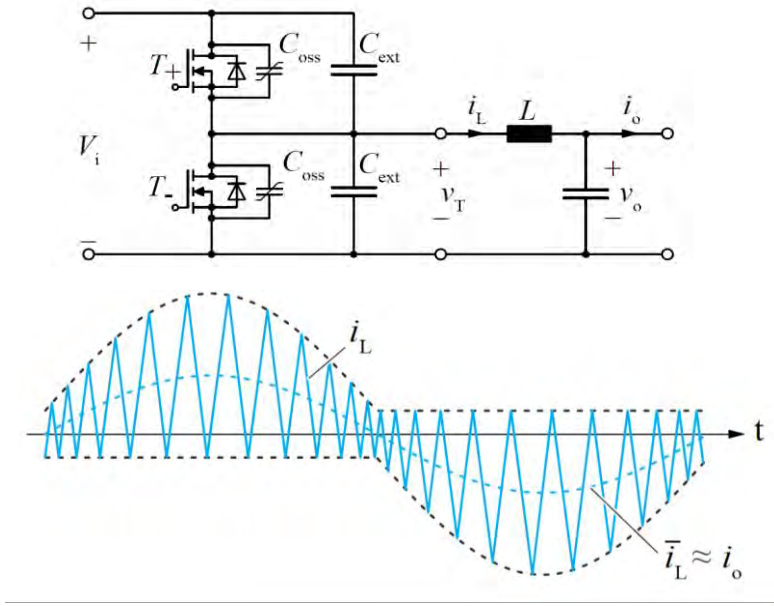

★ Realized Prototype

(b) Opt. for CeraLink Power Pulsation Buffer
(c) Opt. for X6S Power Pulsation Buffer

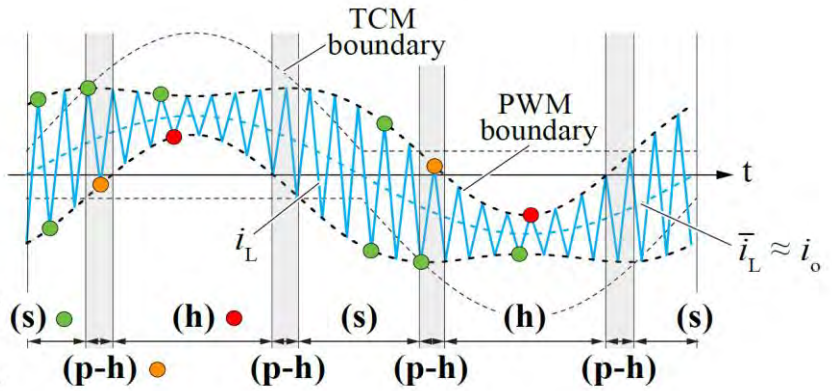
- Further Performance Improvement for Triangular Current Mode (TCM) → PWM

# Little Box 1.0 -- TCM → PWM

- Very High Sw. Frequency $f_S$ of TCM Around Current Zero Crossings
- Efficiency Reduction due to Remaining TCM Sw. Losses & Gate Drive Losses Reduction
- Wide $f_S$ -Variation Represents Adv. & Disadvantage for EMI Filter Design



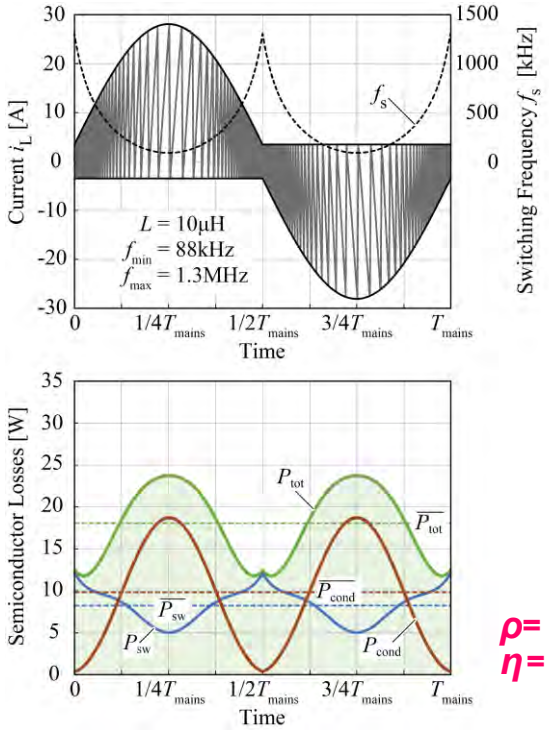

(s) Soft-Switching (ZVS)
(p-h) Partial Hard Switching
(h) Hard-Switching




- PWM -- Const. Sw. Frequency & Lower Conduction Losses
- PWM @ Large Current Rippel -- ZVS in Wide Intervals

# Little Box 1.0 -- TCM → PWM

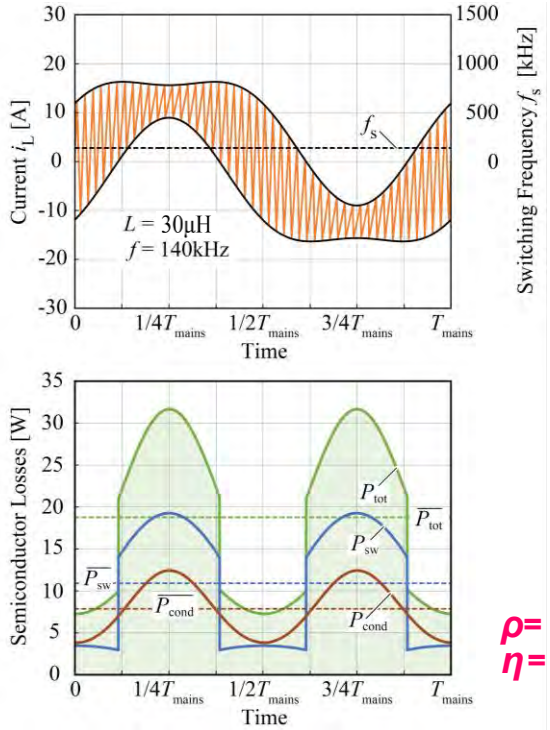
- Very High Sw. Frequency $f_S$ of TCM Around Current Zero Crossings
- Efficiency Reduction due to Remaining TCM Sw. Losses & Gate Drive Losses Reduction







$\rho$= 11.9kW/dm³
$\eta$= 97.4%







$\rho$= 12.5kW/dm³
$\eta$= 97.4%

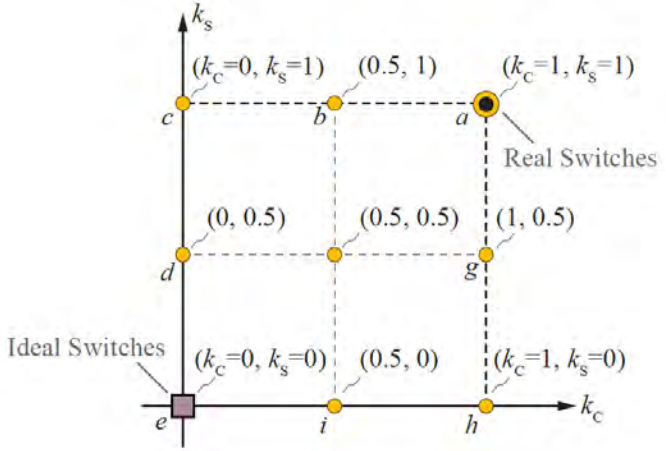
- PWM -- Slightly Higher Max. Power Density @ Same Efficiency

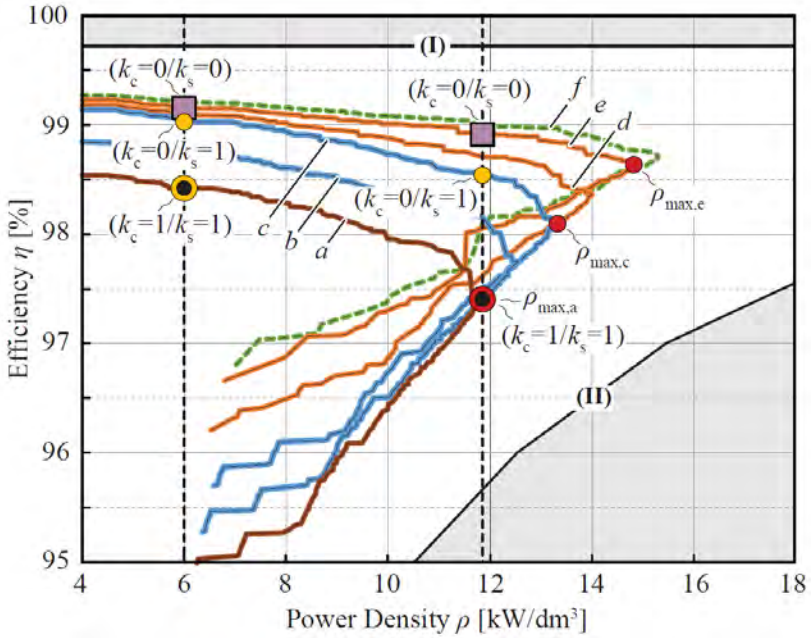
# $\eta\rho$-Pareto Limits for Ideal Switches

Zero Switching / Conduction Losses
TCM vs. PWM Modulation
Design Space Diversity

# Little Box 1.0 @ Ideal Switches

- Multi-Objective Optimization of Little-Box 1.0 (X6S Power Pulsation Buffer)
- Step-by-Step Idealization of the Power Transistors
- Ideal Switches: $k_C = 0$ (Zero Cond. Losses); $k_S = 0$ (Zero Sw. Losses)



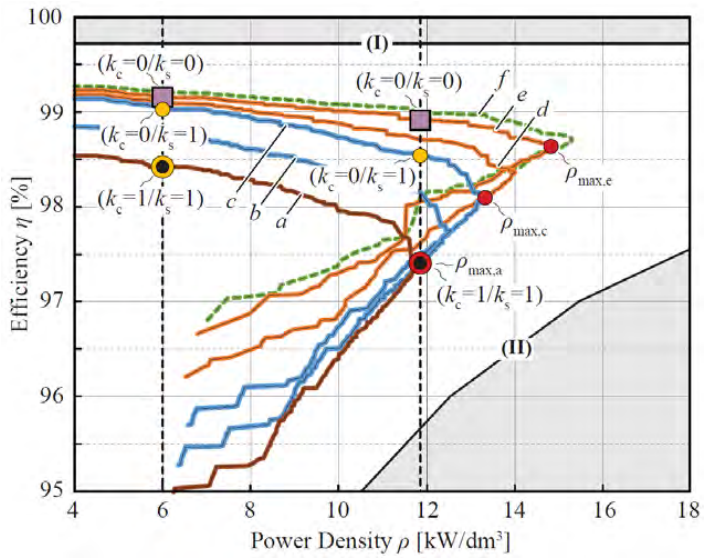



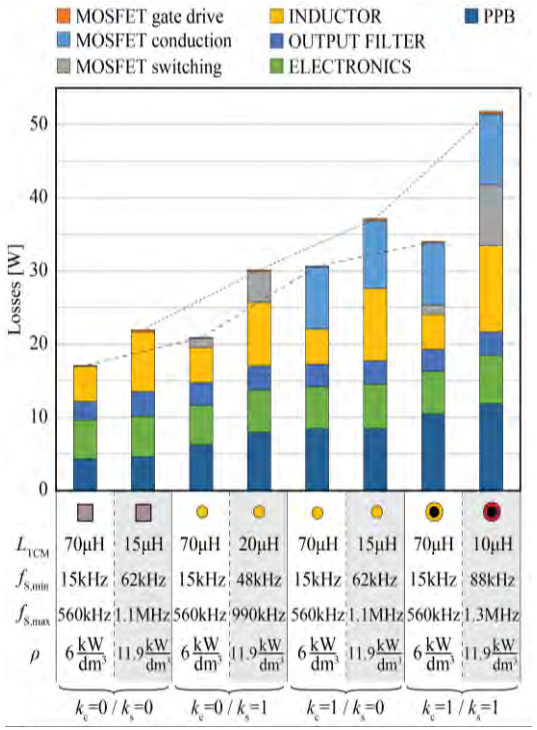

Zero Output Cap. and Zero Gate Drive Losses

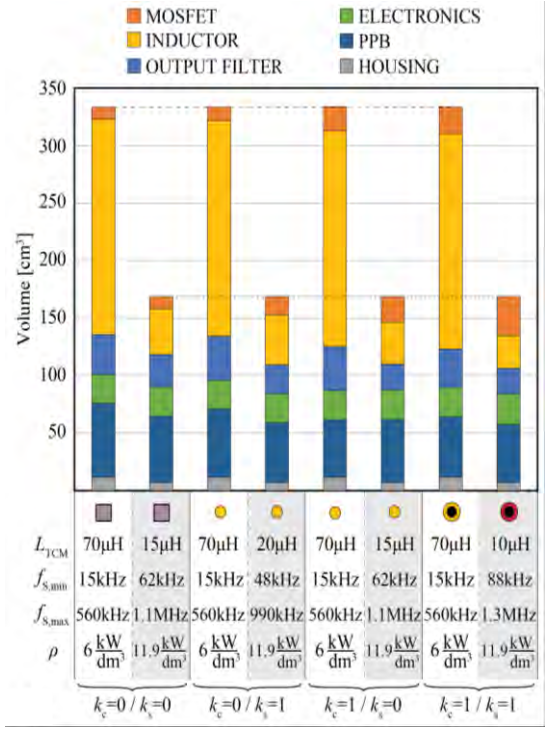
- Analysis of Improvement of Efficiency @ Given Power Density & Maximum Power Density

# Little Box 1.0 @ Ideal Switches -- TCM

- $\Delta\eta$= + 0.5% @ $\rho$= 6kW/dm³ – Main Benefit from Zero Conduction Losses ($k_C$=0)
- $\Delta\eta$= +1.5% @ $\rho$= 12kW/dm³ – Add. Benefit from Zero Sw. Losses ($k_S$=$k_C$=0)



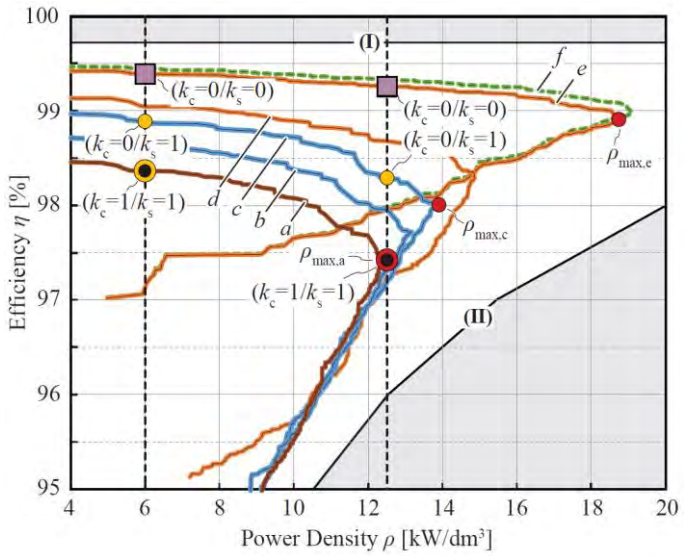



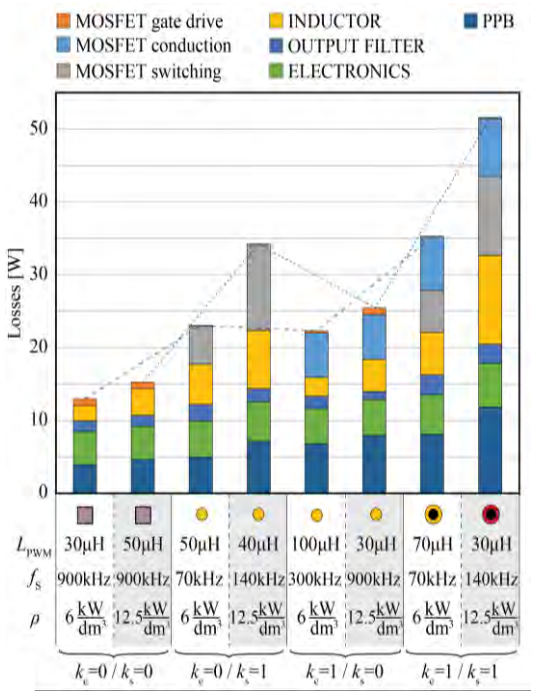



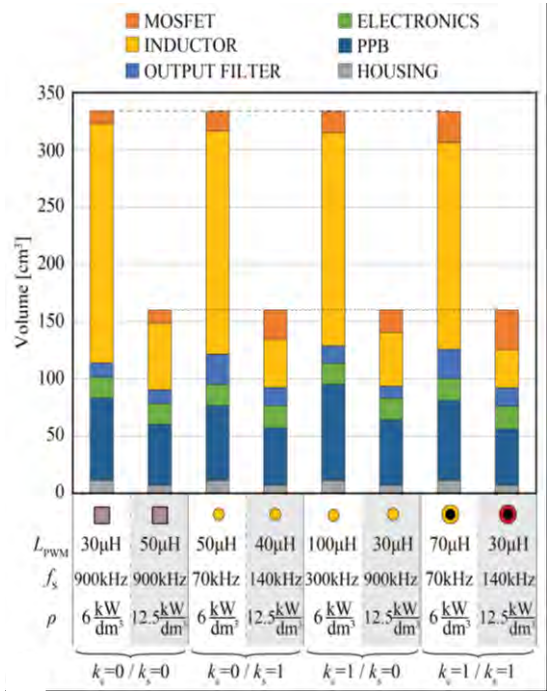

- Minor Improvement of Max. Power Density - $\rho$= 12kW/dm³ → 15kW/dm³ (PPB Cap. & Inductors)
- Finite Remaining Volume & Losses → The Ideal Switch is Not Enough (!)

# Little Box 1.0 @ Ideal Switches -- PWM

- $\Delta\eta$= + 1.0% @ $\rho$= 6kW/dm³ – Benefit from Zero Cond. & Zero Sw. Losses ($k_S$= $k_C$= 0)
- $\Delta\eta$= +1.75% @ $\rho$= 12kW/dm³ – Benefit from Zero Cond. & Zero Sw. Losses ($k_S$= $k_C$= 0)

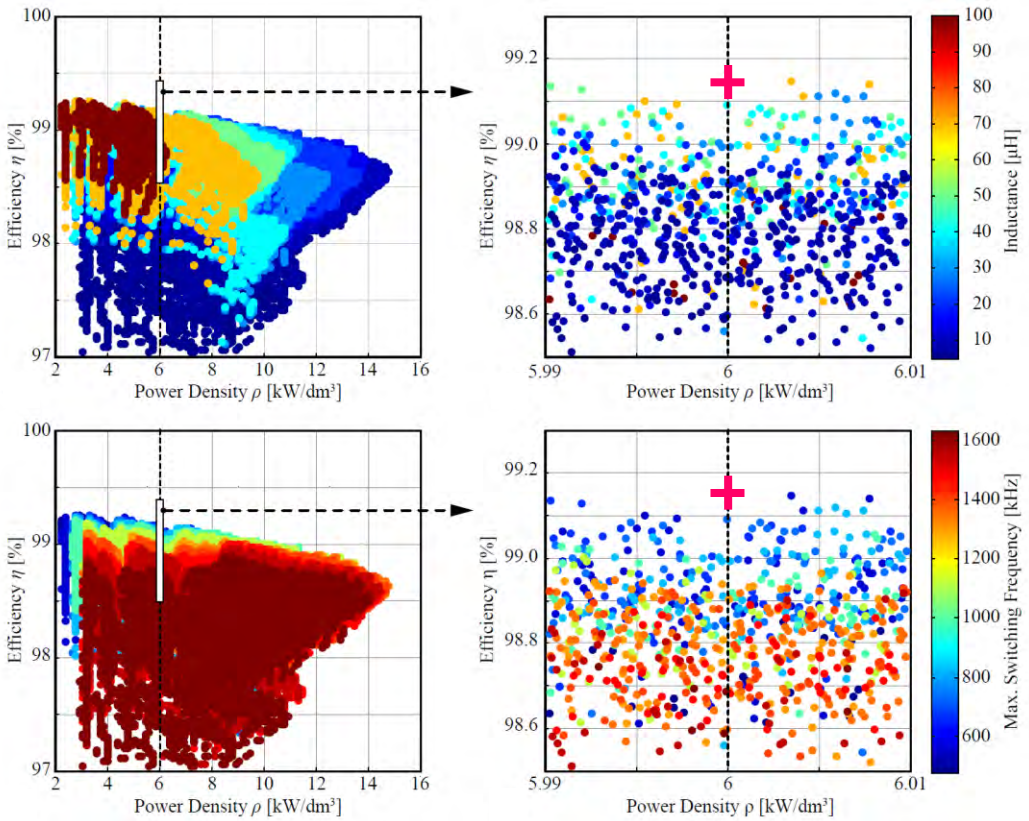



- 50% Improvement of Max. Power Density - $\rho$= 12kW/dm³ → 19kW/dm³ (PPB & Inductors)
- Finite Remaining Volume & Losses → The Ideal Switch is Not Enough (!)

# Little Box 1.0 @ Ideal Switches -- TCM

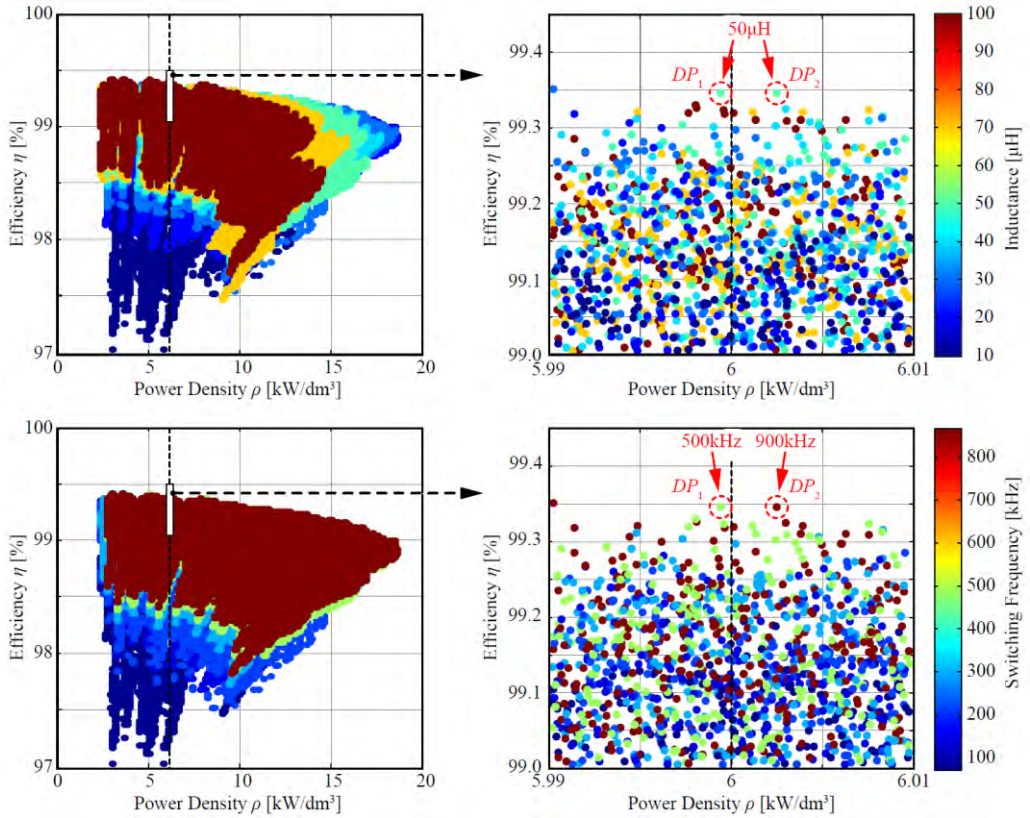



$\rho$= 6kW/dm³
$\eta \approx$ 99.15%

$L$ = 70uH
$f_S$= 15... 560kHz

- $L$ & $f_S$ Coupled Due to TCM Concept
- Limited Design Space Diversity

# Little Box 1.0 @ Ideal Switches -- PWM




$\rho$= 6kW/dm³
$\eta \approx$ 99.35%

$L$= 50uH (30uH)
$f_S$= 500kHz or 900kHz

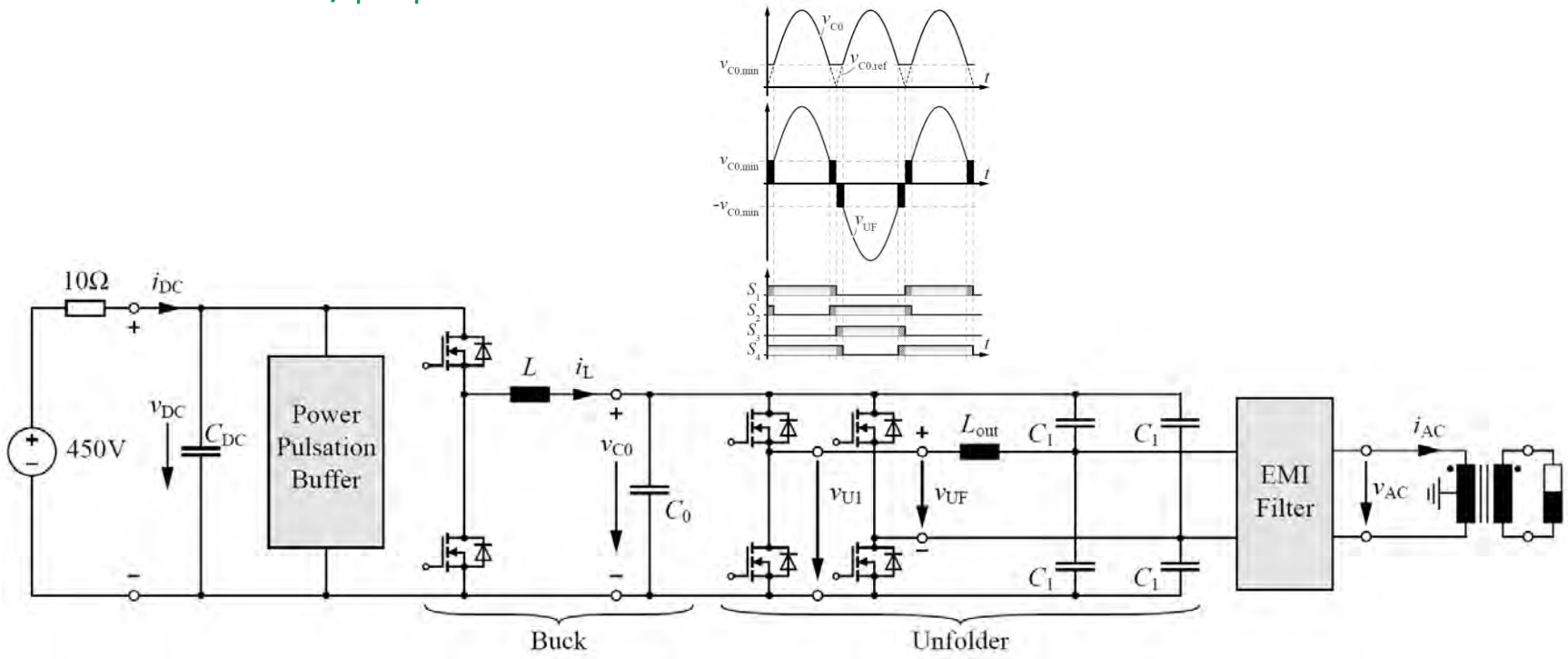
- $L$ & $f_S$ are Independent Variables
- Large Design Space Diversity (Mutual Compensation of HF and LF Loss Contributions)

# Little Box 2.0

DC/ | AC | Converter + Unfolder
PWM vs. TCM incl. Interleaving
ηρ-Pareto Limits for Non-Ideal Switches

# Little Box 2.0 – New Converter Topology

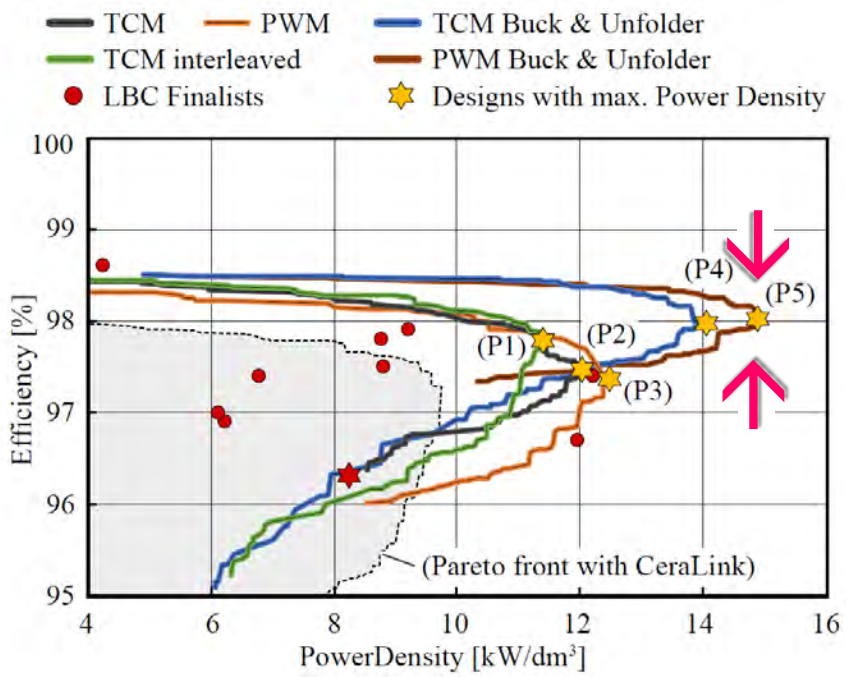
- New Converter Topology - DC/|AC|- Buck Converter + Unfolder
- 60Hz-Unfolder (Temporary PWM for Ensuring Continuous Current Control)
- TCM or PWM of DC/|AC|- Buck-Converter



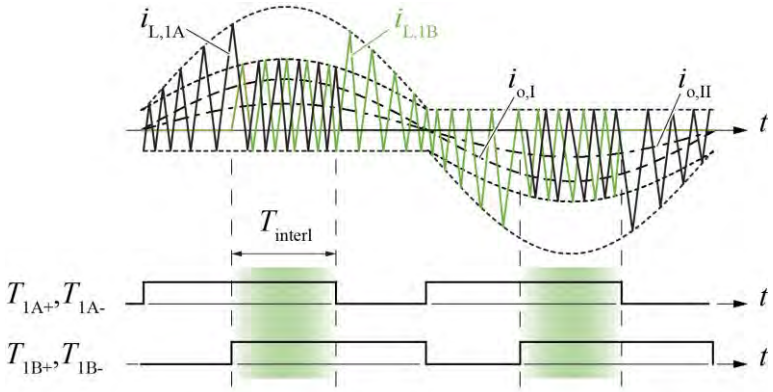

■ Full Optimization of All Converter Options for Real Switches / X6S Power Pulsation Buffer

# Little Box 2.0 – Multi-Objective Optimization

- DC/|AC|- Buck Converter + Unfolder & PWM Shows Best Performance
- Full-Bridge Employs 2 Switching Bridge Legs - Larger Volume & Losses
- Interleaving Not Advantageous – Lower Heatsink Volume but Larger Total Volume of Switches and Inductors

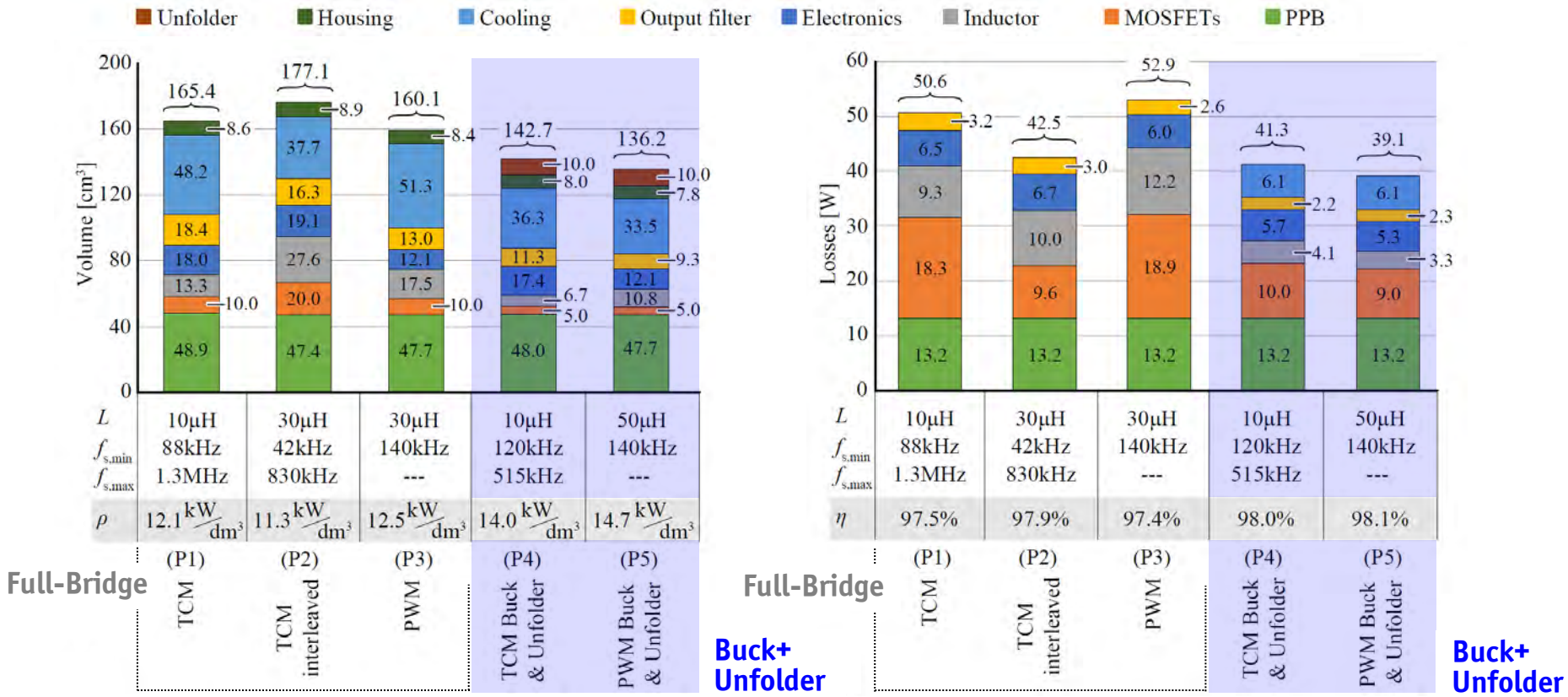



-- 4D-Interleaving Considered for TCM




- $\rho$= 250W/in³ (15kW/dm³) @ $\eta$= 98% Efficiency Achievable for Full Optimization

# Little Box 2.0 – Volume & Loss Distribution @ (P1...5)




- **Volume** Dominated by **Heatsink & PPB** (Power Pulsation Buffer)
- **Losses** for Buck+Unfolder Dominated by **Switches & PPB**

# Little Box 3.0

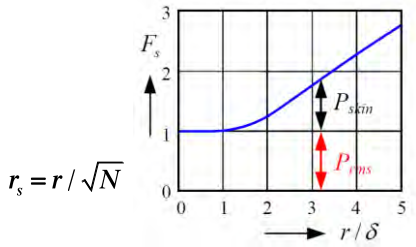
5...10MHz Switching Frequency
Performance of Low-μ HF Magnetic Materials
Electrolytic Caps vs. Power Pulsation Buffer

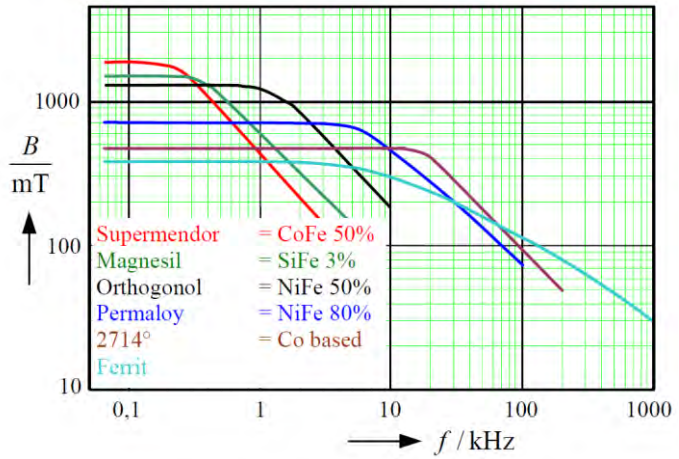
# ▶ Magnetics Operation Frequency Limit (1)

- **Serious Limitation of Operating Frequency by HF Losses**

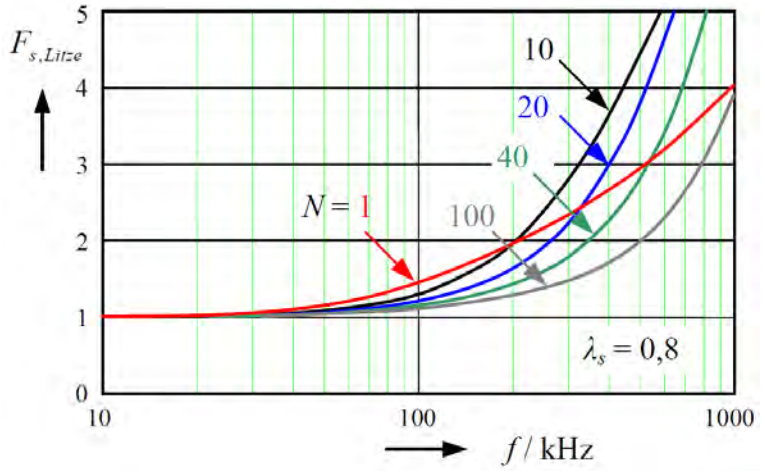
Source: Prof. Albach, 2011

— Core Losses (incr. @ High Frequ. & High Operating Temp.)
— Temp. Dependent Lifetime of the Core
— Skin-Effect Losses
— Proximity Effect Losses




■ Adm. Flux Density for given Loss Density

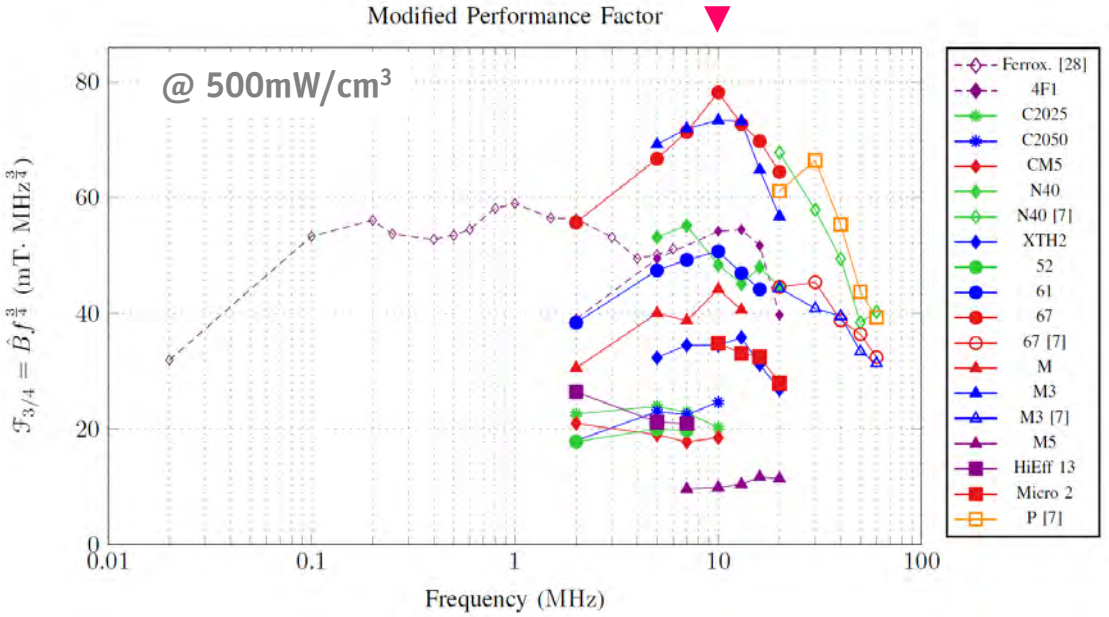


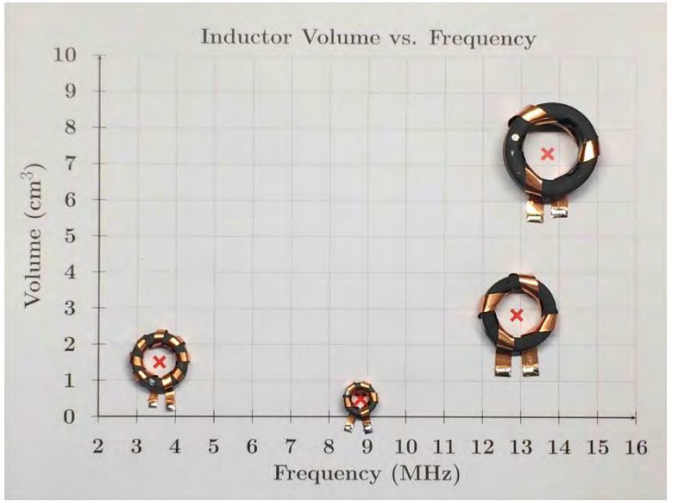

■ Skin-Factor $F_s$ for Litz Wires with $N$ Strands

# ▶ Magnetics Operating Frequency Limit (2)

- (Modified) "Core Material Perform. Factor" $F_{0.75} = B_{pk} \cdot f^{0.75}$ Defined for Def. Core Loss
- Performance Factor prop. to VA Handling Capability – Min. Vol. @ Max. of $F_{0.75}$
- Little Benefit of Increased $f_S$ for Conv. Ferrites in 200kHz...2MHz
- Peak Performance of Low-μ HF Core Materials @ 5-10 MHz

Source: Hanson et al. / ECCE 2015



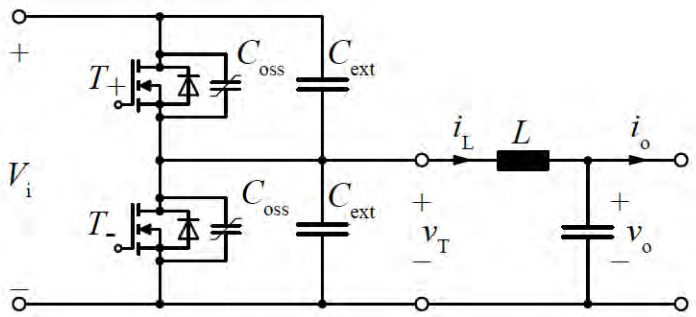



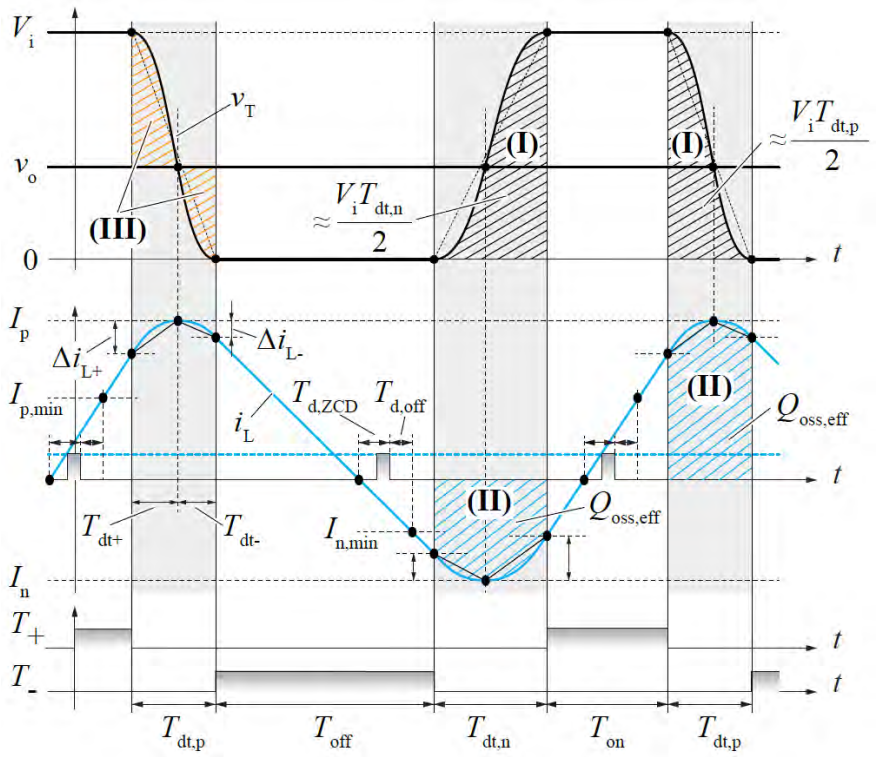

-- Fair-Rite 67 ($\mu_r$=40)
All Inductors w. $Q$= 200

■ $f_S$ in the MHz-Range Results in Very Low EMI Filter Volume

# TCM Digital Control / Timing Challenges @ $f_S$ > 1MHz

- Dead Times Required for Res. Transition (ZVS)
- $i$ = 0 Detection Time Delay
- Signal Isolator & Gate Drive Time Delays
- Rel. Large Cond. Losses @ Low Output Current

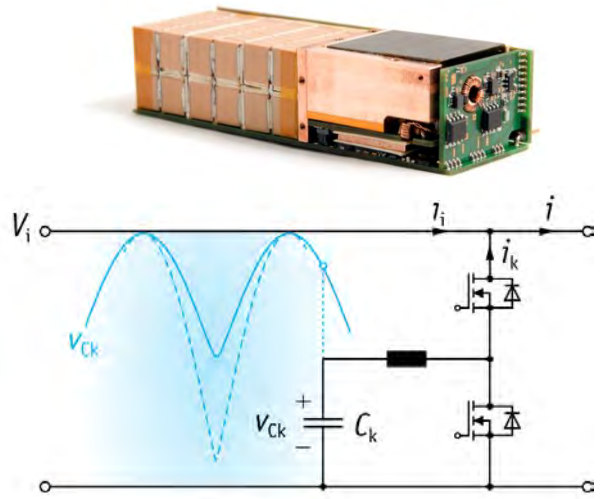


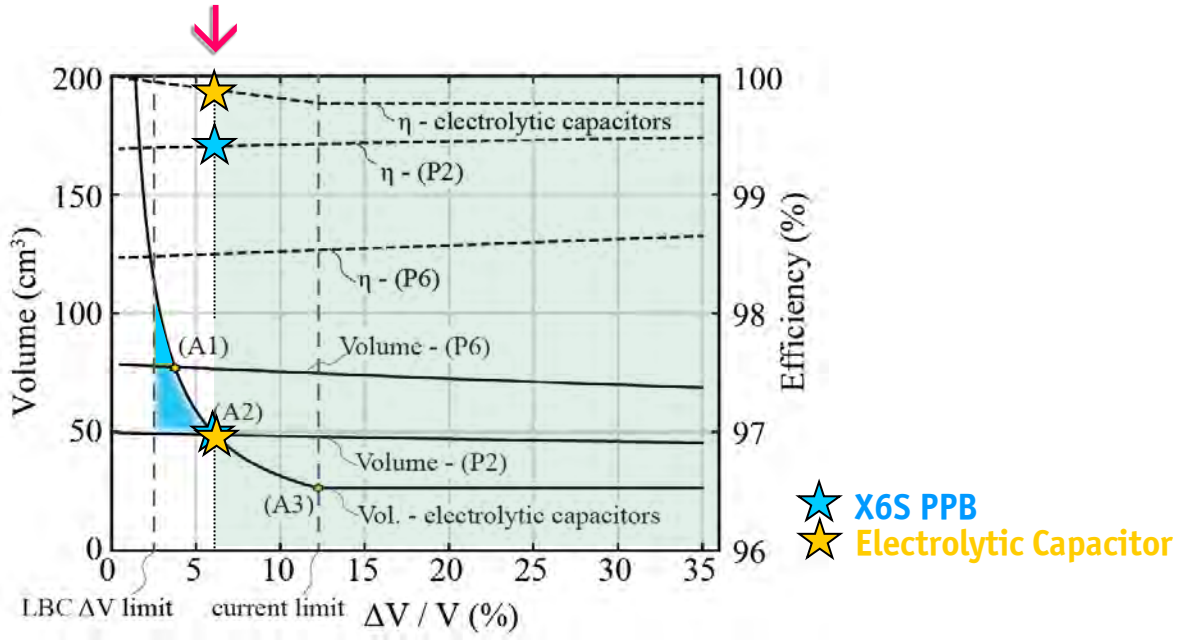




- New High Speed / Low-Volume / Low-Loss $i$= 0 Detection Concepts Required
- Integrated Gate Drive w. (Hysteresis) Current Control Functionality Required

# Power Pulsation Buffer (PPB) vs. Electrolytic Capacitor

- Lower Volume Comp. to Electrolytic Cap. only for $\Delta V/V < 6\%$
- No Efficiency Benefit of PPB (!)

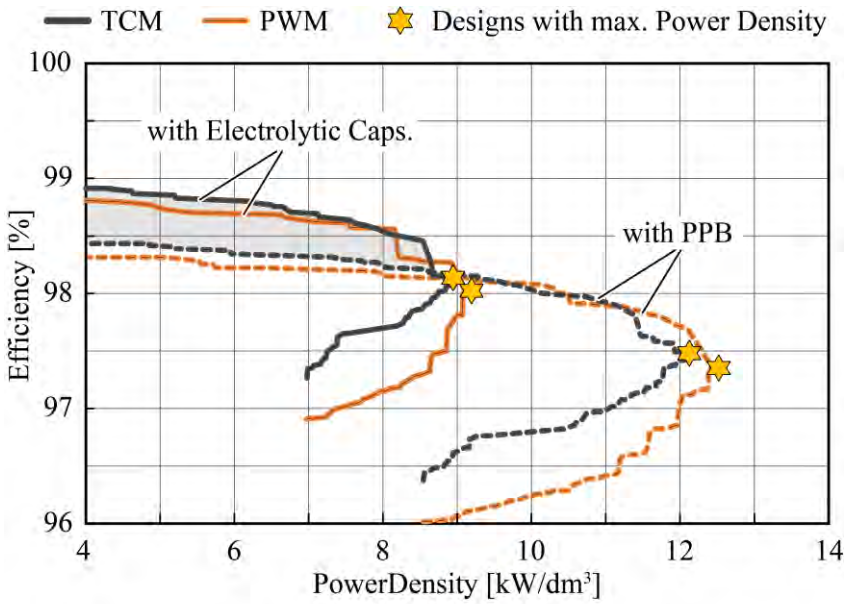



- Electrolytic Capacitors Favorable for High Efficiency @ Moderate Power Density
- E.g. for PFC Rectifiers where Large $\Delta V/V$ is Accpetable – Lower Volume & Lower Losses of Electrolytic Capacitors

# Power Pulsation Buffer (PPB) vs. Electrolytic Capacitor

- Analysis for Google Little Box Challenge Specification $\Delta V/V < 3\%$
- Efficiency Benefit of PPB only for $\rho > 9 kW/dm^3$




- Electrolytic Cap. Favorable for High Efficiency @ Moderate Power Density ($\Delta\eta$= +0.5%)
- E.g. for PFC Rectifiers where Large $\Delta V/V$ is Accpetable – Lower Volume & Lower Losses of Electrolytic Caps (!)

# Conclusions

## The “Ideal Switch" is Not Enough (!)

# Conclusions

- The "Ideal Switch" is NOT Enough - Unfortunately (!)
- "Great Wall" Defined by Magnetics @ 5...10GHz*W (for >10kW & High Efficiency)

→ Research on
* HF Magnetics
* 3D-Heat Management
* Digital Control Circuits
* High Bandwidth Sensors
* Integr. Intellig. Gate Drives
* 3D-Packaging / Integration

→ Alternative
* Multi-Cell Concepts

# Thank You !