Power Electronic Systems
Laboratory

Proceedings of the IEEE Energy Conversion Congress & Expo (ECCE USA 2015), Montreal, Canada, September 20-24, 2015

New Boundary Mode Sinusoidal Input Current Control of the VIENNA Rectifier

M. Leibl,
M. Darani,
J. Deuringer,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

New Boundary Mode Sinusoidal Input Current Control of the VIENNA Rectifier

Michael Leibl, Moreno Darani and Johann W. Kolar
Power Electronic Systems Laboratory
Swiss Federal Institute of Technology
8092 Zurich, Switzerland

Josef Deuringer
Clinical Products Division
Siemens Healthcare GmbH
91054 Erlangen, Germany

***Abstract*—In hard switching boost-type or buck-type three-phase power factor corrected rectifier systems the turn-on losses in continuous conduction mode (CCM) are usually higher than the turn-off losses. This is mainly caused by the reverse recovery effect of the freewheeling diode. The reverse recovery related turn-on losses however may be eliminated if the converter is operated in boundary conduction mode (BCM), i.e. at the boundary of discontinuous conduction mode (DCM) and CCM. This paper shows that the Vienna Rectifier (VR) can be operated in BCM with zero current turn-on and that the reverse recovery current of the freewheeling diodes can be used to achieve partial zero voltage switching (ZVS). The principle of three-phase, three-level BCM control is described using space vectors, the effect of the variable switching frequency on the design of the input filter is investigated in detail and dimensioning criteria for the filter elements as well as the semiconductors are given. A current slope detector circuit using auxiliary windings on the input boost inductors is proposed for turning on the switches at minimum voltage. Further, a method to compensate the delay caused by the freewheeling diode reverse recovery time and an efficient implementation of the modulation with FPGAs using a quadratic counter is proposed. The proposed control scheme is finally experimentally verified on a hardware prototype.**

I. Introduction

The switching frequency of three-phase boost-type PFC rectifier systems in continuous conduction mode (CCM) is significantly limited by the reverse recovery losses of the free-wheeling diodes. In order to obtain switching frequencies in the 100 kHz range, the use of Schottky-barrier Silicon Carbide (SB SiC) diodes is inevitable at DC-link voltages of 400 V or more. However, in discontinuous conduction mode (DCM), the transistor can be turned on at zero current, but in general no zero voltage turn-on is present, if the diode exhibits no reverse recovery effect. In order to minimize peak and RMS values in DCM the switching frequency may be varied such that the converter is always operating at the boundary of CCM and DCM, also referred to as boundary conduction mode (BCM). If instead of the freewheeling diode a second switch (synchronous rectifier) is used, zero voltage switching (ZVS) can be achieved by actively driving the current to a small negative peak value which is sufficient to discharge the transistors output capacitance. This mode is often referred to as triangular current mode (TCM) [1]. Alternatively TCM may also be obtained passively if the free-wheeling diode provides sufficient reverse recovery current to achieve ZVS. The disadvantages of TCM compared to CCM, including higher peak and higher RMS current are often reported to be compensated by the smaller inductance value, the reduced switching losses and lower electro-magnetic emission due to the soft switching transition [2]. In fact the energy which is stored in the inductor is minimized if the inductor value is selected such that BCM (TCM) occurs. Using multi-phase interleaved topologies, the size of the converter EMI input filter and output capacitor can be further reduced and highly efficient as well as highly compact designs are obtained [3]. For operation in TCM, usually synchronous rectification is applied in order to obtain highest efficiencies. However for applications that require only short periods of full power operation, the overall power converter material costs are typically of more concern than the energy conversion efficiency. In this case one would rather use free-wheeling diodes and utilize the reverse recovery current to obtain partial ZVS [4].

Three-phase three-level rectifiers, often referred to as Vienna Rectifier (VR), are usually operated in CCM. Switching frequencies of up to 1 MHz have been achieved using Si MOSFETs and SB SiC diodes [5]. However, operation in DCM with sinusoidal input currents is also possible and has been applied in order to reduce the total harmonic distortion (THD) of the input currents at light load [6]. By operating the rectifier at the boundary of DCM and CCM, zero voltage turn-on of the power transistors can be obtained in case conventional Si freewheeling diodes with sufficient reverse recovery current are employed, i.e. switching frequencies in the 100 kHz range are possible without the need for SB SiC diodes. A a further advantage of BCM (TCM) control no high bandwidth current sensors are necessary, instead only the current zero crossings have to be detected.

In this paper the variable frequency BCM control scheme of the VR is introduced, analyzed and experimentally demonstrated on a prototype. Dimensioning criteria for semiconductors and filter components are derived and the hardware implementation of the controller using a quadratic counter and an auxiliary winding for zero-voltage detection at turn-on is described. Experiments confirm that partial ZVS can be obtained by utilizing the freewheeling diode reverse recovery current and that the proposed compensation of the reverse recovery delay significantly reduces input current distortions.

II. Boundary Conduction Mode Control

In order to obtain sinusoidal input currents when operating the VR in DCM a special modulation scheme has to be used which has been outlined in detail [6]. The basic principle of this control scheme is briefly reviewed in the following and the operation in BCM is introduced.

978-1-4673-7151-3/15/$31.00

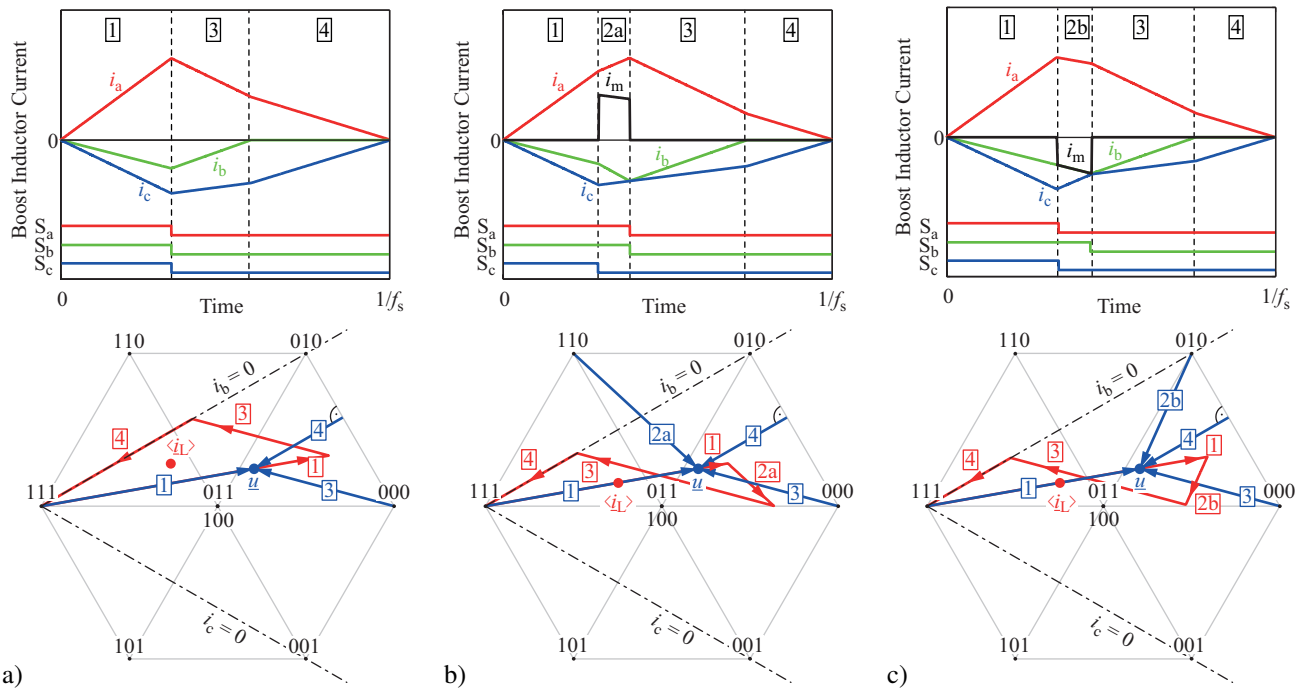

Fig. 2. Boost inductor currents in BCM during one switching period for $u_a > 0 > u_b > u_c$. Each situation is shown in time domain as well as in a space vector diagram. In time domain additionally the current i_m which is flowing into the midpoint and the gate signals are shown. In the space vector diagrams (α,β plane) the phase voltage vector and the vector of the local average of the phase currents are indicated. For each occurring state, the sections of the current vector trajectory are shown in red and the boost inductor voltage space vector is shown in blue. Synchronously switching all the three switches as shown in (a) leads to a local average value of the current which is not in phase with the voltage. Introducing an additional state 2a as shown in (b) allows to regain resistive fundamental behaviour by rotating the current local average value. Also state 2b allows resistive behaviour but the sign of the current flowing into the midpoint is opposite compared to state 2a.

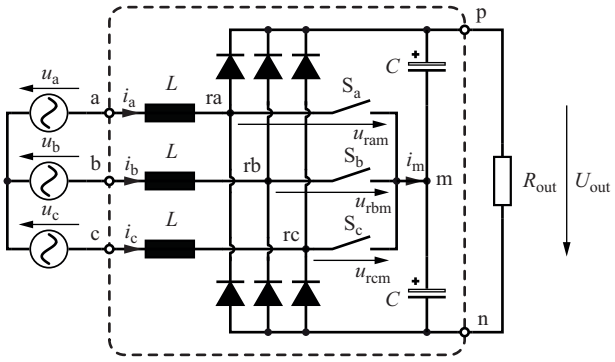

Fig. 1. Basic power circuit of the VR. Three bidirectional switches S_a, S_b, S_c allow to connect each phase to the DC-link midpoint, six diodes conduct the currents during the free-wheeling states to the positive or negative DC-link rail, depending on the current direction.

A. BCM Control Principle

For the analysis of the BCM control scheme, a simplified circuit of the VR as shown in Fig. 1 is considered. When operating in DCM, the boost inductor currents are zero at the beginning of each switching period. The switching period always starts by turning on all the three switches S_a, S_b, S_c simultaneously. During this switching state 1 the boost inductor currents are rising at rates proportional to the corresponding phase voltages. If the switches are also turned off simultaneously the three currents commutate to the according freewheeling diodes and therefore start to decrease (state 3). The current of the phase with the smallest absolute voltage value reaches zero first, leaving only two diodes conducting (state 4). The boost inductor currents during one such switching cycle for $u_a > 0 > u_b > u_c$ (mains voltage phase angle of $\varphi = 10°$ with $u_a = \hat{u}\cos(\varphi)$, $u_b = \hat{u}\cos(\varphi - 120°)$, $u_c = \hat{u}\cos(\varphi - 240°)$) are illustrated in Fig. 2a.

Aiming for a clear representation, space vectors can be used to describe the situation [7]. Phase quantities a,b,c are simply transformed into a space vector (which has α,β coordinates) using $\underline{a} = \exp(j\frac{2\pi}{3})$ and $\underline{u} = u_\alpha + ju_\beta = \frac{2}{3}(u_a + \underline{a}u_b + \underline{a}^2 u_c)$. If the voltage space vector which the active rectifier stage applies is $\underline{u}_r$ and the mains voltage space vector is $\underline{u}$, the resulting rate of change of the boost inductor current space vector is $\frac{d\underline{i}_L}{dt} = \frac{1}{L}(\underline{u} - \underline{u}_r)$.
Therefore, in the simple case that the rectifier is operating with all switches being synchronously turned on and off, the current trajectory starts at the origin and extends into the direction of the mains voltage space vector during state 1. At the moment the switches are turned off the current trajectory changes into the direction of $\underline{u} - \underline{u}_{r,000}$ during state 3. The zero levels of the phase currents are marked with dash-dotted lines in Fig. 2a. As soon as the current trajectory hits such a line, the resulting voltage space vector extends the trajectory along the current-zero line back to the origin (state 4). It is obvious that the average value of the boost inductor current space vector over one switching period (local average value) lies somewhere within the area enclosed by its trajectory which describes a triangle. Since one side of the triangle is aligned to the mains voltage the local average value of the current either is leading or lagging the mains voltage space vector if the switches are synchronously turned off and therefore distorted input currents result after low pass filtering. In order to rotate the local average current space vector such that it lies in phase with the voltage space vector

one has to apply at least one additional switching state. The six additional space vectors that could be inserted between state 1 and state 3 are $\underline{u}_{r,001}$, $\underline{u}_{r,010}$, $\underline{u}_{r,011}$, $\underline{u}_{r,100}$, $\underline{u}_{r,101}$, $\underline{u}_{r,110}$. The space vector diagram clearly shows that for the described condition only two rectifier voltage space vectors can be used to change the angle of the local average current space vector into the right direction. If a new state 2a during which $\underline{u}_{r,110}$ is applied is inserted between states 1 and 3 the local average of the current space vector can be aligned with the voltage space vector as it is shown in the space vector diagram in Fig. 2b. The waveforms of the boost inductor currents for this situation are also shown in Fig. 2b. It is important to note that during state 2a a positive current is flowing into the midpoint of the DC-link. In order to allow active balancing of the two DC-link voltages the second feasible state 2b can be applied alternatively. As shown in the space vector diagram in Fig. 2c the space vector $\underline{u}_{r,010}$ applied during state 2b also allows to align the local average current space vector with the mains voltage space vector. In this case, as indicated in the current waveform diagram a negative midpoint current occurs. It is pointed out that BCM actually only occurs in two phases, the current in the phase with lowest phase voltage absolute value is discontinuous.

B. Calculation of the Duty Times of the Switches

In order to maintain resistive mains behaviour as outlined in the previous section, the necessary durations of states 1,2a and 2b have to be calculated by the current controller, depending on the phase voltages, the DC-link voltage and the required input conductance to be emulated for the mains which is defined by the voltage controller as it determines the power delivered to the DC side. In the previous section it is assumed that $u_\mathrm{a} > 0 > u_\mathrm{b} > u_\mathrm{c}$. Since the VR topology exhibits bridge symmetry, i.e. same behaviour for positive and negative currents, the same considerations also apply to the situation when $u_\mathrm{a} < 0 < u_\mathrm{b} < u_\mathrm{c}$. Taking into account the phase symmetry, i.e. all phases feature the same circuit topology, all permutations of the phases a,b,c are also covered. In fact, if the three mains voltages are sorted by their absolute values and the subscript keywords *max*, *mid* and *min* are assigned to all phase quantities instead of a,b and c such that

$$|u_\mathrm{max}| > |u_\mathrm{mid}| > |u_\mathrm{min}| \tag{1}$$

one can calculate the according switch duty times T_max, T_mid and T_min for resistive mains behaviour according to the equations given in Tab. I for any time in the mains period. In order to balance the DC-link voltages the correct pattern a or b has to be selected as also indicated in Tab. I. The relative duty cycles d_1a, d_2a, d_1b and d_2b are calculated as functions of the instantaneous modulation indices

$$m_\mathrm{max} = \frac{2\,|u_\mathrm{max}|}{U_\mathrm{out}}, m_\mathrm{min} = \frac{2\,|u_\mathrm{min}|}{U_\mathrm{out}}. \tag{2}$$

using the expressions given in [6]. The inductance L is the value of the boost inductors, G the value of conductance emulated for the mains and T_s the switching period.
In BCM the switching frequency is varying such that the rectifier is always operating in boundary conduction mode, i.e. state 4 is immediately followed by state 1. The resulting switching period time in BCM is exactly specified for switching pattern b by the equation

$$T_\mathrm{s,b} = \frac{4GL}{2 - 2m_\mathrm{max} + m_\mathrm{min}}. \tag{3}$$

If pattern a is used, the resulting expression for the switching period is too complex to be shown here. It could be either stored in a look-up table or approximated using the expression for pattern b with a maximum error of less than 4 %. For low load, i.e. low conductance G, the switching period is short and therefore the switching frequency is high. For practical implementation one needs to limit the switching frequency, which can be realized by limiting T_s to a lower limit $T_\mathrm{s,min} = \frac{1}{f_\mathrm{s,max}}$. If the switching frequency is limited the rectifier is no longer operating in BCM and enters DCM.

TABLE I. SWITCH DUTY TIME CALCULATION

$u_\mathrm{out,p} > u_\mathrm{out,n}$	True	False	True	False
$u_\mathrm{min} > 0$	False	True	True	False
T_max	$\sqrt{LGT_\mathrm{s}}(d_\mathrm{1a} + d_\mathrm{2a})$		$\sqrt{LGT_\mathrm{s}}(d_\mathrm{1b} + d_\mathrm{2b})$	
T_mid	$\sqrt{LGT_\mathrm{s}}d_\mathrm{1a}$		$\sqrt{LGT_\mathrm{s}}d_\mathrm{1b}$	
T_min	$\sqrt{LGT_\mathrm{s}}(d_\mathrm{1a} + d_\mathrm{2a})$		$\sqrt{LGT_\mathrm{s}}d_\mathrm{1b}$	

C. Circuit Simulation

The boundary conduction mode control is verified by simulating the circuit in Fig. 1, assuming ideal switches and diodes. The line-to-line mains rms voltage is set to 400 V, the total output voltage is 800 V, the power is 10 kW and the value of the boost inductance is set to 5 μH. The duty cycles are calculated using four look-up tables holding 12×7 values each. The duty cycles are recalculated for each switching cycle and depending on which partial DC-link voltage is higher the according pattern a or b is selected. The switches are only turned on at zero current, therefore a new switching period is only started as soon as all three phase currents are zero.

1) Ideal Conditions: Under ideal conditions as shown in Fig. 1 the switching period T_s for pattern b is approximately described by (3). Based on that, the turn-on times are calculated using the expressions in Tab. I. The resulting waveform of the current in the boost inductor of one phase, i_a, is shown in Fig. 3. The local average of the current $\langle i_\mathrm{a} \rangle$ clearly shows sinusoidal shape. The calculated THD of the local average of the current is 0.5 % and the RMS value of the boost inductor current is 1.17 times higher than the RMS value of its local average. The simulated switching period time is compared to the value calculated with (3). Although the equation is only exact for pattern B, no significant error is observed for pattern A.

2) Effect of Common Mode (CM) Current: In the real circuit there is always a path for CM current to flow, such as the CM capacitors of the EMI filter (Fig. 6) or the ground capacitance of the load. Adding a CM filter as shown in Fig. 6 providing a CM path to the circuit simulation results in an input current waveform as shown in Fig. 4. There is a visible low frequency distortion of the input current that results in a THD of 3.43 %. As can be seen in the close-up view in Fig. 4 the current which is flowing through the CM path of the filter increases the period time. Therefore the simulated period time no longer equals the one calculated with (3) and the duty times calculated with the equations in Tab. I do not result in the desired current average value. Because of the delays, also the

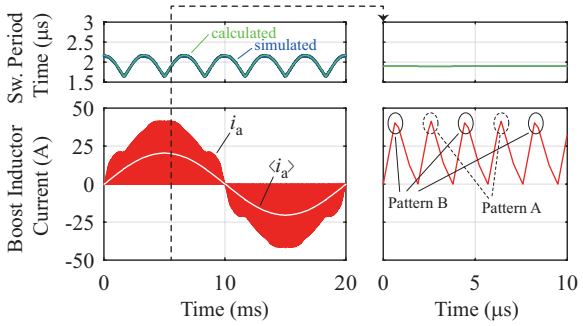

Fig. 3. Simulated waveform of a phase current, i_a, in the boost inductor and comparison of the predicted and the measured length of the switching period. The close-up at a mains voltage angle of $\varphi = 10°$ reveals the two different current shapes of pattern a and b which are applied to balance the DC link voltages. The measured length of the switching period varies with six times the mains frequency and shows only a negligible difference compared to the predicted value. The total harmonic distortion (THD) of the local average of the boost inductor current $\langle i_a \rangle$ is 0.5 % and the boost inductor RMS value is 1.17 times the RMS value of its local average.

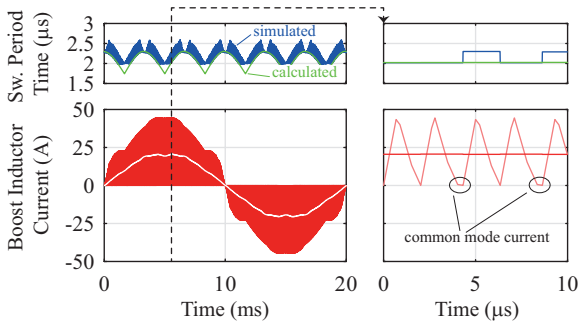

Fig. 4. Simulated waveform of a phase current, i_a, in the boost inductor and comparison of the predicted and the measured length of the switching period with a CM filter with capacitive connection to the DC-link midpoint. The common mode current causes delays which result in low frequency current distortions. The simulated switching period time shows considerable fluctuations and deviates from the calculated switching period time. The THD of the local average of the boost inductor current $\langle i_a \rangle$ is 3.43 % and the boost inductor RMS value is 1.2 times the RMS value of its local average.

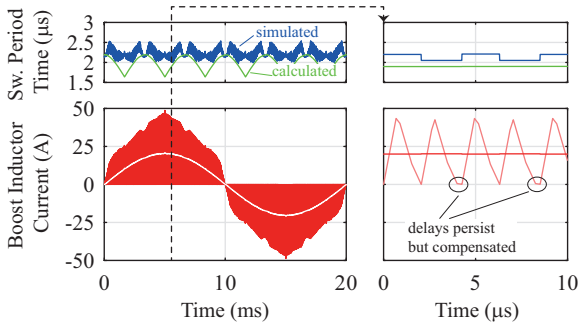

Fig. 5. Simulated waveform of a phase current, i_a, in the boost inductor and comparison of the predicted and the measured length of the switching period with CM filter and delay compensation. The delays introduced by the common mode current remain but their effect is compensated by a slightly higher peak current in the following switching period. The THD of the local average of the boost inductor current $\langle i_a \rangle$ is 0.59 % and the boost inductor RMS value is 1.2 times the RMS value of its local average.

ratio of boost inductor RMS current to input current is 1.2 and slightly higher than in the ideal case. If the switches would be simply turned on after the calculated period time while the CM current is still flowing, the CM current would increase period by period and eventually saturate the CM inductor. Therefore, the delay can not be avoided. An additional delay is introduced by the reverse recovery time of the freewheeling diode. In order to obtain zero current and partial zero voltage turn-on the moment when the freewheeling diode stops conducting has to be detected. Therefore, the reverse recovery time also increases the period time compared to the value calculated with (3).
A convenient way to avoid current distortions introduced by non-predictable delays is to measure the duration of the last switching period and use this value to calculate the duty times for the next period, instead of the calculated period. This way the charge which is transferred in one switching cycle always results in the right average current when related to the previous switching period. As a positive side-effect the inaccuracy introduced by using the same equation for the calculation of the length of the switching period for both patterns a and b is eliminated. The boost inductor current of the rectifier with common mode filter and delay compensation enabled is shown in Fig. 5. The THD is reduced to a value of 0.59 %, the ratio of boost inductor current RMS value to input current RMS value is still 1.2, since the delays are compensated but not eliminated. It is pointed out that in practice delays also occur because of the freewheeling diode's reverse recovery and because of delays in the control system, therefore delay compensation is crucial for reaching low THD.

III. Hardware Implementation

A. Semiconductor Loss Calculation

The actually used VR topology is shown in Fig. 6. It involves six rectifier diodes D_R which are only commutating with mains frequency and can therefore be realized using relatively low cost Si devices which also have comparably low forward voltage drop. In the actual switching frequency commutation only the switch S and the freewheeling diode D_F are involved, simplifying the layout and reducing the parasitic inductance of the commutation loop. In the following the loss calculation for all semiconductors is described.

1) Conduction Losses: For the calculation of the conduction losses in the semiconductors it is assumed that the current is shaped purely triangularly, i.e. different slopes (Fig. 2) and the zero current period in the phase with the smallest absolute voltage value are neglected. Therefore, with the rectifier input current RMS value I and the mains frequency f the current in one boost inductor can be expressed as

$$i(t) = \sqrt{2} I (\sin(2\pi f t) + \mathrm{tri}(2\pi f_s t)). \tag{4}$$

With a 2π periodic triangular function $\mathrm{tri}(\varphi) \in [-1, 1]$. Additionally, it is assumed that the reverse conduction time of the freewheeling diode introduces a delay T_{rr}. If this delay takes up a certain fraction $D_{rr} = \frac{T_{rr}}{T_s}$ of the ideal switching period and the reverse recovery charge itself is neglected, the delay increases all RMS currents by a factor of $\frac{1}{\sqrt{1-D_{rr}}}$. Starting from these assumptions the RMS and average currents in the three semiconductor devices are derived as shown in Tab. II using the modulation index $M = \frac{2\hat{u}}{U_{out}}$ which describes the ratio of the phase voltage amplitude to half of the DC-link voltage. Comparing these equations with the ones for CCM [8] reveals that all RMS values in BCM are higher by a factor of $\frac{2}{\sqrt{3(1-D_{rr})}} \approx 1.3$ assuming a reverse recovery time of 20 % of the ideal switching period. The average values are the same as in CCM. For 10 kW nominal power and 800 V output voltage, the highest currents appear at the lowest specified input voltage

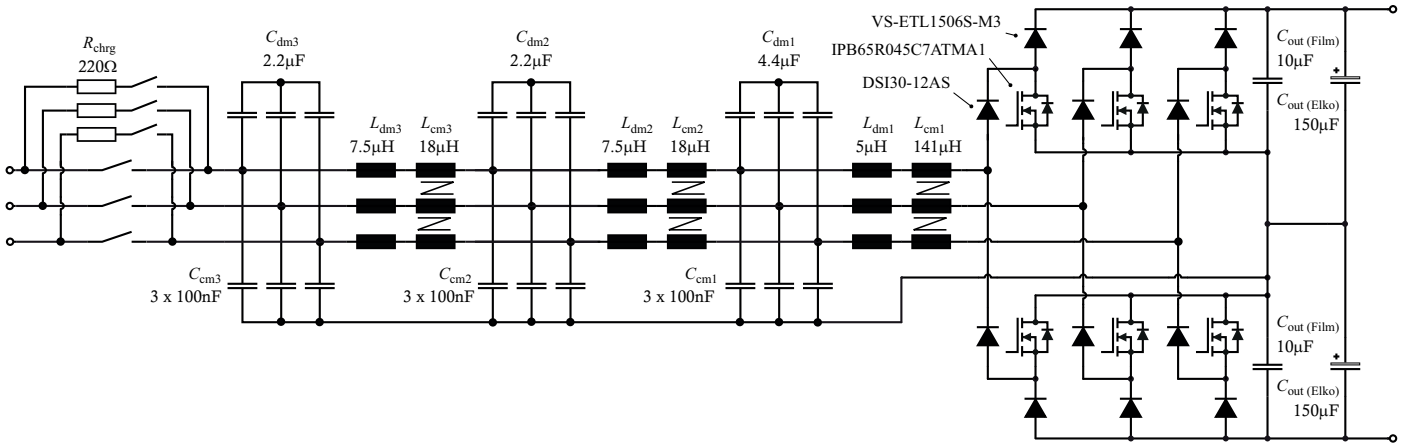

Fig. 6. Complete circuit of the constructed prototype including voltage DC-link pre-charging circuit, three stage DM and CM filter, VR bridge circuit and DC-link.

TABLE II. SEMICONDUCTOR CURRENTS

	RMS Current	AVG Current
Rectifier Diode D_R	$\frac{2}{3\sqrt{1-D_{rr}}}I$	$\frac{\sqrt{2}}{\pi}I$
Free-wheeling Diode D_F	$\frac{4}{3}\sqrt{\frac{M}{\pi(1-D_{rr})}}I$	$\frac{M}{2\sqrt{2}}I$
Switch S	$\frac{2}{3}\sqrt{\frac{1}{1-D_{rr}}\left(\frac{3}{2}-\frac{4M}{\pi}\right)}I$	$\frac{4-\pi M}{2\sqrt{2}\pi}I$

of $U = 290\,\mathrm{V}$ line-to-line RMS. Therefore, the rectifier diodes are dimensioned for a RMS current of 14.8 A and an AVG current of 9.0 A, the free-wheeling diodes for a RMS current of 12.9 A and an AVG current of 4.2 A and the switches for a RMS current of 12.8 A and an AVG current of 4.8 A.

2) Switching Losses: Although it is estimated that due to the reverse recovery current of the diode the output capacitance of the switch is discharged at least partially, for a worst case estimation the switching losses are calculated for a turn-on with the switch output capacitance charged to the DC-link voltage. During the turn-on of the switch also the diode's junction capacitance is charged, which also contributes to the turn-on losses of the MOSFET. The contribution related to the freewheeling diode is the difference of the energy taken from the DC-link and the energy that remains stored in the junction capacitance, which will be released again at turn-off. The total turn on losses can thus be calculated from the transistors output capacitance C_{oss} and the diodes junction capacitance C_j as function of the DC-link voltage U_{dc} using

$$E_{on}(U_{dc}) = \int_0^{U_{dc}} u \cdot C_{oss}(u) + (U_{dc} - u) \cdot C_j(u)\mathrm{d}u. \quad (5)$$

Remark: In the calculation no losses of the switch or diode due to the diode reverse recovery current are considered, as the actual switch turn-on only happens once voltage is built up across the diode. Accordingly, the switch turn-on process is different from a hard turn on. Losses in the diode due to the (decaying) reverse recovery charge are neglected in a first step. As shown in Fig. 7a the total turn-on losses are dominated by the energy E_s stored in the output capacitance of the switch. The diode's contribution consisting of the difference $U_{dc} \cdot Q_d - E_d$ only amounts to only $\approx 20\,\%$.
Gate driver limitations and the common source package inductance of the gate and power path of the switch limit the turn-off time of the MOSFET. Therefore, at high currents as appearing in BCM the voltage at the output capacitance rises

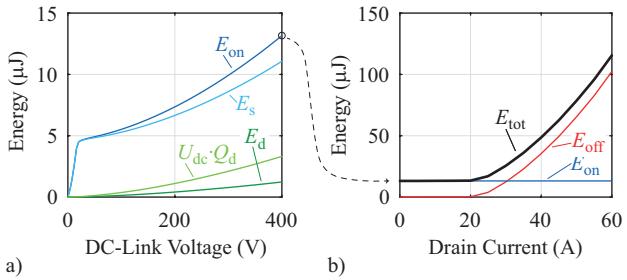

Fig. 7. a) Turn-on energy E_{on} consisting of stored energy in the output capacitance of the switch E_s and the difference between the energy used to charge the diode's junction capacitance $U_{dc} \cdot Q_d$ and the energy that remains stored in the diode's junction capacitance E_d as function of the DC-link voltage. b) Turn-off energy E_{off}, turn-on energy E_{on} and total switching energy E_{tot} depending on the switched current.

faster than the current falls and the turn-off losses are no longer negligible. A SPICE simulation is carried out to determine the turn-off losses using models supplied by the manufacturers. The resulting turn-off energy is shown in Fig. 7b. At peak currents higher than 30 A the turn-off currents dominate the total switching loss energy E_{tot}. Finally, for the calculation of the average switching loss during one mains period the reverse recovery related delay has to be considered because it increases the peak current and reduces the switching frequency. Thus, the switching losses are calculated using the turn-off current $I_{s,off}(t) = \frac{2\cdot\sqrt{2}\cdot I}{1-D_{rr}}\sin(\omega t)$ and the switching frequency $f_s = \frac{(1-D_{rr})^2}{T_s}$ using (3). The loss sharing between the different components and the total calculated converter efficiency depending on the input voltage is shown in Fig. 8. In the nominal input voltage range of 400 V to 480 V the calculated efficiency is well above 98 %. However, high frequency losses occuring in components other than the inductors could give rise to considerable additional losses.

B. EMI Input Filter Dimensioning

For grid connected converters one usually has to design an input filter such that CISPR EMI limits are not exceeded. This section provides a comparison of the noise spectrum in BCM with the one in CCM and describes the filter design procedure used for the construction of the prototype.

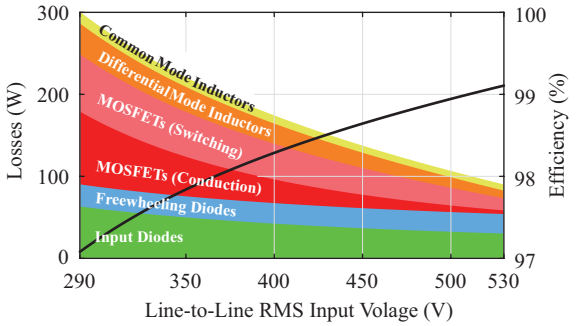

Fig. 8. Loss sharing between the different power semiconductors and filter inductors as well as the calculated efficiency for the specified input voltage range at 10 kW output power and 800 V output voltage.

1) Comparison with CCM: Because of the variable switching frequency and the higher differential mode (DM) noise in BCM it is expected that higher filter attenuation than for CCM operation is necessary. In order to quantify this drawback the noise spectra of BCM and CCM are directly compared and an equivalent CCM switching frequency is determined such that the same DM filter attenuation is exactly sufficient for both BCM and CCM.

First the noise spectra of the VR bridge input voltages $u_{\mathrm{r}km}$ (Fig. 1) as they would be measured with a CISPR quasi-peak (QP) detector shall be examined. Fig. 9 shows the simulated DM and common mode (CM) noise spectra for BCM and CCM operation [9]. As it is shown in Fig. 9a the emitted noise spectrum in BCM depends on the rectifier input voltage. Furthermore, the switching frequency in BCM varies throughout the mains period between a minimum and a maximum value. Therefore, there are no sharp switching frequency peaks appearing in the noise spectrum, instead there are noise plateaus on an interval between the minimum and the maximum switching frequency which occur during one mains period. The plateau at 530 V input voltage is the widest, ranging from 180 kHz to 520 kHz. Because of this wide range the plateaus of the switching frequency harmonics are overlapping each other in this case and the noise spectrum appears almost continuous. However, the frequency variation during one mains period is smaller in case of 290 V and 400 V input voltage. Therefore, the noise plateaus are narrower but also higher. At the lowest input voltage the DM noise level in BCM is higher and the CM noise level is lower than in CCM. This is also observed with operation in DCM with constant switching frequency [6] and can be explained by the small frequency range at the lowest input voltage. At the highest input voltage the switching frequency varies by a factor of ≈ 2.9. Because of this large variation the DM noise level is reduced even below the level of CCM operation.

In order to allow a direct comparison between the noise levels in BCM and in CCM the noise spectrum is shown after filtering with a three stage filter designed such that the worst case BCM noise level exactly touches the CISPR Class A limit. In a next step the switching frequency of the CCM noise spectrum is set such that the worst case DM noise peak after filtering also equals the limit exactly. The result is shown in Fig. 10a which shows the filtered DM noise after filtering for BCM and CCM. The worst case in BCM appears at the lowest switching frequency, which occurs at the highest input voltage. The switching frequency of the CCM noise spectrum has to be set to 200 kHz such that exactly the same DM filter attenuation is required. However, if also the same CM filter attenuation is used (Fig. 10b) the noise peak in CCM would exceed the limit by $\approx 10\,\mathrm{dB}$.

2) Dimensioning: As shown in Fig. 6 the dimensioned input filter consists of three DM and three CM stages, each stage having the same topology. The common mode filter stages use a capacitive feedback to the midpoint [10] of the DC-link which is realized using one capacitor for each phase (Fig. 6). These capacitors provide a small additional DM capacitance negligible at low frequencies but reducing the effect of the relatively high equivalent series inductance of the DM filter capacitors.

In order to determine the values of the DM filter components one has to find the required product of $L_{\mathrm{dm},k}$ and $C_{\mathrm{dm},k}$ of all N filter stages. Using the QP detected noise level $u_{\mathrm{qp,dm}}(f,U)$ as shown in Fig. 9a and the desired limiting noise level $u_{\mathrm{qp,dm,max}}(f)$ the product

$$\Pi_k^N L_{\mathrm{dm},k} C_{\mathrm{dm},k} = \max_{f,U} \frac{2u_{\mathrm{qp,dm}}(f,U)}{(2\pi f)^{2N} u_{\mathrm{qp,dm,max}}(f)} \tag{6}$$

is obtained [9]. The components of the first filter stage however have to be selected independently. The boost inductance is defined by the desired maximum switching frequency. From (3) it can be derived that the maximum switching frequency occurs at a modulation index of $M = \frac{8}{9}$. Therefore the boost inductance value for a given maximum switching frequency $f_{\mathrm{s,max}}$ and a minimum load resistance R_{out} is given as

$$L_{\mathrm{dm},1} = \frac{4R_{\mathrm{out}}}{81 f_{\mathrm{s,max}}}. \tag{7}$$

The DM filter capacitance of the first filter stage is defined by the allowed RMS current or alternatively by a voltage ripple requirement. Using the same assumptions as in Sec. III-A the RMS value of the current in one capacitor of the first DM filter stage is given as

$$I_{\mathrm{Cdm1}} = \frac{1}{\sqrt{3(1-D_{\mathrm{rr}})}} I \tag{8}$$

related to the rectifier input current RMS value I. With the values of the first filter stage given, the values of the remaining DM inductors and capacitors are calculated. In order to minimize the stored energy all remaining filter stages should have equal L and C values. For the prototype according to (6) 82 dB DM filter attenuation is required at 180 kHz. The first stage DM capacitor is selected for a rated RMS current of 12.9 A. Therefore, two $2.2\,\mu$F X2 film capacitors in parallel are used for each phase. The DM inductance of the first stage is $5\,\mu$H for a maximum switching frequency of 630 kHz. In order to achieve a compact design the same $2.2\,\mu$F film capacitor used for the first stage is also selected for the second and third DM filter stage. In order to obtain the required attenuation at least $7.5\,\mu$H DM inductance is required for the second and third stage.

The design procedure for the CM filter is basically the same as for the DM filter. First the required filter attenuation is calculated according to (6). Second the CM capacitance is selected to be the same for all stages at a value of approximately 10 % of the DM capacitance. Finally, the CM inductance is obtained, if it is assumed that the CM inductance of all filter stages is

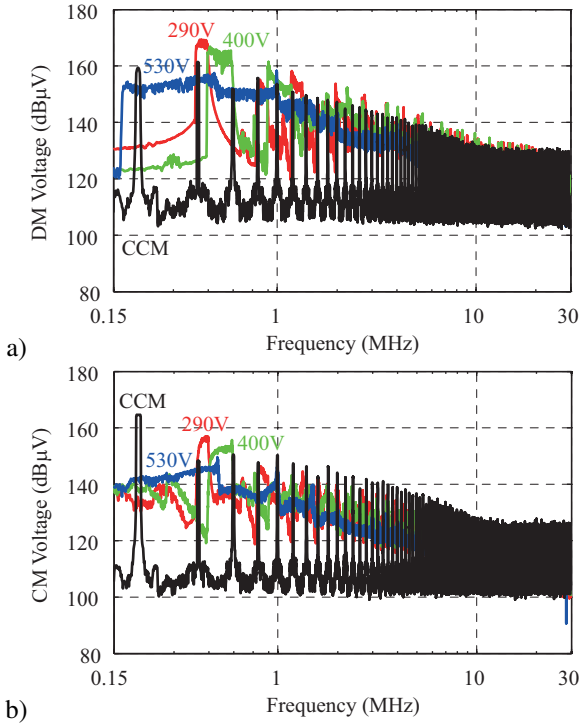

Fig. 9. Simulated DM (a) and CM (b) QP EMI noise spectra of the BCM VR prototype at different input voltage levels compared to the noise spectrum of CCM operation at 200 kHz switching frequency.

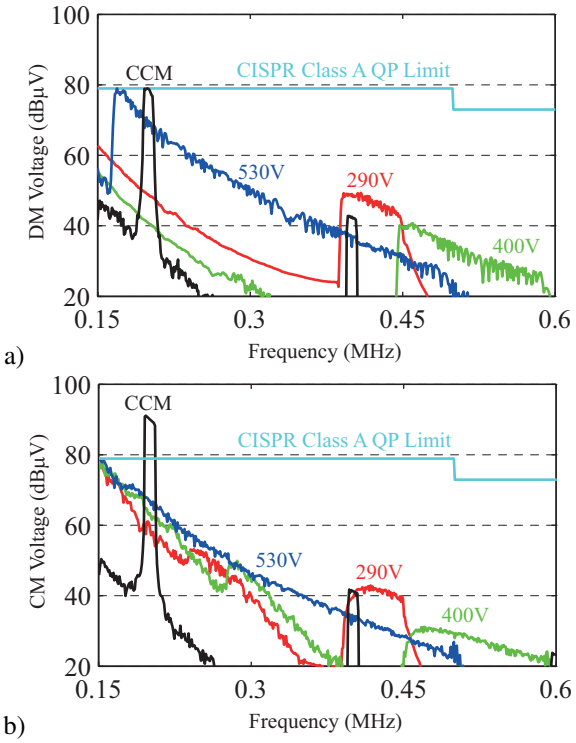

Fig. 10. Simulated DM (a) and CM (b) QP EMI noise spectra after attenuation by a three-stage filter which is designed such that the worst case noise level in BCM exactly reaches the CISPR Class A limit.

the same. Because of the large high frequency CM voltage component that the first filter stage is subjected to, usually a higher inductance value than for the remaining stages is used in order to reduce the core losses. For the prototype also different core materials are selected, while the first stage uses ferrite, the second and third are equipped with nano-crystalline cores. Therefore, in order to achieve the required attenuation of 69 dB at 150 kHz the CM capacitance of each stage is set to 0.3 μF, the CM inductance of the first stage is set to 150 μH and the CM inductance of the second and third stage is set to 35 μH.

C. Controller Implementation

In order to realize a delay compensation as proposed in Sec. II-C2 the duty times of the switches must be updated each switching cycle based on the duration of the previous one. This calculation according to Tab. I involves a square root and a multiplication. Because of the high and variable switching frequency, it is desired that the PWM is implemented on a FPGA. Therefore, instead of calculating the square root, a quadratic counter is used which is easily realized using a linear counter and one addition. The next quadratic counter value q_n can be calculated from the present quadratic counter value q_p and the present linear counter value c_p as $q_\mathrm{n} = q_\mathrm{p} + 2 \cdot c_\mathrm{p} + 1$. Therefore, the switch of phase k is on for

$$t^2 < T_\mathrm{s} L G d_k^2 = T_\mathrm{s} \cdot T_{\mathrm{set},k}, \tag{9}$$

with t^2 representing the quadratic counter value, the previous switching period T_s and a value $T_{\mathrm{set},k}$ provided by a DSP, but only updated at 30 kHz. The DSP calculates $T_{\mathrm{set},k}$ depending on the conductance G, the inductance L and the relative duty cycle d_k. The quadratic counter compare value, i.e. the product $T_\mathrm{s} T_\mathrm{set}$ for the next switching period can also be calculated without multipliers by continuously adding up T_set during the

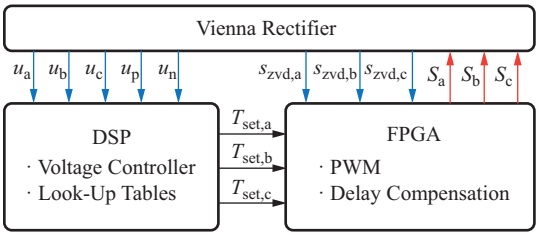

Fig. 11. Implementation of BCM control using a DSP that calculates $T_{\mathrm{set},k}$ values for each phase k according to (9) representing the duty cycles and sends them to an FPGA which generates the PWM with variable switching frequency based on the current slope detector signals.

period and thus multiplying it with the length of the switching period. The principle of this control is illustrated for one phase in Fig. 12. It is implemented on a FPGA with 100 MHz clock frequency. The current slope detector signals are also directly processed on the FPGA. The DSP measures the phase- and DC-link voltages, executes the voltage controller and calculates the values $T_{\mathrm{set},k}$ which are sent to the FPGA as shown in Fig. 11.

D. Current Slope Detector

In order to maintain operation in BCM the moment when the freewheeling diode stops conducting has to be detected. Since the current in the boost inductor is already reversed at the point in time where the freewheeling diode starts to block it will discharge the output capacitance of the switch at least partially before rising again. This change in slope of the current can easily be detected using auxiliary windings on DM and CM inductors which allow to measure the total voltage $u_{L\mathrm{dm},k} + u_{L\mathrm{cm},k}$ of each phase k. The sign of this voltage indicates the slope of the current. As shown in Fig. 13a Schmitt

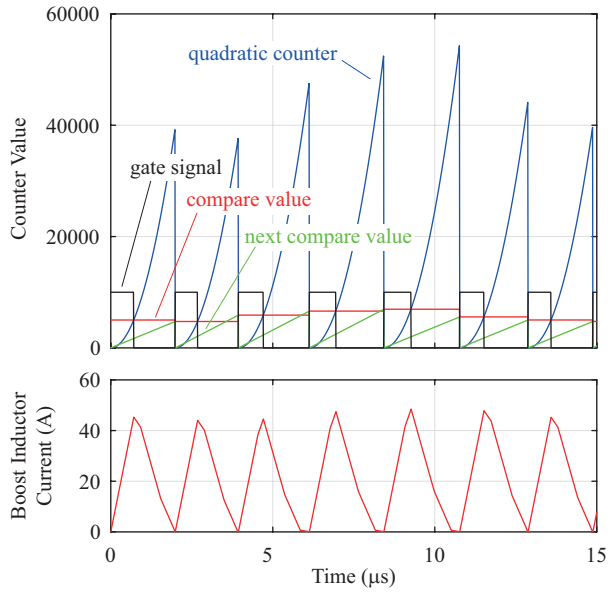

Fig. 12. Simulation of delay compensation using a quadratic counter. The switch is turned on if the quadratic counter value is smaller than a compare value which is recalculated each switching period by adding up an increment calculated on the DSP at a rate lower than the switching frequency.

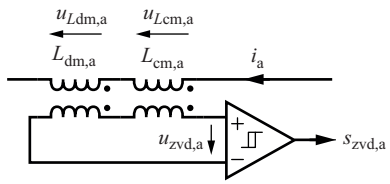

Fig. 13. Current slope detector used to detect the moment when the freewheeling diode stops conducting. The output signal represents the slope of the current in the boost inductor.

trigger is connected to the auxiliary winding to generate a signal $s_{\mathrm{zvd},k}$ that represents the slope of the current in the boost inductor of the according phase.

Fig. 14 shows the boost inductor current, the rectifier input voltage, the voltage at the auxiliary winding and the output signal of the current slope detector for a mains phase angle of $\varphi = 10°$. It can be observed that as soon as the diode stops conducting and the rectifier input voltage drops below the voltage of the corresponding differential mode capacitor, the sign of the voltage at the auxiliary winding and therefore the output signal of the current slope detector changes. However, for starting a new period only the zero voltage signals of two phases are used, the signal of the phase carrying the smallest current is discarded since the current is discontinuous and may cross zero several times, as it is observed at a mains angle of $\varphi = 70°$ (Fig. 15).

Instead of using auxiliary windings the input voltages of the rectifier bridge could also be measured directly and compared to the corresponding DM capacitor voltages which are measured anyway. Detecting the current zero-crossing is not an option since the current crosses zero before the moment when the diode stops conducting and the switches should be turned on.

IV. Results

Because of dv/dt related noise on the voltage measurements and on the current slope detector signals only experiments

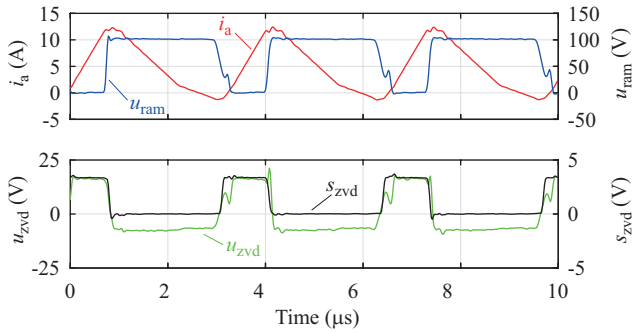

Fig. 14. Measurement of boost inductor current i_{a}, corresponding rectifier input voltage u_{ram}, auxiliary winding voltage $u_{\mathrm{zvd,a}}$ and current slope detector signal $s_{\mathrm{zvd,a}}$ at a mains voltage angle of $\varphi = 10°$.

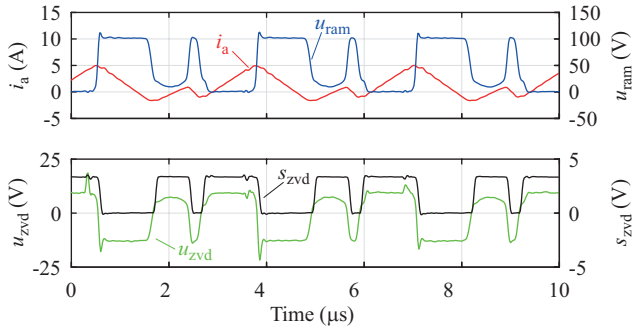

Fig. 15. Measurement of boost inductor current i_{a}, corresponding rectifier input voltage u_{ram}, auxiliary winding voltage $u_{\mathrm{zvd,a}}$ and current slope detector signal $s_{\mathrm{zvd,a}}$ at a mains voltage angle of $\varphi = 70°$. Since the current is close to the zero crossing, the current is discontinuous and oscillates with the switch output capacitance. In this case the current slope detector output signal is not used.

at 2.5 kW output power and 400 V output voltage have been carried out so far. However, the proposed control scheme and the delay compensation are verified. Fig. 17 shows the boost inductor current of one phase and the rectifier input voltage at a mains angle of 10°. By using the slope detectors the switches are turned on after all diodes have stopped conducting. Variable delays are introduced by the CM filter and by the freewheeling diode reverse recovery time. Since the switching period is calculated according to (3) and delays are not compensated, the current shape is visibly distorted and the measured THD is 6.98 %. If the proposed delay compensation which uses the length of the previous switching period as reference is activated, the input current distortion is considerably reduced (Fig. 18) and the measured THD is 4.45 %.

V. Conclusion

Employing BCM operation of three-phase three-level rectifiers in order to ensure zero current (and partial zero voltage) turn-on is proposed. A 10 kW rectifier prototype is constructed for operation in BCM with switching frequencies ranging from 180 kHz to 630 kHz using only silicon power semiconductors. The BCM control scheme is described using space vectors and equations for calculating the duty times and the switching period are provided. The noise spectrum of variable switching frequency BCM control is compared to the noise spectrum of constant switching frequency CCM. The required DM filter attenuation for BCM is approximately the same as it would be required for CCM operation at the lowest BCM frequency which occurs at the highest input voltage. The required CM

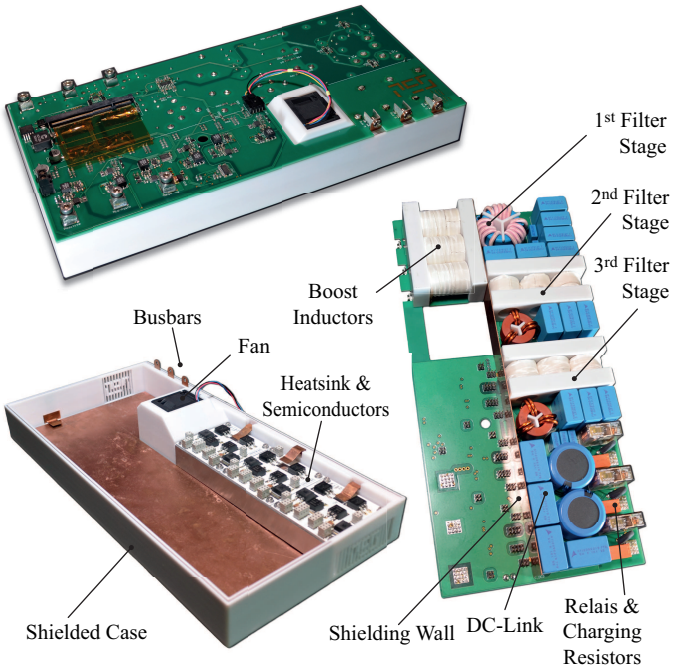

Fig. 16. Constructed laboratory prototype. The three DM inductors are realized as coupled inductors in order to save space and material. The filter is designed for CISPR Class A compliance. All power semiconductors are mounted on aluminium core PCBs which are directly attached to a heatsink. A nominal output power of 10 kW and outside dimensions of 325 mm × 157 mm × 45 mm (12.8 in × 6.2 in × 1.8 in) result in a power density of 4.4 kW/dm^3 (71 W/in^3).

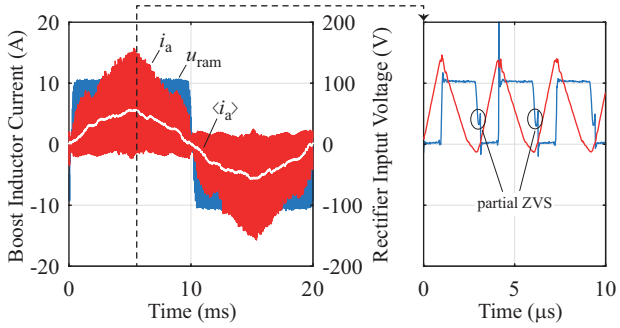

Fig. 17. Measured boost inductor current i_a and its local average $\langle i_a \rangle$ as well as the rectifier input voltage u_{ram} at 10° mains voltage angle using the calculated length of the switching period according to (3) and variable switching frequency using the current slope detectors. Non-constant delays introduce low frequency current distortions as also observed in the simulation.

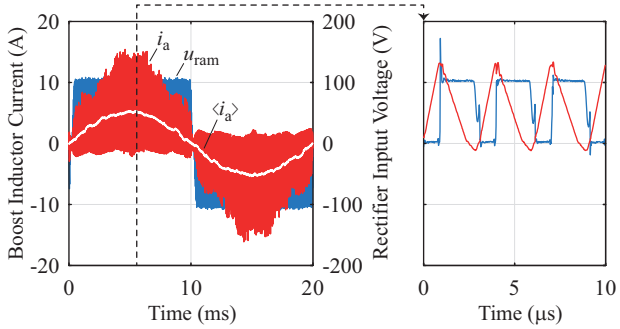

Fig. 18. Measured boost inductor current i_a and its local average $\langle i_a \rangle$ as well as the rectifier input voltage u_{ram} at 10° mains voltage angle with active delay compensation and current slope detection. Delay compensation is implemented on the FPGA using a quadratic counter compensating delays in the following period.

attenuation in BCM is around 10 dB lower than in CCM. Equations for calculating the RMS and AVG values of the currents in the power semiconductors are provided. Compared to CCM operation the RMS current of all components in BCM is higher by a factor of ≈ 1.3 because of the triangular current shape and the reverse recovery time of the freewheeling diodes which is assumed to take up a fraction of 20 % of the switching period.

Circuit simulations and measurements on the laboratory prototype show that the CM filter and the reverse recovery time of the freewheeling diode cause deviations of the length of the switching period from the calculated value. As a result the average current during the switching period also deviates and low frequency current distortions leading to an increase in THD of ≈ 3 % occur. A method to compensate these delays and to prevent current distortions is proposed and verified on the prototype. Instead of using the calculated length of the switching period for the calculation of the duty times of the switches, the measured length of the previous switching period can be used. This way a delay is immediately compensated in the following switching period. The delay compensation can be efficiently realized on a FPGA without multipliers by using a quadratic counter. Auxiliary windings on the inductors allow to detect the end of a switching period, i.e. the moment when the freewheeling diodes stop conducting. Further research will address an experimental verification of the calculated efficiency and the conducted EMI noise emissions.

References

[1] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat Interleaved Triangular Current Mode (TCM) Single-Phase PFC Rectifier," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 873–882, Feb 2014.

[2] J.-S. Lai and D. Chen, "Design Consideration for Power Factor Correction Boost Converter Operating at the Boundary of Continuous Conduction Mode and Discontinuous Conduction Mode," in *Proc. of Applied Power Electronics Conference and Exposition (APEC)*, Mar 1993, pp. 267–273.

[3] L. Huber, B. Irving, and M. Jovanovic, "Open-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1649–1657, July 2008.

[4] H. Yu, X. Huang, and J.-S. Lai, "A Novel Load Adaptive Zero Voltage Switching Utilizing Diode Reverse Recovery Current for Soft-Switching Choppers," in *Conf. Record of the IEEE Industry Applications Conference*, vol. 3, Sept 2001, pp. 1845–1850 vol.3.

[5] M. Hartmann, S. Round, H. Ertl, and J. W. Kolar, "Digital Current Controller for a 1 MHz, 10 kW Three-Phase VIENNA Rectifier," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2496–2508, Nov 2009.

[6] M. Leibl, J. W. Kolar, and J. Deuringer, "New Current Control Scheme for the Vienna Rectifier in Discontinuous Conduction Mode," in *Proc. of IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 1240–1247.

[7] J. W. Kolar, H. Ertl, and F. C. Zach, "Space vector-based analytical analysis of the input current distortion of a three-phase discontinuous-mode boost rectifier system," in *Proc. of 24th Annual IEEE Power Electronics Specialists Conference (PESC)*, 1993, pp. 696–703.

[8] T. Friedli, M. Hartmann, and J. W. Kolar, "The Essence of Three-Phase PFC Rectifier Systems Part II," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 543–560, Feb 2014.

[9] M. L. Heldwein, "EMC Filtering of Three-Phase PWM Converters," Ph.D. dissertation, ETH Zurich, Power Electronic Systems Laboratory, 2008.

[10] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI Filter Design for a 1MHz, 10kW Three-Phase/Level PWM Rectifier," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1192–1204, April 2011.