The Essence of the Little Box Challenge-Part A: Key Design Challenges & Solutions

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***Abstract*—In order to expedite the development of power electronic systems towards higher power density and efficiency at a lower cost of implementation, Google and IEEE initiated the Google Little Box Challenge (GLBC) aiming for the worldwide smallest 2 kVA / 450 V DC / 230 V AC single-phase PV inverter with η > 95 % CEC weighted efficiency and an air-cooled case temperature of less than 60 °C by using latest power semiconductor technology and innovative topological concepts. This paper, i.e., Part A of a discussion of *The Essence of the Little Box Challenge*, documents all important R&D activities and engineering considerations of the authors endeavor to implement the world's most compact inverter; Part B is intended to convey the main findings and lessons learned from the participation in the GLBC. First, the key technical challenges of the GLBC are discussed and the technologies and concepts selected by the authors among different options are described in detail. Relevant design considerations, such as constant frequency pulse width modulation (PWM) or triangular current mode (TCM) operation of the bridge-legs, selection of power semiconductor technology, interleaving of bridge-legs, sizing of the power buffer capacitor, limitation of ground/leakage currents, etc., to achieve an ultra-compact implementation are discussed. Based on this overview, two promising inverter concepts to tackle the GLBC, (i) an H-bridge based inverter with DC-link referenced output filter and (ii) a DC/|AC| buck-stage with series-connected low-frequency (LF) |AC|/AC unfolder inverter, are then analyzed in detail. Based on the results of a multi-objective $\eta\rho$-Pareto optimization, a comparative evaluation of the performance in terms of efficiency (η) and power density (ρ) of the two considered inverter concepts is provided. It is shown that with the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter operated with 140 kHz PWM a power density of 14.7 kW/dm^3 (240 W/in^3) with a maximum efficiency of 98.1% at 2 kW output power can be achieved. These claims are then verified in Part B by means of experimental results obtained from prototype realizations and compared to the achievements of other GLBC finalists. The conclusions are of general importance and are providing key guidelines for the future development of ultra-compact power electronic converters.**

***Index Terms*—GaN, high power density, little box challenge, microinverter, power buffer, PV inverter, wide bandgap (WBG), zero voltage switching.**

Manuscript received October 10, 2019; revised January 7, 2020; accepted February 7, 2020. Date of publication June 30, 2020; date of current version June 15, 2020. *(Corresponding author:Dominik Neumayr.)*

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Digital Object Identifier 10.24295/CPSSTPEA.2020.00014

I. Introduction

During the last decades, the advances in power semiconductors and microelectronics have been—besides innovative topologies, modulation and control concepts—the driving force for the development of new power electronic converters towards higher compactness/power density, efficiency and cost reduction [1]. In particular, wide bandgap (WBG) power semiconductors are expected to bring a significant improvement of the performance of converter systems. Following this idea, Google and IEEE launched the Google Little Box Challenge (GLBC, [2]) on July 22nd, 2014, aiming for a massive enhancement of the power density of a 2 kVA single-phase DC/AC converter system compared to state-of-the-art technology, advertising $1 million prize money. The challenging specifications and the attractive prize money created a remarkable interest in the power electronics community, which led to the participation of 2000+ teams—companies, research institutes and universities—in the GLBC. Finally, 100+ teams submitted technical descriptions of realized systems. Out of these applications, 18 finalists were selected, whereby the achieved power densities were mainly in the range of 120–220 W/in^3. With this, a distinctly higher performance compared to the minimum requirement of 50 W/in^3 according to the state-of-the-art was achieved. The Power Electronic Systems Laboratory (PES) at the ETH Zurich, in collaboration with the Fraunhofer Institute for Reliability and Microintegration (FH-IZM) and the Fraza Company, has been selected as one of the 18 finalists [3], who presented their technical approaches on October 21st, 2015 and handed over the prototype to the National Renewable Energy Laboratory (NREL), Golden (Co), USA, for final testing. The winner of the grand prize of the $ 1 million has been announced in Feb. 2016. The winning team from the Belgium Company CE+T, which had the most power dense inverter passing all tests, e.g., also the 100 hours testing, achieved a power density of 8.72 kW/dm^3 (142.9 W/in^3).

This paper is intended to provide a condensed review of the technical concepts and approaches presented in scientific literature and focuses on the reasoning behind the authors' design choices and innovations to implement the Google Little Box inverter. Due to the large scope of the topic, the paper is split in two consecutive parts. Part A of the paper presented herein is structured in the following way: First, in Section II the technical requirements of the GLBC are presented. Then, in Section III the key design challenges—component miniaturization, compensation of the 120 Hz DC voltage ripple, electromagnetic interference (EMI) and ground current limits, 60 °C maximal surface temperature, and the very short competition time-frame

TABLE I
KEY INVERTER SPECIFICATIONS OF THE GOOGLE LITTLE BOX CHALLENGE.

Parameter	Requirement
Input voltage source	450 V_{dc} with 10 Ω
Output voltage & frequency	240 V_{rms}/60 Hz
Maximum output power S	2 kVA
Power factor (cos φ_0)	0.7, . . ., 1, lead & lag
Maximum load steps	500 VA
Power density	> 3 kW/dm³(> 50 W/in³)
CEC efficiency	⩾ 95 %
Lifetime (test duration)	> 100 h
Max. outer enclosure temperature	⩽ 60 °C
Input voltage ripple (120 Hz)	⩽ 3 % (i.e., ⩽ 12 V pk-pk)
Input current ripple (120 Hz)	⩽ 20 % (i.e., ⩽ 1 A pk-pk)
Ground/leakage current	⩽ 50 mA (initially ⩽ 5 mA)
Electromagnetic compliance	FCC Part 15B/CISPR11 class B
Output voltage/current THD	< 5 %

—are discussed in detail, highlighting the design choices and numerous novel concepts proposed by the authors. Based on this discussion, two promising inverter concepts, (i) an H-bridge based inverter with DC-link referenced output filter and (ii) a DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter, both equipped with a buck-type parallel current injector (PCI) active power buffer, are then analyzed in detail. In order to comparatively evaluate the performance of the selected inverter concepts, the main findings of a multi-objective $\eta\rho$-Pareto optimization carried out in previous work of the authors (cf., [4], [5]) are revisited in Section IV-A. The claimed performance of the optimized inverter systems are then verified and compared to the approaches and achievements of other GLBC finalists by means of implemented hardware prototypes and latest experimental results as presented in Part B of this paper. In order to keep the main part of the paper as brief as possible, complementing material on design considerations is compiled in Appendices A-E.

II. TECHNICAL SPECIFICATION

The key inverter specifications of the GLBC are listed in Table I and the basic test setup is depicted in Fig. 1. As a minimum requirement to participate in the competition, a power density of $\rho > 50$ W/in³ and a California Energy Commission (CEC) weighted efficiency,

$$\eta_{CEC} = 0.04 \times \eta_{10\,\%} + 0.05 \times \eta_{20\,\%} + 0.12 \times \eta_{30\,\%} + 0.21 \times \eta_{50\,\%} + 0.53 \times \eta_{75\,\%} + 0.05 \times \eta_{100\,\%},$$

of greater than 95 % was specified.

The specified 450 V DC source at the input was decoupled from the device under test (DUT) by means of a 10 Ω resistor as illustrated in Fig. 1, which allowed to measure the limited double-line frequency voltage ripple at the DUT DC input and also emulated the $v-i$ relationship of a PV module. Due to the inserted 10 Ω resistor, V_{dc} reduces with increasing load from 450 V DC at idle operation to 400 V DC at nominal output power of 2 kVA (cos $\varphi_0 = 1$). The inverter input voltage ripple was limited to 2.5% (10 V pk-pk)[1] of the average input voltage, V_{dc}, which demanded to include an energy storage in the converter in order to buffer the fluctuating power at the AC side intrinsic to single-phase power conversion systems. The specified maximum output power was 2 kVA with a power Factor (cos φ_0) between 0.7,...,1, leading and lagging, and the inverter had to be able to handle stepwise load variations as high as 500 VA. Although the inverter was not required to feature galvanic isolation, for reasons of safety and protection of the testing equipment, a 1:1 isolation transformer was specified to be inserted between the DUT AC output and the load. Depending on the preference of the contestants, a 240 V split-phase grounding configuration as drawn with solid lines in Fig. 1 or a 240 V-to-ground configuration as indicated with dashed lines in Fig. 1 was possible. In order to limit initial inrush currents at the DC input (charging of the storage capacitor) and the transformer magnetizing inrush currents at the AC side, 100 Ω resistors were temporarily inserted between the DUT and the DC input and the isolation transformer, respectively, and bypassed during regular operation after startup. Furthermore, electromagnetic compliance according to the rules for "unintentional radiators" as stated in the FCC Part 15 B standard (equivalent to EN 55022/32 class B, residential equipment) was required. For the purpose of measuring conducted emissions, the EMI test receiver (line impedance stabilization network, LISN) was specified to be inserted between the DUT and the isolation transformer. The emissions were measured at 400 W partial and 2 kW nominal load (cos $\varphi_0 = 1$). The ground or leakage current flowing in the wire connecting the converter chassis to ground, i_g, and the wire that connected either the split-phase of the isolation transformer or the neutral conductor, i_{gt}, to ground was limited to 50 mA and was not allowed to be exceeded any time during the testing. This requirement was revised from the initially specified 5 mA leakage current since the parasitic capacitance (≈ 120 nF, certainly < 200 nF) formed between the floating DC supply to ground (capacitance of the positive and negative terminals, p and m) was larger than first anticipated by the contest organizers. The THD levels including noise (i.e., including all spectral components which are not a multiple of the fundamental frequency) of the AC output voltage and current were required to be less than 5% without scrutiny of individual harmonics as specified in grid connection standards such as the IEEE 1547 or IEC 61727.

III. 5 KEY DESIGN CHALLENGES & SOLUTIONS

In the following, the 5 key design challenges of the GLBC from the point of view of the authors are described and different technical approaches and design considerations, with special focus on the authors' design choices are discussed. In particular, novel concepts and innovations proposed by the authors will be highlighted. As it will become clear, the key design challenges are highly interlinked and thus impose a multi-objective design problem which will be addressed in Section IV.

[1]The specified 20% input current ripple limit (cf., Table I) is more stringent and, for the stated $R_s = 10$ Ω input resistor, implies a 2.5% (10 V pk-pk) limit for the maximal permissible 120 Hz input voltage ripple.

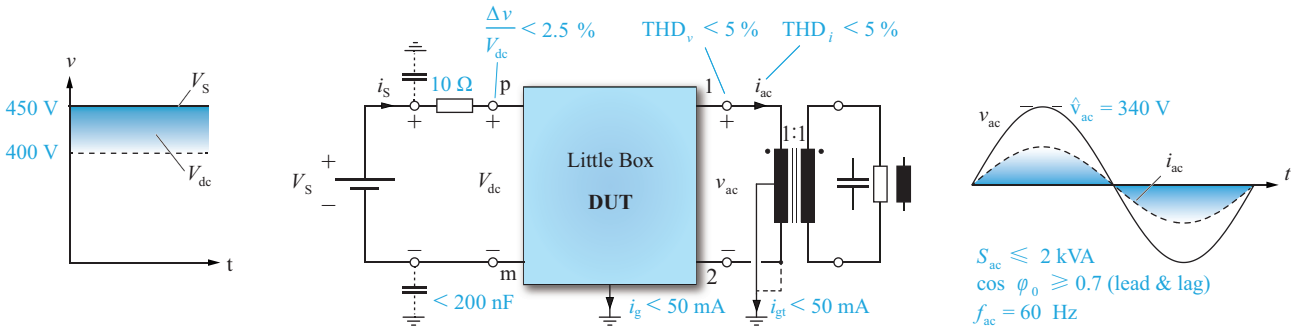

Fig. 1. Goolge Little Box Challenge test configuration with specified 10 Ω input resistor and 1:1 isolation transformer at the output.

A. Component Miniaturization / High Frequency Operation

In order to drastically shrink the size of the converter bridge-legs and EMI filter passives and break through the status quo in power density, a high switching frequency in the range of 100 kHz–1 MHz, constituting a factor 10–100 increase compared to state-of-the-art Si-IGBT based inverter systems, was selected.

1) WBG Semiconductors: The unprecedented performance of WBG semiconductor technology enables such high switching frequencies and is therefore considered as one of the key technologies for an ultra-compact converter design. To compare the performance of different power semiconductors, the figure of merit (FOM) proposed in [6],

$$\mathrm{FOM}(V) = \frac{1}{R_{\mathrm{ds,on}} Q_{\mathrm{oss}} | V}, \qquad (1)$$

is a very useful metric. The charge stored in the transistor's output capacitance, Q_{oss}, allows to roughly estimate the resulting (capacitive) switching losses for hard-switching and the on-state resistance, $R_{\mathrm{ds,on}}$, is representative for the conduction losses. In [7], (1) was calculated for over hundred commercially available Si, SiC and GaN power semiconductors and plotted as a function of their rated blocking voltage $V_{\mathrm{ds,max}}$ = 75V ... 1.7 kV as depicted in Fig. 2. It is worth noting that GaN and SiC devices at 650 V rated voltage are comparable in performance and that they clearly outperform Si as a result of their superior physical material properties. So it comes at no surprise that the majority of the GLBC finalist teams employed WBG technology in their converter prototypes: 10 teams were using normally-off GaN high electron mobility transistors (HEMTs) including both p-type gate structure [8] and gate injection technique [9] (gate injection transistor – GIT), 3 teams were using SiC MOSFETs and only 2 teams were using Si MOSFETs. Interestingly, the performance advantage decreases with decreasing voltage blocking capability and at 100 V rated voltage, GaN and Si devices are showing similar performance.

Eventually, the authors selected GaN over SiC, because GaN HEMT technology was available in ultra-compact surface mounted devices (SMD) packages ($(8 \times 8 \times 1.3)$ mm^3) allowing to minimize parasitic loop inductances (e.g., power and gate-source loop inductance) and, in combination with

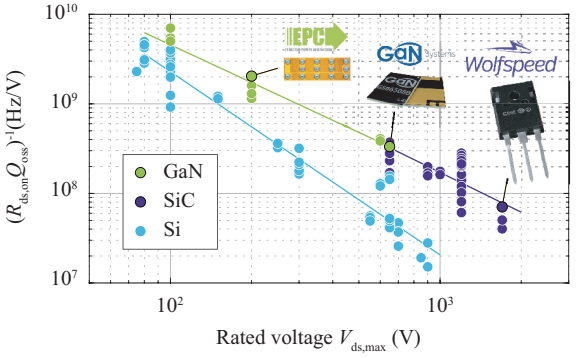

Fig. 2. FOM = $1/(R_{\mathrm{ds,on}}Q_{\mathrm{oss}})$ for the majority of commercially available Si, $R_{\mathrm{ds,on}}Q_{\mathrm{oss}}$ SiC and GaN power semiconductors in dependency of the rated blocking voltage [7].

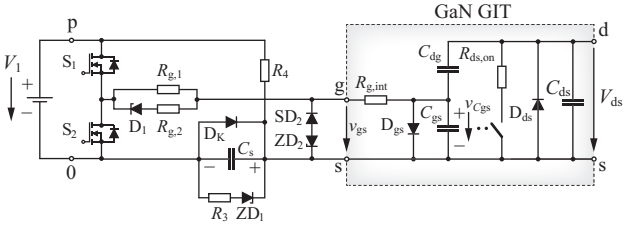

Fig. 3. Proposed improved GaN GIT gate drive circuit [10], [11] to guarantee a reliable gate drive operation with consistent performance regardless of duty-cycle and switching frequency.

an adequate gate drive, achieving lowest possible switching losses. In particular, due to a close collaboration with a large power semiconductor manufacturer, 600 V/70 mΩ GaN GIT devices were at the authors disposal throughout the competition. The very high switching speeds (high $\mathrm{d}v_{\mathrm{ds}}/\mathrm{d}t$), the very low gate-source threshold voltage of $V_{\mathrm{gs,th}} \approx 1.2$ V and the diode characteristic of the gate-source terminals, required a sophisticated and reliable gate drive circuitry which was not met with state-of-the-art concepts. Thus, a new GaN GIT gate drive circuit as depicted in Fig. 3 was proposed [10], [11] which (i) allows to generate a bipolar (≈ +4 V/ − 6V) gate drive voltage from a single supply voltage, (ii) ensures the required quiescent current of 10 mA to keep the device safely in the on-state, and (iii) enables operation of the gate drive independent of duty-cycle and switching frequency. The performance of the

gate drive was verified for switching frequencies up to 1 MHz and the reliability was successfully tested under hard switching conditions with $dv_{ds,max}/dt$ stresses above 500 kV/μs. The reader is referred to [10] for a detailed explanation of the working principle and experimental results.

Although the performance of the latest generation of power devices (including Si) is ever improving, still no "ideal switch" is available on the market. At 400 V DC-link voltage and 15 A hard-switched current, a dissipated energy in the order of 50–60 μJ per totem-pole bridge-leg and switching cycle must be expected for GaN GIT technology [10] which clearly prohibits switching frequencies in the MHz range. With zero voltage switching (ZVS), however, the dissipated energy can be reduced by a factor of about 10 to ≈ 5 μJ per bridge-leg and switching cycle [12], [13]. Still, the remaining soft-switching losses of the GaN semiconductor technology are detrimental to the efficiency and, because of the increase in cooling effort, also to the power density and thus still prevent a multi-MHz operation.

A major aspect in this context is the accurate quantification and the identification of the origin for the remaining ZVS losses in GaN [12], [13]. As described in more detail in Appendix A, lossy charging and discharging of the power transistor's parasitic output capacitance, C_{oss}, is the reason behind the observed power loss at very high switching frequencies despite employing a soft-switching modulation scheme.

2) Bridge-Leg Control Strategies: By means of the widely accepted triangular current mode (TCM) control technique [14], [15], ZVS of a bridge-leg can be achieved in every operating point throughout the AC period and switching frequencies up to ≈ 1 MHz can be attained. Depending on the input and output voltage of the bridge-leg (cf., Fig. 4 (a)), the turn-on and turn-off intervals are computed such that a triangular shape of the filter inductor current results, which features on average over a switching cycle the required output current $\bar{i}_L = i_o$. In addition, the output current direction is reversed before each second switching transition, such that after turning off the previously conducting switch the output current $\bar{i}_L$ leads to a switching node voltage transition by charging/discharging the parasitic output capacitances, C_{oss}, of the switches and thus the complementary switch can be softly turned-on (cf., Fig. 4 (b)). To account for the changing operating point, that is output voltage and current, the timing intervals of a switching cycle are adjusted throughout the AC period. One strategy is to keep a constant minimum switched current needed to perform a complete resonant transition within a defined maximum dead time interval as depicted in Fig. 4 (c). In case of the positive AC half-cycle this minimum current has negative polarity and vice versa. The resulting switching frequency varies over time as illustrated in Fig. 4 (e).

One of the major challenges is to reliably implement TCM control with switching frequencies up to the MHz range. The difficulty is that (i) there are no compact current transducers available which would satisfy the bandwidth requirements and (ii) conventional microcontrollers are often too slow

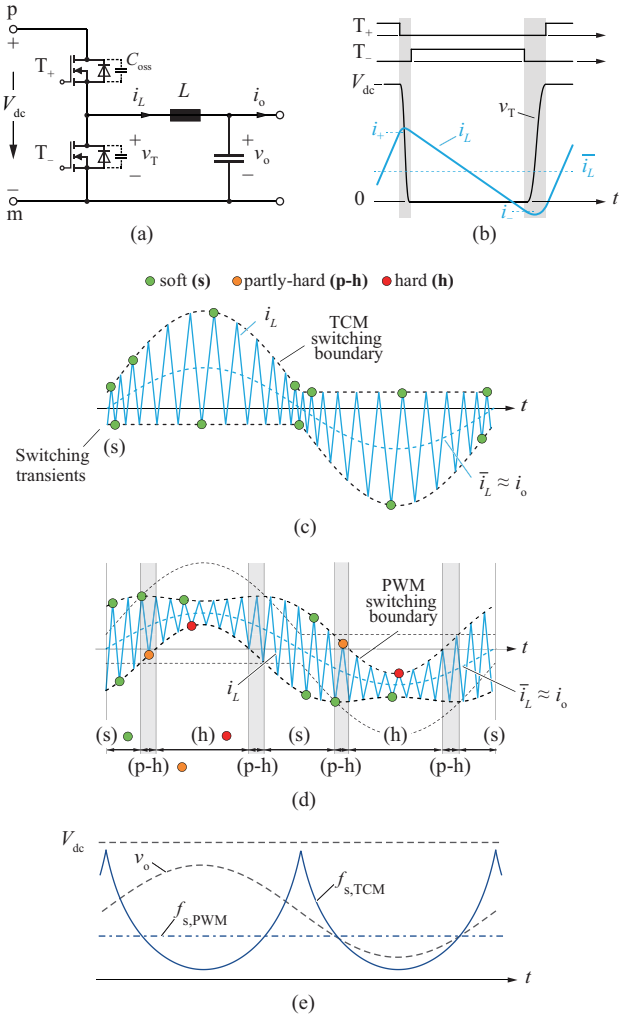

Fig. 4. (a) Bridge-leg with DC-link referenced filter (synchronous buck-type converter) explicitly showing the parasitic output capacitance C_{oss} of the power transistors. (b) Detail of the TCM current waveform within a switching cycle. Schematic inductor current waveform over the course of an AC period for (c) TCM control of the bridge-leg where the current to perform ZVS is kept constant and (d) PWM control of the bridge-leg where the constant switching frequency envelope of the inductor current results in different switching transitions: soft-switching (s), partial hard-switching (p-h) and hard-switching (h). (e) Varying and constant switching frequency over the course of the AC period in case of TCM and PWM, respectively.

(difficult to achieve controller execution at several 100 kHz), are lacking enough PWM resolution and simply don't offer enough flexibility to reliably implement TCM control in the MHz range. For this reason, the authors implemented an approach were the basic timing intervals (turn-on, turn-off, dead-time) of the bridge-legs are computed by means of a conventional microcontroller at a repetition rate of around 20 kHz and the actual TCM control was then performed by means of an additional field programmable gate array (FPGA) device running at above 200 MHz. Besides the timing signals coming from the microcontroller, the information of the inductor current zero-crossing (ZC) is also considered in the FPGA to cope with measurement and parameter inaccuracies, and delays introduced

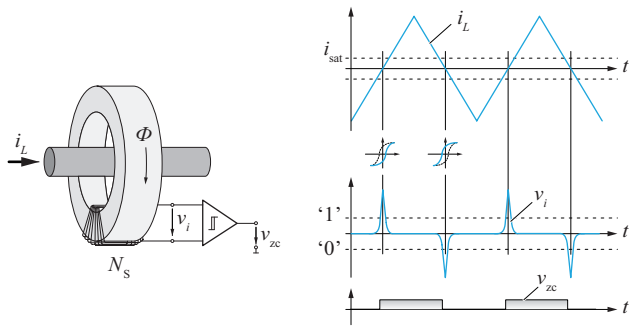

Fig. 5. Zero crossing detection (ZCD) by means of voltage v_i induced in the pick-up coil (N_s = 10 turns) when the magnitude of current i_L falls below the saturation threshold i_{sat} of the employed magnetic core.

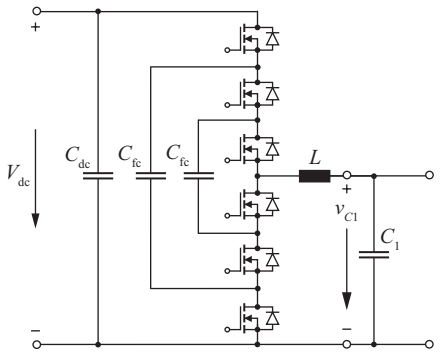

Fig. 6. 4-level flying capacitor bridge-leg with LC output filter.

by the control electronics (gate drive, ZC detector, etc.).

Among several concepts, a magnetic induction based zero crossing detection (ZCD) concept as depicted in Fig. 5 was implemented since it features isolation, low complexity and a high signal-to-noise ratio (SNR). In order to saturate the magnetic core already at low currents, a ferrite core material with low saturation flux density, high permeability over a wide frequency range, and a core shape without air gap should be selected. Furthermore, for minimizing losses, the core volume should be as small as possible. The implemented ZCD, based on a R4 toroidal core (R4 × 2.4 mm × 1.6 mm) using N30 ferrite from EPCOS and a pick-up coil with N_s = 10 turns, was successfully tested at switching frequencies up to 2.5 MHz. Depending on the inductor current slope (di_L/dt), the induced voltage reaches values from 20 V up to 160 V, which makes the ZCD circuit robust against electric disturbances.

In contrast to TCM control, conventional PWM features a constant switching frequency (cf., Fig. 4 (e)) but suffers from high turn-on switching losses which limits the maximal feasible switching frequency. However, this drawback is mitigated by the fact that with a relatively large current ripple, i.e., a design with small filter inductance value, also for PWM the average switching losses can be considerably reduced. As can be seen in Fig. 4 (d), due to the high current ripple, soft-switching during turn-on and turn-off can be achieved around the fundamental current ZCs also with PWM as long as the switched current maintains a certain minimum value to completely charge/discharge the parasitic output capacitances of the half-bridge (cf., (s) in Fig. 4 (d)). If the switched current still shows the correct polarity for a resonant transition, but the amplitude is not large enough to complete the resonant voltage transition within the specified dead time, a partial hard turn-on occurs (cf., (p-h) in Fig. 4 (d)). However, this still causes much lower turn-on switching losses than full hard-switching (cf., (h) in Fig. 4 (d)) [16]. In this way, switching frequencies of a few hundreds of kHz can be applied for constant frequency PWM with the advantage that typically a microcontroller suffices (no need for ZCD circuitry and FPGA for generating switching signals).

3) 2-Level vs. Multilevel Bridge-Leg: In the past, multilevel converters have been employed primarily in high-voltage/high-power applications to overcome the blocking voltage and current limitations of the involved power semiconductors. Recently, multilevel converters became also a popular choice in low-voltage (400 V) applications, since the higher component count and realization effort can be justified by two key features beneficial to achieve a high power density: A first major advantage of the multilevel converter is the reduction of volt-seconds applied to the filter inductor and the resulting drastic reduction in filter size. Since the amplitude of the voltage steps applied to the filter inductor is only $V_{dc}/(N-1)$ and the effective pulse frequency is $(N-1)f_{sw}$, where N is the number of voltage levels, a multilevel inverter can have an $(N-1)^2$ times smaller filter inductor compared to a 2-level converter at same filter inductor current ripple. Second, the performance of Si and WBG power devices with respect to the FOM given by (1) (cf., Section III-A1), is inversely proportional to the rated blocking voltage raised to the power of 1.4–2.0. According to this scaling law and for the same total switching loss, a multilevel converter can exhibit lower total on-state conduction loss compared to a 2-level implementation, despite that several low-voltage devices are connected in series [17]. In order to implement a larger number of voltage levels (> 5), the cascaded H-bridge, the multiple point clamped (MPC) and the flying capacitor (FC, cf., Fig. 6) topologies are commonly suggested in literature [18], [19]. Since only a single DC voltage source and no additional clamping diodes are required, the FC multilevel converter is particularly well suited to achieve a high power density as was demonstrated by one of the GLBC finalists [20], [21].

However, a clear limitation of the multilevel approach is the extra volume occupied by the gate drive circuitry since the stacked power transistors comprising the multilevel bridge-leg require individual control signal and gate drive supply voltage isolation. Furthermore, the capacitor voltage balancing of multilevel converters is crucial as a deviation from the nominal values can lead to harmonics and distortions in the AC output voltage and/or can even lead to system failure. In case of the FC multilevel converter, it is known that with phase-shifted PWM (each switching cell has a dedicated phase-shifted carrier signal) the individual capacitor voltages are passively balanced during stationary operation (natural balancing). However,

because of poor balancing dynamics under certain operating conditions, a deviation from the nominal FC voltages is likely to occur during critical operating modes such as load transient and system start-up, and can cause an over-voltage across the transistors and/or permanently damage the system [22]. For the above mentioned reasons and due to the performance advantage of 600 V GaN over Si, the authors eventually selected the conventional 2-level bridge-leg design for the implementation of the Little Box.

4) Multi-Gap Inductor Design: With reference to Section III-A2, the likely operating conditions of a high-frequency (HF) filter inductor in a high power density inverter—large current ripple and high frequency—demand for a sophisticated design to keep the winding and core losses to a minimum and achieve a low component volume. The large current ripple dictates a very high copper filling factor and the high switching frequencies up to the MHz range demand MnZn ferrite core materials with very low specific core loss density (e.g., DMR51, N87, PC200, 3F4). Inductors realized with highly permeable ferrite materials require a discrete air gap in the magnetic circuit to prevent saturation of the core material and/or to tune the inductance value, unlike iron-powder cores with an inherent distributed gap. This large discrete air gap can be divided into several partial gaps in order to reduce the air gap fringing field and consequently reduce the proximity losses in the winding to promote a very compact design. If the partial gaps are distributed over the entire length of the inner limb of e.g., an E-type or pot core, the H-field in the winding window shows a quasi one-dimensional distribution running in parallel to the inner limb [23]–[25]. This promotes to use copper foil for the winding since the individual layers of the foil are aligned in parallel with the H-field and excessive eddy current losses can be avoided. Due to the higher filling factor of foil compared to HF litz wire, a lower winding resistance can be achieved. Unfortunately, as documented in detail in [26] and briefly summarized in Appendix B, the authors identified that the manufacturing of a multi-gap core structure—composed of multiple stacked MnZn ferrite plates—can lead to a large increase of core loss which potentially outweighs the saving in winding loss due to the fringing field reduction.

As a consequence, the number of partial gaps in the implemented multi-gap inductors used in the Little Box 1.0 prototype (LB 1.0, cf., Section II of Part B) was reduced from originally 50 to only 24 gaps in the final inductor design in order to lower the resulting core losses. Since no effective measure could be identified to minimize the surface related core losses [26], a conventional single-gap inductor design with HF litz wire (instead of foil) was adopted for the implementation of the Little Box 2.0 (LB 2.0, cf., Section III of Part B).

B. Compensation of the 120 Hz Power Pulsation

One of the key technical challenges in the implementation of the Google Little Box was to shrink the volume of the energy storage required to cope with the twice mains-frequency (120 Hz) pulsating power at the AC side while meeting the stringent 2.5% DC input voltage ripple. In a conventional inverter design, typically bulky electrolytic capacitors C_{dc} are installed to continuously absorb and release energy,

$$\Delta E = \int_0^{\pi} S \cdot \sin(\varphi) \cdot \frac{1}{2\omega} \mathrm{d}\varphi = \frac{S}{\omega} = 5.3\ \mathrm{J}, \tag{2}$$

where S is the apparent power as listed in Table I. This fluctuating energy can also be expressed as a function of the capacitor voltage ripple Δv,

$$\begin{aligned} \Delta E &= \frac{1}{2} C_{dc} \left[(V_{dc} + \Delta v/2)^2 - (V_{dc} - \Delta v/2)^2 \right] \\ &= C_{dc} \cdot \Delta v V_{dc}, \end{aligned} \tag{3}$$

which allows to determine the minimum DC-link buffer size as

$$C_{dc} \geqslant \frac{\Delta E}{\Delta v V_{dc}} = \frac{5.3\ \mathrm{J}}{(2.5\% \cdot 400\ \mathrm{V}) \cdot 400\ \mathrm{V}} = 1.3\ \mathrm{mF}, \tag{4}$$

in order to meet the voltage ripple specification. However, conventionally installed electrolytic capacitors are poorly utilized since only $\Delta E/(1/2 C_{dc} V_{dc}^2) = 5.1\ \mathrm{J}/104\ \mathrm{J} = 4.9\%$ of the average stored energy is actually used for the buffering process.

As an alternative concept to suppress the input voltage ripple, a series resonance $L_f C_f$-circuit constituting a notch-filter at twice the AC frequency could be installed in parallel to the DC-link as shown in Fig. 7 (a). However, besides the unreasonably large inductance value L_f, the main disadvantage of this approach are the high voltages occurring across the filter components and the comparably high losses occurring in L_f.

Fig. 7 (b) shows the typical two-stage configuration known from PV inverter systems, where the first DC/DC stage decouples the buffer capacitor C_b from the system input and regulates the input voltage V_{dc} such that the PV module is operated at it's maximum power point (MPP). Since the maximal voltage swing across the buffer capacitor C_b is not restricted by the specified 2.5% input ripple requirement anymore, the size of C_b can be significantly reduced. However, the buffer capacitor voltage v_b cannot fall below 340 V for a proper operation of the inverter. A clear disadvantage in terms of overall efficiency is that the entire power flowing from the DC-source to the load is being processed by two converter stages.

In order to only cope with the fluctuating power, the usage of additional auxiliary converters in various configurations, typically equipped with a dedicated buffer capacitor exhibiting a wide voltage fluctuation, has been thoroughly studied in literature and a comprehensive overview is given in [27]–[31].

Main concepts relevant for and/or employed in the GLBC are briefly described in the following. Fig. 7 (c) depicts the PCI approach [5], [32]–[35], where the buffer converter connected in parallel at the converter DC input injects a current i_b to compensate the fluctuating portion of current $i = p_{ac}/V_{dc}$, which ideally results in a constant input current i_s and consequently in a constant voltage V_{in} at the converter input.

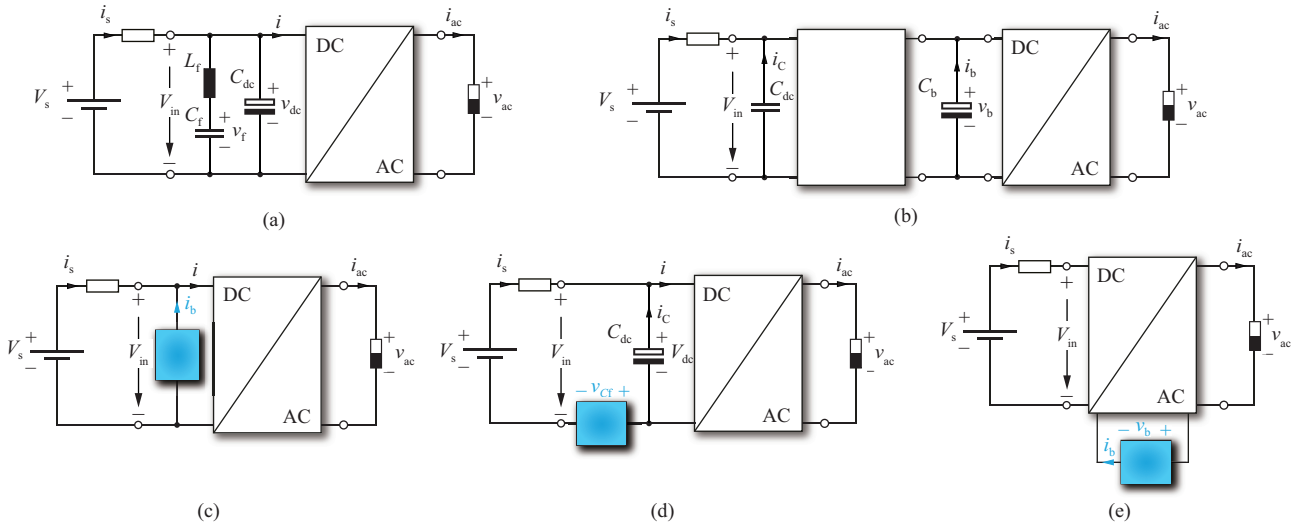

Fig. 7. Several passive and active power pulsation buffer approaches to meet the GLBC input voltage V_{in} (= V_{dc}, dependent on the employed power buffer concepts) ripple requirement and reduce the size of the buffer capacitor. (a) Double-line frequency notch-filter. (b) Two-stage approach with preceding DC/DC stage. (c) Parallel current injector (PCI) buffer approach. (d) Series voltage injector (SVI) compensating the residual fluctuation of the DC-link voltage. (e) Inverter with built-in active power buffer (AC-side).

In a different approach as described in [36], depicted in Fig. 7 (d), and employed by one of the GLBC finalists [37], [38], conventional passive capacitive buffering of the DC-link is used, however, the total installed capacitance value is less than what would actually be needed to comply with the 2.5% voltage ripple requirement. In order to meet the specified input voltage ripple, an additional series voltage injector (SVI) converter impresses voltage v_{Cf} which compensates the residual 120 Hz voltage ripple still present in v_{dc} resulting in a constant input voltage V_{in}. The key advantage of this concept is that the SVI converter can be implemented with low-voltage (LV) components and only processes a small share of the entire fluctuating power, $\hat{p}_{SVI} = I_s \cdot \hat{v}_{Cf} \approx 100$ W, since, for a defined DC-link capacitance of around 400–600 μF, the amplitude of v_{Cf} required to compensate the remaining voltage ripple only amounts to approximately 20 V and $I_s = 5$ A in the nominal operating point (cf., Table I). As described in [39]–[41], i.e., publications of another GLBC finalist, also the PCI buffer concept (cf., Fig. 7 (c)) can be realized by means of a partial-power processing auxiliary converter if an additional DC-blocking capacitor (stacked on top of the auxiliary converter and jointly forming the parallel branch) is employed.

Fig. 7 (e) depicts the AC-side or built-in power buffer concept presented in [30], [42]–[46], where part of the main inverter circuit and control system is shared with the active power buffer. To give a specific example, in the concept presented in [30], [42], a virtual, unbalanced 3-phase system in established by introducing an additional inverter bridge-leg and connecting the buffer capacitor to the neutral phase of the inverter. Depending on the output power level and power factor, the amplitude and phase-shift of the buffer capacitor voltage v_b is adjusted such that the pulsating AC power is compensated.

It should be noted, that regardless of the employed buffer

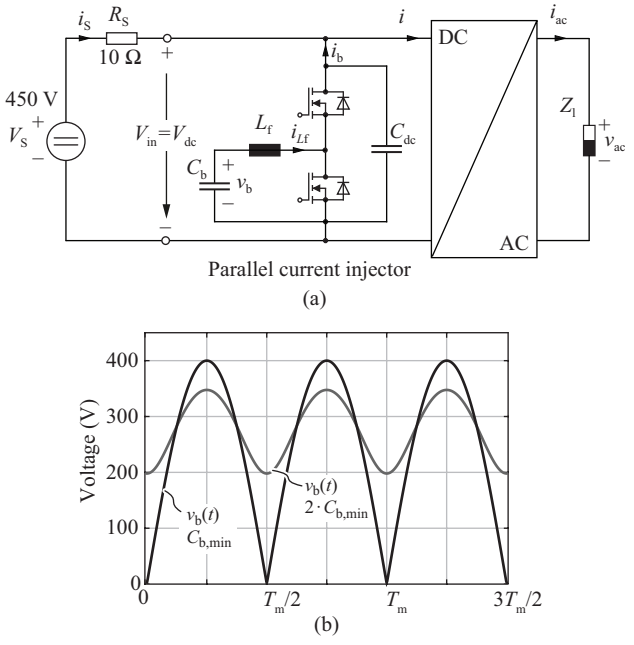

Fig. 8. (a) Synchronous buck-type implementation of the PCI power buffer concept. (b) Characteristic buffer capacitor voltage waveforms for different capacitance values.

approach, at least 15–20 μF of capacitance C_{dc} is installed in the DC-link in order to eliminate switching noise and to reduce the commutation loop inductance of the bridge-legs of the inverter stage.

The authors selected the synchronous buck-type implementation of the PCI buffer concept [5], [32] shown in Fig. 8 (a) as most promising approach due to several reasons as discussed in the following.

First, only a single capacitor is needed for the implementation of the buck-type PCI buffer and, as can be seen from the

characteristic buffer capacitor voltage waveform of the buck-type PCI in Fig. 8 (b), operating the auxiliary converter with the minimum buffer capacitance value of

$$C_{\mathrm{b,min}} = \frac{2S_{\mathrm{b}}}{\omega V_{\mathrm{dc}}^{2}} = 66.3\,\mu\mathrm{F} \tag{5}$$

results in a perfect utilization of the buffer capacitor. In order to provide voltage margin to cope with load transients, it is more reasonable to install at least $2 \cdot C_{\mathrm{b,min}}$ which reduces the voltage swing at the buffer capacitor (cf., Fig. 8 (b)). Second, the GaN bridge-leg design of the main inverter can be reused for the implementation of the PCI buffer which keeps the overall engineering effort and system complexity reasonable. Moreover, the stand-alone architecture allows to design and test the PCI buffer independent from the inverter and, due to the feasible DC-bias voltage, is expected to perform better during abrupt load transients since there is always energy stored in the capacitor as opposed to the built-in/AC-side active power buffer concept.

1) Buffer Capacitor Design: As a consequence of the large feasible buffer voltage ripple of the considered buck-type PCI (cf., Fig. 8 (b)), comparably small capacitance values in the range of 100–200 μF are needed, thus realizing the buffer capacitor with ceramic capacitor technology becomes a viable option. Since the effective energy density of electrolytic capacitors is reduced due to lifetime related current stress constraints, 2.2 μF/450 V class II X6S MLCC and 2 μF/500 V CeraLink capacitors were identified to be the most promising candidates for realizing an ultra-compact power buffer [47]–[49]. Striving for maximal compactness in the GLBC, film capacitors were not considered in the power buffer design because of their low energy density compared to ceramic capacitors. However, film capacitors could be an interesting option if the main motivation for the replacement of electrolytic capacitors are the associated reliability concerns and not a high compactness.

Since the prevailing capacitance of the considered ceramic capacitors, class II/X6S MLCC and CeraLink, strongly depends on the actual operating point, that is DC-bias voltage and superimposed 120 Hz AC voltage ripple, the capacitance and loss density maps were experimentally determined in order to optimally dimension the buffer capacitor. From the analysis described in more detail in Appendix C, it can be concluded that the CeraLink capacitor features a slightly higher capacitance density but the power losses caused by the 120 Hz voltage ripple are much higher than those of the class II/X6S MLCC which ultimately translates into lower efficiency and larger cooling volume of the PCI buffer. However, one of the undisputable advantages of the CeraLink capacitor technolgoy are the higher maximum rated operating temperature of 125 °C and the advanced packaging options—available in a package with 20 chips mounted in parallel by means of a silver sintered connection onto a common lead-frame—for an uncomplicated and reliable mechanical assembly. On the contrary, the class II/X6S MLCC is only available as single chips which makes the assembly of large capacitor blocks very challenging. Moreover, stacking of several MLCC chips to achieve a very tight packaging poses a major reliability risk.

2) Control System for the Active Power Buffer: One drawback of using an active approach to cope with the 120 Hz power pulsation is the required control system which significantly increases the overall complexity of the inverter system compared to purely passive DC-link buffering with electrolytic capacitors. The objectives of the envisioned buffer control system are (a) the compensation of the fluctuating AC power by proper DC-link current injection, (b) a tight control of the DC-link voltage during load transients, and (c) the control of the mean/bias voltage of the buffer capacitor. A comprehensive review and comparison of different active power buffer control methods is provided in [50], [51].

The cascaded control system proposed by the authors for the buck-type PCI buffer [5], which combines all aforementioned control objectives into a single reference value for the underlying filter inductor current controller, will be described in more detail in Section II-B of Part B of this publication.

C. EMI & Ground Current Limits

As mentioned in Section II, the parasitic capacitance (≈ 120 nF) formed between the positive and negative terminals of the specified DC source and ground turned out to be larger than first anticipated. For this reason, Google relaxed the originally specified 5 mA ground current limit to 50 mA at a very late point of the competition. This decision was heavily criticized by many contestants because this suddenly allowed inverter concepts which are causing a low-frequency (LF) common-mode (CM) voltage at the output because the higher required CM attenuation of the EMI filter could be achieved fairly easy without significant additional volume by an increase of the installed CM capacitance (Y-capacitors). Since the new 50 mA limit was posted just 1 month before the deadline for the submission of the final technical approach document, it was not possible to revise the converter design and competitors which did not select their inverter concept based on preventing the generation of an LF CM voltage at the inverter output perhaps had a strategic advantage.

Interestingly, the parasitic capacitance formed between actual PV cells and the grounded metallic module case, is in the range of 50–150 nF/kW for crystalline-Silicon PV cells [52], [53], i.e., in the same order of magnitude as specified in the GLBC. To provide galvanic isolation for safety reasons and prevent the flow of ground currents between the PV panels and the utility grid, PV converter systems type either incorporated HF transformers at the DC-side or LF transformers at the AC side in the past. However, the demand for converters with higher efficiency, higher power density and lower cost, eventually led to the adoption of transformerless inverter designs. Due to the high parasitic capacitance of the PV modules, the ground current problem in single-phase PV inverter systems was thoroughly investigated both in industry and academia [54]–[57]. As detailed in [54], both the selected modulation technique (unipolar vs. bipolar PWM) and the

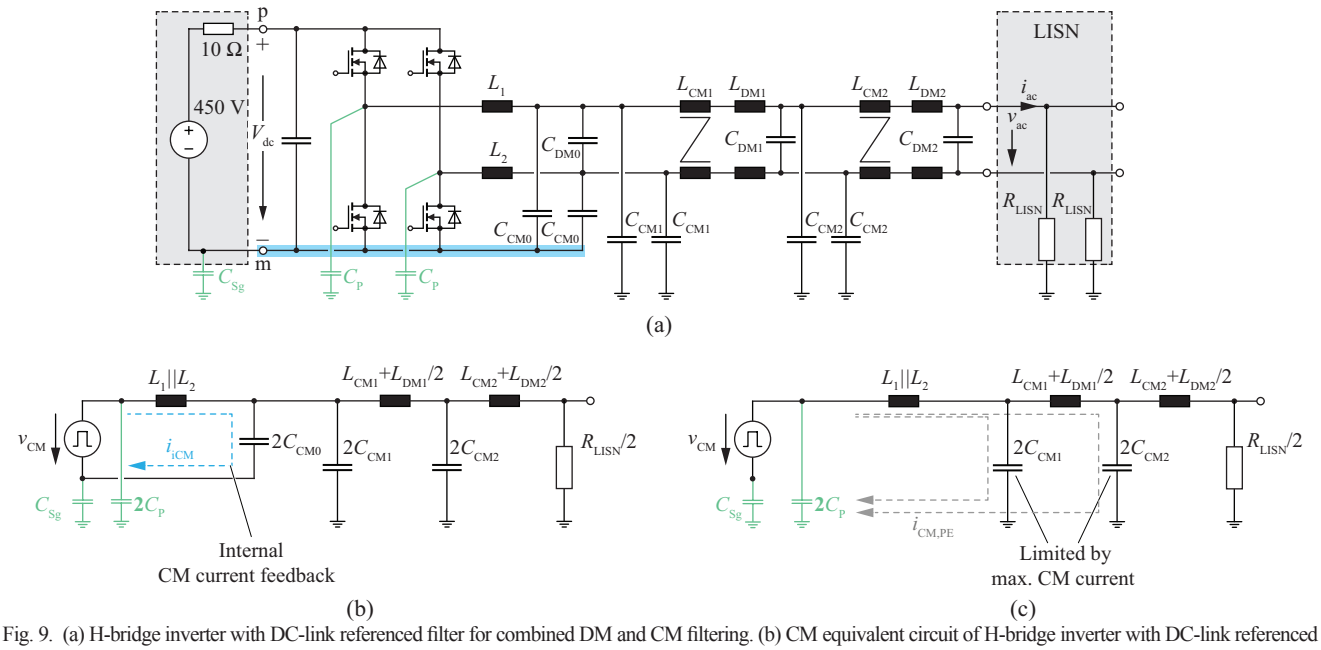

Fig. 9. (a) H-bridge inverter with DC-link referenced filter for combined DM and CM filtering. (b) CM equivalent circuit of H-bridge inverter with DC-link referenced filter showing the internal CM current feedback introduced by C_{CM0}. (c) CM equivalent circuit of H-bridge inverter with conventional DM output filter.

inverter topology (half-bridge vs. H-bridge inverter design) affects the generation of CM voltages.

It is well known that the 2-level H-bridge inverter (cf., Fig. 9) can be operated with bipolar PWM which results in a constant CM voltage, $v_{cm} = V_{dc}/2$, throughout the PWM cycle, i.e., no switching frequency component of v_{cm} occurs, but utilizes both voltage polarities, $v_{dm} = \{+V_{dc}, -V_{dc}\}$, to generate the desired output voltage. This effectively solves the issues of leakage currents but results in a larger current ripple and larger differential-mode (DM) EMI noise, as opposed to unipolar PWM which utilizes also the zero-voltage state, $v_{dm} = \{+V_{dc}, 0, -V_{dc}\}$. Because of the resulting 3-level voltage waveform with twice the effective switching frequency which reduces the output filter size and potentially improves efficiency (smaller current ripple), unipolar PWM is widely accepted in industry. However, by introducing a zero-voltage state where either both high-side or both low-side switches of the H-bridge are turned on, HF pulsed CM voltage is being generated at the output.

With the aim of using unipolar PWM and still preventing the generation of CM voltage, inverter topologies with additional decoupling circuits have been proposed which disconnect the switching stage from the DC source during the free-wheeling state. Relevant DC-based decoupling topologies include but are not limited to the H5 inverter [58], the active clamped H6 inverter [59] and the passive clamped H6 inverter [60]. Relevant AC-based decoupling topologies include the HERIC inverter [61] and the HBZVR-D inverter [62]. Since the additional power semiconductors utilized in the DC-or AC-based decoupling networks cause additional power losses, increase the volume of the switching stage, and because 3rd party IP was not permitted as stated in the legal terms and conditions of the GLBC, a different approach based on the conventional H-bridge inverter but with a new output filter arrangement for the combined attenuation of DM and CM noise was adopted by the authors. Details are described in the following.

1) DC-Link Referenced Output Filter: Fig. 9 (a) shows the H-bridge inverter with the proposed DC-link referenced filter arrangement and subsequent 2-stage EMI filter. As can be seen, each bridge-leg is equipped with an individual LC filter, where the filter capacitor, C_{CM0}, is connected between the respective phase and the negative DC-link terminal m. The corresponding CM equivalent circuit of the H-bridge inverter with proposed DC-link referenced output filter and conventional DM output filter is illustrated in Fig. 9 (b) and (c), respectively. It can be seen that the filter capacitor C_{CM0} introduces a CM current feedback in the equivalent circuit. Since the capacitance of the C_{CM0} is not limited by the maximal allowed ground current, a large portion of the ground current can be confined already within the switching stage which contributes to a reduction of the EMI filter volume (smaller CM chokes). It is of course also possible to include additional filter capacitors referenced towards the positive DC-link terminal p (cf., Fig. 2 in Part B of this paper). The reference to both DC-link terminals promotes a quasi-constant effective filter capacitance even if ceramic capacitors are employed because the configuration counteracts the nonlinear dependency of capacitance on voltage.

2) 1 vs. 2 HF Bridge-Leg Inverter Designs: The inverter with LF unfolder discussed in [63]–[66] and is shown in Fig. 10 (a), employs a single HF bridge-leg with LC output filter (synchronous DC/|AC| buck converter) to generate a rectified sinusoidal voltage, $v_{C1} = |\hat{V}_o \cdot \sin(\omega t)|$, and subsequently performs |AC|/AC unfolding by means of an LF H-bridge. Since this inverter concept only requires an single HF bridge-leg with HF filter inductor, as opposed to the H-bridge inverter (cf., Fig. 9 (a)) with two HF bridge-legs and two HF filter inductors, potentially a higher power-density can be achieved.

Considering a reversed power flow direction, one can

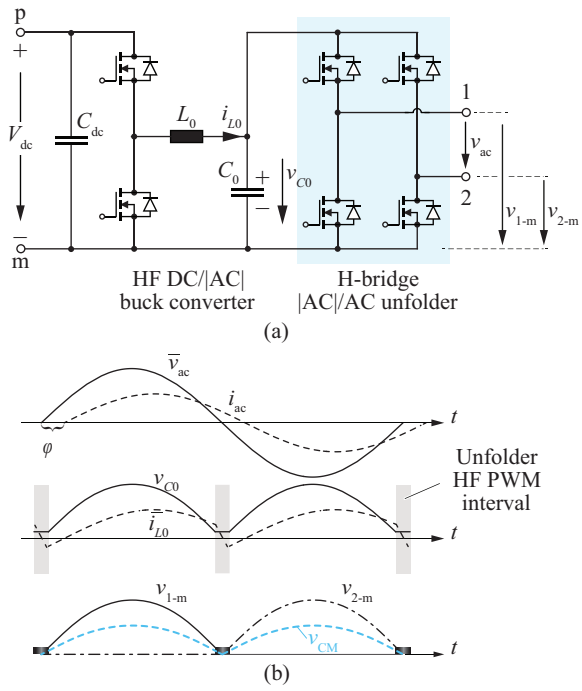

Fig. 10. (a) Topology of the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter; Synchronous DC/|AC| buck converter stage generating a rectified sinusoidal voltage and subsequent H-bridge performing the |AC|/AC unfolding. (b) Characteristic waveforms and resulting low-frequency CM voltage.

immediately notice that the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology actually corresponds to a well-known conventional PFC boost rectifier [67], where the input diode bridge is substituted by an active unfolder H-bridge. In order to prevent voltage/current distortions around the AC voltage ZCs known from such power factor correction (PFC) rectifier systems, to allow a proper control of the output current during transients, and to support current control for reactive loads where voltage and current are out of phase, the authors proposed a mode of operation where the buck-stage output voltage is kept above a defined minimum voltage, $v_{C0,\min} \approx$ 25−50 V, and the unfolder H-bridge is temporarily operated with HF PWM to ensure the correct AC output voltage. In Fig. 11 (a) and (b) characteristic waveforms are depicted for bipolar and unipolar PWM operation of the unfolder stage, respectively. Since only a low voltage level is switched during a short interval of the AC period, switching losses of the unfolder H-bridge are negligible.

However, compared to the H-bridge inverter with two HF bridge-legs, a clear drawback of the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter is that an LF CM component of the output voltage,

$$v_{\mathrm{cm}} = \frac{v_{1-\mathrm{m}} + v_{2-\mathrm{m}}}{2} = \hat{V}_{\mathrm{ac}}/2 \cdot \left|\sin(\omega t)\right|, \qquad (6)$$

with spectral components at even multiples of the AC frequency is being generated as illustrated in Fig. 10 (b). However, since it is possible to employ the combined DM and

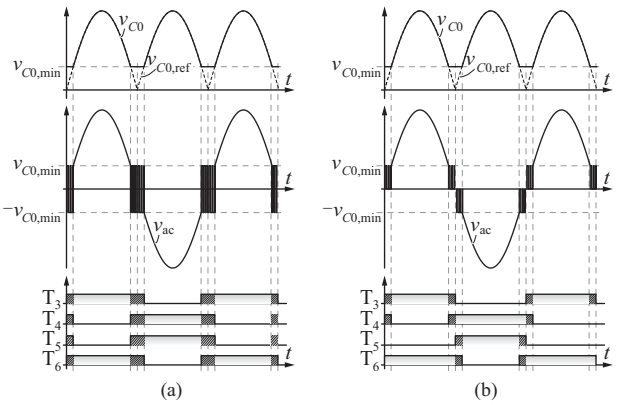

Fig. 11. Clamping of the DC/|AC| buck-stage output voltage of Fig. 10 (a) to $v_{C0,\min} > 0$ and temporary operation of the unfolder H-bridge with (a) bipolar and (b) unipolar HF PWM to prevent distortions around the zero-crossing of the AC voltage.

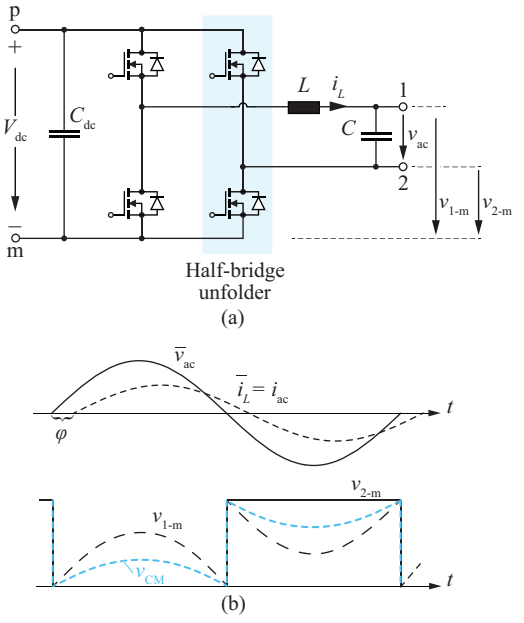

Fig. 12. (a) Half-bridge unfolder based inverter topology resembling an H-bridge inverter with asymmetrical bridge-leg filter configuration (only HF bridge-leg is equipped with filter inductor). (b) Characteristic waveforms and resulting low-frequency CM voltage.

CM filter structure as described previously in Section III-C1 (cf., Fig. 9 (a)), where the DC-link referenced filter capacitors allow to confine a large portion of the CM current within the converter, and because of the reduced size of the required CM chokes the implementation of a compact EMI filter is feasible.

As known from totem-pole bridgeless PFC rectifiers, the line-frequency unfolding can also be performed utilizing one of the two bridge-legs of the H-bridge inverter as shown in Fig. 12 (a). During the positive half-cycle of the AC voltage, the LF bridge-leg connects phase 2 to the negative input terminal m and during the negative AC half-cycle to the positive input terminal p. It follows that the HF bridge-leg must generate the voltage,

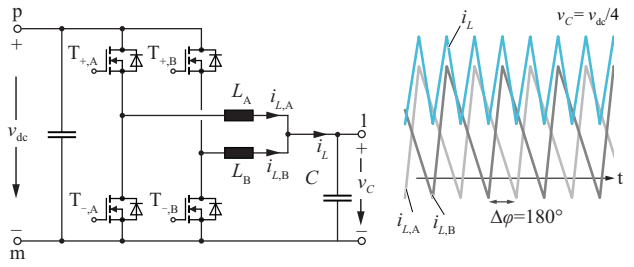

Fig. 13. Interleaving of bridge-legs in order to decrease conduction losses and/or reduce the size of the output and EMI filter due to current ripple cancellation and increase of the effective output frequency.

$$\underline{v}_1 = \begin{cases} \hat{V}_{ac} \sin(\varphi), & \text{for } 0 \leqslant \varphi \leqslant \pi \\ V_{dc} - \hat{V}_{ac} \sin(\varphi), & \text{else} \end{cases} \quad (7)$$

as output of phase 1 with respect to m in order to obtain the desired sinusoidal output voltage as shown in Fig. 12 (b). Accepting a more challenging control due to the rapid change of the phase voltage reference around the ZCs, lower conduction losses are achieved as compared to the H-bridge unfolder (cf., Fig. 10 (a)) with two switches in the conduction path. However, the half-bridge unfolder inverter has a clear drawback concerning the generated LF CM voltage and/or the CM filter effort. The LF CM voltage shown in Fig. 12 (b) exhibits high dv/dt transitions around the ZCs and therefore, a DC-link referenced filter cannot be applied, which means that the CM filter capacitors (Y-capacitors) are limited to a maximum allowed value to comply with the specified ground current limits which in turn results in larger CM chokes of the EMI filter. Hence, the larger EMI output filter effort has to be weighted against the slightly lower efficiency and higher circuit complexity of the H-bridge unfolder approach.

3) 4D-Interleaving of Bridge-Legs: In order to decrease conduction losses and/or reduce the size of the output filter and/or EMI filter, parallel connection and phase-shifted operation of multiple HF bridge-legs as depicted in Fig. 13 is a well known concept. If the two bridge-legs ($T_{+,A}$, $T_{-,A}$ and $T_{+,B}$, $T_{-,B}$) are operated with half a pulse interval phase shift, i.e., the switching frequency ripple components of the inductor currents $i_{L,A}$ and $i_{L,B}$ are phase-shifted by $\Delta\varphi = 180°$, which is referred to as symmetric interleaving (in general $\Delta\varphi = 360°/n$ for n interleaved bridge-legs), the harmonics of $i_L = i_{L,A} + i_{L,B}$ are cancelled at odd multiples of the switching frequency and the size of the output filter can be reduced [68], [69].

For the case of having two bridge-legs in parallel it can be argued that the conduction losses are halved but the total switching losses remain, since two bridge-legs are switched at half the current. However, this only holds if the dissipated energy per switching cycle is linear with respect to the switched current, i.e., $E_{loss}(I_{sw}) \approx kI_{sw}$. Depending on the semiconductor technology, performance of the employed gate drive and commutation loop inductance, in practice there is often a more quadratic

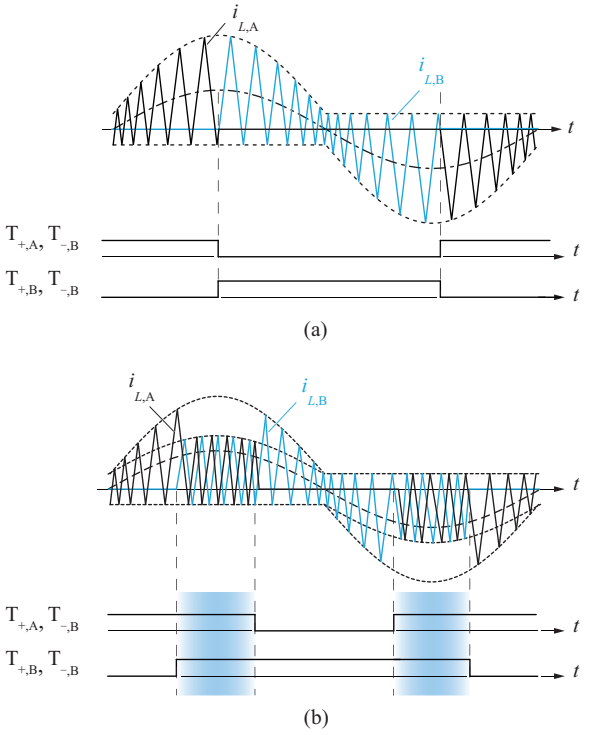

Fig. 14. Schematic of the current waveforms for the proposed/implemented 4D-interleaving scheme [70] in order to achieve high converter efficiency and low cooling system volume. (a) No interleaving but alternating operation of two bridge-legs at low output power. (b) Interleaved operation of the bridge-legs around the current maximum (peak instantaneous power) at high (average) output power. The width of the interleaving interval in which both bridge-legs are operated is adjusted depending on the actual load.

dependency on switched current with capacitive switching loss offset [12]. It therefore can be argued that at low and moderate output power levels with comparably low conduction losses it can be beneficial in terms of total converter losses to operate only a single bridge-leg. In order to still share the losses between both bridge-legs and thus keep the operating temperature of the power transistors as low as possible, alternating operation of the interleaved bridge-legs over an equal interval within the AC period as indicated in Fig. 14 (a) is advantageous. At higher output power levels, when conduction losses start to become dominant, both bridge-legs are operated simultaneously as shown in Fig. 14 (b). Naturally, the overlapping interval when both bridge-legs are active is centered around the peak value of the output current (maximum instantaneous power for cos $\varphi_0 = 1$) and broadens with increasing output power. Since the bridge-legs are located at different positions in space (3D) and the interleaving interval is a function of time (1D), this novel concept proposed/adopted by the authors for the implementation of the Little Box 1.0 (cf., Section II in Part B of this publication) is denominated as 4D-interleaving [4], [70]. The optimal overlap resulting in highest efficiency while meeting EMI limits, can be predetermined for all operating points and stored in a look-up table (LUT) or can be calculated online by means of a learning algorithm.

D. 60 °C Temperature Limit

Arranging all converter components tightly to achieve a minimum construction volume is challenging and typically an iterative design process. Bulky components of different shape and size such as the output and EMI filter passives must be arranged to achieve minimum volume while facilitating a good electrical layout of the printed circuit board (PCB). At the same time, a cooling system is required for dissipating the component losses and/or to keep the temperature of the enclosure and any accessible part of the converter below 60 °C for a maximal ambient temperature of 30 °C, as stated in the GLBC technical requirements. The component arrangement must also allow for air ducts to cool components which are not directly connected to the baseplate of the heat sink or additional heat conduction elements, e.g., copper plates or heat pipes, must be incorporated to enable heat transfer from the lossy components to the heat sink.

As described in more detail in Appendix D, a parallelfin type heat sink design with blowers performs best for comparably long cooling units with a large baseplate area for direct component attachment. Because of the flat dimensions of the blower, a sandwich-like arrangement with two heat sinks at the top and bottom and the converter in the center is possible and has been used for the implementation of the Little Box 1.0 (cf., Fig. 3 in Part B of this paper). A heat sink design with fans performs best when the total length of the cooling unit is short. Thus, this configuration is well suited for a component arrangement where only the power transistors are attached to the heat sink and the filter passives are cooled by the air flow exiting the heat sink as realized for the Little Box 2.0 (cf., Fig. 11 in Part B of this paper).

Finally, for a cooling system with given performance (cf., cooling system performance index (CSPI, see Appendix D), the questions arises whether it can be beneficial to allow a heat sink temperature above 60 °C and to introduce an additional thermal insulation layer as schematically shown in Fig. 15 (a). This question is quantitatively addressed in Fig. 15 (b), where the total volume of the cooling system (including insulation layer) to dissipate 40 W of losses is depicted as a function of the heat sink temperature for two different CSPI values and cubic shape of the heat sink (worst case consideration with minimum surface per volume ratio). As can be seen clearly, to achieve a minimum volume of the cooling system it is best to select a heat sink temperature of 60 °C, and to exclude the thermal insulation layer.

E. Time-to-Market

On July 22nd, 2015, exactly one year after the technical requirements of the GLBC were posted, the technical approach document with details about the selected concept and the achieved prototype performance had to be submitted by the participants. In this respect, another key challenge was the comparably short given time-frame of just one year to design, implement and test a complete cutting-edge converter system

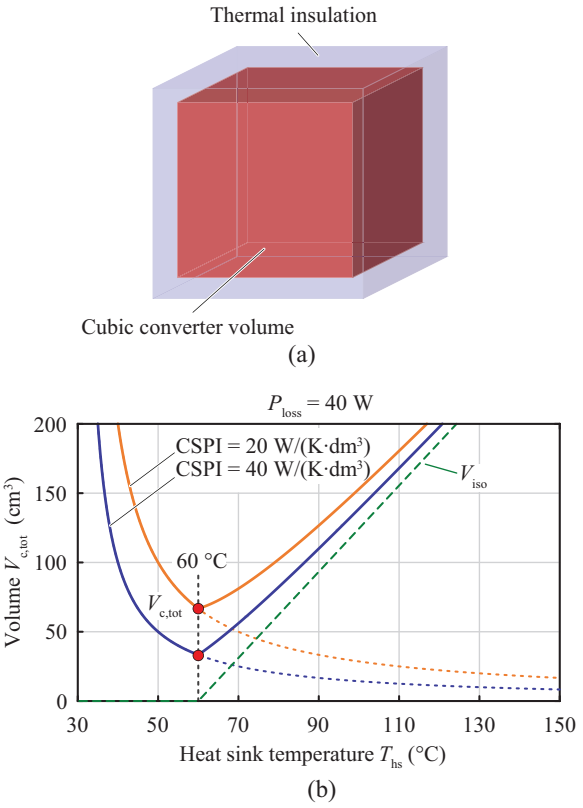

Fig. 15. (a) Heat sink with additional thermal isolation layer to allow operating temperatures above 60 °C. (b) Total volume of cooling system as a function of heat sink temperature.

from scratch. This comparably short time-to-market did only allow for few hardware iteration cycles and might also explain why none of the presented prototypes [3] relied on advanced 3D integration techniques such as PCB embedding of active and passive components [71].

In order to overcome this challenge and expedite the development process, the authors relied on a multi-objective Pareto optimization, also referred to as virtual prototyping, to obtain the best set of system parameters in a very short period of time. The authors comparative evaluation of the $\eta\rho$-performance of two selected inverter concepts will be presented in the next section.

IV. Comparative Evaluation of Inverter Concepts Selected by the Authors

Based on the main considerations of the authors to overcome the design challenges of the GLBC described in the previous sections, two inverter concepts, namely the H-bridge inverter with DC-link referenced output filter as shown in Fig. 16 and the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology as shown in Fig. 17 are selected for further studies and a comparative evaluation. The H-bridge topology was selected because ideally no LF CM voltage is generated at the output and the originally specified ground current limit of 5 mA can be met without the need for bulky CM chokes. In order to further reduce the size of the EMI filter, the DC-

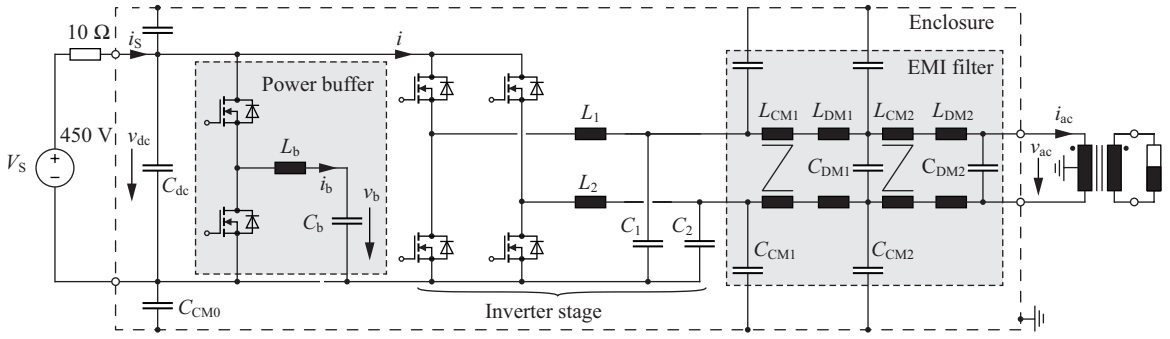

Fig. 16. H-bridge based inverter (HF operation of both bridge-legs) with DC-link referenced output filter, buck-type PCI power buffer and 2-stage EMI filter. The inverter is embedded in the test setup according to the GLBC specification with split-winding grounding scheme of the isolation transformer.

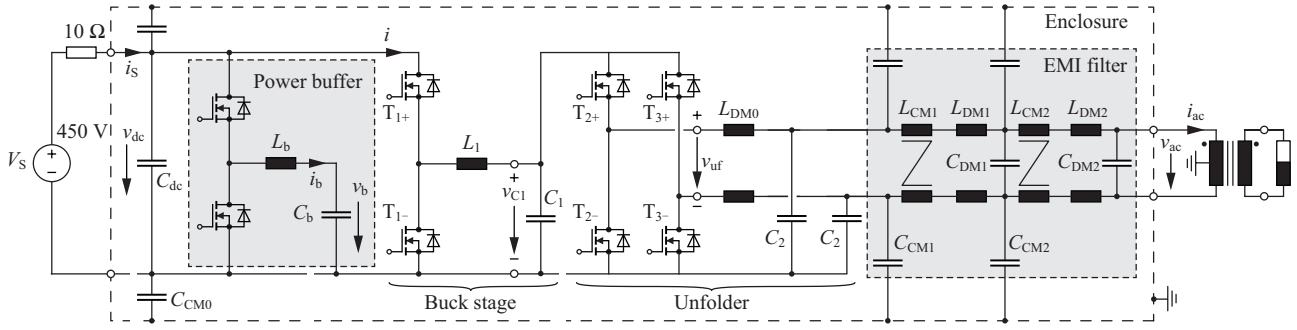

Fig. 17. DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter with buck-type PCI power buffer and 2-stage EMI filter. The H-bridge based unfolder is equipped with DC-link referenced output filter and is temporarily operated with HF PWM around the ZCs of the AC voltage (cf., Section III-C2). The inverter is embedded in the test setup according to the GLBC specifications with split-winding grounding scheme of the isolation transformer.

link referenced output filter configuration is employed which facilitates a combined DM and CM filtering (cf., Section III-C1). As mentioned previously, the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter topology is also considered for further analysis because compared to the H-bridge inverter, almost half the volume of the entire switching stage can be saved (neglecting the volume contribution of the H-bridge unfolder) with the downside of generating an LF CM voltage at the output (cf., Section III-C2). The H-bridge unfolder was preferred over the half-bridge unfolder (cf., Fig. 12 (a)) as it allows to utilize the DC-link referenced filter configuration and therefore reduces the size of the CM chokes in the EMI filter. As can be seen from Figs. 16 and 17, both selected inverter concepts are based on 2-level bridge-legs. As outlined previously in Section III-A3, a multilevel implementation of the bridge-legs was not considered because of the anticipated increase in volume introduced by the higher semiconductor count, the increased gate driving requirement (supply voltage and gate signal isolation), and because of the more involved control systen to facilitate capacitor balancing under all operating conditions.

For both inverter concepts, the buck-type PCI buffer (cf., Section III-B) is selected to cope with the pulsating AC power since (i) it features excellent capacitor utilization and (ii) allows to employ the same bridge-leg design as used in the main inverter to achieve maximal performance with minimal increase of overall complexity.

As mentioned previously, in order to comparatively evaluate both selected inverter concepts regarding maximal achievable $\eta\rho$-performance, a Pareto optimization considering the design space summarized in Appendix E was carried out. The optimization of the buck-type PCI power buffer is described in detail in [5] and revealed that a power density of 41.3 kW/dm^3 (677.1 W/in^3) and an efficiency of 99.4% (12 W of losses at rated power) can be achieved with TCM control of the bridge-leg, C_b = 110 μF buffer capacitor employing 450 V class II/X6S capacitors, and L_b = 30 μH filter inductance. For the Pareto optimal PCI buffer design (set of parameters achieving maximal PCI buffer power density), the optimization of the H-bridge and DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter concepts was carried out as reported in [4].

In Fig. 18 (a) the calculated performance and the designs with highest power density (S1)–(S5) are visualized for the considered inverter concepts for different operating modes (TCM/PWM) and with/without 4D-interleaving of two bridge-legs (cf., Section III-C3). It can be noticed that compared to the H-bridge inverter topology (S1–S3), with the DC/|AC|buck-stage and |AC|/AC H-bridge unfolder inverter topology (S4, S5) approximately a 15%–20% higher power density at even higher efficiency (around +0.5%) can be achieved. Furthermore, for both circuit topologies, PWM (S3, S5) results in a slightly higher power density than TCM (S1, S2, S4).

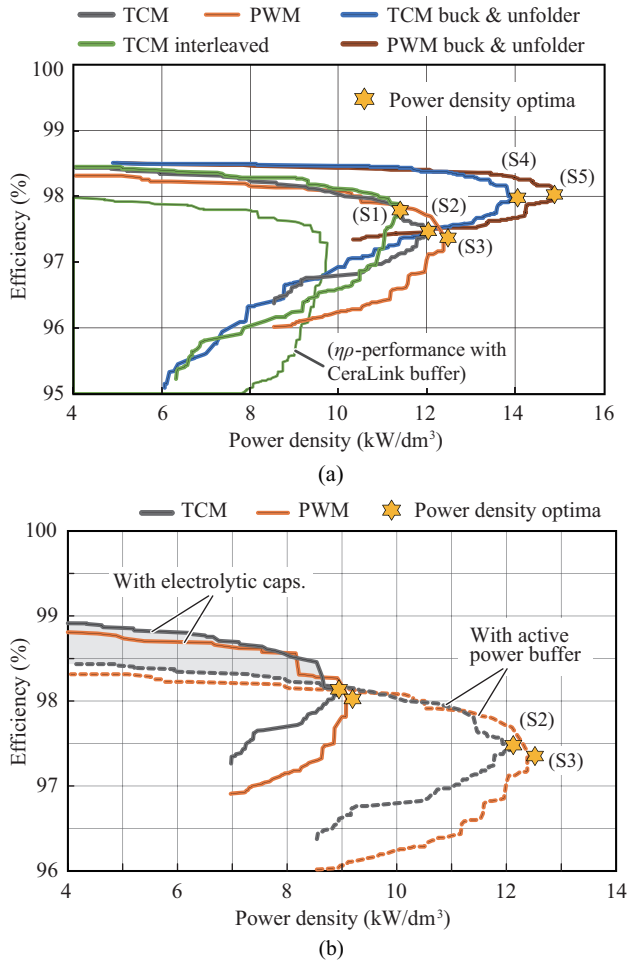

Fig. 18. (a) Computed $\eta\rho$-performance of the H-bridge inverter and DC/|AC| buck-stage with |AC|/AC H-bridge unfolder inverter concept including the active power buffer for different operating modes (TCM/PWM) and with/without interleaving of bridge-legs. (b) Impact of employing the active power buffer on the overall $\eta\rho$-performance in comparison to a passive power buffer using electrolytic capacitors.

Interestingly, interleaving of bridge-legs (S1) is not beneficial for the given GLBC specifications and the objective of achieving maximum power density. Also included in Fig. 18 (a), is the resulting Pareto front of the H-bridge inverter with 4D interleaved bridge-legs and TCM operation, if the CeraLink capacitor technology is employed in the PCI buffer instead of the class II/X6S MLCC. From Fig. 18 (b) it can be clearly seen that it is advantageous to employ an active power buffer instead of a conventional capacitive buffered DC-link, since a power density improvement of around 35 % is possible.

A more detailed comparison of the designs with highest power density (S1)–(S5) with respect to the volume and loss distribution of each design is given in Fig. 19. Considering the H-bridge inverter topology, TCM modulation and interleaving of two bridge-legs results in the highest efficiency, however, also in the largest volume. This can be explained by the fact that, due to the interleaving, twice the number of semiconductors devices and inductors are used and thus, on the one hand the volume is increased (cf., Fig. 19 (a)), but on the other hand

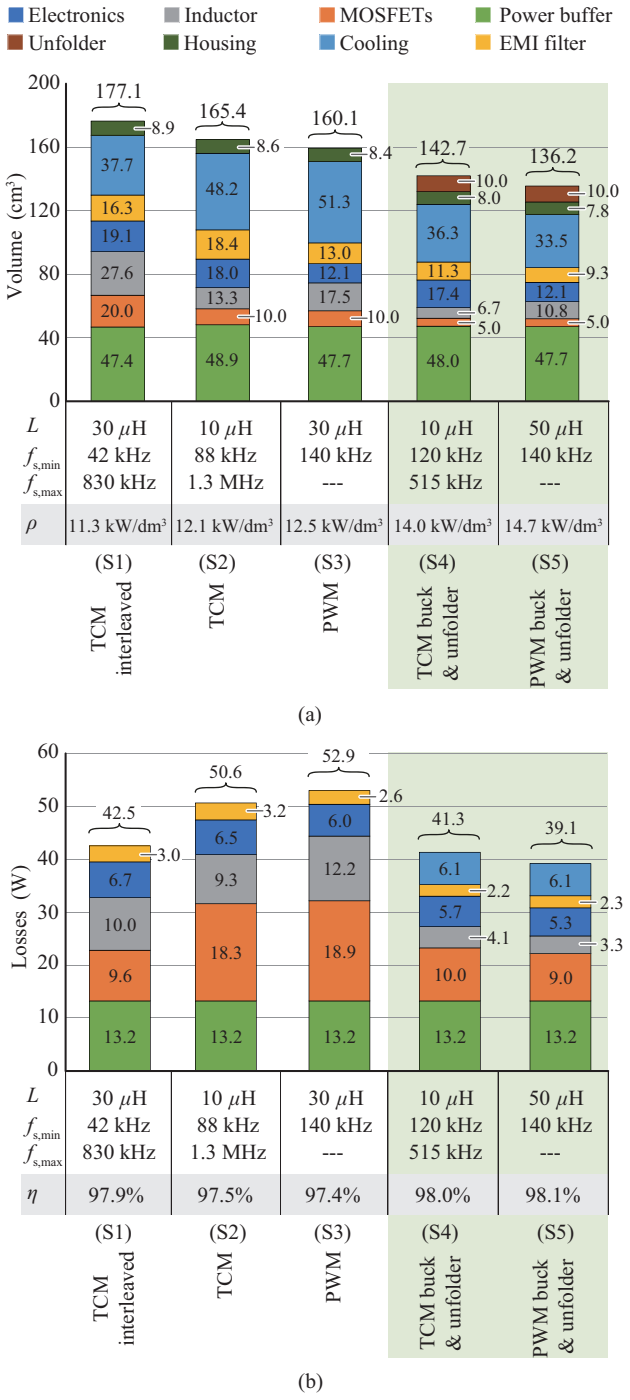

Fig. 19. (a) Volume distribution and (b) loss distribution of all designs achieving the respective highest power density (S1–S5), cf., Fig. 18.

the output current is shared between the bridge-legs resulting in lower power transistor losses (cf., Fig. 19 (b)). The highest power density is obtained with constant switching frequency PWM, however, with the drawback of the lowest efficiency.

Compared to TCM operation, the volume is mainly saved in the electronics, since with PWM no ZCD circuits and FPGA are needed, and in the EMI filter, since the (constant) switching frequency of the optimal design is just below the lower FCC/CISPR limit of 150 kHz and thus only higher-order harmonics

have to be attenuated. In contrast, the volume occupied by the inductor and heat sink slightly increases due to the higher losses.

For the DC/|AC| buck-stage and |AC|/AC H-bridge un-folder inverter topology, the gain in power density is mainly achieved with the volume reduction of the power transistors and the HF filter inductors, since only one HF bridge-leg is needed for the implementation of the buck-stage (cf., Section III-C2) and the volume contribution of the H-bridge unfolder is comparably low. Interestingly, despite the additional conduction losses of the H-bridge unfolder, the concept achieves the highest overall converter efficiency and therefore the lowest heat sink volume. The difference in system performance between TCM modulation and PWM is again found in the electronics and EMI filter.

V. Conclusion

In this paper, i.e., Part A of a discussion of *The Essence of the Little Box Challenge*, the key design challenges and the technical concepts adopted by the authors to implement an ultra-compact single-phase inverter and overcome the Google Little Box Challenge were described in detail. Relevant design considerations such as the selection of the power semiconductor technology, comparison of different bridge-leg control strategies, 2-level vs. multilevel bridge-leg implementation, etc., to achieve a miniaturization of a high-frequency (HF) operated bridge-leg with LC output filter, which constitutes the fundamental building block of the inverter system, were addressed. In order to reduce the size of the energy storage required to cope with the 120 Hz power pulsation intrinsic to single-phase DC/AC converter system, the advantage of replacing bulky electrolytic DC-link capacitors with an additional auxiliary converter and well utilized buffer capacitors was emphasized. Regarding the specified ground current requirements, the difference between a 1 or 2 HF bridge-leg inverter design regarding the generation of an LF CM output voltage component was analyzed and the merits of a DC-link referenced filter structure which allows a combined DM and CM filtering in a single-stage was highlighted. Concerning the EMI requirements of the GLBC, the concept of 4D-interleaving was introduced which allows to operate the interleaved bridge-legs with an optimal over-lapping interval (with respect to the AC period) for maximal conversion efficiency while meeting the EMI requirements. Two promising inverter concepts, namely the H-bridge inverter with DC-link referenced output filter of each bridge-leg and the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter, both equipped with a buck-type PCI active power buffer, were selected for further study and comparative evaluation. Based on the results of a multi-objective $\eta\rho$-Pareto optimization incorporating the described design considerations, it is shown that, despite of higher switching losses, operation with constant switching frequency just below 150 kHz PWM achieves a higher power density compared to TCM control. This is explained by the fact that, for the given GLBC specifications and the performance of the employed GaN semiconductor technology, the loss savings of operating with ZVS throughout the AC period are less compared to the added conduction losses caused by the high RMS current and remaining ZVS switching losses resulting from the TCM control. Furthermore, it is shown that with the DC/|AC| buck-stage and |AC|/AC H-bridge unfolder inverter operated with PWM and a comparably large current ripple (small buck-stage filter inductance value) a power density of 14.7 kW/dm^3 (240 W/in^3) with an efficiency of up to 98 % at 2 kW output power is possible. Compared to the H-bridge inverter concept, this inverter therefore features a $\approx$ 15%–20% higher power density and a 1.7% higher efficiency at 2 kW rated power.

In Part B of the compilation of main results of the GLBC at hand, the claimed performance, particularly the almost factor 5 higher power density compared to the minimum GLBC requirement (50 W/in^3), is verified by means of prototype implementations and experimental measurements. The achieved $\eta\rho$-performance is then compared to the achievements of other GLBC finalists. Finally, overall conclusions are drawn which are providing key guidelines for the future development of ultra-compact industrial converter systems.

Appendix

A. GaN dv_{ds}/dt-Related Soft-Switching Losses

Although the performance of the latest generation of power devices (including Si) is ever improving, still no "ideal switch" is available in the market. Available GaN HEMTs still suffer from the dynamic on-state resistance phenomena, where the actual on-state resistance of a device during operation is much higher compared to the static $R_{ds,on}$ specified in the datasheet. This phenomena can be explained by stored and/or trapped charges in the channel of GaN devices, which causes a temporary increase of the drain-source resistance after the transistors are turned on. The magnitude of this temporary resistance increase is to a large extend determined by the applied blocking voltage and becomes worse at high switching frequencies since there is less effective time for the detrapping process when the on-state resistance returns back to the nominal value. Novel high-fidelity on-state resistance probing circuits were developed in [72], [73] which allow to characterize this behaviour of GaN devices. It is e.g., reported in [72], that 200 V GaN HEMTs can exhibit a dynamic on-state resistance of up to a factor of 2.5 higher than what is actually specified in the datasheet provided by the manufacturer. Similar observations are reported in [74] for normally-off 600 V GaN HEMTs.

Another imperfection is the energy dissipation associated with the charging and discharging of the power transistor's parasitic output capacitance, C_{oss}, which manifests in significant power loss at very high switching frequencies despite employing a ZVS modulation scheme. This lossy charging process of the parasitic capacitor is known from Si super-junction MOSFETs [75] and has recently also been observed

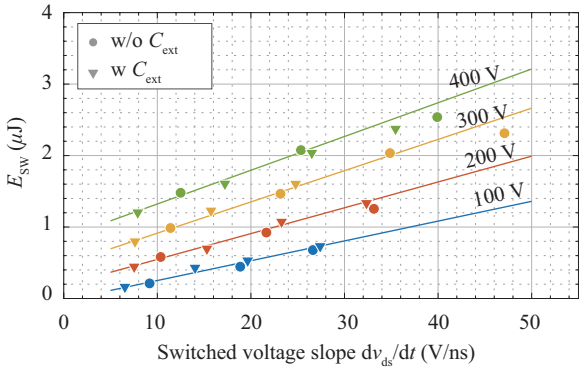

Fig. 20. E_{sw} reported in [12] as function of dv_{ds}/dt obtained for several switched currents I_{sw} (5A,...,20 A) for different V_{DC} voltage levels (100 V,...,400 V). E_{sw} without (dots) and with (triangles) added capacitance C_{ext} = 100 pF are well aligned.

in GaN HEMTs [12], [76]. In the work presented in [12], ZVS losses of a 600 V GaN HEMT (Infineon CoolGaN) were determined by means of a sophisticated calorimetric measurement setup. It was identified that the dissipated energy per switch and cycle, E_{sw}, is depending approximately linear on the slope of the drain-source voltage, dv_{ds}/dt, as shown in Fig. 20. By adding an external capacitance C_{ext} = 100 pF (C0G MLCC, considered lossless) in parallel to the tested GaN transistor, the voltage slope across the device is reduced for the same switched current I_{sw}. Still, as can be seen from the figure, the E_{sw} measurements are well aligned. The measured loss of a subsequent experiment with permanently turned off test devices (GaN transistors with negative gate bias connected in parallel to the transistors of an active bridge-leg in order to cycle C_{oss} in a typical manner with high dv_{ds}/dt) was in excellent agreement with E_{sw} shown in Fig. 20, pinpointing the observed soft-switching losses to the lossy charging/discharging process of C_{oss}. Hence, for a very high switching frequency in the MHz range, the loss contribution of ZVS cannot be neglected: A GaN half-bridge circuit operating at 1 MHz with a switched current of 15 A (corresponds to 50 V/ns in Fig. 20), suffers from a power loss of $P_{sw} \approx 2 \times 1$ MHz $\times$ 2.7 μJ = 5.4 W. At an operation of several MHz, the switching losses would be detrimental to the efficiency and, because of the increased cooling effort, also to the power density. On top of that, a potential increase of conduction losses due to the mentioned dynamic $R_{ds,on}$ phenomena must be taken into consideration when operating at very high switching frequencies. Consequently, as will be further elaborated in Part B of the paper, high power densities were achieved by many GLBC finalists with moderate switching frequencies of a few hundreds of kHz and, given the super-fast switching characteristics of GaN power transistors without reverse recovery, strictly ensuring ZVS throughout the entire mains period turned out to be not necessary to achieve an ultra-compact inverter design.

B. Increased Core Losses in Multi-Gap Inductors

As described in Section III-A4, in order to reduce the proximity losses of the HF inductor winding, the discrete air gap in the employed MnZn ferrite E-core is divided into several partial gaps. Unfortunately, the manufacturing of a multi-gap core structure—the center leg of the E-core composed of multiple stacked MnZn ferrite plates—can lead to an increase of the core losses which potentially outweighs the saving in winding losses as analyzed in detail in [26]. Based on literature, the dominating cause of the excess core loss are shallow layers of deteriorated magnetic performance just underneath the plate surfaces. Reasons for the deterioration are mechanical stresses exerted during machining of the ferrite plates and non-ideal conditions during sintering as described in literature or highlighted by manufacturers, respectively. Fig. 21 (a) illustrates the impact of the additional surface related core losses by showing the total power losses of a composite core section assembled from individual d_p thick plates relative to the losses of a solid ferrite piece with d_{bulk} total length. The depicted data is based on the experimental results obtained in [26] for MnZn ferrite material 3F4 from FerroxCube at 125 mT and 400 kHz. With decreasing thickness of the ferrite plates, more and more plates must be stacked to reach the same length as the solid reference sample. Consequently, the total losses

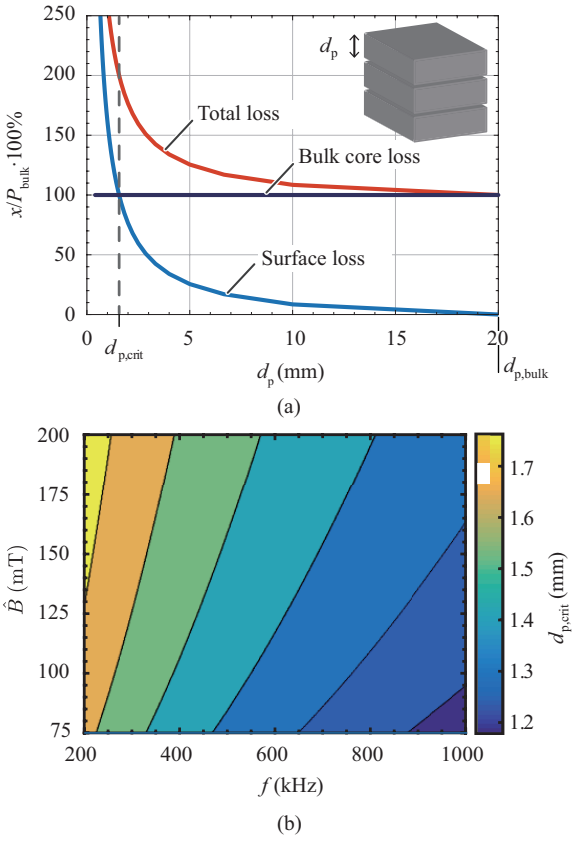

Fig. 21. (a) Surface losses and total losses of a section of magnetic core assembled using individual d_p thick plates relative to the losses of a solid ferrite piece of same total length, d_{bulk} = 20 mm, based on experimental results obtained for 3F4 at 125 mT and 400 kHz. The critical plate thickness $d_{p,crit}$ is defined to be reached when the surface losses are equal to the bulk core losses. (b) Critical thickness of 3F4 ferrite material examined in [26] depending on the actual operating point $\{\hat{B},f\}$.

increase since more and more deteriorated surface layers are introduced in the sample. The critical plate thickness, $d_{p,crit}$, is defined to be reached when the surface loss is equal to the bulk core loss, that is to say when the total core losses have doubled compared to the solid (single piece) ferrite sample. Moreover, the critical plate thickness varies depending on the actual operating point—peak flux density and frequency—as depicted in Fig. 21 (b). It can be concluded that there is a clear trade-off between eddy current losses in the winding and increased core losses due to the stacking of plates. Hence, it is less obvious whether the multi-gap inductor design actually achieves a better performance regarding efficiency η, and power density, ρ, compared to a conventional single-gap implementation of the bridge-leg filter inductors.

C. Buffer Capacitor Technology

As discussed in Section III-B1, class II MLCC and CeraLink capacitor technology is the preferred choice for the implementation of ultra-compact active power buffers. Generally, class II ceramics feature a high relative permittivity and are therefore well suited for energy storage application. Adversely, the relative permittivity is not constant but strongly depends, among several other factors, on the applied DC bias voltage. With increasing DC bias voltage, the effective capacitance of class II ceramics drastically drops, decreasing the capacitance density at higher operating voltage levels. On the contrary, the capacitance of a CeraLink capacitor is increasing with DC bias voltage, resulting in the highest capacitance at DC-link voltage levels around 400 V for 500 V rated voltage [77]. Besides the bias voltage dependency, the capacitance value of ceramic capacitors also depends on the prevailing large-signal AC ripple. In order to capture this non-linear behaviour and correctly dimension the active power buffer capacitor, an experimentally determined capacitance and loss density map as illustrated in Fig. 22 was obtained in [48]. Shown are contour plots of the measured capacitance (μF/cm^3) and loss density (W/cm^3) at 60 °C operating temperature as a function of applied DC bias and large-signal 120 Hz AC ripple. A DC bias of 300 V and a superimposed AC voltage with 130 V_{pp} amplitude is a typical operating point of a 2 kW buck-type active power buffer equipped with a 150 μF buffer capacitor as employed by the authors in the GLBC [5]. In this operating point, the X6S MLCC features a capacitance density of 8.4 μF/cm^3, as opposed to the slightly higher 9.5 μF/cm^3 of the CeraLink. However, the loss density of the X6S MLCC amounts to just 56 mW/cm^3. By contrast, the CeraLink dissipates roughly 1 W/cm^3 in the very same operating point. It can be concluded, that although the CeraLink features a slightly higher capacitance density, the power losses caused by the 120 Hz voltage ripple are by a factor of 18 higher than those of the X6S MLCC which translates in lower efficiency and larger cooling volume. However, an undisputable advantage of the CeraLink is the higher maximum rated operating temperature of 125 °C (as compared to 105 °C of the class II/X6S MLCC) and the advanced packaging options—available in a package with 20 chips mounted in parallel by means of a silver sintered

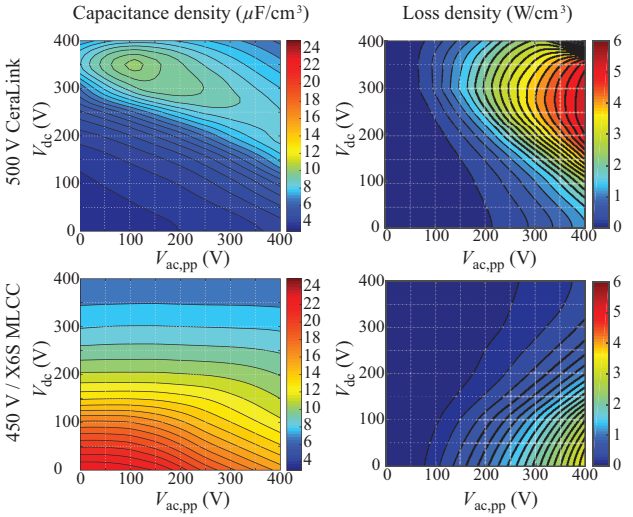

Fig. 22. Contour plot of capacitance density and loss density of a 500 V CeraLink and 450 V class II/X6S capacitor technology with respect to DC bias V_{dc} and 120 Hz AC excitation $V_{ac,pp}$ at 60 °C operating temperature.

connection onto a common lead-frame—for an uncomplicated and reliable mechanical assembly.

To minimize the risk of mechanical failure during assembly or during the 100 hours testing (cf., Section II), it was decided to use the CeraLink capacitor technology for the implementation of the buffer capacitor employed in the Little Box 1.0 (LB 1.0, cf., Section II of Part B), despite the higher losses since the resulting overall efficiency of the inverter still meets the GLBC requirements. Eventually, aiming for highest possible performance, the class II/X6S MLCC technology was used for the implementation of the Little Box 2.0 prototype (LB 2.0, cf., Section II of Part B).

D. Blower vs. Fan Heat Sink Design

As depicted in Fig. 23 (a) and (b), either a fan, characterized by comparably low pressure difference and high air flow rate, or a blower, characterized by comparably high pressure difference and low air flow rate can be used to implement basic heat sink building blocks. The performance of these building blocks as a function of total length of the cooling system is compared in Fig. 23 by means of the cooling system performance index, i.e., the thermal conductance G_{th} per volume,

$$\mathrm{CSPI} = \frac{G_{th}}{Vol_c} = \frac{1}{R_{th} \cdot Vol_c}, \tag{8}$$

where Vol_c is the volume occupied by the heat sink and the fans/blowers and R_{th} is the thermal resistance of the heat sink to ambient, computed with the model described in [78] and the technical parameters listed in Table II. For the parallel-fin type heat sink, it can be seen that a combination of heat sink and blower performs best when the total length ($l_{tot} = v + l$ for the blower and $l_{tot} = u + l$ in case of the fan, cf., Fig. 23 (a)) of the cooling unit is comparably long (> 20 mm in Fig. 23 (c)) with a

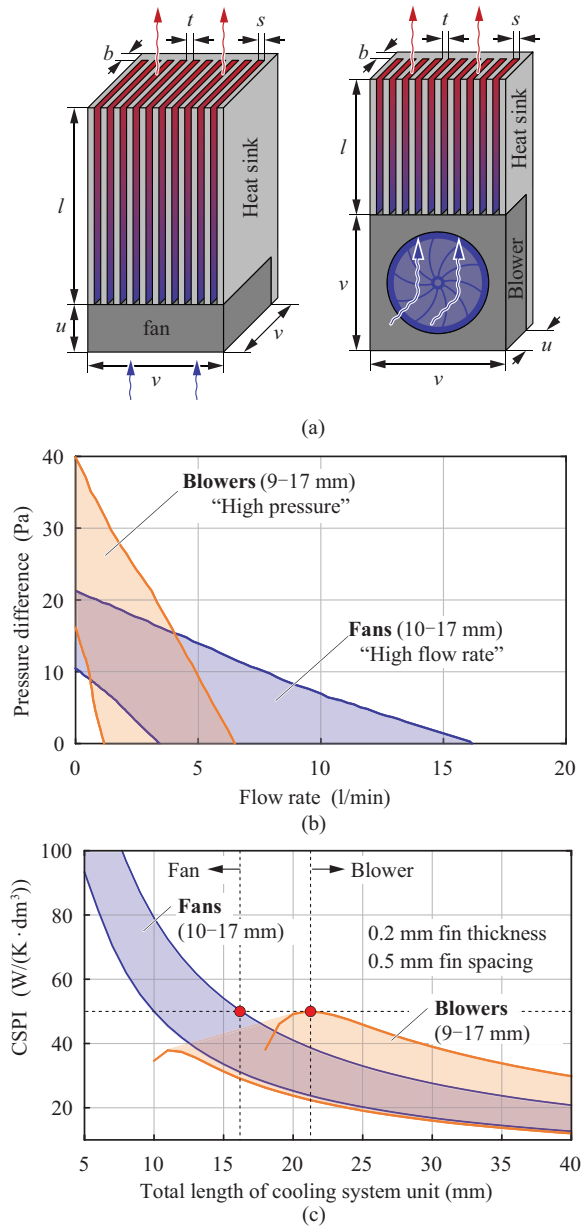

Fig. 23. Characteristics and cooling system performance index (CSPI) of forced-air cooled heat sinks. (a) Fan and blower based heat sink building blocks. (b) Pressure difference in dependency of air flow rate. (c) CSPI (W/(K·dm^3)) of the heat sinks as a function of total length, $l_{tot} = u + l$, for the fan and $l_{tot} = v + l$ for the blower as indicated in (a).

large baseplate area for direct component attachment. Because of the small height, u, a sandwich like arrangement with two heat sinks at the top and bottom and the converter in the center is possible. On the other hand, the combination of heat sink and fan performs best when the total length of the cooling unit is short and very high CSPI values can be achieved. This is well suited for a component arrangement where only the power transistors are attached to the heat sink and the filter passives are cooled by the air flow exiting the heat sink.

Besides the conventional parallel-fin type heat sink, more advanced duct structures, such as e.g., the hexagon (honeycomb) duct adopted by the winning team of the GLBC (CE+T Power), can further increase the CSPI but require advanced and more expensive manufacturing capabilities [79], [80]. Furthermore, thanks to the recent advances in metallurgy, 3D printing of aluminium allows to create customized heat sinks of almost arbitrary shape as demonstrated by another GLBC finalist [81].

TABLE II
PARAMETER OF FORCED-AIR COOLED HEAT SINK

Sunon micro fans	UF3A3-700, UF3C3-700, UF3F3-700, UF3H3-700 (v = 10−17 mm)
Sunon micro blowers	UB393-700, UB3C3-700, UB3F3-700, UB3H3-700 (v = 9−17 mm)
Heat sink type	Extruded parallel-fin heat sink
Material	Copper
Min. fin thickness	t_{min} = 0.2 mm
Min. fin spacing	s_{min} = 0.5 mm
Baseplate thickness	b = 1 mm

As will be described in Section II of Part B, a dual-sided cooling system based on ultra-flat blowers is employed in the Little Box 1.0 (LB 1.0) prototype. The baseplate of the heat sinks covers the entire cross-section of the converter (top and bottom) and theoretically achieves a CSPI of ≈ 35 W/(K·dm^3). However, additional heat distribution elements are needed to conduct the heat from the lossy components, e.g., the power inductors, to the baseplate of the respective heat sink, which reduces the effective CSPI to ≈ 25 W/(K·dm^3). In case of the Little Box 2.0 (LB 2.0) prototype described in Section III of Part B, a fan based design with a single heat sink placed in front of the power inductors was adopted. Only the power transistors are attached to the baseplate of the heat sink and the power inductor are cooled with the air exiting the fins. Without the need of additional heat distribution elements inside the converter, the CSPI could be increased to ≈ 37 W/(K·dm^3).

E. Definition of the Optimization Design Space

The design considerations presented in this paper are incorporated in the $\eta\rho$-Pareto optimization design space summarized in Table III. For the implementation of the bridge-legs, 600 V, 70 mΩ GaN gate injection transistors (GITs) from Infineon (CoolGaN, [82]) and 650 V, 25 mΩ GaN HEMTs from GaN system are considered. As described in Section III-A2, TCM operation with resulting varying switching frequency and PWM operation with constant switching frequency are considered for the operation of the converter bridge-legs. The $\eta\rho$-performance benefit of interleaving two HF bridge-legs and the paralleling of multiple transistors per switch is also investigated. Besides the 2-stage EMI filter structure shown in Figs. 16 and 17 to meet the specified CISPR11 class B limits, also the option of a single-stage EMI filter design is included in the design space. The size of the Y-capacitors (C_{CM1}, C_{CM2}) is limited to meet the 50 mA ground

TABLE III
SYSTEM PARAMETERS & DESIGN SPACE OF THE LITTLE BOX PARETO OPTIMIZATION

Feature	Range/Option	Description/Comment
S_{ac}	2 kW	Optimization carried out for rated power ($\cos\varphi_0 = 1$).
Q_{filt}	250 VAr	Reactive power considered in optimization of power buffer.
V_S	400 V	Nominal input voltage at rated power.
Semiconductor	600 V/70 mΩ GaN HEMT(GIT)	Infineon CoolGaN.
	650 V/25 mΩ GaN HEMT	GaN Systems (considered for the H-bridge unfolder).
#Parallel devices	1−2	1−2 devices in parallel per switch.
C_{ext}	[0 pF, 600 pF]	Capacitor in parallelto C_{oss} toreduce dv_{ds}/dt related soft-switching losses (only in case of TCM).
Modulation	TCM	Frequency variation depends on inductance value.
	PWM	Current ripple envelope depends on inductance value and switching frequency.
$f_{s,TCM}$	[30 kHz, 1.5 MHz]	Acceptable range of frequency variation for TCM.
$f_{s,PWM}$	[50 kHz, 500 kHz]	Range of applicable constant switching frequencies for PWM.
HF Inductor technology	Custom single-gap core inductor design	MnZn ferrite core N87; solid, foil and HF-litz wire winding.
#Interleaved bridge-legs	1−2	4D-interleaving with variable overlap only considered for TCM.
$L_{1/2}$, L_b	[5 μH, 100 μH]	Range of bridge-leg filter inductance value.
Capacitor technology	2.2 μF, 450V class II/X6 SMLCC	Considered for C_b, $C_{1/2}$, and DM filter capacitors in the EMI filter.
	2.0 μF, 500V CeraLink	EPCOS/TDK 2nd gen. CeraLink, considered for C_b and C_{dc}.
C_b	[120 μF, 350 μF]	Range of buffer capacitance value.
$V_{b,0}$	$1/2 C_b \cdot V_{b,0}^2 \in [E_{0,min}, E_{0,max}]$	Range of buffer bias voltage / avg. stored energy.
EMI filter	1- and 2-stage custom filter design	VITROPERM 500F toroidal core, solid wire winding, 450 V class II X6S MLCC for X-capacitors (DM) and 630 V /X7R MLCCs for Y-capacitors (CM).
Heatsink	CSPI=25.7 W/(K·dm^3)	Value obtained from experimentally verified forced-air cooled heat sink.

current requirement. For the design of the HF inductors $L_{1/2}$, L_b), different core shapes with MnZn ferrite core materials N87 and air gap sizes as well as different winding types, such as HF litz, foil or solid wire with different numbers of turns, are considered. As described in Section III-B1, 2.2 μF, 450 V class II/X6S MLCC and 2 μF, 500 V CeraLink capacitors are considered for the implementation of the buck-type PCI power buffer capacitor. For the implementation of the bridge-leg output filter ($C_{1/2}$) and the DM filter C_{DM1}, C_{DM2} capacitors, 450 V class II/X6S MLCC technology is considered.

In the $\eta\rho$-Pareto optimization all available degrees of freedom, i.e., all design space variables as listed in Table III, are considered for both topologies. As an example, for the H-bridge inverter topology operated with TCM modulation, the number of interleaved bridge-legs, the number of parallel transistors per switch, the output inductor value $L_1 = L_2$, and the output capacitor $C_1 = C_2$ can be iterated, while with PWM additionally the switching frequency f_s can be selected independently in the specified range. The interested reader is referred to [4], [5] for more technical details and a descriptive flowchart of the implemented algorithm.

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