Power Electronic Systems
Laboratory

IET Power Electronics, pp. 1-9, April 2019

Three-Phase Buck-Boost PFC Rectifier with Common-Mode Free Output Voltage and Low Semiconductor Blocking Voltage Stress

J. Miniböck,
M. Mauerer,
J. Huber,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

Three-phase buck–boost PFC rectifier with common-mode free output voltage and low semiconductor blocking voltage stress

ISSN 1755-4535
Received on 24th August 2018
Revised 8th March 2019
Accepted on 8th April 2019
E-First on 12th June 2019
doi: 10.1049/iet-pel.2018.5850
www.ietdl.org

Johann Miniböck[1], Mario Mauerer[2] ✉, Jonas E. Huber[2], Johann W. Kolar[2]

[1]*m-pec Power Electronics Consulting, Walkenstein, Austria*

[2]*Power Electronic Systems Laboratory, ETH Zurich, Physikstrasse 3, 8092 Zurich, Switzerland*

✉ *E-mail: mauerer@lem.ee.ethz.ch*

Abstract: Three-phase buck–boost power-factor correction (PFC) rectifiers are characterised by a unity power-factor mains behaviour and/or sinusoidal input currents and are providing a wide-output voltage range. In this study, an extension of a state-of-the-art three-phase buck–boost PFC rectifier topology is proposed. The DC output of the new topology does not suffer from a high-frequency common-mode voltage with respect to the (grounded) mains star point, which alleviates electromagnetic interference concerns. Also, the blocking voltage requirements of the AC-side switches are reduced significantly (almost by a factor of two for a 400 V line-to-line mains and a 400 V DC output), which facilitates a broad selection of cost-effective power semiconductors for the system's realisation. The rectifier can be controlled with a simple feedback system and the concept is especially suitable for low-power applications. A 1 kW hardware demonstrator is employed to verify the results of theoretical considerations. The system seamlessly operates in the buck and boost regime and achieves conversion efficiencies of 95.3% and mains current total harmonic distortion figures in the range of 1–5%.

1 Introduction

Three-phase rectifier systems that provide power-factor correction (PFC) and wide-output voltage ranges are often realised as combinations of two converter stages: either a boost-type or a buck-type PFC rectifier stage ensures sinusoidal mains currents and generates an intermediate DC voltage that is either subject to a lower or an upper bound with respect to the AC voltage, respectively. Thus, a subsequent DC–DC conversion stage is required to achieve a wide range of controlled DC output voltages [1]. This comparably high topological complexity is accompanied by correspondingly complicated control and modulation methods which typically require several current sensors and involve the generation of several independent pulse-width modulation signals for the individual power semiconductors [2].

There are emerging applications such as more electric aircraft, where PFC functionality and possibly also compatibility with widely varying AC-to-DC voltage ratios are required even for systems with comparably low-power ratings, i.e. below 1 kW [3, 4]. A two-stage approach would be overly complex and costly for such low-power systems. Accordingly, single-stage buck–boost three-phase PFC rectifier systems are an interesting alternative [3–11]. These converters feature sinusoidal input currents, a high-power factor (i.e. ohmic mains behaviour), a wide-output voltage range, and optionally also galvanic isolation [6–8, 10] – all with minimum control complexity, i.e. without requiring any current sensors. Furthermore, these systems can continuously operate with a wide range of mains frequencies, e.g. in airborne applications.

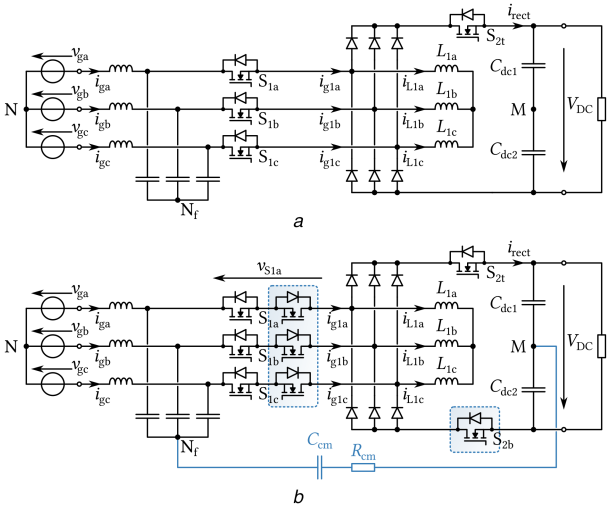

Fig. 1 *Three-phase buck–boost PFC rectifier topologies*
(a) State-of-the-art buck–boost three-phase PFC rectifier [5], ***(b)*** Proposed extension of the basic topology

The state-of-the-art three-phase buck–boost PFC rectifier topology (see Fig. 1*a*) has been proposed by Pan and Chen already in 1994 [5]; however, topological variations are still in the scope of current research (see, e.g. [4], where the three inductors are connected in a delta-configuration instead of the original star connection).

However, the topology introduced in [5] (compare Fig. 1*a*) could be improved concerning two aspects: first, there is a significant high-frequency common-mode (CM) voltage from the DC output midpoint (M) to the mains star point (N), and/or typically also to ground, which raises concerns regarding electromagnetic interference (EMI) and disturbances caused to a supplied load. Second, the AC-side switches (S_{1x}) are subject to high blocking voltage stresses (e.g. about 966 V for a 400 V line-to-line mains and 400 V DC output).

In this work, we, therefore, propose an extension of the state-of-the-art topology that mitigates these two issues [12]. The extended topology (compare Fig. 1*b*) retains the advantageous simplicity of the original's structure and control, provides a CM free output voltage, and allows for the use of power semiconductors with lower blocking voltage ratings.

This paper first reviews the operating principle of both topology variants as shown in Fig. 1 in Section 2, which provides the basis for discussing the improvements achieved with the proposed extension in Section 3. Finally, Section 4 provides an extensive experimental analysis of the proposed converter. Section 5 concludes this paper.

2 Operating principle of three-phase buck–boost PFC rectifiers

The basic operating principle of both three-phase buck–boost PFC rectifiers as shown in Fig. 1 is essentially the same and will be briefly discussed as follows.

2.1 Key waveforms and switching states

Fig. 2 shows the key waveforms for one mains period and Fig. 3 for several switching periods (note that these waveforms are identical for both topology variants as shown in Fig. 1), whereby the specifications of the hardware prototype given in Table 1 and a mains frequency of $f_g = 800$ Hz are considered. Figs. 4 and 5 show the corresponding switching states of the state-of-the-art topology and of the proposed topology, respectively. In both cases, the input filter is not shown as it is not relevant for describing the operating principle.

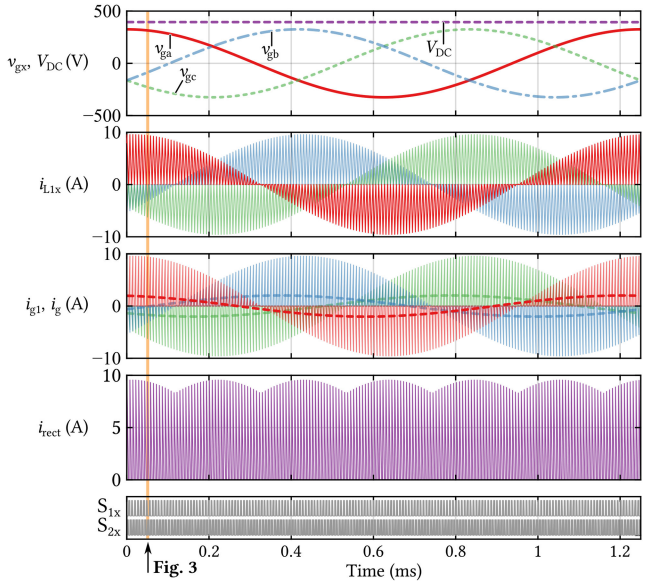

Fig. 2 *Simulated key waveforms of three-phase buck–boost PFC rectifiers. Fig. 3 shows details of the time interval highlighted in orange, i.e. several switching periods*

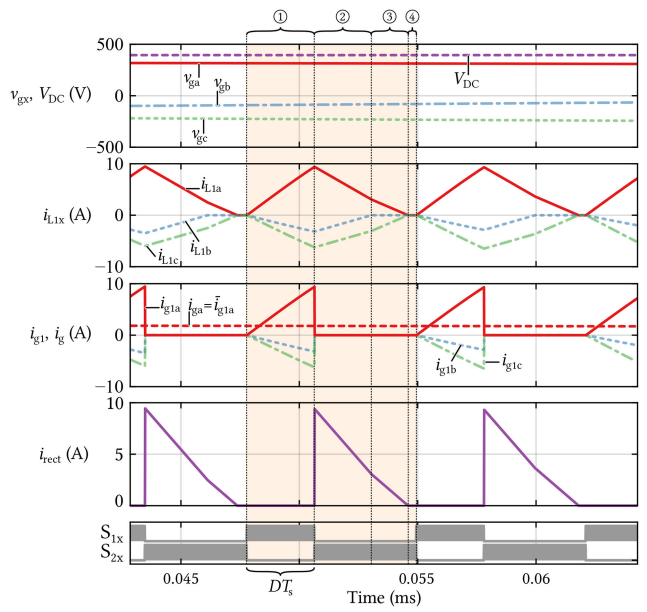

Fig. 3 *Magnified view of the simulated waveforms of the considered three-phase buck–boost rectifiers. Note that parasitic capacitances of the power semiconductors are not considered*

The simplicity of the system originates mainly from the operation in discontinuous conduction mode (DCM), i.e. the currents in the inductors L_{1a}, L_{1b}, and L_{1c} are zero at the beginning of each switching period, and all switches are turned off.

During the first interval of a switching period, denoted by ① in Figs. 3–5, the AC-side switches S_{1a}, S_{1b}, and S_{1c} are turned on simultaneously, and hence the phase voltages are applied to the star-connected buck–boost inductors L_{1a}, L_{1b}, and L_{1c}. Starting from zero, the currents i_{L1a}, i_{L1b}, and i_{L1c} change with a slope that is proportional to the corresponding phase voltage. No current flows through the diode bridge, regardless of the output voltage level, because the DC side is disconnected by the DC-side switch (or switches). At the end of this magnetisation interval ①, all AC-side switches are turned off simultaneously and the DC-side switch S_{2t} (and S_{2b} in case of the extended topology) are turned on. Note that thus the modulation signals are identical for all three phases, and a common duty cycle D is employed.

In the first demagnetisation interval ②, the energy stored in the three buck–boost inductors L_{1a}, L_{1b}, and L_{1c} is transferred through the diode bridge to the DC side. Interval ② ends when the current in the inductor that started this interval with the lowest absolute current value reaches zero (i_{L1b} in the highlighted switching period).

In the subsequent second demagnetisation interval ③, only the two other inductors conduct current (L_{1a} and L_{1c} in the chosen example switching period) until their remaining magnetic energy has been transferred to the DC side, and hence their currents become zero, too.

Finally, the currents in all three inductors remain zero during interval ④, corresponding to DCM operation. The DC-side switches are turned off at the end of interval ④, directly before the next switching period starts.

2.2 Power transfer

The AC phase currents (before filtering) consist of a series of triangular current pulses, whose peak values are proportional to the corresponding (local average of the) phase voltage, i.e. the mains current pulses have a sinusoidal envelope (compare Figs. 2 and 3 [5]).

Note that these pulsed currents must be filtered by a low-pass input filter in order to comply with EMI regulations. This filter is typically realised with one or several inductor–capacitor (LC) stages (only one stage is shown in Fig. 1). Furthermore, it may be required to add a CM filter consisting of a CM choke in series to the filter inductors and a CM filter capacitor connected between N_f and ground/Earth, besides filter capacitors at the mains terminals again including a CM capacitor. Further details are given in Section 4.5. However, for the following fundamental considerations, the input filter can be neglected. Note further that the discussion equally apply to the standard and the proposed topology.

Considering phase a, the local peak of the phase current varies over the mains period according to

$$\hat{i}_{g1a}(t) = \frac{\bar{v}_{ga}(t)}{L_1} DT_s, \tag{1}$$

with $L_1 = L_{1a} = L_{1b} = L_{1c}$, and the local average current is given by

Table 1 Key specifications and characteristics of the prototype

P_N	1 kW	V_{LL}	400 V	f_g	50, …, 800 Hz	THD	<5%
V_{DC}	400 V	f_s	140 kHz	L_{1x}	100 µH	η	>90%

Component values of the prototype system are given in Fig. 8.

$$\bar{i}_{g1a}(t) = \frac{D}{2}\hat{i}_{g1a}(t) = \frac{D^2 T_s}{2L_1}\bar{v}_{ga}(t), \tag{2}$$

where $\bar{x}$ denotes the local average of x (i.e. the average over one switching period). Thus, the local average of the phase current is proportional to the phase voltage

$$\bar{i}_{ga}(t) = \frac{1}{R_{eq}}\bar{v}_{ga}(t), \tag{3}$$

which corresponds to ohmic mains behaviour: the converter emulates a star connection of three resistors of

$$R_{eq} = \frac{2L_1}{D^2 T_s}, \tag{4}$$

resulting in a power transfer from the AC-to-DC side of

$$P = 3\frac{\hat{V}_g^2}{R_{eq}} = \frac{V_{LL}^2}{R_{eq}} = \frac{V_{LL}^2 T_s}{2L_1}D^2, \tag{5}$$

where $\hat{V}_g$ denotes the amplitude of a mains phase voltage and V_{LL} is the root-mean-square (RMS) value of the mains line-to-line voltage; $\hat{V}_g = V_{LL}\sqrt{2/3}$.

Alternatively, the converter's power transfer behaviour can be derived via the magnetic energy stored in the three inductors L_1, which will be helpful for the subsequent discussion of the DCM operation boundary. Assuming $D = \text{const.}$, the total energy stored in all three inductors at the end of interval ① is given by

$$\begin{aligned} W_{mag,1}(t) &= \frac{L_1}{2}\left(\hat{i}_{g1a}(t)^2 + \hat{i}_{g1b}(t)^2 + \hat{i}_{g1c}(t)^2\right) \\ &= \frac{L_1}{2}\left(\frac{\hat{V}_g D T_s}{L_1}\right)^2\left(\sin^2(\omega t) + \sin^2\left(\omega t + \frac{2\pi}{3}\right)\right. \\ &\left. + \sin^2\left(\omega t + \frac{4\pi}{3}\right)\right) = \frac{\hat{V}_g^2 D^2 T_s^2}{2L_1}\frac{3}{2} = \text{const.}, \end{aligned} \tag{6}$$

where the change of the mains voltages during a switching period is neglected.

Note that W_{mag} does not change over the mains period, corresponding to a constant power consumption from the three-phase mains as

$$P = \frac{W_{mag}}{T_s} = \frac{V_{LL}^2 T_s}{2L_1}D^2, \tag{7}$$

which equals the expression obtained in (5).

The power transfer and hence the output voltage can, therefore, directly be controlled by adjusting a single parameter: the common duty ratio D. Thus, the control circuitry can advantageously be of very simple structure and there is especially no need for any current sensors.

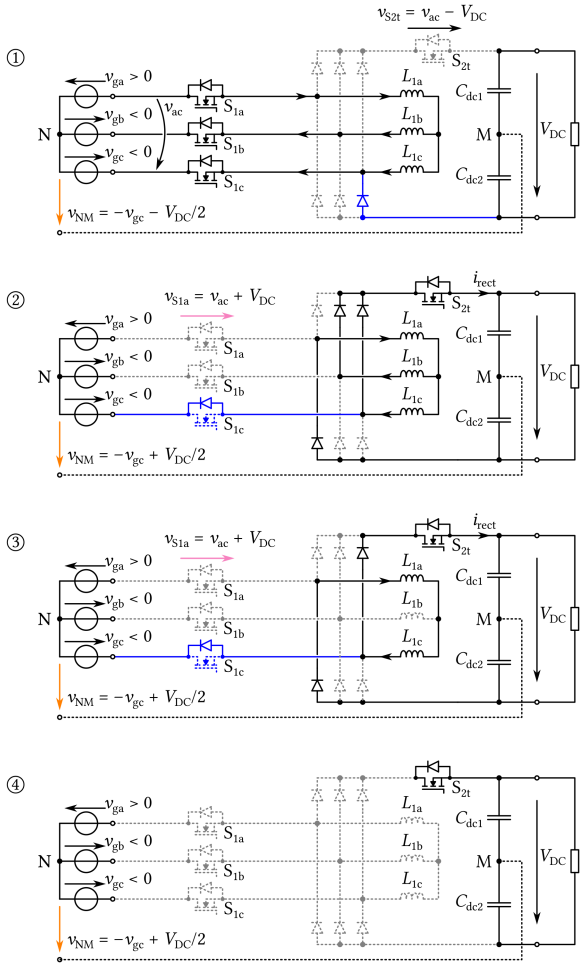

Fig. 4 *Current paths in the state-of-the-art topology (see Fig. 1a, input filter not shown) during the four switching states indicated in Fig. 3. The connections shown in blue do not carry current, but define the potential of the output voltage midpoint M. Note how phase c is connected to the negative DC rail during the magnetisation interval, but to the positive DC rail during the demagnetisation intervals*

2.3 Ensuring DCM operation

To ensure DCM operation, all three inductors must be demagnetised completely within the time interval $(1-D)T_s$, i.e. W_{mag} must be completely transferred to the DC output during the intervals ② and ③.

This demagnetisation process is driven by the DC output voltage that is applied to an effective inductance L_{eff} formed by L_{1a}, L_{1b}, and L_{1c} and the diode rectifier. From Figs. 4 and 5, it can be seen that the effective inductance during the demagnetisation depends on the current flows and is either $L_{eff} = 3/2\,L_1$ (interval ②) or $L_{eff} = 2\,L_1$ (interval ③).

Hence, for the converter to operate in DCM, the inequality

$$W_{mag}(t) < W_{demag}(t) \tag{8}$$

must always hold, i.e.

$$\frac{V_{LL}^2 T_s^2}{2L_1}D^2 < (1-D)^2 T_s \frac{V_{DC}^2}{L_{eff}^2}. \tag{9}$$

Clearly, the limiting case occurs for $L_{eff} = 2\,L_1$, i.e. the case where one of the three-phase voltages equals zero, as the corresponding inductor current in the whole switching interval. Then, solving (9) for D yields

$$D < \frac{V_{DC}}{V_{DC} + \sqrt{2}V_{LL}}, \tag{10}$$

which is a sufficient condition for the rectifier to operate in DCM. This has been verified by detailed circuit simulations.

During the design phase, however, L_1 should be selected such that DCM is ensured for the desired operating range defined by P_{max} (including control margin), $V_{DC,min}$, and a given grid voltage level, i.e. V_{LL}. Solving (7) for L_1 and inserting (10) yield the upper limit for L_1 that ensures DCM operation for the specified conditions as

$$L_1 < \frac{V_{LL}^2 T_s}{2P_{max}}\left(\frac{V_{DC,min}}{V_{DC,min} + \sqrt{2}V_{LL}}\right)^2. \tag{11}$$

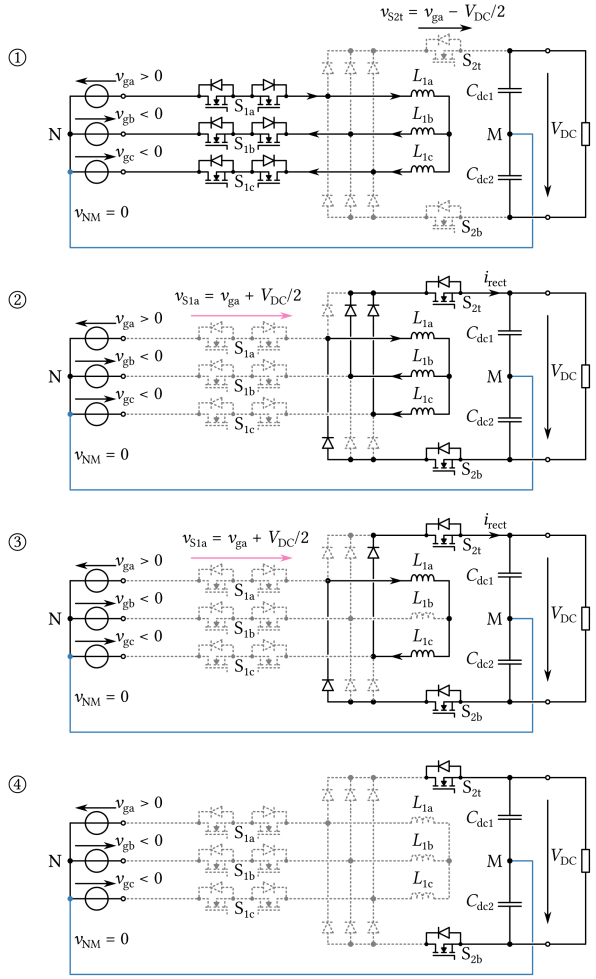

Fig. 5 *Current paths in the proposed topology (see Fig. 1b, input filter not shown) during the four switching states indicated in Fig. 3. Note that compared with the state-of-the-art topology, the potential of the output voltage midpoint M is now fixed and tied to the mains star point N. Note further the lower blocking voltages applied to the semiconductors*

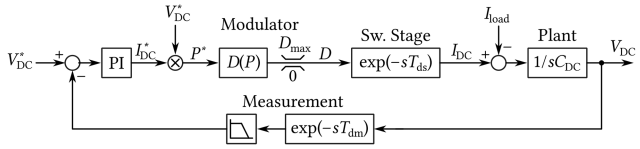

Fig. 6 *Output voltage control of three-phase DCM buck–boost PFC rectifiers. Note that some calculations are explicitly shown for clarity, even though they could be included in the gain of the PI controller*

For a given system, the above equation can be rearranged to calculate the maximum power that can be transferred while maintaining DCM operation as

$$P_{max} = \frac{V_{LL}^2 T_s}{2L_1}\left(\frac{V_{DC,\,min}}{V_{DC,\,min} + \sqrt{2}V_{LL}}\right)^2. \tag{12}$$

2.4 Control

As mentioned earlier, the control system (compare Fig. 6) of three-phase buck–boost PFC rectifiers can be extremely simple because of DCM operation. Essentially, there is only a single control loop for the voltage of the DC output capacitor: according to (7), there is a direct relationship between the desired power transfer P^* and the required duty ratio as

$$D(P^*) = \sqrt{\frac{2L_1}{V_{LL}^2 T_s} P^*}. \tag{13}$$

The converter realises this power flow (approximately, because of non-idealities etc.) within the next switching period and can thus be modelled as a gain and a delay $T_{ds} \simeq T_s$; in principle, there are no energy storages other than the output capacitor involved. Note, however, that the voltage measurement may introduce low-pass behaviour and further (sampling) delay T_{dm}.

On the basis of the control structure shown in Fig. 6, the design of the controller itself is thus straightforward, with the plant being described as

$$G_{plant}(s) = \frac{1}{sC_{DC}} e^{-s(T_{ds}+T_{dm})}, \tag{14}$$

where no (relevant) low-pass behaviour of the measurement is assumed. Suitable parameters for the proportional–integral (PI) controller can easily be found based on basic control engineering considerations. Note that in cases where a very high control bandwidth (with respect to the input filter cut-off frequencies) shall be achieved, it may become necessary to include the AC-side input filter in the considerations.

Note further that if the operation in DCM shall be ensured, the duty cycle D must be limited according to (10).

2.5 Timing requirements

Note that an overlap, i.e. the concurrent on-state of the AC-side and the DC-side switches at the end of interval ① would introduce harmonic distortion to the rectifier input currents: the inductor currents would potentially (depending on the DC output voltage) not be proportional to the phase voltages anymore, as current could directly flow from the grid to the DC side. However, an interlock time between the turn-off of the AC-side switches after the magnetisation interval and the subsequent turn-on of the DC-side switches is also not feasible, as a path for the inductor currents must immediately be provided. Consequently, the switching of the AC-side and DC-side switches must be performed with high temporal accuracy, which is facilitated by modern gate driver and signal isolation circuits that are characterised by short propagation delays and delay variations (see, e.g. [13]). If an accurate switch timing is not possible, it may be necessary to employ an overvoltage snubber to protect the switches during this break-before-make switching pattern.

Similarly, during certain operating conditions (e.g. transients, see Section 4.3 below), the inductor currents i_{L1x} may not necessarily become zero during the demagnetisation intervals (③ and ④), and hence the converter might temporarily operate in a continuous conduction mode (CCM). Hence, a precise switch timing or a snubber circuit is also essential when commutating from the DC-to-AC-side switches in order to always provide a current path for the inductor current.

3 Topology evolution

3.1 Issues of the state-of-the-art topology

In the state-of-the-art topology (compare Figs. 1*a* and 4), there is a switching-frequency CM voltage between the midpoint of the DC output voltage (M) and the (grounded) star point of the grid (N). During the magnetisation interval ①, the most negative phase voltage (v_{gc} in the highlighted switching period in Fig. 3, compare also Fig. 4) is connected to the negative DC terminal via the corresponding diode (any current flow is prevented by S_{2t}). However, because of the current directions in the buck–boost inductors L_{1a}, L_{1b}, and L_{1c}, the upper diode of the bridge leg becomes conducting during the first demagnetisation interval. This connects the most negative phase voltage to the positive DC terminal since the AC-side switch of this phase cannot block any voltage in the required direction due to the anti-parallel diode. Therefore, the CM voltage undergoes a fast transition with a magnitude of V_{DC}.

Furthermore, the peak blocking voltage applied to the AC-side switches (during the diode bridge conduction intervals ② and ③) amounts to the peak value of the line-to-line voltage plus the output

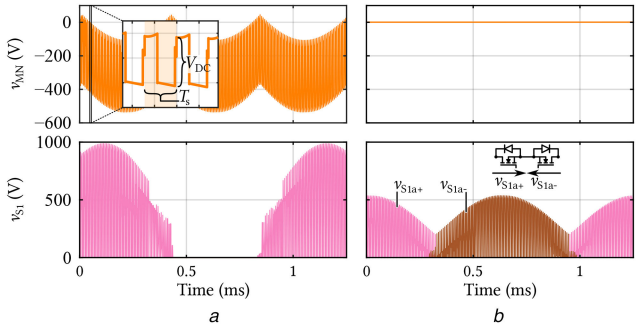

Fig. 7 *Improvements of the proposed topology compared with the state-of-the-art. Simulated waveforms*

(a) CM voltages between *M* and *N* in Fig. 1, ***(b)*** Voltage stress of the AC-side switches

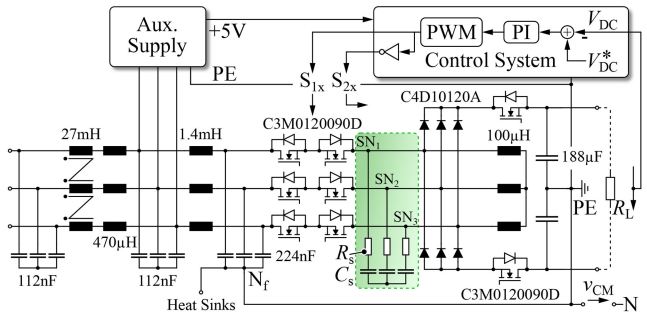

Fig. 8 *Power circuit of the proposed three-phase buck–boost PFC rectifier (compare Fig. 1b). The hardware prototype is shown in Fig. 9. All indicated component values are given for a single component, whereas the values of the unlabelled parts are derivable through symmetry. The highlighted snubber circuit improves the THD of the grid currents, as further described in Section 4.2*

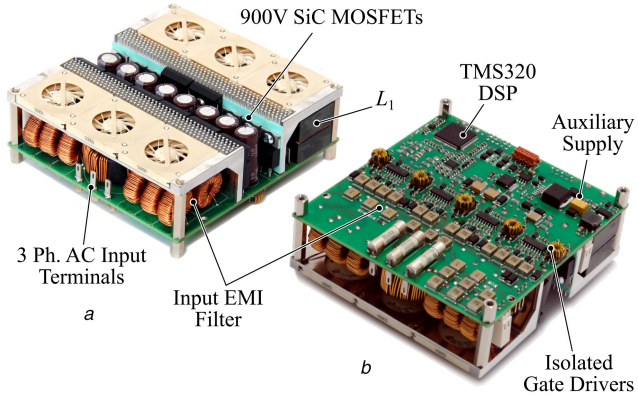

Fig. 9 *Hardware prototype based on SiC MOSFETs and diodes. It is rated for an output power of 1 kW and the output voltage can be varied seamlessly from about 100 to 450 V due to the topology's buck–boost capability*

(a) Top side, ***(b)*** Bottom side. Dimensions: $10 \times 10.5 \times 3.5\,\text{cm}^3$ (resulting in $2.7\,\text{kW/l} = 44.6\,\text{W/in}^3$)

DC voltage, i.e. max $(v_{S1}) = \sqrt{2}V_{LL} + V_{DC}$, which results in 966 V for the considered system (400 V grid and 400 V DC output voltage). Therefore, considering typical semiconductor blocking voltage ratings, 1200 V or, taking into account reliability, even 1700 V devices must be employed.

The simulation results shown in Fig. 7*a* illustrate these two shortcomings of the state-of-the-art topology.

3.2 Proposed extensions and improvements

The proposed topology shown in Fig. 1*b* overcomes the aforementioned issues. First, a second DC-side switch S_{2b} is added, which allows to fully separate the DC output from the AC side during the magnetisation interval. Second, the midpoint of the output voltage is connected to a capacitive star point N_f, which is formed by the AC-side filter capacitors. This connection can either be direct or, alternatively, a series resistor–capacitor (RC) element can be inserted in order to damp transient oscillations if required. This connection ties the reference potential of the DC output to the grid star point and reduces the voltage stress of the DC-side switches from max $(v_{S2}) = \sqrt{2}V_{LL} - V_{DC}$ to max $(v_{S2}) = \sqrt{2/3}V_{LL} - V_{DC}2$ (ideally, i.e. not considering any switching-frequency ripples and switching overvoltages), corresponding to a reduction from 166 to 127 V for the considered specifications.

Note that this implies that the DC-side switches would not be required in case of $V_{DC} > \sqrt{2}V_{LL}$ (original topology) or $V_{DC} > 2\sqrt{2/3}V_{LL}$ (proposed topology), whereby the systems would operate in a non-DCM mode during start-up until V_{DC} has increased to meet the mentioned condition.

On the other hand, the connection between the DC and the AC sides introduces an additional current path, which makes it necessary to employ bidirectional switches (i.e. an anti-serial connection of two metal–oxide–semiconductor field-effect transistors (MOSFETs), preferably in common-source configuration for easy driving) to ensure a full disconnection of the AC side from the DC side during the demagnetisation intervals. Alternatively, depending on the system specifications, integrated bidirectional gallium nitride (GaN) FETs could be employed [14]. Advantageously, the maximum blocking voltage stress of the AC-side switches is (ideally) reduced to max $(v_{S1}) = \sqrt{2/3}V_{LL} + V_{dc}2$ (neglecting potential switching transients), which corresponds to only 527 V in the considered system (400 V line-to-line voltage and 400 V DC output voltage). This is a reduction by almost a factor of two compared with the state-of-the-art topology. Fig. 7 illustrates the improvement in terms of CM voltage noise and blocking voltage stress of the AC-side switches.

4 Experimental analysis

The proposed topology, as illustrated in Fig. 1*b* and with the specifications outlined in Table 1, is implemented in a 1 kW hardware prototype to verify the aforementioned advantages. Fig. 8 illustrates the detailed circuit schematic representation, which is based on 900 V silicon carbide (SiC) MOSFETs and 1200 V SiC power diodes. The DC-link midpoint is directly connected to the AC-side capacitive star point N_f, as detailed in the previous section.

The demonstrator hardware is depicted in Fig. 9. It features a boxed volume of 0.37 l or 22.4 in^3, which results in power densities of 2.7 kW/l or 44.6 W/in^3, respectively. It contains all necessary circuits including an auxiliary power supply. No current sensors are required, and only one voltage sensor is utilised for the control of the output voltage. No overvoltage snubber is required for the diodes or MOSFETs. As explained in Section 2, the commutation from the AC-to-DC-side switches (and vice versa) does neither allow for an overlap of conduction states nor an interlock time in order to prevent harmonic distortion of the grid currents and to always provide a path for the current of the inductors L_1. The utilised gate drivers (*Silicon Labs Si827x* [13]) enable a precise and fast switching of the involved power MOSFETs, which results in no excessive switching overvoltages (compare Fig. 10 below). Thus, the converter can seamlessly transition between buck and boost operations, as the commutation timing remains identical for both operating modes (i.e. V_{DC} can be above or below the peak phase voltage $\sqrt{2/3}V_{LL}$).

As illustrated in Fig. 8, an RC snubber can be employed and connected to the three switch nodes SN_x. The reasons and details of this arrangement are further outlined in Section 4.2 below.

Different measurements are performed with the system. A three-phase AC grid simulator (*Spitzenberger DM 3000/PAS*) provides the input voltage. Key performance parameters such as efficiency η, grid current distortion, or power factor are determined with a precision power analyser (*Yokogawa WT3000*). The grid

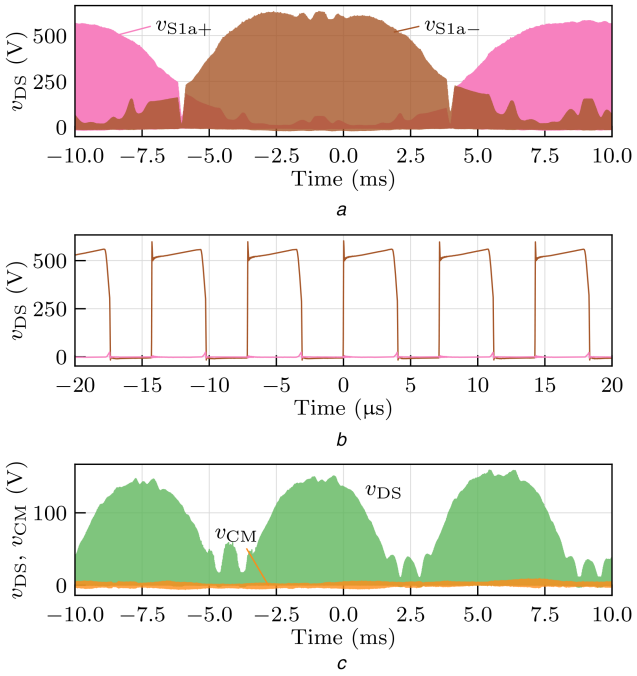

Fig. 10 *Measured MOSFET drain–source voltages*
(a), ***(b)*** AC-side switches (compare Fig. 7*b*), ***(c)*** DC-side switch voltage (S_{2t}). $V_{LL} = 400\,\text{V}$, $f_g = 50\,\text{Hz}$, $V_{DC} = 450\,\text{V}$, and $P_{out} = 1\,\text{kW}$

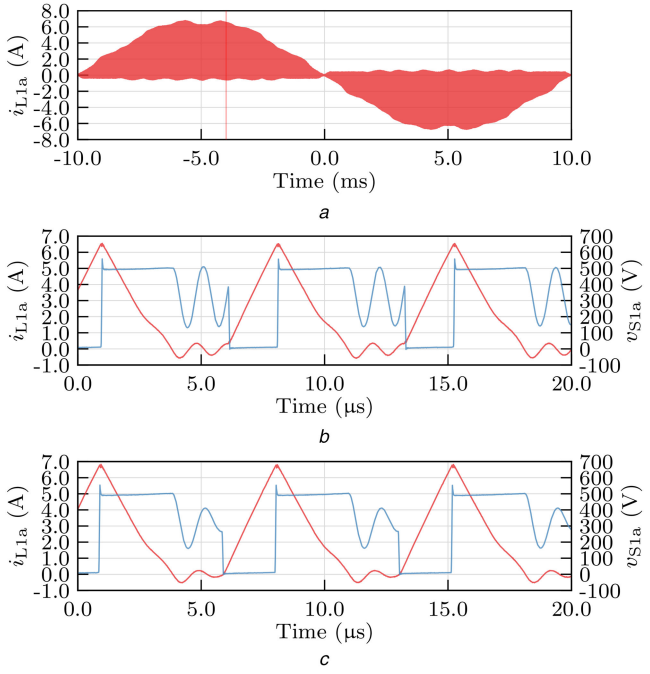

Fig. 11 *Measured key current waveforms and AC-side switch voltages for* $V_{LL} = 400\,\text{V}$, $f_g = 50\,\text{Hz}$, *and* $V_{DC} = 400\,\text{V}$
(a) Current of the inductor L_{1a} during a 50 grid mains period, ***(b)*** Enlarged portion (arbitrary selection) of (a) at $t = -2.5\,\text{ms}$ [compare the red line in (a)]. Also shown is the AC-side switch voltage v_{S1a} of the corresponding phase (compare Fig. 1*b*), ***(c)*** Identical output power and operating conditions as in (b), but with $1.5\,\text{k}\Omega + 330\,\text{pF}$ RC snubbers connected to the switching nodes (compare Fig. 8)

current total harmonic distortion (THD) is determined by the instrument as follows:

$$\text{THD}(\%) = \frac{\sqrt{\sum_{k=2}^{100} i_{gx,k}^2}}{i_{gx}} 100, \tag{15}$$

where $i_{gx,k}$ denotes the amplitude of the kth integer harmonic current component and i_{gx} is the RMS value of the grid current, considering all harmonics.

4.1 Verification of proposed improvements

Fig. 10 verifies the reduced blocking voltage requirements of the AC- and DC-side power MOSFETs (compare Section 3), which match with the simulation results of Fig. 7*b*. The blocking voltage measurements also coincide with the derivations outlined in Section 3. Note that the (small) voltage slope of the drain–source voltage during the AC-side transistor's turn-off intervals (compare Fig. 10*b*) are caused by LC oscillations in the converter's input filter. More details of the filter are given in Section 4.5 below.

Furthermore, the CM voltage from the DC midpoint to the star point of the three-phase voltage source is, as expected, zero, which is verified with the measurement in Fig. 10*c*.

4.2 Switching behaviour and grid current distortion

The inductor current i_{L1a}, together with the AC-side switch voltage v_{S1a} (compare Fig. 1*b*), is illustrated in Figs. 11*a* and *b*. The switching waveforms correspond to the simulated behaviour outlined in Figs. 2 and 3 above. However, at the end of the demagnetisation of all three inductors, during interval ④ (compare Fig. 3), the switch voltages and inductor currents begin to oscillate as shown in Fig. 11*b*. During this time, the switch nodes SN_x (compare Fig. 8) are not clamped to a fixed potential, as the inductors are demagnetised and no current is being conducted. Hence, the potentials of these voltages begin to oscillate, which is caused by the LC resonant tanks formed by the MOSFET and diode parasitic output capacitances and the buck–boost inductors L_1. This behaviour is commonplace in many power converters operating in DCM (e.g. buck, boost, flyback etc.). At the end of the switching period and/or beginning of the subsequent switching cycle, the AC-side switches are turned on and the potentials of the switch nodes SN_x become fixed again.

These parasitic oscillations cause non-zero initial values of the inductor currents i_{L1x}, which lead to the fact that the final peak inductor currents at the end of interval ① are not directly proportional to the local grid voltage anymore. Similarly, the turn-on switching times of the AC-side switches vary due to oscillating initial blocking voltages at the turn-on instants. This non-ideal switching behaviour introduces harmonic distortion of the grid input currents of the rectifier.

Fig. 12*a* illustrates the input current distortion of the rectifier. These waveforms can also be replicated in the circuit simulation model by considering the non-linear parasitic output capacitances of the MOSFETs and diodes.

The observed effects can be mitigated by damping the parasitic oscillations during the demagnetisation intervals by means of RC snubbers, connected as shown in Fig. 8. By attenuating the parasitic LC oscillations, the initial current of each buck–boost inductor can be (ideally) rendered zero at the beginning of each pulse interval, and the switch blocking voltages at their turn-on instant are rendered (ideally) constant. By adding three RC snubbers with $R_s = 1.5\,\text{k}\Omega$ and $C_s = 330\,\text{pF}$ to the switch nodes, the measured waveforms illustrated in Fig. 11*c* are obtained. The attenuating effect of the snubbers is clearly visible. Consequently, the grid current THD is improved, as the measurement results in Fig. 12*b* demonstrate. By adding the snubbers, the input current THD improves from 4.89 to 3.08% in this example.

Owing to the attenuation requirement of the snubber, the rectifier dissipates an additional ≃17.8 W of losses in the snubber resistors, which, for the case at hand, reduces the conversion efficiency from 95.1 to 93.1%.

Consequently, there is a trade-off between grid current THD and snubber losses. Computer circuit simulations, which consider different snubber component values R_s and C_s, and the non-linear parasitic MOSFET and diode capacitances are performed to illustrate this. Fig. 13 shows the resulting THD and snubber losses as a function of the snubber resistance and capacitance. The considered hardware configuration operates with a 400 V, 50 Hz grid at 400 V output voltage with $P_{out} = 800\,\text{W}$. The investigation shows that there is an optimal R_sC_s combination that minimises both THD and snubber losses. Furthermore, with snubber capacitance values of more than ≃330 pF, the best achievable THD

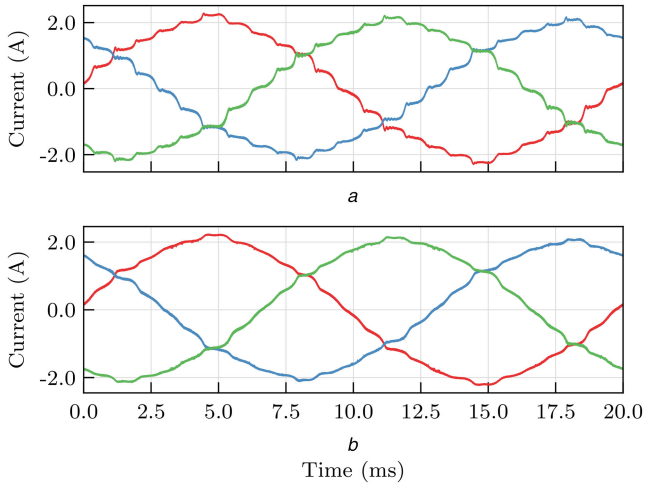

Fig. 12 *Measured rectifier input currents for $V_{LL} = 400\,\text{V}$, $f_g = 50\,Hz$, $V_{DC} = 450\,\text{V}$, and $P_{\text{out}} = 1\,\text{kW}$*

(a) Distorted grid currents due to the parasitic oscillations after the demagnetisation of the three inductors. THD = 5.1%, ***(b)*** RC snubbers (1.5 kΩ + 330 pF) provided to dampen the parasitic oscillations and reduce input current distortion. THD = 3.95%. The snubbers introduce additional 17.8 W of losses

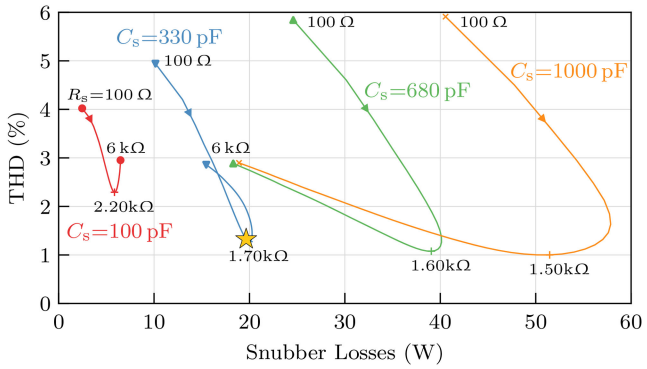

Fig. 13 *Simulated dependencies of the grid current THD and the snubber losses for different R_sC_s combinations (compare Fig. 8). Four different snubber capacitance values are considered, while the snubber resistance R_s is swept from 100 Ω to 6 kΩ. The data (60 points for each sweep) is obtained with circuit simulations that model all important non-linear device capacitances. The star indicates the selected snubber design (1.5 kΩ + 330 pF) of the prototype for $V_{LL} = 400\,\text{V}$, $f_g = 50\,\text{Hz}$, $V_{DC} = 400\,\text{V}$, and $P_{out} = 800\,\text{W}$*

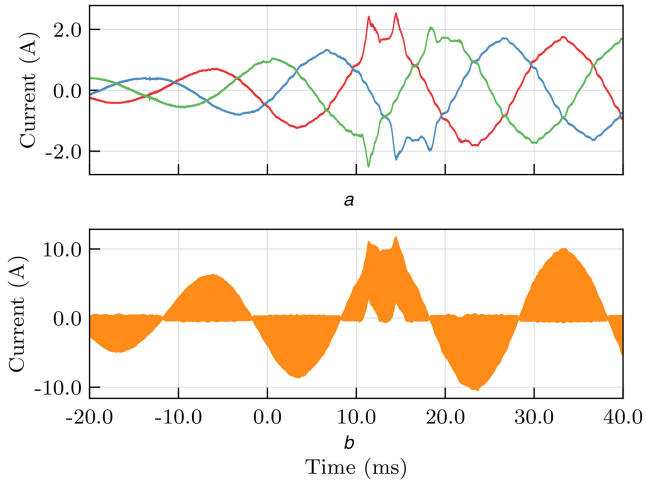

Fig. 14 *Measured currents during a load step from 200 to 900 W with a PI-controlled output voltage of $V_{DC} = 440\,\text{V}$*

(a) Converter input currents, ***(b)*** Current of the inductor L_{1a}

has not improved anymore. For the experimental analysis of the RC snubber, a combination of $R_s = 1.5\,\text{k}\Omega$ and $C_s = 330\,\text{pF}$ has, therefore, been selected. Note that the losses of this snubber combination, which is indicated by the star in Fig. 13, coincide well with the measurements shown in Figs. 11 and 12, where the snubber increases the losses by approximately the predicted ≃18 W.

The experimentally determined THD values (compare Fig. 12) are not as low as suggested by the simulation results. This is due to the presence of other non-linear elements such as the ceramic input filter capacitors that also contribute to the converter's current distortion. They are not considered in the model to reduce simulation complexity.

4.3 Transient behaviour

The effect of the output voltage control is illustrated with a load step in Fig. 14, where the output power is increased from 200 to 900 W by means of a relay that connects a second load resistor in parallel to the first load resistor. The DC output voltage reference is set to 440 V and a simple PI controller is used to adjust the duty cycle D accordingly (see Section 2.4 and also Fig. 8).

Since there is no limitation of the duty cycle according to (10), the inductor currents can briefly transition into a CCM regime during the transient. This behaviour is expected and it consequently leads to distorted rectifier input currents. Most importantly, the measurement illustrates that an interlock time between the turn-off of the DC-side switches and the turn-on of the AC-side switches, during which all power MOSFETs are turned off, is not feasible in this topology as a conduction path for the non-zero inductor current during CCM converter operation always has to be provided.

Note that if the snubbers used to improve the THD are utilised (compare Section 4.2 above), they provide a closed current path at all times during the commutation interval, which alleviates requirements for the temporal precision of the AC- and DC-side transistor switching actions. Nonetheless, due to the gate drivers of the hardware demonstrator that provide low propagation delay skews (compare beginning of Section 4), the demonstrator can also operate in CCM without the RC snubbers.

4.4 Conversion efficiency

The converter's power conversion efficiency from its AC input to the DC output is measured for different operating conditions, with and without the optimised RC snubber (1.5 kΩ + 330 pF), compare Fig. 15. The input power factor is always >0.992.

The rectifier can also operate at elevated grid frequencies (e.g. considering aircraft applications), as its switching and modulation scheme is independent of the input grid frequency [5]. Owing to increased losses of the input filter components, the efficiency deteriorates at higher grid frequencies, e.g. at 500 Hz and output power of 1 kW, the efficiency drops from 95.3% (50 Hz) to 94.0% ($V_{\text{LL}} = 400\,\text{V}$ and $V_{\text{DC}} = 450\,\text{V}$).

Note that in Fig. 15, the measurements without the damping RC snubber show more variation than the measurements obtained with the RC snubber, which result in smoother curves. This is caused by the parasitic oscillations of the switch nodes (compare Section 4.2 above). Depending on the operating point (i.e. output voltage and/or power) of the converter, the switching instants of the AC-side switches occur at different time instants during the parasitic oscillations, which results in varying switch voltages, and thus varying capacitive turn-on losses. This affects both switching losses and THD. The dampening RC snubbers lead to a more consistent switching behaviour. Hence, efficiency and THD are less affected by small changes in the operating point.

4.5 EMI performance

The demonstrator system comprises an input filter in order to comply with common standards for conducted emissions into the grid (compare Fig. 8). Note that the filter stages are damped in the high-frequency domain by the usage of iron powder cores. Fig. 16 illustrates the result of a corresponding EMI compliance

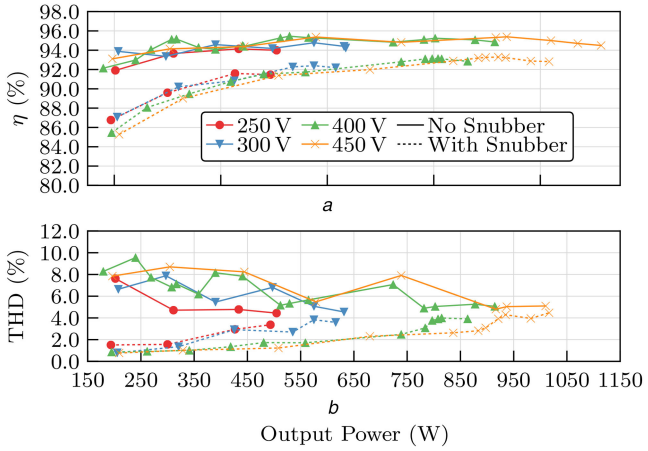

Fig. 15 *Key converter characteristics for $V_{LL} = 400\,\mathrm{V}$, $f_g = 50\,\mathrm{Hz}$, and different output voltages V_{DC} and output power levels. The utilised snubbers comprise RC series elements of $1.5\,\mathrm{k\Omega}$ and 330 pF*

(a) Power conversion efficiency. The power requirements of the auxiliary supply and the cooling systems ($\simeq 4.3\,\mathrm{W}$) are not considered for these measurements, ***(b)*** Grid current THD (phase *a* measured)

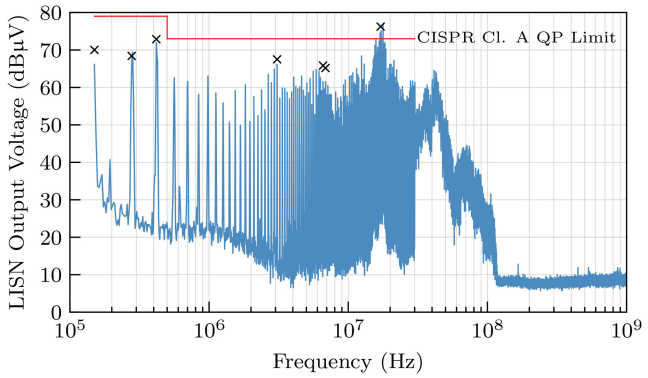

Fig. 16 *Measurement of the conducted emissions of a grid phase according to CISPR 11. Illustrated is the spectrum as obtained with the RMS detector. The markers indicate selected measurements with the quasi-peak detector according to the considered norm. The addition of the RC snubber at the switch nodes affects this spectrum only negligibly*

measurement. The input filter (whose differential-mode corner frequencies are more than a factor 10 below the switching frequency, compare Fig. 8), effectively attenuates low-order harmonics of the switching frequency and its side bands such that the rectifier is compliant with the *Class A, Group 1* specification of the *CISPR 11* norm [15]. However, at $\simeq$17 MHz, the limit is violated by $\simeq$3.2 dB. The spectrum at these frequencies is strongly affected by parasitic elements such as the capacitance of the load to Earth and/or the switching transients of the power semiconductors and must be evaluated and mitigated individually for each system. For the demonstrated measurement, a geometrically large laboratory load resistor in a grounded case is utilised, whose Earth capacitance reduces the margins of the high-frequency spectral components.

5 Conclusion

In this work, an extension of a state-of-the-art three-phase buck–boost PFC rectifier topology has been proposed in order to improve two aspects.

First, the output DC voltage of the proposed topology does not show any high-frequency CM component with respect to the grid star point or ground. Thereby, concerns regarding EMI or a potential disturbance of a supplied load are mitigated.

Second, the voltage stress of the AC-side switches is significantly reduced, which facilitates the selection of power semiconductors with good cost-performance ratios, also in case of comparably high line-to-line voltages such as 400 V. For grids with 115 V phase voltage (200 V line-to-line) as found on aircraft, the proposed topology could be realised using 600 V power semiconductors. The requirement of bidirectional switches on the AC side will not impact the chip area usage severely due to the individually reduced blocking voltage ratings. Also, bidirectional GaN power transistors could be employed in the future [14]. Furthermore, the absence of a significant high-frequency CM voltage component of the output voltage reduces CM filtering efforts, and hence the size and costs of the corresponding passive components.

A 1 kW hardware demonstrator system with a closed-loop output voltage controller has been built and used to verify the theoretical considerations. Peak power conversion efficiencies reach 95.3%, while the grid input current distortions remain below ~5%.

Experiments reveal the negative influence of the parasitic MOSFET and diode capacitances on the grid current THD. It is shown how an RC snubber can be introduced and optimised in order to improve the rectifier input current THD, at the expense of additional snubber losses. However, an optimal snubber combination, which minimises both THD and losses, can be found. It is verified how an optimised RC snubber can improve the grid current THD to levels around 3%, while the efficiency is reduced to about 93% due to the additional snubber losses.

All in all, the converter topology can operate as a buck or boost converter, and with a wide range of mains' frequencies without changes in its modulation or control scheme, which is compellingly straightforward and does not require any current sensors. This low complexity and the comparably high efficiency and power density (2.7 kW/l or 44.6 W/in^3) render the topology highly suitable for low-power three-phase rectifier applications, e.g. for future aircraft or for the DC-link supply of low-power drive or automation systems.

6 Acknowledgments

The authors thank H. Sarnago and Ó. Lucía from the University of Zaragoza, Spain, for interesting discussion on the non-isolated and isolated three-phase buck–boost PFC rectifier concepts.

7 References

[1] Singh, B., Singh, B.N., Chandra, A., *et al.*: 'A review of three-phase improved power quality AC–DC converters', *IEEE Trans. Ind. Electron*, 2004, **51**, (3), pp. 641–660

[2] Friedli, T., Hartmann, M., Kolar, J.W.: 'The essence of three-phase PFC rectifier systems – part II', *IEEE Trans. Power Electron.*, 2014, **29**, (2), pp. 543–560

[3] Nikitin, A.V., Stonestreet, A., Tidball, K.D., *et al.*: 'Ultra linear switching rectifiers (ULSRs) for high-quality regulated 3-phase AC to DC conversion'. Proc. Int. Power Electron. and Intelligent Motion Conf. (PCIM), Nuremberg, Germany, 2017, pp. 1–8

[4] Gangavarapu, S., Rathore, A. K.: 'Three phase buck–boost derived PFC converter for more electric aircraft', *IEEE Trans. Power Electron.*, 2019, **34**, (7), pp. 6264–6275

[5] Pan, C.-T., Chen, T.-C.: 'Step-up/down three-phase AC to DC converter with sinusoidal input current and unity power factor', *IEE Proc., Electr. Power Appl.*, 1994, **141**, (2), pp. 77–84

[6] Kolar, J.W., Ertl, H., Zach, F.C.: 'A novel three-phase single-switch discontinuous-mode AC–DC buck–boost converter with high-quality input current waveforms and isolated output', *IEEE Trans. Power Electron.*, 1994, **9**, (2), pp. 160–172

[7] Pollock, C., Miti, E.K.: 'Isolated step up/down three-phase AC to DC power supply', *IET Electron. Lett.*, 1995, **31**, (18), pp. 1527–1529

[8] Jorquera, H., Henrard, P., Sadarnac, D., *et al.*: 'A novel three-phase, one interrupter, isolated unity power factor rectifier with automatic current shaping'. Proc. Seventh Int. Power Electron. Variable Speed Drives Conf. (IEE Conf. Publ. No. 456), London, UK, 1998, pp. 22–27

[9] Yang, L., Liang, T., Chen, J.: 'Analysis and design of a novel three-phase AC–DC buck–boost converter', *IEEE Trans. Power Electron.*, 2008, **23**, (2), pp. 707–714

[10] Yang, L., Liang, T., Chen, J., *et al.*: 'Analysis and design of a novel, single-stage, three-phase AC/DC step-down converter with electrical isolation', *IET Power Electron.*, 2008, **1**, (1), pp. 154–163

[11] Borges, A.R., Barbi, I.: 'Study of single stage buck–boost three-phase rectifier with high power factor operating in discontinuous conduction mode (DCM)'. Proc. Brazilian Power Electronics Conf. (COBEP), Bonito-Mato Grosso do Sul, Brazil, September 2009, pp. 870–877

[12] Miniböck, J.: 'Dreiphasen-hoch-tiefsetz-gleichrichter-system mit sinusförmigem eingangsstrom und geregelter gleichtaktfreier ausgangsspannung (in German)'. Austrian Patent Appl., 5 January 2017

[13] Silicon Labs Co.: 'Si827x digital signal isolator', Datasheet, rev. 0.6, December 2017

[14] Morita, T., Yanagihara, M., Ishida, H., *et al.*: '650 V 3.1 mΩ cm^2 GaN-based monolithic bidirectional switch using normally off gate injection transistor'. Proc. IEEE Int. Electron Devices Meeting, Washington, DC, USA, 2007, pp. 865–868

[15] Burkart, R., Kolar, J.W.: 'Overview and comparison of grid harmonics and conducted EMI standards for LV converters connected to the MV distribution system'. Proc. Power Electronics South America Conf. (PCIM), Nuremberg, Germany, 2012