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# On the Tradeoff Between Input Current Quality and Efficiency of High Switching Frequency PWM Rectifiers

Michael Hartmann, *Member, IEEE*, Hans Ertl, *Member, IEEE*, and Johann W. Kolar, *Fellow, IEEE*

**Abstract**—Due to their basic physical properties, power MOSFETs exhibit an output capacitance  $C_{oss}$  that is dependent on the drain-source voltage. This (nonlinear) parasitic capacitance has to be charged at turn-off of the MOSFET by the drain-source current in rectifier applications that yield input current distortions. A detailed analysis shows that the nonlinear behavior of this capacitance is even more pronounced for modern super junction MOSFET devices. Whereas  $C_{oss}$  increases with increasing chip area, the on-state resistance of the MOSFET decreases accordingly. Hence, a tradeoff between efficiency and input current distortions exists. A detailed analysis of this effect considering different semiconductor technologies is given in this study and a Pareto curve in the  $\eta$ -THD<sub>I</sub> space is drawn that clearly highlights this relationship. It is further shown that the distortions can be reduced considerably by the application of a proper feedforward control signal counteracting the nonlinear switching delay due to  $C_{oss}$ . The theoretical considerations are verified by experimental results taken from 10-kW laboratory prototypes with the switching frequencies of 250 kHz and 1 MHz.

**Index Terms**—Efficiency, high-frequency power converters, input current quality, super junction (SJ).

## I. INTRODUCTION

IN response to new application fields such as power electronics in aircraft [1] modern rectifier systems have to satisfy more demanding requirements concerning efficiency, weight, and compactness. Furthermore, they have to comply with emerging standards containing rigorous input current harmonic limits. Active pulse width modulation (PWM) rectifiers with low total harmonic distortion (THD) of the input current and a high power factor are required. Active three-phase rectifiers typically show a large high-frequency noise level and passive low-pass filters have to be used to reduce conducted emissions. These passive

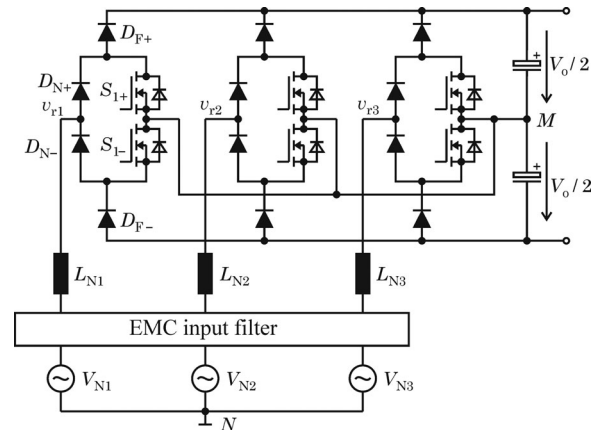


Fig. 1. Active three-phase/level PWM-rectifier used to study the tradeoff between input current quality and efficiency.

elements together with the boost inductance occupy a relatively large portion of the system volume (approximately 30%) and their size can only be reduced by increasing the switching frequency [2].

As presented in [3], the three-phase/level rectifier topology shown in Fig. 1 emerged as an ideal topology for a high power density unity power factor rectifier. Due to its reduced semiconductor voltage stress, high-efficiency MOSFETs with a breakdown voltage of 600 V can be applied even for a grid voltage of  $V_N = 230$  V and an output voltage of  $V_o = 800 V_{DC}$ . Also, the recently developed three-level unidirectional rectifier topology given in [4] exhibits these advantages. In order to achieve a high system efficiency, conduction losses as well as switching losses have to be reduced. The on-state resistance of high-voltage (HV) MOSFETs ( $V_{BR,SS} = 600$  V) is dominated by the drift region resistance and it is well known that this resistance  $R_{DS,on}$  is intrinsically dependent on the breakdown voltage  $V_{BR,SS}$  of the device

$$R_{DS,on} \propto V_{BR,SS}^{2.4...2.7} \quad (1)$$

[5]. Super junction (SJ) devices, e.g., CoolMOS [6], [7], break with this rule and achieve much lower area specific on-state resistances [8]. During the on- or off-state of a power MOSFET either the applied voltage or the current through the device is small. The situation is completely different during the switching action when considerably large current and voltage levels occur simultaneously. In case of the intended power factor correction (PFC) applications also reverse recovery currents of the boost diodes have to be

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considered. This results in switching losses that are often dominant for high-frequency (hard) switched converters. In order to limit switching losses if the converters' switching frequency is raised, the overlapping time where considerably large current and voltage levels occur have to be reduced. This can be done by an increase of the switching speed of the devices. The switching speed is determined mainly by parasitic elements of the power devices (MOSFETs and diodes) and by the wiring. Hence, the parasitic capacitances of the MOSFET mainly influence the system behavior and efficiency [9]. With respect to losses a more meaningful figure of merit (FOM)

$$\text{FOM} = \frac{1}{R_{\text{DS,on}} E_{400\text{V}}} \quad (2)$$

can be defined, where  $R_{\text{DS,on}}$  is the MOSFETs on-state resistance and  $E_{400\text{V}}$  is the stored energy in the MOSFETs output capacitance  $C_{\text{oss}}$  at  $V_{\text{DS}} = 400\text{V}$ . Modern SJ devices exhibit smaller output capacitances (at  $V_{\text{DS}} = 400\text{V}$ ) than standard HV-MOSFETs and are, therefore, ideally suited for hard-switched high-frequency rectifier systems. The MOSFETs output capacitance is proportional to the chip area  $A_{\text{Chip}}$  and shows a strong nonlinear dependence on the applied drain-source voltage. For typical SJ devices, this capacitance rises from a few 100 pF to over 10 nF for low-blocking voltage levels. As reported in [10], this effect causes long delay times at turn-off of the device that results in significant current distortions at lower current levels. This effect is even more distinctive if higher switching frequencies are used or if a device with a large chip area is applied. This is in basic contradiction to the requirement of low conduction losses (low  $R_{\text{DS,on}}$ ). A tradeoff between efficiency and input current quality has to be accepted at selection of the switches.

In Sections II and III, the origin and impact of the input current distortions are analyzed in detail, and in Section V, the power losses of the rectifier system are calculated. Based on these results a  $\eta$ -THD<sub>I</sub> Pareto curve is derived in Section VI that clearly illustrates the tradeoff between efficiency and input current quality. More information about the Pareto curve concept can be found in [11].

## II. SWITCHING MODEL OF A POWER MOSFET

In Fig. 2, the structure of a "conventional" HV-MOSFET is shown together with the structure of an SJ device. For HV-MOSFETs, a low-doped  $n^-$  drift-zone (resulting in a wide depletion zone at blocking of the device) is used to achieve the required breakdown voltage. The degree of doping and the length of this  $n^-$  layer is, therefore, dependent on the breakdown voltage and as the full drain-source current has to flow through this layer also the on-state resistance of the device depends on the breakdown voltage that finally results in the relation given in (1). As also depicted in Fig. 2(a), the structure of an HV-MOSFET results in a triangular electrical field distribution.

In order to further improve the on-state resistance of HV-MOSFETs, SJ devices have been introduced [6]. SJ devices are based on the idea of charge balancing between alternating n- and p-regions during the blocking state. As apparent in Fig. 2(b),

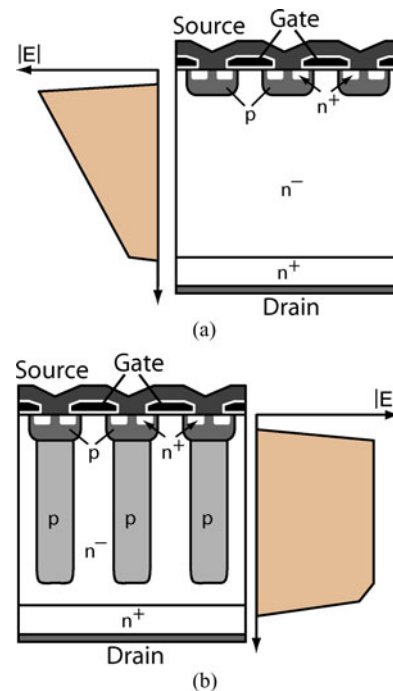


Fig. 2. Cross section and electrical field distribution of (a) conventional HV-MOSFET and (b) SJ device (e.g., CoolMOS). Whereas the HV-MOSFET shows a triangular shaped electrical field distribution, an SJ device shows a mostly squared distribution.

p-pillars are inserted that range deep into the  $n^-$  layer. The additional charge of the higher doped n-layer (used to reduce the on-state resistance) is balanced by the p-doped regions<sup>1</sup> and this yields a lateral electrical field component. If a blocking voltage is applied to the device the space charge region initially grows laterally along the p-n junction and at a relative low blocking voltage, e.g., 50 V, the full area is depleted. In order to further increase the blocking voltage the depleted region acts like a pin structure and only the vertical electrical field component is increased for higher blocking voltages resulting in an almost rectangular electrical field distribution. The SJ-structure has been analyzed in detail in [12] and the calculation shows that the on-state resistance  $R_{\text{DS,on,SJ}}$  is only linearly dependent on the breakdown voltage  $V_{\text{BR,SS}}$

$$R_{\text{DS,on,SJ}} \propto V_{\text{BR,SS}}. \quad (3)$$

The operating principle of SJ devices is based on a perfect charge compensation in the n- and p-pillars and as is shown in [13] a charge imbalance would yield a reduced breakdown voltage  $V_{\text{BR,SS}}$ . The fabrication of mostly charge compensated n- and p-pillars is hence the key to enabling this technology. Detailed information on the device physics, implementation issues, and behavior of SJ devices can be found in [14]–[16].

In Fig. 3(a), a simplified equivalent circuit of a power MOSFET is shown which is valid for frequencies up to several MHz. The capacitances  $C_{\text{GS}}$ ,  $C_{\text{GD}}$ , and  $C_{\text{DS}}$  are actually distributed over the whole surface area of the device and are

<sup>1</sup>Since the additional charges in the  $n^-$ -layer are compensated by the p-columns these devices are also called "charge-compensated devices."

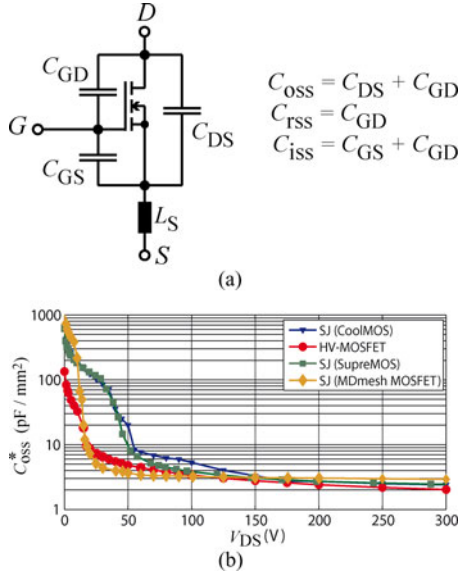


Fig. 3. (a) Equivalent circuit of a power MOSFET valid for frequencies up to several megahertz. (b) Measured area specific output capacitance  $C_{oss}^*$  as a function of the applied blocking voltage  $V_{DS}$  of several SJ devices from different manufacturers [CoolMOS (IPP60R099CP), SupreMOS (FCA22N60), and MDmesh power MOSFET (STW42N65M5) compared to an HV-MOSFET (IRFP27N60)].

lumped to these single capacitors. In addition, the parasitic inductance of the source lead  $L_S$  is depicted. High  $di/dt$ -rates of the drain-source current induce a voltage that reduces the effective gate voltage in terms of a negative feedback. This parasitic inductance has a major impact on switching losses and its impact can only be reduced by increasing the gate voltage. Whereas  $C_{GS}$  shows only minor variations with applied drain-source voltage  $V_{DS}$  the capacitances  $C_{GD}$  and  $C_{DS}$  are strongly dependent on  $V_{DS}$ .

If a blocking voltage is applied to an HV-MOSFET a space charge region grows into the epi-layer  $n^-$  that is modeled by the nonlinear drain-source capacitance  $C_{DS}$ . In general the capacitance value of a junction depletion capacitance approximately varies in proportion to  $1/\sqrt{V_{DS}}$  where  $V_{DS}$  is the applied blocking voltage. The capacitance value is further directly proportional to the chip area  $A_{chip}$  and a capacitance value per chip area  $C_{DS}^*$  can be defined. The nonlinear capacitance  $C_{DS}$  can, therefore, be modeled by

$$C_{DS} \approx A_{chip} \cdot C_{DS,0}^* \sqrt{\frac{V_{DS,0}}{V_{DS}}} \quad (4)$$

There,  $V_{DS,0}$  is the drain-source voltage where the chip area-dependent capacitance  $C_{DS,0}^* = C_{DS,0}/A_{chip}$  is measured. Further details can be found in [17]. The voltage dependence of the gate-drain capacitance  $C_{GD}$  is very similar to  $C_{DS}$  even if it is not a junction-depletion capacitance but this is not discussed further here for the sake of brevity.

Fig. 3(b) shows the measured output capacitance per chip area  $C_{oss}^* = C_{DS}^* + C_{GD}^*$  of a “conventional” HV-MOSFET (IRFP27N60) compared to the output capacitance of SJ devices of different manufacturers. The behavior given in (4) is obvious for the HV-MOSFET.

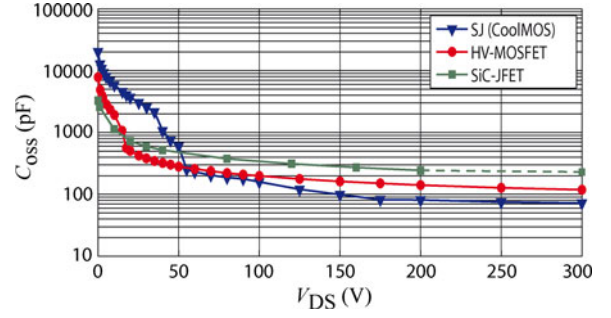


Fig. 4. Measured output capacitance  $C_{oss}$  of an HV-MOSFET (IRFP27N60), an SJ device (IPP60R099CP), and an SiC-JFET (1200 V/30 A, normally OFF) as a function of the applied blocking voltage  $V_{DS}$ .

In SJ MOSFETs, the space charge region starts to grow along the p-n junctions of the inserted p-stripes if a blocking voltage is applied to the device that yields to a drastically increased internal surface of the p-n junction [7]. Consequently,  $C_{oss}$  is very large at low  $V_{DS}$  and (4) is not valid for these devices. At a relative low blocking voltage ( $\approx 50$  V) the depletion layers of the p-n junctions merge and at this point  $C_{oss}$  decreases abruptly. According to Fig. 3(b), all SJ devices show this effect and the devices from different manufacturers only differ in the drain-source voltage where this abrupt decrease occurs.

In Fig. 4, the measured output capacitances  $C_{oss}$  of an SJ device (IPP60R099CP) and an HV-MOSFET (IRFP27N60) are plotted together with the output capacitance of a 1200 V/30 A normally OFF SiC-JFET device (SJEP120R063). Specific parameter of the devices are listed in Table I. The small chip area required for the SJ device yields to a small  $C_{oss}$  at  $V_{DS} = 300$  V. Because of the larger chip area, the HV-MOSFET shows a higher  $C_{oss}$  at  $V_{DS} = 300$  V but its capacitance only rises according to (4) and is much smaller than  $C_{oss}$  of the SJ device for  $V_{DS} < 50$  V. In comparison to the devices based on the Si-technology, the SiC JFET requires the smallest chip area but shows the largest  $C_{oss}$  at 300 V. However, only a rather small rise can be observed at smaller drain-source voltages.

#### A. Turn-on delay of MOSFET

The turn-on transient of the MOSFET is mainly determined by the applied gate driver, gate voltage  $V_G$ , and gate resistance  $R_G$ . In a first step, the gate voltage is charged until the threshold voltage  $V_{GS,th}$  is reached. Then, the MOSFET starts to conduct current and the drain-source current  $i_{DS}$  rises according to the transconductance  $g_m$  of the device. During this time the drain-source voltage is still high that yields to losses in the device. After the MOSFET conducts the full current  $I_{DS}$  the drain-source voltage drops. The slew rate of the falling drain-source voltage is defined by the Miller capacitance of the MOSFET  $C_{GD}$  and the applied gate driver  $dv_{DS}/dt = i_G/C_{GD}$ , where  $i_G$  is the gate current that is preset by the gate driver. The whole switching transient is determined by the gate driver and a considerably large gate voltage in combination with a small gate resistance allows us to achieve very small turn-on switching transients and turn-on delays. Please note that the increase of turn-on switching speed is limited by turn-on switching transient

TABLE I  
PARAMETERS OF THE MOSFETs USED FOR BENCHMARKING

	$V_{BR,SS}$ (V)	$A_{Chip}$ (mm <sup>2</sup> )	$C_{oss}^*$ (nF/mm <sup>2</sup> ) (300 V)	$R_{DS,on}^*$ ( $\Omega$ mm <sup>2</sup> ) (25 °C)	$(R_{DSon}E_{400V})^{-1}$ ( $\Omega\mu$ J) <sup>-1</sup> (FOM)	$Q_G^*$ (nC/mm <sup>2</sup> ) (15 V)	$E_{400V}$ ( $\mu$ J) (400 V)
SJ-MOSFETs							
CoolMOS: IPP60R099CP	650	30	2.4	2.7	0.97	2.8	11.5
MDmesh MOSFET: STW42N50M5	650	33	2.9	2.6	1.58	4.3	8
SupreMOS: FCA22N60	600	19.5	2.45	3.2	0.81	3.89	7.5
HV-MOSFET: IRFP27N60	600	59	2	10.6	0.44	3.0	12.5
SiC JFET: SJEP120R063	1200	8	12.5	0.36	2.26	7.5 <sup>1)</sup>	4.9

<sup>1)</sup>  $V_{gate} = 2.5$  V.

oscillations analyzed in [18]. As will be further discussed in Section V, the turn-on transient lasts about 10 ns (see also Fig. 12) which is very small compared to the turn-off delay of the MOSFET to be discussed later. In addition, since the delay times of the gate driver and of the required isolation (e.g., optocoupler) exceed this value, the influence of the turn-on delay on the input current quality is not further discussed here. Switching losses are, however, generated during the turn-on transient and that will be discussed in Section V in more detail.

### B. Turn-off Delay of MOSFET

At turn-off of the power MOSFET the nonlinear output capacitance  $C_{oss}$  has to be charged. In PFC applications, the input current has to charge this capacitance which results in an input current-dependent voltage-rise of the drain-source voltage  $V_{DS}$ . Fig. 5(a) shows the measured turn-off behavior of a CoolMOS device with a chip area of  $A_{Chip} = 30$  mm<sup>2</sup> (CoolMOS IPP60R099CP) for an input current of 1.3 A. A gate resistance of  $R_G = 7.5$   $\Omega$  and a gate voltage of  $V_G = 14$  V has been used for the measurements. Directly after the gate-source voltage  $V_{GS}$  is brought to zero by the gate driver the drain-source voltage is still small. According to Fig. 4, the nonlinear output capacitance shows values in the range of some nanofarad and the voltage raise  $dv_{DS}/dt = i_{DS}/C_{DS}$  is, therefore, very small. As the drain-source voltage slowly rises the voltage-dependent output capacitance  $C_{oss}$  gets smaller which results in higher  $dv/dt$  of the drain-source voltage. As  $C_{oss}$  is charged by the input current, the voltage rise and, therefore, also the turn-off delay, is strongly dependent on this current that finally results in considerably large duration for turn-off until the output voltage is fully charged. Similar to MOSFET data sheets the total turn-off delay can be separated in a pure delay time  $t_{d(off)}$ , where the dramatically increased  $C_{oss}$  for  $V_{DS} < 50$  V (see also Fig. 3) is charged, and in a rise time  $t_r$ . This current-dependent turn-off delay distorts the intended pulse pattern in terms of extended on-times and its influence rises with increased switching frequency. The drain-source current-dependent turn-off delays of several SJ devices of the CoolMOS CP-series (Infineon Inc. IPP60R099CP) and HV-MOSFETs (Vishay Siliconix Inc. IRFP27N60) have been measured. Using the specific chip areas  $A_{Chip}$  of the devices (see Table I), the chip area-specific turn-off delays,  $delay^* = delay/A_{Chip}$  of the devices can be calculated. MOSFET devices of the same semiconduc-

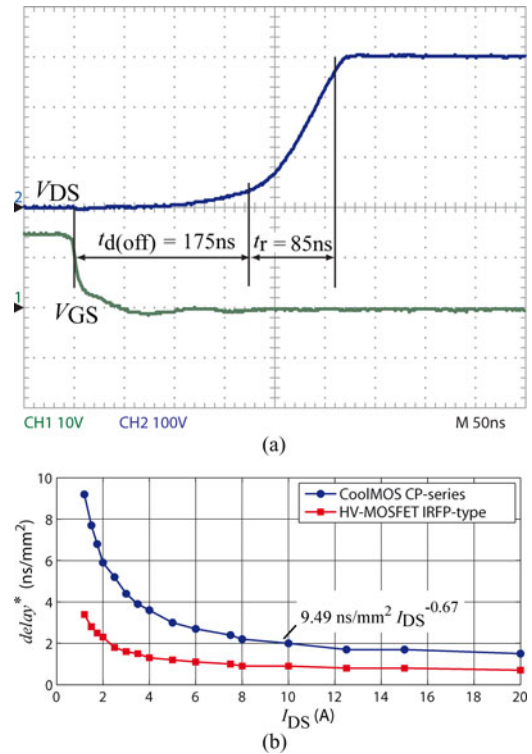


Fig. 5. (a) Measured inductive turn-off switching characteristic of an SJ device with a chip area of  $A_{Chip} = 30$  mm<sup>2</sup> (CoolMOS IPP60R099CP) at a drain current of 1.3 A using a gate resistance of  $R_G = 7.5$   $\Omega$  and a gate voltage of  $V_G = 14$  V. (b) Measured chip area dependent turn-off delay of the CoolMOS CP-series and the HV-MOSFET IRFP-type as a function of  $I_{DS}$ .

tor family (e.g., CoolMOS devices) roughly show equal chip area-dependent turn-off delays that are plotted in Fig. 5(b). As the nonlinear output capacitance  $C_{oss}$  is charged by the drain-source current, which is in PFC application equal to the input current, the turn-off delay increases as the drain-source current reduces. According to Fig. 5(b), the SJ devices show a higher chip-area-specific turn-off delay than the HV-MOSFET devices as the nonlinear capacitance of SJ devices rises abruptly due to its physical construction if the drain-source voltage is below a specific level (see Section II). This can also be seen in the comparatively pronounced increase of turn-off delay at smaller  $I_{DS}$  of SJ devices. According to [17],  $C_{oss}$  shows only minor dependence on temperature and hence the turn-off delay can be modeled without consideration of the temperature that has been

TABLE II  
PARAMETERS USED TO APPROXIMATE THE TURN-OFF DELAYS BY (5)

Semiconductor family	$del^*$	$\alpha$
CoolMOS CP-series	9.49 ns/mm <sup>2</sup>	-0.67
CoolMOS IPP60R099CP	284 ns ( $I_{DS}$ ) <sup>-0.67</sup>	
HV-MOSFET IRFP-type	3.64 ns/mm <sup>2</sup>	-0.54
HV-MOSFET IRFP27N60	214 ns ( $I_{DS}$ ) <sup>-0.54</sup>	

confirmed by measurements. The measured turn-off delays can be fitted by

$$\text{delay} \approx A_{\text{Chip}} \text{del}^* (I_{DS})^\alpha \quad (5)$$

using the least-square method where  $del^*$  and  $\alpha$  are the variable parameters,  $I_{DS}$  is the drain-source current at turn-off in Ampere, and  $A_{\text{Chip}}$  is the chip area of the device. This approximation will be used in the next section to determine the resulting input current distortions. The corresponding parameters ( $del^*$  and  $\alpha$ ) for the two semiconductor families are listed in Table II.

### III. EVALUATION OF INPUT CURRENT DISTORTIONS

In this section, the effects of this duty cycle distortion will be analyzed. The required duty cycle  $d_i \in [0 \dots 1]$  of phase number  $i$  of the intended rectifier system can be determined by evaluating the inductor voltage balance of the boost inductors (see Fig. 1). Because the voltage, averaged over the switching frequency, over the boost inductor must be zero, the rectifier circuit must generate an averaged rectifier voltage equal to the phase voltage [e.g.,  $V_{N1} = \hat{V}_N \sin$ ], where  $\hat{V}_N$  is the peak value of the phase voltage and  $\varphi_N = \omega_N t$  is the phase angle. Only half of the output voltage  $V_o/2$  is used in the intended three-level Vienna rectifier topology and the duty cycles of the three phases are, therefore, given by

$$d_i(\varphi_N) = 1 - \frac{\hat{V}_N}{V_o/2} \left| \sin \left( \varphi_N - \frac{2\pi}{3}(i-1) \right) \right| \quad (6)$$

where for the sake of simplicity a possible third-harmonic injection used to increase the input voltage range at a given output voltage level is not included (see also [19]). This duty cycle is calculated by the controller, and the generated pulse patterns of (6) are dependent on the input current enlarged by the turn-off delay of the MOSFET [see Fig. 5(b)]. Note that the duty cycle is limited to 1 (MOSFET is permanently ON). In Fig. 6, the duty cycle without turn-off delay (indicated in Fig. 6 with Ref.) according to (6) of switch  $S_1$  is plotted in conjunction with the grid voltages for an output power of  $P_o = 5$  kW and a modulation index of  $M = 0.813$ . As a unity power factor shall be achieved by the rectifier system, the input currents are assumed to be in phase with the input voltages and are, therefore, not shown. The duty cycle shows the well-known shape where the duty cycle at  $v_N(\varphi_N)$  near zero ( $\varphi_N = 0^\circ, 180^\circ, \dots$ ) is almost 1 and near ( $\varphi_N = 90^\circ, 270^\circ, \dots$ ) almost zero. Next to the ‘‘ideal’’ duty cycle, the distorted duty cycle  $d_{i,d}$ , enlarged by the current-dependent turn-off delay of the MOSFET according to (5)

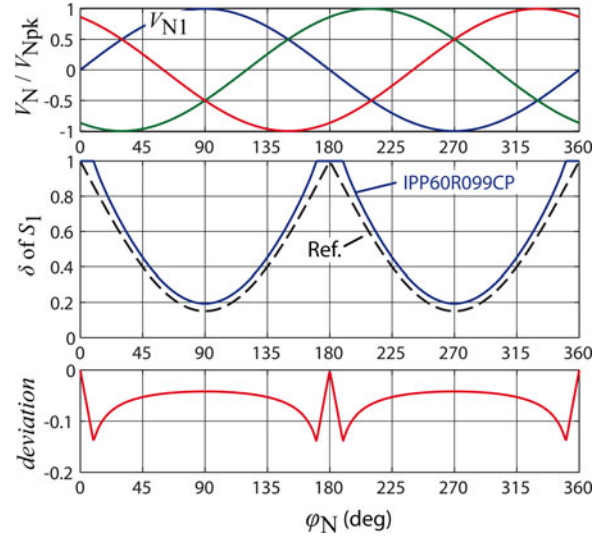


Fig. 6. Duty cycle of switch  $S_1$  without turn-off delay and distorted duty cycle due to the turn-off delay of the MOSFET for a modulation index of  $M = 0.813$ , a switching frequency of 1 MHz and an output power of  $P_o = 5$  kW considering the SJ-MOSFET IPP60R099CP with a chip area of  $A_{\text{Chip}} = 30$  mm<sup>2</sup>.

$$\begin{aligned} d_{i,d}(\varphi_N) &= d_i(\varphi_N) + \text{delay}(I_{DS}(\varphi_N)) \\ &= 1 - \frac{\hat{V}_N}{V_o/2} \left| \sin \left( \varphi_N - \frac{2\pi}{3}(i-1) \right) \right| \\ &\quad + A_{\text{Chip}} \text{del}^* (I_{DS}(\varphi_N)) \end{aligned} \quad (7)$$

is shown. An SJ device with  $A_{\text{Chip}} = 30$  mm<sup>2</sup> (CoolMOS IPP60R099CP) is used for the calculations given in Fig. 6. Also, the calculated error  $\text{error}(\varphi_N) = d_i(\varphi_N) - d_{i,d}(\varphi_N)$  is depicted. The biggest deviations can be observed in the vicinity of the phase-voltage zero-crossings where the duty cycle is near 100%. It is also apparent that small duty cycles (turn-on times smaller than the turn-off delay) cannot be implemented.

Subsequently, the measured delays given in Fig. 5 are used in a computer simulation to determine the resulting input current distortions. This is not easily possible in an analytical manner as the current controller is partially able to compensate this error. The current controller is designed according to [19] and a nonlinear block modeling the nonlinear turn-off delay according to (5) is connected in series to the PWM module. The turn-off instants of the PWM-signal are delayed with this nonlinear block. The current control loop is closed and the input current distortions are evaluated by the calculation of the  $\text{THD}_I$ -value of the simulated input currents considering  $N = 50$  harmonics of the fundamental

$$\text{THD}_I = \sqrt{\frac{\sum_{n=2}^N I_{(n)}^2}{I_{(1)}}}. \quad (8)$$

The results of this calculation for a switching frequency of 1 MHz ( $V_N = 230$  V,  $V_o = 800$  V,  $P_o = 10$  kW) are plotted in Fig. 7 for HV-MOSFETs as well as for CoolMOS devices. The simulated  $\text{THD}_I$ -values here take only the current distortions caused by the turn-off delay into account and serve as a good comparison diagram. An implemented system, however, will

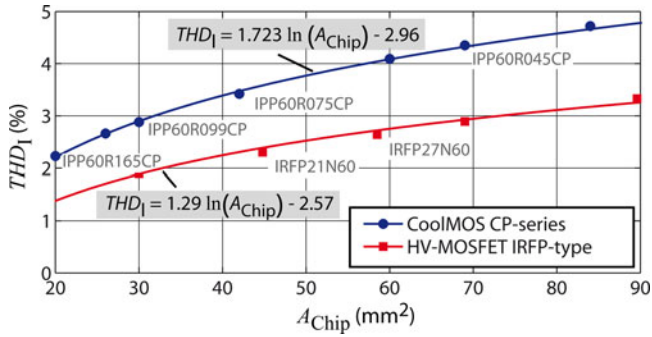


Fig. 7. Simulated  $THD_I$  of the input currents as a function of chip area  $A_{Chip}$  for a 10-kW rectifier system with a switching frequency of 1 MHz ( $f_N = 50$  Hz,  $V_N = 230$  V,  $V_o = 800$  V).

show higher  $THD_I$ -values as other effects such as cusp distortion, discontinuous mode (DCM) operation, or subsequent nonideal sampling will also take effect.

A curve fitting is used to approximate the delays for further calculations and the corresponding functions for the two semiconductor families are also given in Fig. 7. Consistent with Fig. 5, the HV-MOSFET shows a better chip area-dependent input current quality. The calculated  $THD_I(A_{Chip})$  will be combined in Section VI with the calculated efficiency  $\eta(A_{Chip})$  which finally results in the  $\eta$ - $THD_I$ -Pareto curve.

Fig. 8(a) shows the simulated input current quality as a function of chip area  $A_{Chip}$  and switching frequency  $f_s$  for the CoolMOS-CP series. In Fig. 8(b), the input current distortions are given for different CoolMOS-CP devices as a function of  $f_s$ . The corresponding specifications of the devices are listed in Table I. It is obvious that the input current distortions rise with higher switching frequency. The distortions caused by the turn-off delay are smaller than 2.5 % for all semiconductors, if a switching frequency below 250 kHz is used. If, however, a switching frequency of 1 MHz is applied, only devices with chip areas below 30 mm<sup>2</sup> (CoolMOS IPP60R165CP and IPP60R099CP) will show input current distortions near 2.5%.

In Figs. 7 and 8, the input current distortions are plotted for nominal output power of 10 kW. Considerably increased input current distortions, however, occur at operation with partial load as the input current that also charges  $C_{oss}$  gets smaller. Also, a higher mains frequency, as is, for instance, used in aerospace applications ( $f_N = 360$  Hz . . . 800 Hz), results in increased input current distortions. Fig. 9 shows the simulated  $THD_I$  value at  $P_o = 5$  kW as a function of  $f_s$  for a mains frequency of  $f_N = 400$  Hz.

As expected, increased input current distortions can be read at partial load. A device with a preferably small chip size, which consequently shows a smaller output capacitance  $C_{oss}$  and smaller turn-off delay, should, therefore, be used for a high-frequency implementation, especially if a high input current quality at partial load is required.

#### IV. FEEDFORWARD COMPENSATION OF THE DELAY

The input current distortions caused by the turn-off delay of the MOSFET can be reduced considerably, if a feedfor-

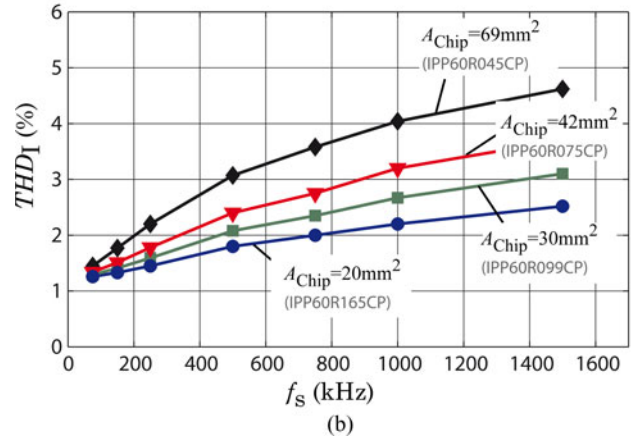
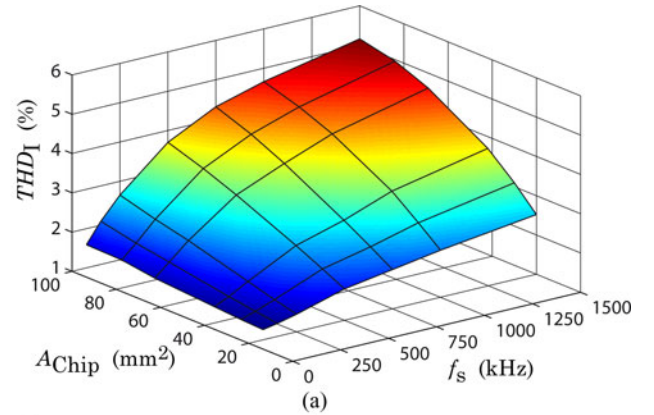


Fig. 8. (a) Simulated  $THD_I$  of the input currents as a function of chip area  $A_{Chip}$  and switching frequency  $f_s$  for the CoolMOS CP-series at  $P_o = 10$  kW. (b) Simulated  $THD_I$  as a function of  $f_s$  for CoolMOS-CP devices showing different chip areas ( $f_N = 50$  Hz,  $V_N = 230$  V,  $V_o = 800$  V).

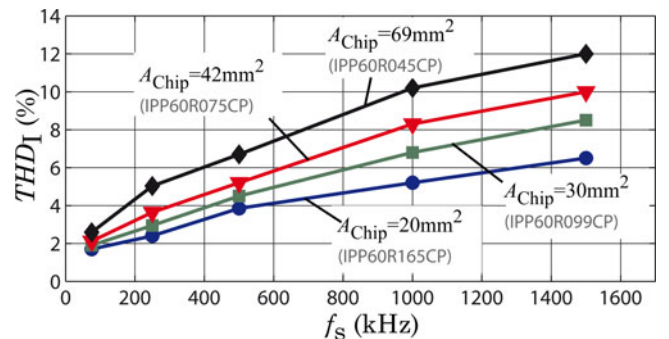


Fig. 9. Simulated  $THD_I$  of the input currents as a function of switching frequency  $f_s$  for the CoolMOS CP-series at half output power  $P_o = 5$  kW and  $f_N = 400$  Hz ( $V_N = 230$  V,  $V_o = 800$  V).

ward compensation is implemented. Thereto, the input current-dependent turn-off delay given in (5) can be added to the current controller output  $d_{i,contr}(\varphi_N)$  in terms of a feedforward control signal  $d_{pre}(\varphi_N)$  that results in the effective duty cycle  $d_{i,eff}(\varphi_N)$

$$d_{i,eff}(\varphi_N) = d_{i,contr}(\varphi_N) - d_{i,pre}(\varphi_N). \quad (9)$$

The effective duty cycle is then transferred to the PWM in order to generate the pulse patterns for the MOSFETs and the resulting pulse pattern is finally enlarged by the turn-off delay of the MOSFET in hardware. The duty cycle is, therefore, reduced in

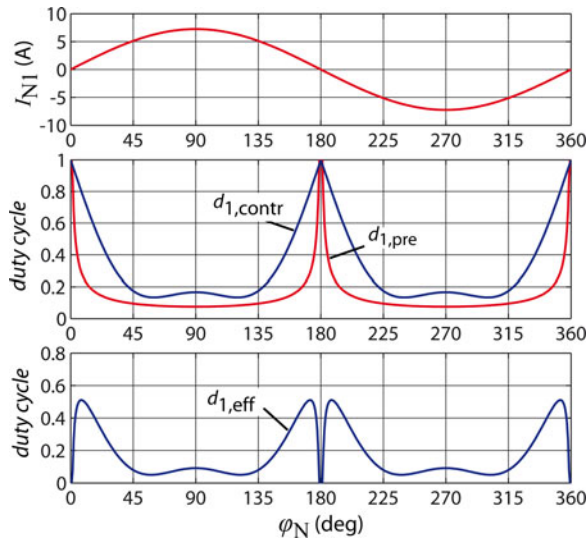


Fig. 10. Ideal duty cycle  $d_{1,contr}(\varphi_N)$  generated from the current controller and feed-forward signal  $d_{1,pre}(\varphi_N)$  signal used to compensate the turn-off delays of the MOSFET leading to the resulting effective duty cycle  $d_{1,eff}(\varphi_N)$ . The effective duty cycle will be distorted (enlarged) by the turn-off delay of the MOSFET in hardware.

software using the calculated feedforward control signal under consideration that it is enlarged in hardware by the unwanted turn-off delay of the MOSFET. As the calculation of  $d_{i,pre}(\varphi_N)$  [see (5)] is a time-consuming task in a digital controller implementation using a digital signal processor (DSP) or an field programmable gate array (FPGA), the delay given in Fig. 6 can be approximated by piecewise linear functions.

Fig. 10 shows the required duty cycle  $d_{1,contr}(\varphi_N)$  in order to generate sinusoidal input currents. This duty cycle is generated by the current controller and a third-harmonic injection signal is included that is used to increase the input voltage range. In addition, the necessary feedforward control signal  $d_{i,pre}(\varphi_N)$ , used to compensate the unwanted turn-off delay and the resulting effective duty cycle  $d_{1,eff}(\varphi_N)$ , is plotted. The greatest influence of the precontrol signal can be observed in the vicinity of the input currents zero crossings, where the duty cycle  $d_{1,contr}(\varphi_N)$  is almost 1. The duty cycle there has to be reduced considerably because the input current, which charges the output capacitance  $C_{oss}$  is small and enlarges the pulse width. According to Fig. 10, the duty cycle distortion can be compensated over long periods but, dependent on the used switch, a minimum pulse length of 100–200 ns is required in order to fully turn on the MOSFET that limits the effectiveness of the proposed feedforward compensation signal. As discussed in [19], a symmetrical PWM must be used in order to achieve low input current distortions. This offers the advantage of directly sampling the current's average value if the sampling action is synchronized with the PWM. Due to the asymmetrical nature of the turn-off delay the sampled current is not equal to the average value which is another reason for input current distortions if the turn-off delay is not exactly compensated by the feedforward signal. The proposed feedforward control signal only compensates the signal distortions caused by the turn-off delays of the MOSFETs. As a result, especially zero crossing distortions caused by the cusp



Fig. 11. Constructed ac current transformer with a sensitivity of 100 mV/A to measure the drain-source current  $I_{DS}$  of the MOSFET.

effect or by the DCM operation of the rectifier will remain. Also distortions caused by (small) phase differences between input voltage and input current, e.g., as they may occur in electronics for modern aircrafts due to the high, variable mains frequency of 360–800 Hz, are not reduced using the proposed feedforward control signal.

## V. POWER MOSFET LOSSES

As a next step, the power losses of the rectifier system have to be calculated. In general, the power losses  $P_{FET}$  of a MOSFET can be divided into switching losses  $P_{sw}$  and conduction losses  $P_{con}$

$$P_{FET} = P_{sw} + P_{con}. \quad (10)$$

Although the conduction losses can be calculated using the on-state resistance  $R_{DSon}$  of the MOSFET, the determination of the switching losses is a more complex task. If the MOSFET turns on/off the inductive current has to commutate between the free-wheeling diode and the MOSFET. In consequence, the diode and possible stray elements (stray inductances/capacitances of the wiring) have to be included in this calculation. Several research groups developed models for switching loss calculation [20]–[22] however, the most accurate approach is to measure the switching losses of the MOSFET diode combination. Due to the intended switching frequency of 1 MHz the SiC diode IDT10S60 has been selected. It is well known that SiC diodes show no reverse recovery current and that a capacitive displacement current flows if a blocking voltage is applied.

Switching losses are usually separated into turn-on losses and turn-off losses. Turn-on losses can be determined by a voltage/current measurement according to [23]. The accurate measurement of the drain-source current  $i_{DS}$  is a challenging task as the required current measurement equipment increases the inductance of the commutation loop. This influences the switching transient and, therefore, increases the switching losses. A small current transformer (see Fig. 11), which can be directly plugged on the connection leads of a MOSFET in the TO220 or TO247 case, is used to measure the drain-source current. The ac current probe shows a sensitivity of 100 mV/A. The additional inductance in the commutation loop, due to the current sensor, has been measured to be only  $\approx 3$  nH which is tolerable for the application at hand.

At turn-off of the device the nonlinear capacitance  $C_{oss}$  is charged by  $I_{DS}$  and, therefore, causes no losses. However,



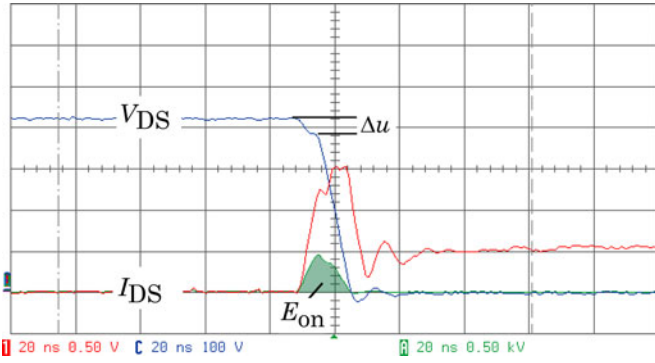


Fig. 12. Measured MOSFET turn-on switching transient at  $I_{DS} = 5\text{ A}$  and  $V_{DS} = 400\text{ V}$  for  $R_G = 7.5\ \Omega$  and  $V_G = 14\text{ V}$ . CHI:  $I_{DS}$  (5 A/Div), CHC:  $V_{DS}$  (100 V/Div), CHA:  $p(t) = v_{DS}(t) \times i_{DS}(t)$ , time scale 20 ns/Div.

according to [24], the energy stored in  $C_{oss}$  contributes considerably to the switching losses because  $C_{oss}$  has to be discharged at turn-on through the channel of the MOSFET. These losses are not covered by the switching loss measurement but can be calculated using the stored energy  $E_{400V}$  given in Table I.

A boost-type test circuit has been used to determine the turn-on losses. In order to give a fair comparison of different semiconductors, the switching transients ( $v_{DS}$  and  $i_{DS}$ ) of the SJ device IPP60R099CP are used as reference. The gate-resistors are modified until the switching transients approximately match the reference and then the devices will show approximately equal turn-on losses (independent of the chip area). This is, however, only possible for devices showing chip areas in the same order of magnitude. The comparably fast switching transient reference may not be achieved for a device with a considerably larger chip area. The internal gate resistor of the MOSFET and the negative feedback behavior of the parasitic source inductance  $L_S$  may inhibit such a fast transient. In this study, only MOSFET devices that are able to achieve the switching transient reference are considered.

Fig. 12 shows a measurement of the turn-on voltage and current transients of the CoolMOS device IPP60R099CP at  $I_{DS} = 5\text{ A}$  and  $V_{DS} = 400\text{ V}$  using a gate resistance of  $R_G = 7.5\ \Omega$  and a gate voltage of  $V_G = 14\text{ V}$ . The switching action takes about 10 ns and a current overshoot up to 15 A can be measured that is mainly caused by the capacitive displacement current of the SiC diode. Channel A (green curve) corresponds to the instantaneous power  $v_{DS} \times i_{DS}$  and its area is equivalent to the turn-on switching loss energy  $E_{on}$ . Different MOSFET/diode combinations may show diverse switching transients. The reverse recovery current of the diode may for instance be much higher if a Si diode is used instead of the SiC diode. MOSFET devices from various vendors differ in the gate threshold voltage  $V_{G(th)}$  and transconductance  $g_m$  where the transconductance  $g_m$  defines the turn-on slew rate of  $I_{DS}$ . The threshold voltage as well as  $g_m$  is further dependent on the junction temperature  $T_j$  and as the parasitic capacitances of the MOSFET devices show no temperature dependence these two elements are responsible for the slight temperature dependence of the turn-on switching loss energies.

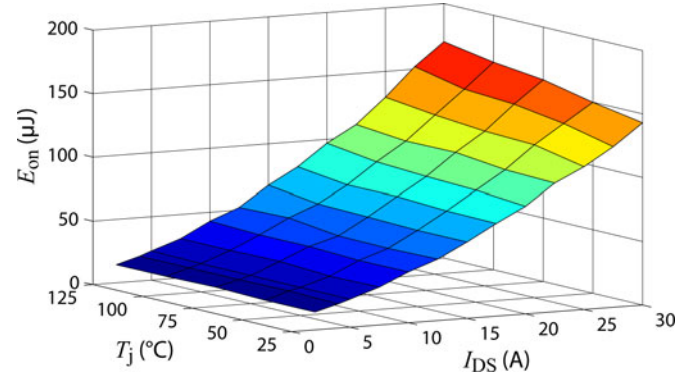


Fig. 13. Measured turn-on energies of the CoolMOS-CP semiconductor family as a function of drain-source current  $I_{DS}$  and temperature  $T_j$  at  $V_{DS} = 400\text{ V}$ .

The measured turn-on switching loss energies as a function of  $I_{DS}$  and the junction temperature ( $\Delta T = T_j - 25\text{ }^\circ\text{C}$ ) are given in Fig. 13. For further loss calculations the measured turn-on switching energy curves can be fitted by

$$E_{on}(\Delta T, I_{DS}) = (k_0 + k_1 I_{DS} + k_2 I_{DS}^2) (1 + (\gamma I_{DS}) \Delta T) \quad (11)$$

As a comparison of different CoolMOS devices with diverse chip areas shows, the energy stored in  $C_{oss}$  is also directly proportional to  $A_{chip}$  and under consideration of (11) the total switching losses can be calculated by

$$P_{sw} = \frac{1}{T_N} \int_0^{T_N} f_s E_{on}(\Delta T, I_{DS}(t)) dt + f_s E_{400V}^* A_{chip} \quad (12)$$

where  $T_N$  is the period of the mains current. Additionally, the required gate drive power  $P_g$  can be expressed as a function of the chip area

$$P_g = Q_g^* A_{chip} V_g f_s \quad (13)$$

In order to calculate the conduction losses of the MOSFET, its on-state resistance has to be determined. The  $R_{DSon}$  is a function of the junction temperature  $T_j$  and the drain-source current and a curve fit on data sheet values results in

$$R_{DSon}(\Delta T, I_{DS}) = \frac{R_{DSon,25}^*}{A_{chip}} (1 + \alpha_1 \Delta T + \alpha_2 \Delta T^2) \times (1 + \beta_1 I_{DS} + \beta_2 I_{DS}^2) \quad (14)$$

where  $R_{DSon,25}^*$  is the chip area-dependent on-state resistance at  $T_j = 25\text{ }^\circ\text{C}$  and  $I_{DS} = 0$ . Hence, the conduction losses

$$P_{con} = \frac{1}{T_N} \int_0^{T_N} R_{DSon}(\Delta T, I_{DS}) I_{DS}^2(t) dt \quad (15)$$

have to be calculated by integration over one mains period  $T_N = 1/f_N$  because (14) is nonlinear. The total MOSFET losses can be calculated by use of (10).

Both (11) and (14) require the junction temperature

$$T_j = T_s + R_{th,js}^* A_{chip} P_{FET} \quad (16)$$

which is a function of the chip area-dependent thermal interface (expressed by  $R_{th,js}^*$ ) to the heat sink (heat sink temperature  $T_s$ )

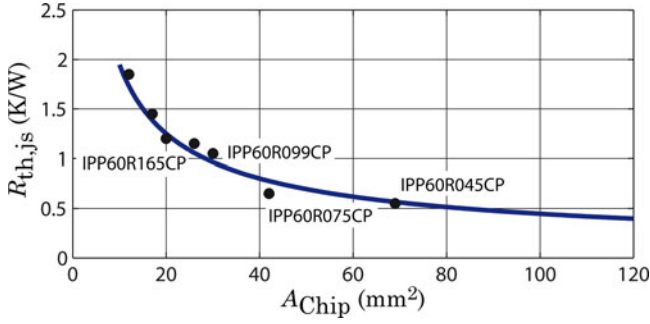


Fig. 14. Chip area-dependent thermal resistance  $R_{th,j,s}^*$  of several discrete CoolMOS-CP devices considering a thermal conducting electrical isolation sheet. A curve fitting is given that is used for further calculations.

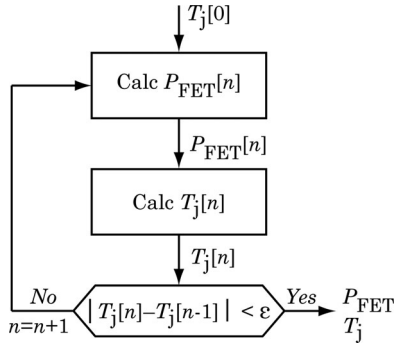


Fig. 15. Graphical illustration of the iteration process used to calculate the final junction temperature  $T_j$  and total MOSFET losses  $P_{FET}$ .

and of the total MOSFET losses. Hence, (12) and (15) have to be solved iteratively by the application of (10) and (16).

An appropriate model of the thermal interface to the heat sink  $R_{th,j,s}(A_{Chip})$  is thereto required. A chip area-dependent thermal resistance  $R_{th,j,s}(A_{Chip})$  is proposed in [25] where the whole chip is implemented using a single power module employing an  $Al_2O_3$  DCB ceramic substrate. Discrete semiconductors using the TO220 or TO247 cases shall, however, be applied for the application at hand. Several devices have, therefore, been examined and the corresponding thermal resistances are plotted in Fig. 14 considering also an isolation sheet with a thermal resistance of  $R_{th,iso} = 0.7$  K/W. A curve fit on the thermal resistances results in

$$R_{th,j,s}^* = 8.5 \text{ K/W} \left( \frac{A_{Chip}}{[mm^2]} \right)^{-0.64} \quad (17)$$

for CoolMOS-CP devices in the TO220 and TO247 case.

Due to the thermal capacitances of the MOSFET devices roughly a constant junction temperature  $T_j$  of the MOSFET is assumed during one mains period and in addition it is assumed that the cooling system ensures a constant heat sink temperature  $T_s$ . Based on this assumption, the total MOSFET power losses can be calculated using the iteration process illustrated in Fig. 15.

At the beginning of the iteration, a junction temperature  $T_j[0]$  is defined. Based on this temperature, the MOSFET losses  $P_{FET}[n]$  are calculated. According to (17) and (16), the calculated power losses on the other hand yield to the junction

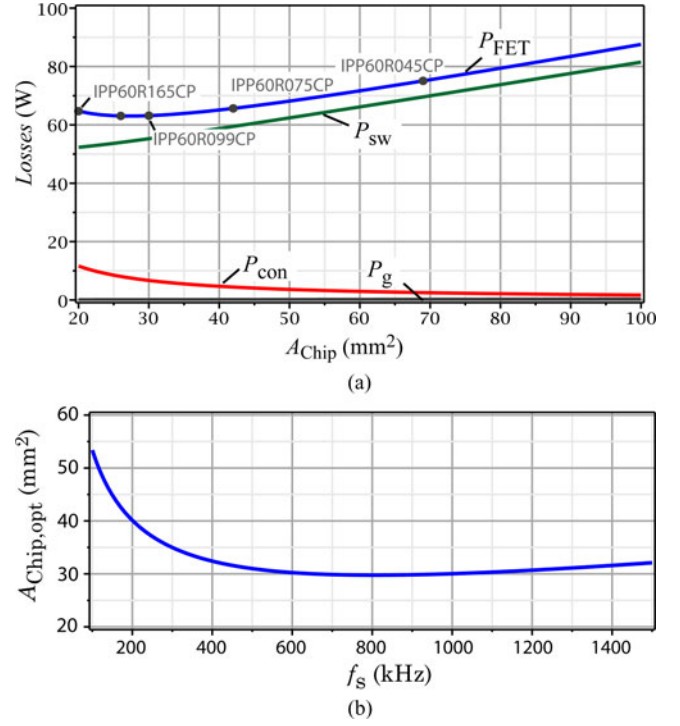


Fig. 16. (a) Dependence of the calculated power MOSFET losses  $P_{FET}$  consisting of conduction losses  $P_{con}$  and switching losses  $P_{sw}$  on the chip area  $A_{Chip}$  at a switching frequency of  $f_s = 1$  MHz and  $P_o = 10$  kW. (b) Optimal chip area  $A_{Chip,opt}$  yielding to minimal MOSFET power losses as a function of switching frequency  $f_s$ .

temperature  $T_j[n]$ . This temperature is compared to the junction temperature of the former calculation step. If the deviation is below  $\epsilon$ , the iteration terminates. As the switching losses  $P_{sw}$  as well as the conduction losses  $P_{con}$  are monotonically increasing functions in respect to the junction temperature  $T_j$ , this iteration process converges.

By application of this iteration process, the chip area-dependent power losses of SJ devices (CoolMOS-CP series) applied in the intended three-phase rectifier system (see Fig. 1) with a switching frequency of  $f_s = 1$  MHz and an output power of  $P_o = 10$  kW are calculated and the results are depicted in Fig. 16(a). It is obvious that for a switching frequency of 1 MHz the total semiconductor losses are dominated by switching losses.

The optimal chip area  $A_{Chip,opt}$  yielding to minimal semiconductor losses can be calculated as a function of the switching frequency  $f_s$  and the results are given in Fig. 16(b) for the CoolMOS-CP series. The optimal chip size decreases for higher switching frequencies and shows a minimum at  $f_s \approx 800$  kHz. Due to the better thermal interface of a larger chip area and the linearly increasing switching losses for higher switching frequencies, the optimal chip size increases for switching frequencies above 800 kHz. A chip size of  $A_{Chip} \approx 30$  mm<sup>2</sup> can, therefore, be used if a switching frequency of  $f_s = 1$  MHz is applied. As the switching losses rise linearly with switching frequency, the CoolMOS-CP series reaches the maximum temperature of  $T_{j,max} = 150$  °C at a switching frequency of 1.2 MHz for a heat sink temperature of 50 °C. A maximum

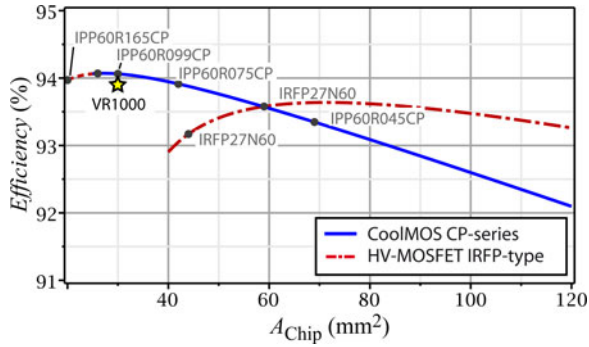


Fig. 17. Calculated total system efficiency as a function of the chip area  $A_{\text{Chip}}$  for a switching frequency of 1 MHz and an output power of  $P_o = 10$  kW. In addition, the measured efficiency of the finally constructed rectifier system VR1000 employing a CoolMOS device with a chip area of  $A_{\text{Chip}} = 30$  mm<sup>2</sup> (CoolMOS IPP60R099CP).

switching frequency of 1.2 MHz can, therefore, be implemented using the CoolMOS-CP series.

As a next step total system losses must be calculated. Only the results of this calculation are included in this study for the sake of brevity. Details on loss calculation of the intended rectifier system can be found in [26]. The resulting calculated system efficiency for a system employing SJ devices of the CoolMOS-CP series is given in Fig. 17 together with the efficiency of a system using HV-MOSFETs. In addition, the efficiency of the implemented laboratory prototype VR1000 employing a CoolMOS device with a chip area of  $A_{\text{Chip}} = 30$  mm<sup>2</sup> (CoolMOS IPP60R099CP) is depicted and is in good agreement with the calculated results. The three-phase power analyzer DEWE-2600 from Dewetron Inc., has been used for efficiency measurement. Due to the very high switching frequency and, in consequence, the high switching losses, only an efficiency of 94% can be achieved if SJ devices are applied. The junction temperature of the SJ devices for a chip area below 25 mm<sup>2</sup> (marked with a red dotted line) would rise above the limit of 150 °C and a practical implementation would, therefore, be inhibited because of the limited performance of the thermal interface. Due to the significant higher chip area-dependent  $R_{\text{DSon}}^*$  of HV-MOSFET devices, a larger chip area is required for such an implementation and a maximum efficiency of 93.6% is achievable. The chip area-dependent energy  $E_{400V}^*$  stored in  $C_{\text{oss}}$  of the HV-MOSFET is smaller than  $E_{400V}^*$  of the SJ devices (see Table I) and hence a system employing HV-MOSFETs would show a higher efficiency compared to a system using SJ devices for  $A_{\text{Chip}} > 60$  mm<sup>2</sup>. Because an implementation using SJ-devices would, however, show a higher efficiency at a smaller chip size, an implementation using SJ devices is preferred for a switching frequency of 1 MHz.

## VI. $\eta$ -THD<sub>I</sub> PARETO CURVE

In Section III, the influence of the turn-off delay of the MOSFET on the input current quality has been evaluated (see Fig. 7). The result of this analysis is a curve showing the THD<sub>I</sub> of the input currents as a function of the chip area. On the other hand, the result shown in Section V is an efficiency curve as a function of

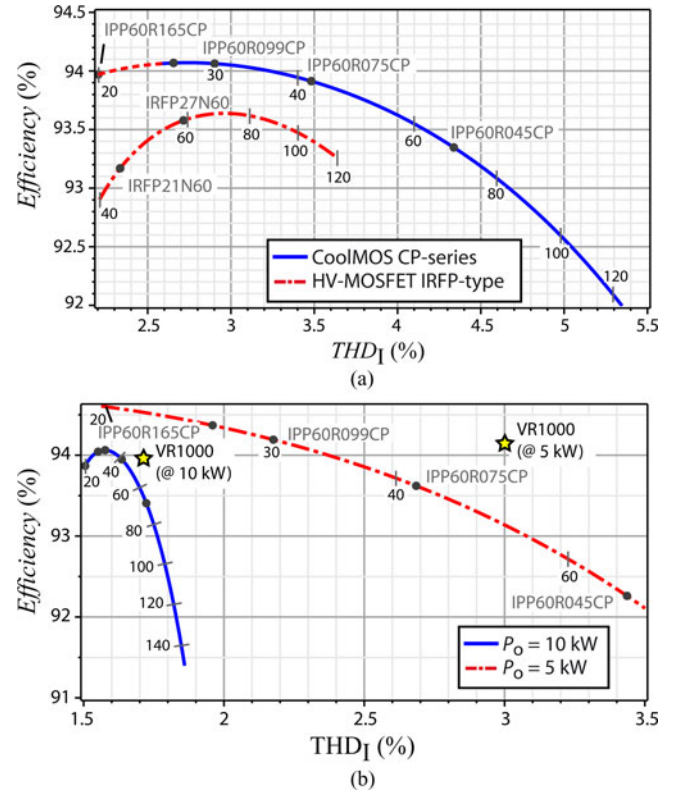


Fig. 18. Graphical representation of the tradeoff between input current quality (expressed by the THD<sub>I</sub> value) and calculated efficiency for a 10-kW rectifier system with a switching frequency of 1 MHz. (a) System operated without precontrol signal and (b) with precontrol signal at 10 and 5 kW. Corresponding chip areas  $A_{\text{Chip}}$  are marked in the curves. In addition, the specific performance of the constructed laboratory prototype VR1000 at  $P_o = 5$  kW and  $P_o = 10$  kW are given.

the chip area (see Fig. 16). The two results can be combined and the calculated system efficiency  $\eta$  can be plotted as a function of input current distortion THD<sub>I</sub>, where  $A_{\text{Chip}}$  acts as a parameter. This results in a  $\eta$ -THD<sub>I</sub> Pareto curve where the tradeoff between efficiency and input current quality is clearly illustrated. The input current quality as well as the system efficiency is strongly dependent on the switching frequency. Thereby, for every selected switching frequency required to achieve an intended power density, an own  $\eta$ -THD<sub>I</sub> Pareto curve can be drawn. Fig. 18(a) shows the resulting  $\eta$ -THD<sub>I</sub> Pareto curve for a switching frequency of 1 MHz and an output power of 10 kW for the SJ devices (CoolMOS-CP) and HV-MOSFETs if the proposed precontrol signal is not used. The corresponding chip areas are marked in the two curves. A maximal efficiency of 94% can be achieved for CoolMOS-CP devices and a THD<sub>I</sub> of 3% can be read at this point. A better THD<sub>I</sub> is inhibited by the thermal interface of the devices. On the contrary, a classical HV-MOSFET shows a substantial better THD<sub>I</sub> at same chip size but is not able to show its strength because of higher losses.

If the proposed precontrol signal added to the current controller, the input current distortion can be mostly compensated which results in the Pareto curve given in Fig. 18(b). The THD<sub>I</sub> stays below 2% for a system operating at 10 kW. If the system is, however, operated at partial load (e.g., 5 kW) a considerably

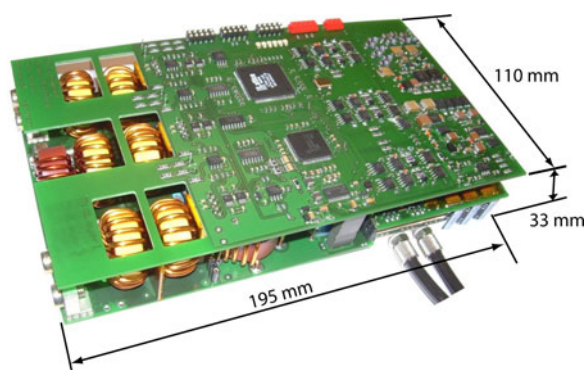


Fig. 19. Constructed 10-kW three-phase/level rectifier system employing a switching frequency of 1 MHz (Dimensions: 195 mm  $\times$  110 mm  $\times$  33 mm, power density: 14.1 kW/L).

increased  $\text{THD}_I$  can be read. In Fig. 18(b), the measured performance of the constructed laboratory prototype VR1000 (see Section VII) at  $P_o = 5$  kW and  $P_o = 10$  kW is given. In consonance to the results given in Fig. 17, the achieved efficiency is in good agreement with the calculated results. The measured input current distortions are, however, considerably larger than the calculated ones. The derived input current qualities only include the input current distortions caused by the turn-off delay of the MOSFETs and characterize only the minimum possible  $\text{THD}_I$ . Additional effects such as cusp distortion, the DCM operation of the rectifier or not perfectly calibrated current sensors yield increased input current distortions. The input current quality of the calculated Pareto curves are, therefore, the maximum achievable input current quality and constructed hardware may show higher  $\text{THD}_I$  values.

## VII. EXPERIMENTAL RESULTS

The calculation results are verified using a 10-kW rectifier system operating with a switching frequency of 1 MHz (see Fig. 19). The water-cooled prototype shows the dimensions 195 mm  $\times$  110 mm  $\times$  33 mm which yields a remarkable power density of 14.1 kW/L. A modern high-speed FPGA is used for the implementation of the current controller [19]. The rectifier system employs the CoolMOS device IPP60R099CP with a chip area of  $A_{\text{Chip}} = 30$  mm<sup>2</sup> which, according to Fig. 18, shows an optimal chip area. The measured input current taken from the prototype system operated with the proposed feedforward control signal is given in Fig. 20 where the measured efficiency is also depicted. The measurements have been performed using the oscilloscope LeCroy Waverunner LT264M in combination with the Tektronix current clamp A6302. The three-phase power analyzer DEWE-2600 from Dewetron has been used for measuring the THD value of the input currents. Compared to the calculation results given in Fig. 16(b), the constructed system shows a reduced efficiency. The reason for this is a PCB-layout error in the power circuit leading to unfavorable (additional) parasitic capacitances. These additional parasitic capacitances result in considerably increased switching losses which ultimately leads to the reduced efficiency. The additional switching losses can

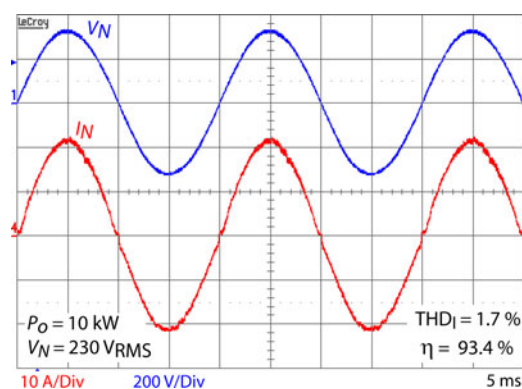


Fig. 20. Measured input current waveform taken from the constructed 10-kW rectifier system operated with the proposed feedforward signal at  $f_s = 1$  MHz ( $f_N = 50$  Hz,  $V_o = 800$  V); CH1 (blue):  $V_{N1}$ , 200 V/Div, CH2 (red):  $I_{N1}$ , 5 A/Div, time base: 1 ms.

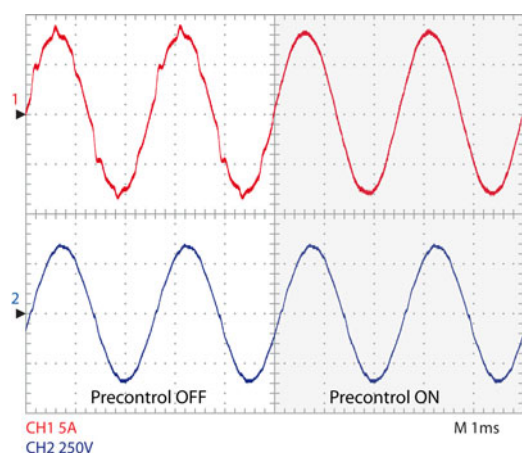


Fig. 21. Measurement of the input current with and without feedforward compensation of the turn-off delay. Measurement is taken from a system with  $f_s = 250$  kHz ( $V_N = 230$  V,  $f_N = 400$  Hz,  $V_o = 800$  V,  $P_o = 4.7$  kW); CH1 (red):  $I_{N1}$ , 5 A/Div, CH2 (blue):  $V_{N1}$ , 250 V/Div, time base: 1 ms.

well be determined by performing a switching loss measurement at the constructed hardware prototype (see [23]) and by comparing the measured loss energies with the results given in Fig. 13. In order to benchmark different semiconductor families, however, the results of the switching loss measurements given in Fig. 13, where all measurements are taken on the same test setup, are used in Section V. The efficiencies of the constructed rectifier system VR1000 shown in Figs. 17 and 18(a) are corrected by the additional switching loss energies caused by the error on the PCB-layout in order to be able to compare the calculation results with the constructed hardware. A redesign of the PCB-layout of the power circuit would result in the illustrated efficiencies.

The rectifier prototype is operated using the feedforward compensation signal as in practice. An operation without this compensation signal would yield heavily distorted input currents at the zero crossings.

In order to verify the effectiveness of the proposed precontrol signal, a 10-kW rectifier prototype with a switching frequency of 250 kHz is used instead of the rectifier system with  $f_s = 1$  MHz. The measurement results of the rectifier system operating at  $f_N = 400$  Hz and  $P_o = 4.7$  kW, with and without the feedforward signal, are given in Fig. 21. Whereas the system without the precontrol shows significant input current distortions at the zero crossings of the measured phase, and at the zero-crossings of the two other phases (every  $60^\circ$ ), input current quality is improved considerably if the precontrol is enabled. A  $\text{THD}_I$  of only 3.4% is measured without the feedforward signal and a  $\text{THD}_I$  of 1% is achieved if the proposed precontrol signal is used. The measurement clearly illustrates that the turn-off delay yields significant input current distortions even at a “moderate” switching frequency of 250 kHz.

### VIII. CONCLUSION

Because of the parasitic output capacitance  $C_{oss}$  of the MOSFET, the duty cycles generated from the controller are enlarged in relation to the input current. This yields substantial input current distortions. This effect is even more distinct if SJ devices are used instead of classical HV-MOSFETs. However, SJ devices offer a considerably reduced on-state resistance that results in reduced conduction losses. Due to the smaller chip area required to realize a specific  $R_{Dson}$ , SJ devices also show smaller switching losses. Measuring the corresponding switching loss energies is a good and easy way to determine switching losses. In order to get accurate results, the switching losses have to be performed at the constructed hardware as parasitic capacitances and inductances of the PCB-layout considerably influence switching losses. The relationship between efficiency and input current quality has been illustrated in a Pareto curve in the  $\eta$ - $\text{THD}_I$  space. Indeed, SJ devices show higher input current distortions but an implementation using HV-MOSFETs results in a considerably reduced efficiency compared to a implementation using SJ devices. It has been shown that the input current distortions can be reduced significantly if a proper precontrol signal is applied. Hence, SJ devices are particularly suited for this type of rectifier if the proposed precontrol signal is applied.

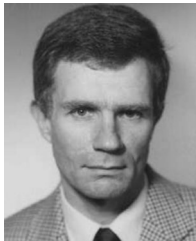
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