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G. Gong
D. Hassler
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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Guanghai Gong, Dominik Hassler, and Johann W. Kolar, *Fellow, IEEE*

***Abstract*—AC test power sources are essential for testing electric equipment that is ac-mains connected. Typically, linear power amplifiers (LPAs) are mainly employed as ac test sources because of their high fidelity and excellent dynamic behavior. However, these LPAs have very high losses in their output stages, which make the systems bulky and expensive due to the large heatsinks that are required. In recent years, two approaches have attracted popular interest to improve the efficiency of ac power sources. These are hybrid operation, i.e., combination of linear and switch mode, and multilevel switch-mode inverters. In this paper, three types of multilevel power amplifiers, based on hybrid or switching technology, are presented, namely: hybrid multicell amplifier (H-MCA), amplitude-modulated (AM) + pulsewidth-modulated (PWM) MCA (AP-MCA), and PWM MCA (P-MCA). For each of these topologies, the operating principle and control scheme are introduced. Finally, a 1-kVA laboratory prototype, which can realize all the three topologies, is built, and the measured performance based on this universal prototype are compared.**

***Index Terms*—Linear power amplifier (LPA), multicell inverter.**

I. Introduction

AC TEST power sources are essential for testing electric equipment that is connected to the ac mains. These ac test sources are required to have low output impedance, clean output voltage, and highly dynamic behavior so that they are able to simulate different mains conditions in order to realize different tests on the electric equipment.

Presently, linear power amplifiers (LPAs) are mainly employed in ac test sources because of their high fidelity and excellent dynamic behavior. However, these LPAs have very high losses in their output stages, which make the systems bulky and expensive due to the large heatsinks that are required. In recent years, switch-mode power amplifiers, mainly class-D and class-E amplifiers, have replaced LPAs in various applications where high fidelity is not required. The main reason for their use is that they have a much higher efficiency, which results in the realization of a compact and low-cost design. However, switch-mode power amplifiers produce additional EMI and a suitable low-pass filter is necessary between amplifier and load. This results in two disadvantages: first, the system bandwidth is limited by the low-pass filter, and second, the output impedance of the amplifier is significantly increased at the natural frequency of the low-pass filter.

Therefore, there is growing research interest in realizing high efficiency and high-bandwidth ac power sources by combining LPA and switch-mode converters that result in the reduction of the system losses while keeping the high dynamic performance of the LPAs.

Since the power losses of LPA are terminated by the voltage drop across the power transistors and the current flowing through the power transistors, there are only two approaches to lower the power losses, i.e., decreasing the voltage drop across the power transistors or reducing the transistor currents. All the hybrid topologies are based on these two considerations. Yundt [1] classifies the composite amplifiers into four groups: series voltage, parallel voltage output, parallel current, and series current output. However, this classification does not include another hybrid topology that employs a tracking power supply (TPS) to adjust the supply voltages according to the required linear amplifier output voltage. This topology can significantly reduce the voltage drop across the linear amplifier power transistors, which results in a reduction of the amplifier power losses. Furthermore, voltage sources are typically required for ac-power-source applications as well as other industrial applications like stage acoustic amplifiers, etc.

Based on the aforementioned considerations, the voltage-source-hybrid power amplifiers are classified into three types, as shown in Fig. 1.

A. Type I: Envelope Configuration

In contrast to the conventional class-AB amplifiers, this type of hybrid amplifier replaces the constant dc supplies by switch-mode power supplies that are able to vary their output voltages according to the instantaneous LPA output voltages. Therefore, LPA power losses are dramatically reduced because the voltage drop across LPA power transistors is kept to a minimum voltage level. However, the disadvantage of this configuration is that the LPA should deliver the full output power and sustain the full output-voltage stress. This makes it difficult to design the LPA for high-voltage applications [1]–[8].

B. Type II: Series Configuration

In this type of topology, a main ac voltage source that delivers the bulk of the output voltage is connected in series with an LPA that only outputs the small amount of correc-

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G. Gong was with Power Electronics Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8006 Zurich, Switzerland. He is now with the Traction Converters Department, ABB Switzerland, Turgi 5300, Switzerland (e-mail: guanghai.gong@ch.abb.com).

D. Hassler and J. W. Kolar are with the Power Electronics Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8006 Zurich, Switzerland (e-mail: hassler@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

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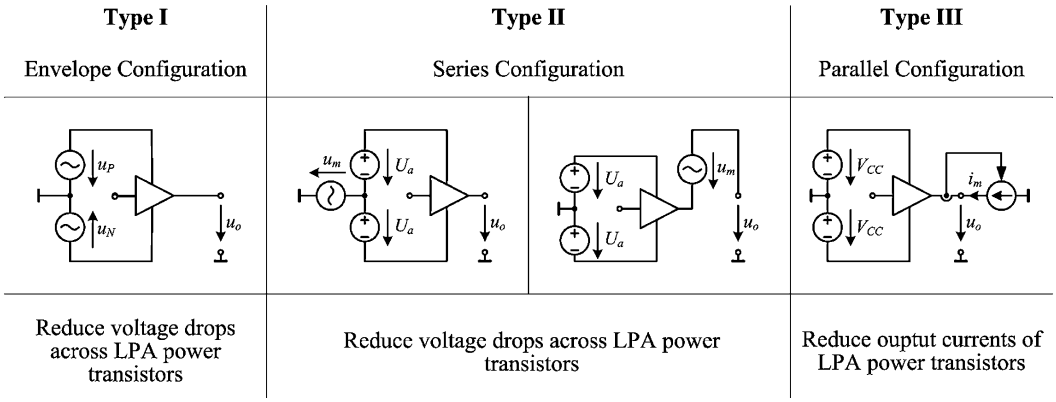

Fig. 1. Classification of hybrid power amplifiers.

tion voltage that supplements the voltage difference between output voltage u_o and main voltage u_m. Therefore, LPAs with low voltage supplies can be employed in high-voltage applications, which significantly reduces the voltage drop across LPA power transistors. There are two possibilities to connect these two parts. One possibility is to connect the main ac voltage source to the ground of LPA dc power supplies [9], [10], and the other way is to connect it with the LPA output voltage in series [1], [11].

C. Type III: Parallel Configuration

AN LPA and a current controlled switch-mode amplifier are connected in parallel at the output. There the switch-mode amplifier contributes the main load current and the linear amplifier generates the difference current. With this topology, a relatively small current is flowing through the LPA so that the losses can be significantly reduced and the output impedance is defined by the LPA stage. However, a high-voltage LPA is still required for a mains simulation application and switching noise can appear in the output voltage due to the increased output impedance of LPA at high frequencies. This type of topology is especially preferred for audio amplifier applications [12]–[17].

Besides, the approaches of the hybrid configuration to improve the efficiency of ac test power supplies, multilevel inverters employing pure switching-mode operation have become increasingly popular in ac-power-source applications. The main advantages of multilevel converters are voltage stress reduction of the power devices, low electromagnetic interference (EMI), low switching losses, and a high-quality output waveform. These make multilevel inverters particularly welcome for such industrial applications like medium-voltage drivers, static var compensator (SVC), STATCOMs, and grid interfaces for renewable energy sources such as solar photovoltaic. There are mainly three types of topologies that have been proposed for multilevel inverters: diode-clamped, flying-capacitor, and cascaded multilevel inverters [18], [19].

In this paper, three types of multilevel power amplifiers based on hybrid (linear and switching) or switching technology are compared, namely:

1) Hybrid Multicell Amplifier (H-MCA);
2) AM + PWM MCA (AP-MCA);
3) PWM MCA (P-MCA).

Here, the symmetric cascaded multicell inverter is implemented for these three amplifiers. The main reasons are as follows.

1) The isolation stages are required for ac-power-sources applications.
2) The symmetric topology gives great freedom to expand or shrink the output-voltage range with minimum effort.
3) The component dimensioning is identical for each cell unit.

For each of these topologies, the operating principle and control scheme are introduced. Finally, a 1-kVA laboratory prototype is built that is able to implement all three topologies, and the measured performances from this universal prototype are compared.

II. Hybrid MCA

H-MCA is shown in Fig. 2(a), and consists of: 1) a high slew-rate LPA; 2) a multicell inverter, which is connected in series with the LPA to generate the output voltage; and 3) a bidirectional, multioutput, isolated dc–dc converter that provides the dc voltages for cell units and LPA and allows bidirectional energy flow in the case of nonresistive loads. A similar topology, "quasi-linear amplifier," has been already proposed in [11]. There, the "quasi-linear amplifier" consists of low-switching-frequency inverters connected in series with an LPA to generate gradient coil currents with fast ramp time for MRI systems. However, this "quasi-linear amplifier" acts as a current source, while the topology in this paper operates as a voltage source that has very low output impedance and includes an isolation power stage.

The representative waveforms of a ten-cell cascaded power amplifier are shown in Fig. 2(b), where the multicell inverter generates the stepped high-voltage u_{mo} according to the reference output voltage u_o^* and the switching frequency of the cells is low. Furthermore, the output voltage of the LPA u_{la} is regulated to compensate for the small voltage difference between u_{mo} and u_o. Therefore, a low-voltage LPA can be employed. The gray area between $u_{mo} - U_a$ and $u_{mo} + U_a$ is the voltage range that can be achieved by the multicell cascaded power amplifier for the reference voltage u_o^*.

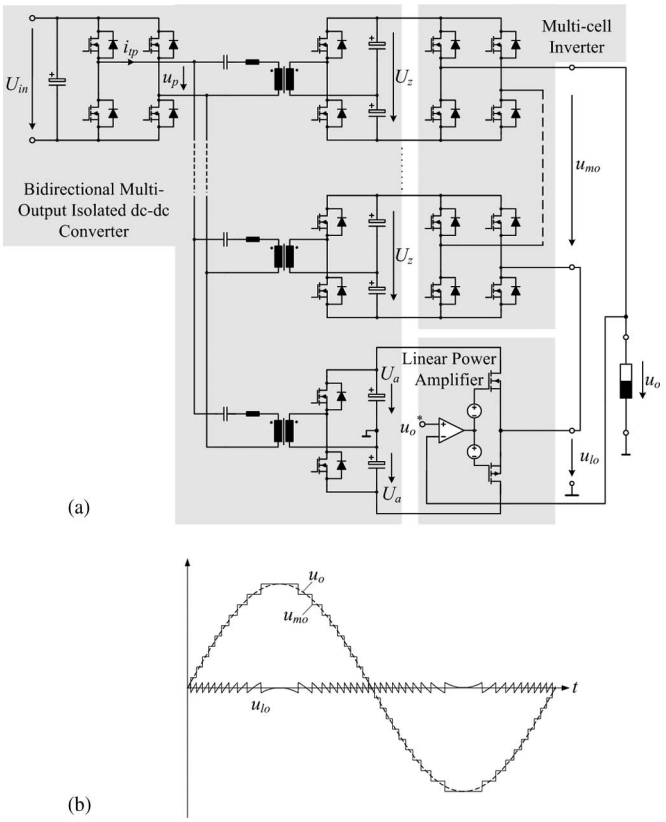

Fig. 2. Topology of an (a) isolated multicell cascaded power amplifier and representative waveforms of the output voltage u_o, multicell output voltage u_{mo}, and linear power amplifier output voltage u_{lo} of a (b) ten-cell cascaded power amplifier.

A. Operating Principle

The control scheme of a simplified two-cell cascaded power amplifier is shown in Fig. 3. Here, two H-bridges are connected in series with the LPA to form the output voltage. The H-bridge units are controlled in an open-loop manner and each H-bridge cell can output three possible voltages, U_z, 0 V, and $-U_z$, where U_z is the dc supply voltage of the cell units. The LPA is operated in a closed loop with a high bandwidth so that it can compensate for the voltage difference between output voltage u_o and multicell voltage u_{mo}.

The control signals of the H-bridge units are directly generated by comparing the reference output voltage u_o^* and step voltages $-3/2U_z$, $-1/2U_z$, $+1/2U_z$, and $+3/2U_z$. For instance, the output voltage of unit 1 is 0 V, i.e., T_3 and T_4 are ON, when u_o^* is between $-1/2U_z$ and $+1/2U_z$. If u_o^* increases and reaches $+1/2U_z$, T_3 is turned off and T_1 is turned on, thus unit 1 outputs $+U_z$. Alternatively, unit 1 will produce an output voltage $-U_z$ when u_o^* decreases and reaches $-1/2U_z$. The total multicell voltage u_{mo} is dependent on the reference output voltage u_o^*, as is demonstrated in Fig. 4. Furthermore, this topology can be easily expanded to an n-cell cascaded power amplifier with very low effort.

In Fig. 3, the dc voltage of the LPA U_a is required to be higher than $1/2U_z$ in order to have sufficient voltage regulation margin. The system just uses a single voltage loop control and the control signal of the LPA is formed by summing the feed-

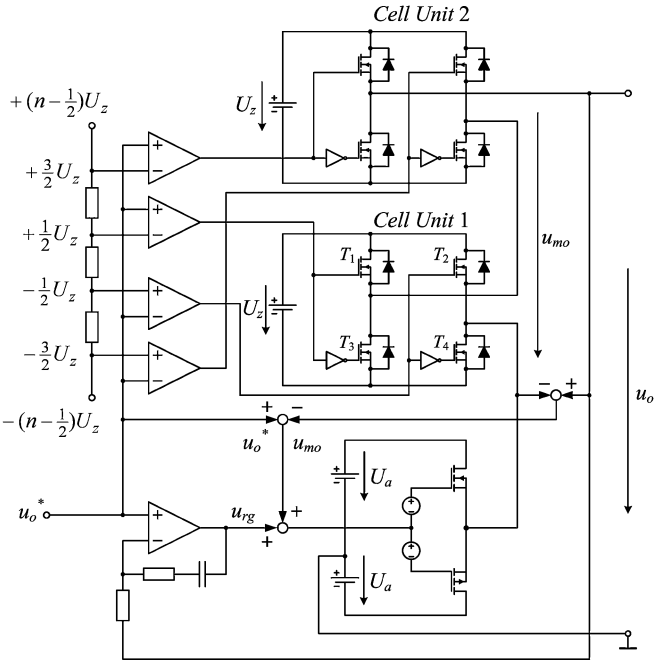

Fig. 3. Control scheme of two-cell cascaded power amplifier.

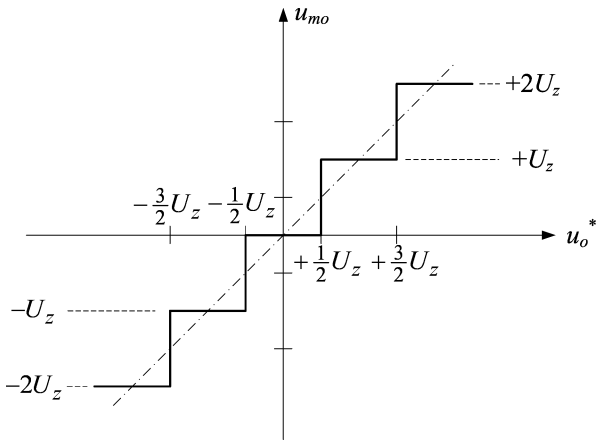

Fig. 4. Multicell voltage u_{mo} in dependency on the reference output voltage u_o^*.

forward voltage u_o^*–u_{mo} and the output of the voltage regulator u_{rg}.

B. Control Design

For the system control design, we at first use ideal voltage sources to substitute the dc–dc isolated converter since the output impedance of the dc–dc converter is negligible considering the system control design. The simplified H-MCA circuit scheme is shown in Fig. 5, where an additional *dv/dt* filter with the parameters of $L_F = 6.8$ μH, $L_d = 66$ μH, $R_d = 6$ Ω, and $C_F = 220$ nF is inserted at the output of the H-bridge units. This is because the LPA has a limited bandwidth, and this filter is employed to limit the slope of the step voltages to 15 V/μs for $U_z = 40$ V so that the LPA is able to compensate the small voltage difference between u_{mo} and u_o. In Fig. 5, we see that

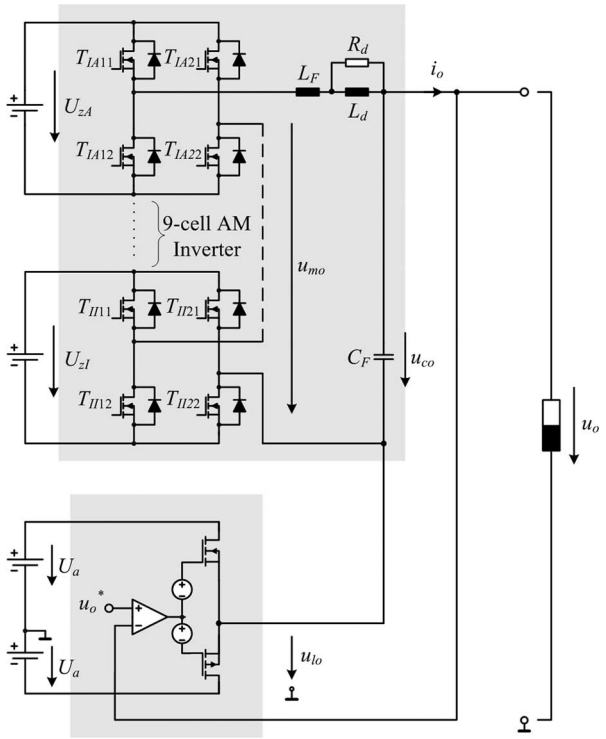

Fig. 5. Simplified H-MCA scheme by replacing the dc–dc isolated converter with ideal voltage sources.

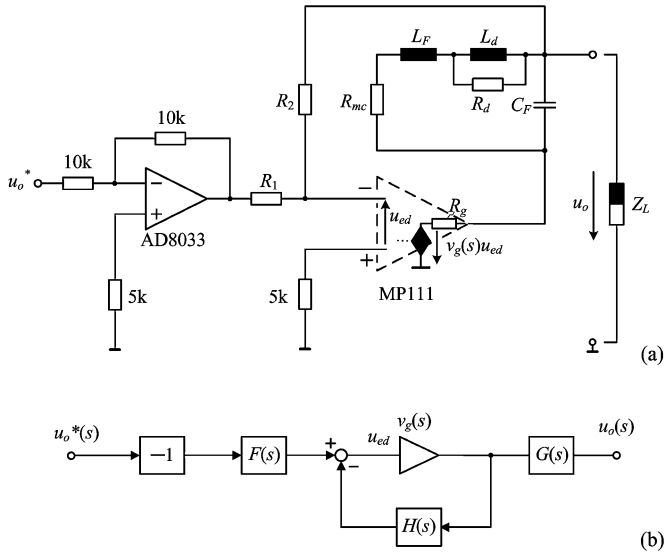

Fig. 6. (a) Circuit scheme and (b) control block scheme for H-MCA output voltage control design.

the multicell inverter is in the feedback loop, and therefore, the output impedance of the complete multicell inverter including the *dv*/*dt* filter has to be considered for the control design.

The circuit scheme for H-MCA output voltage control design is shown in Fig. 6 (a), where the multicell inverter is replaced by the output impedance network Z_{mo} and MP 111D is replaced by a voltage-controlled voltage source with its output resistance $R_g = 3\,\Omega$ at dc [20]. As described in [21], the dominant factors affecting the open-loop transfer function are the input stage transconductance g_i and the so-called dominant capacitor $C_{\rm dom}$. The value of g_i is determined by the input differential stage design. The capacitor $C_{\rm dom}$ is the negative-feedback capacitor of the voltage-amplifying stage. For MP 111D, $C_{\rm dom}$ can be varied by external capacitors. Therefore, the open-loop transfer function can be defined as

$$v_g(s) = \frac{g_i}{C_{\rm dom}s}\frac{1}{\tau_1 s+1}\frac{1}{\tau_2 s+1} \tag{1}$$

where the τ_1 and τ_2 represent the high-frequency poles caused by the parasitic circuit parameters of the output stage. By fitting (1) to the measured Bode plots of the APEX MP111D open-loop transfer function $v_g(s)$, the parameters can be determined as $g_i = 3.9\,\mathrm{mA/V}$, and $\tau_1 = \tau_2 = 0.46\,\mu\mathrm{s}$.

The front-end inverter is to provide the inverting function and possible scaling function if needed for the reference voltage u_o^*. Since the AD8033 has a high bandwidth of 80 MHz, this inverter is considered to be ideal. For the circuit diagram shown in Fig. 6(a), we can derive the control block diagram, as depicted in Fig. 6(b). In this diagram, the feed-forward transfer function $F(s)$ is defined as

$$F(s) = -\frac{R_2 + Z_{mo}(s) + R_g}{R_1 + R_2 + Z_{mo}(s) + R_g}. \tag{2}$$

and the feedback transfer function $H(s)$ is

$$H(s) = \frac{R_1}{R_1 + R_2 + Z_{mo}(s) + R_g}. \tag{3}$$

The MP 111D output and system output are coupled via a relatively low-impedance network Z_{mo} compared to R_2, thus there is a small voltage difference considering the small-signal values. Therefore, a correction function $G(s)$ is given as

$$G(s) = \frac{R_1 + R_2}{R_1 + R_2 + Z_{mo}(s) + R_g}. \tag{4}$$

Finally, the closed-loop input-to-output transfer function $G_{io,cls}$ is calculated as

$$G_{io,cls}(s) = \frac{u_o(s)}{u_o^*(s)} = -F(s)\,G(s)\,\frac{v_g(s)}{1 + v_g(s)\,H(s)}. \tag{5}$$

The closed-loop output impedance $Z_o(s)$ is

$$Z_o(s) = \frac{Z_{mo}(s) + R_g}{1 + v_g(s)\,H(s)}. \tag{6}$$

When the load Z_L is connected, the closed-loop transfer function $G_{io,cls}$ should be modified because of the system output impedance. Therefore, $G_{io,cls}$ is rewritten as

$$G_{io,cls}(s) = -F(s)\,G(s)\,\frac{v_g(s)}{1 + v_g(s)\,H(s)}\,\frac{Z_L(s)}{Z_L(s) + Z_o(s)}. \tag{7}$$

The control design for H-MCA is quite simple because we only have few parameters to vary, which are as follows.

1) The external capacitor $C_{\rm dom}$
2) Feedback factor determined by R_1 and R_2.

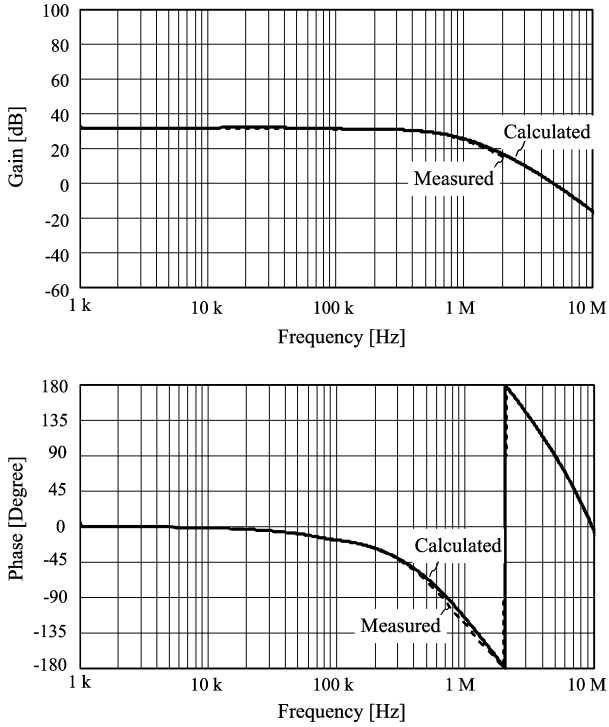

Fig. 7. Comparison of measured and calculated Bode plots of system closed-loop small-signal input-to-output transfer function. Operation parameters: $U_o = 120\,\mathrm{V}$, $C_{\mathrm{dom}} = 34\,\mathrm{pF}$, $R_L = 35\,\Omega$, and $U_a = 30\,\mathrm{V}$.

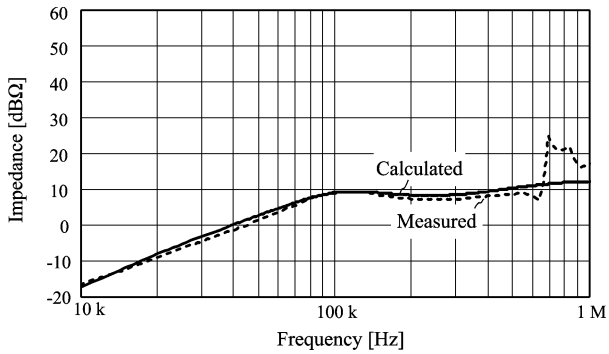

Fig. 8. Comparison of measured and calculated Bode plots of system output impedance. Operation parameters: $U_o = 120\,\mathrm{V}$, $C_{\mathrm{dom}} = 34\,\mathrm{pF}$, $R_L = 35\,\Omega$, and $U_a = 30\,\mathrm{V}$.

For a practical tradeoff between the system stability and dynamic behavior, $C_{\mathrm{dom}} = 33\,\mathrm{pF}$, $R_1 = 5\,\mathrm{k}\Omega$, and $R_2 = 200\,\mathrm{k}\Omega$ are selected for the control design. The designed control system achieves a crossover frequency of 460 kHz and phase margin of 68°.

The measured and calculated Bode plots of system closed-loop input-to-output transfer function are compared in Fig. 7. These two curves are perfectly matching up to 2 MHz. From the measured data, it shows that the closed-loop control system has a bandwidth of 570 kHz (at 32 dB – 3 dB = 29 dB).

Fig. 8 compares the calculated and measured system small-signal output impedance. These two Bode plots match quite well.

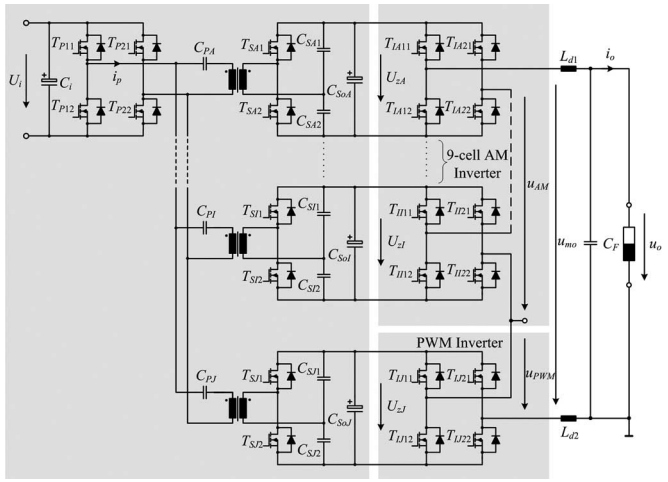

Fig. 9. AP-MCA circuit diagram.

III. AM + PWM Multicell Amplifier

In Section II, the H-MCA shows its wide bandwidth performance, high output-voltage quality, and low output impedance; however, the system efficiency is impaired by the LPA that contributes around 60% of the total system losses. In order to achieve higher system efficiency, we use a PWM inverter cell with a 500 kHz switching frequency to substitute the LPA unit in H-MCA. Consequently, the *dv/dt* limit filter has to be replaced by another filter design that aims to sufficiently eliminate the switching ripple. Afterward, this system turns out to be a pure switch-mode amplifier with mixed AM and PWM control, thereby the system is called AM + PWM MCA (AP-MCA). There is another research approach for this type of switch-mode amplifier, where only one cell is supplied by a dc power supply and the dc voltages of the other cells are provided by flying capacitors [22]. By properly controlling the charge and discharge currents through the capacitors, it is possible to keep the voltages across the flying capacitors constant.

A. Operation Principle

The circuit diagram of AP-MCA is shown in Fig. 9, where the AM inverters as well as the dc-link power supplies are the same as H-MCA. However, the LPA together with its isolation dc supply stage are replaced by a PWM inverter and its dc power supply. The AM inverter and PWM inverter are connected in series for generating the total inverter output voltage u_{mo}. As with any other switch-mode amplifier, an output filter has to be employed to eliminate the switching ripples.

The modulation of AM inverter is completely the same as H-MCA (see Fig. 4) and the principle of the system control is also the same. Fig. 10 demonstrates the key waveforms of AP-MCA, where the AM inverter produces the large-scale voltage u_{AM}, and the PWM inverter is regulated to generate the small compensation signal. The total multicell inverter voltage u_{mo} is formed by the summation of u_{AM} and u_{PWM}. The sinusoidal output voltage u_o is achieved by the low-pass filtering of u_{mo}.

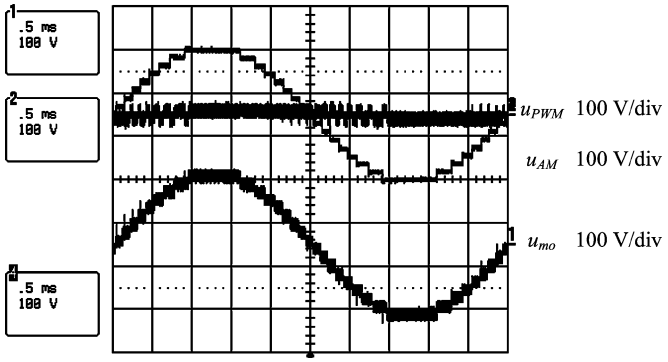

Fig. 10. Measured key waveforms of AP-MCA.

B. Control Design

1) Overview of System Control: The main difference with the AP-MCA is that digital control is employed for the output voltage control, where it is realized by the analog control in H-MCA. Here, the output voltage u_o and its reference signal u_o^* are measured through the analog interface circuits and are converted to digital signals by the ADCs integrated in the DSP. The DSP then calculates the output of digital proportional–integral (PI) controller and converts it to a count number, which is to be sent to field-programmable gate array (FPGA). The 500-kHz PWM signals are generated by FPGA by comparing the received count number to the digital internal 500 kHz triangular carrier.

The multicell inverter uses the same amplitude modulation, as in H-MCA shown in Fig. 4. Also, the implementation in the hardware for determining the switching signals of the multicell inverter is same as in H-MCA, where we use analog fast comparators to directly compare the reference signal with threshold voltage levels set by the DACs.

2) System Modeling: The simplified AP-MCA control system scheme is shown in Fig. 11(a), where the digital control part is inside the dashed frame and outside the frame are the analog parts including the power circuit and measurement circuits. The PWM inverter is considered as a controlled voltage dU_z that is proportional to the duty cycle ratio d [23], and the AM multicell inverter is regarded as a disturbance voltage sources $u_{\rm AM}$ that is connected in series with dU_z.

The output filter is calculated to ensure the switching ripple in the output voltage is smaller than 0.5%. Here, R_{mc} is the total on-resistance of the inverter MOSFETs in the output conducting loop, and there are always 20 MOSFETs conducting at the same time. Therefore, this is calculated as

$$R_{mc} = 20 \times R_{\mathrm{ON},irf} = 0.2\,\Omega \tag{8}$$

.

The switching losses of the PWM inverter can be derived as

$$P_{sw} = 2 f_s E_{\rm sloss} \tag{9}$$

where the switching energy losses are from [24]. Since the switching voltage is constant $U_{sw} = U_z$, the switching losses is approximated as

$$P_{sw} = k_{sw} I_{sw}. \tag{10}$$

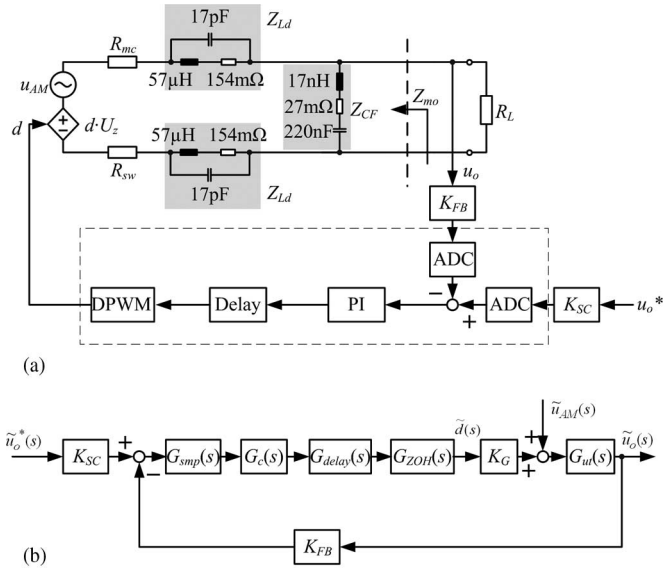

Fig. 11. (a) Simplified AP-MCA system control scheme and the according (b) control system block diagram.

On the other hand, the switching losses can be represented by inserting a virtual resistor R_{sw} in the circuit, as shown in Fig. 11(a). Consequently, the switching losses can be also expressed as

$$P_{sw} = R_{sw} I_{sw}^2. \tag{11}$$

By differentiating (11) with I_{sw}, we have

$$\frac{dP_{sw}}{dI_{sw}} = k_{sw} = 2 R_{sw} I_{sw}. \tag{12}$$

Therefore, the virtual resistor R_{sw} is derived as

$$R_{sw} = \frac{k_{sw}}{2 I_{sw}}. \tag{13}$$

Since digital control is employed for AP-MCA, we have to treat this system as a sampled-data control system. There are two approaches that may be used in analyzing a sampled-data control system: the direct (DIR) or the digitization (DIG) control-design techniques. The DIR design is based on z-domain. Its main advantage is that less constraints on the controller parameters are required to meet the system specifications. Furthermore, the switch-mode converter is inherent a sampled-data system. The disadvantage of this method is that there is a limited amount of experience for designing a suitable digital controller in z-domain. Whereas, the DIG design uses s-domain transfer functions to express the digital units, therefore we can utilize the well-established s-domain knowledge to design the appropriate controllers. Afterward, the s-domain controllers are transformed to z-domain by use of the Tustin algorithm for the digital implementation in DSP [25].

For designing the controller of AP-MCA, the DIG method is used. The functional block diagram of AP-MCA control system, which is a so-called pseudocontinuous-time (PCT) system, is demonstrated in Fig. 11(b). In the following content, each control block unit will be described.

First, the control block units in continuous-time domain are introduced. Based on Fig. 11(a), the small-signal transfer function from $\tilde{u}_{\rm PWM}(s)$ or $\tilde{u}_{\rm AM}(s)$ to the output voltage $\tilde{u}_o(s)$ is

$$G_{ut}(s) = \frac{R_L \parallel Z_{CF}(s)}{R_{mc} + R_{sw} + 2Z_{Ld}(s) + R_L \parallel Z_{CF}(s)}. \quad (14)$$

The gain K_G is equal to the dc-link supply voltage of the PWM inverter, i.e.,

$$K_G = U_z. \quad (15)$$

The output-voltage feedback factor $K_{FB} = 0.01$ and the scaling factor of the reference voltage $K_{SC} = 0.4$.

The following control block units to be introduced are in discrete-time domain, i.e., implemented in DSP+FPGA. As described before that the measured signals of u_o and u_o^* are sampled by the ADC incorporated in DSP, and the PCT approximation of the sampler is given as [25]

$$G_{\rm smp}(s) = \frac{1}{T_{\rm smp}} \quad (16)$$

where $T_{\rm smp}$ is the sampling time. Since FPGA receives the discrete PI control value that is a normalized count number in the hardware implementation and updates the PWM signal at the sampling frequency, this digital PWM (DPWM) effectively embeds a zero-order holder (ZOH) that converts the discrete signal to the analog signal. The s-domain transfer function of ZOH is [25]

$$G_{\rm ZOH}(s) = \frac{1 - e^{-T_{\rm smp}s}}{s}. \quad (17)$$

We can combine $G_{\rm smp}(s)$ and $G_{\rm ZOH}(s)$ together to form the transfer function of the sampler and holder,

$$G_{\rm SZOH}(s) = \frac{1 - e^{-T_{\rm smp}s}}{T_{\rm smp}s}. \quad (18)$$

The system delay time is defined as the time interval between the moment that data is sampled and the updating action of duty cycle. During the system operation, this interval is actually changing. Here, the maximum delay time, $T_{\rm smp}$, is assumed for this system,

$$G_{\rm delay}(s) = e^{-T_{\rm smp}s}. \quad (19)$$

If the root locus method is utilized for the compensation design, the Padé approximation has to be applied to $G_{\rm SZOH}(s)$ and $G_{\rm delay}(s)$. The second-order Padé approximation of $G_{\rm SZOH}(s)$ is

$$G_{\rm SZOH,PA}(s) = \frac{12}{12 + 6T_{\rm smp}s - T_{\rm smp}^2 s^2}. \quad (20)$$

This approximation is good for the frequency range up to $1/3T_{\rm smp}$. However, the frequency-response compensation method based on Bode plots is employed for the controller design in this system. In this case, the Padé approximations for $G_{\rm SZOH}(s)$ and $G_{\rm delay}(s)$ are not necessary.

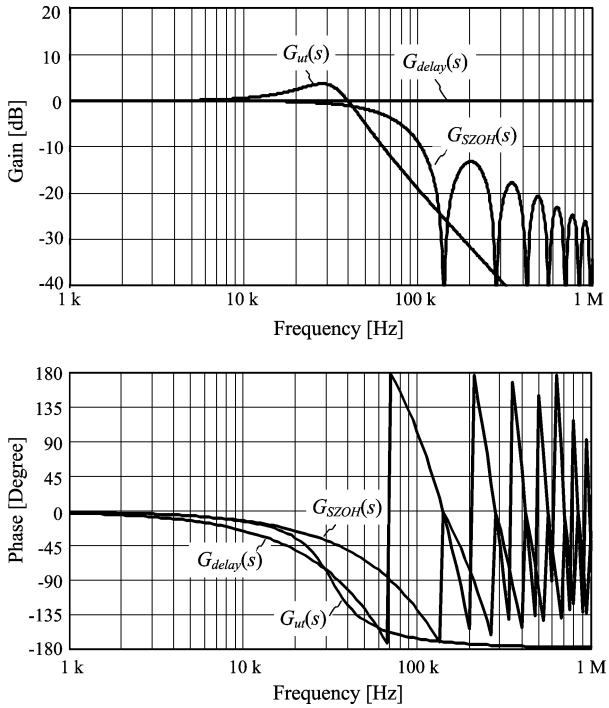

Fig. 12. Bode plots comparison of the three transfer functions in the control plant. Operation parameters: $R_L = 35\,\Omega$, $T_{\rm smp} = 7\,\mu$s.

3) PI Controller Design: Based on the aforementioned modeling analysis, the open-loop plant transfer function is given by

$$G_{\rm plant}(s) = K_G G_{ut}(s)\, G_{\rm SZOH}(s)\, G_{\rm delay}(s). \quad (21)$$

Fig. 12 compares the Bode plots of $G_{ut}(s)$, $G_{\rm SZOH}(s)$, and $G_{\rm delay}(s)$, where $G_{\rm delay}(s)$ shows the largest impact to the system phase angle and its phase angle starts to decrease dramatically after 10 kHz. For PCT system control design, the bandwidth is typically limited to 1/20th of the sampling frequency [26]. In this circuit, $T_{\rm smp} = 7\,\mu$s; therefore, the typical achievable bandwidth is about 7 kHz. A simple PI controller is designed to compensate $K_{\rm FB}G_{\rm plant}(s)$ shown in Fig. 13. The transfer function of the PI controller is given as

$$G_c(s) = K_{\rm PI}\left(1 + \frac{1}{T_{\rm PI}s}\right) \quad (22)$$

where the calculated PI parameters are: $K_{\rm PI} = 0.45$ and $T_{\rm PI} = 3.2 \times 10^{-6}$ s. The open-loop transfer function of the compensated system is written as

$$G_{\rm open}(s) = K_{\rm FB}G_{\rm plant}(s)\, G_c(s). \quad (23)$$

Fig. 13 shows that the compensated system achieves a bandwidth of 4.5 kHz and a phase margin of 70° for nominal load.

4) System Transfer Functions: Obviously, the closed-loop input-to-output transfer function can be derived as

$$G_{\rm io,cls}(s) = K_{\rm SC}\frac{G_{\rm plant}(s)\, G_c(s)}{1 + G_{\rm open}(s)} \quad (24)$$

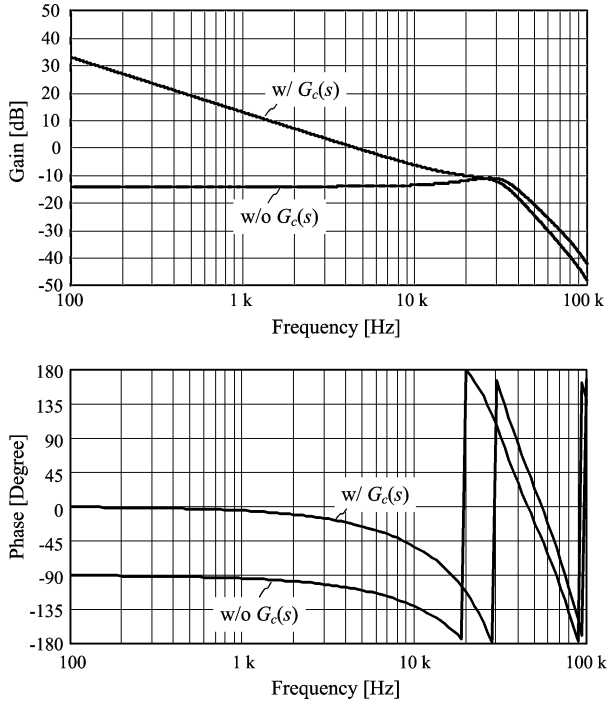

Fig. 13. System open-loop Bode plots with and without the controller $G_c(s)$.

and the closed-loop transfer function from the disturbance voltage $\tilde{u}_{\rm AM}(s)$ to $\tilde{u}_o(s)$ is

$$G_{do,\rm cls}(s) = \frac{u_{ut}(s)}{1 + G_{\rm open}(s)}. \tag{25}$$

According to Fig. 11, the output impedance without closed-loop control is

$$Z_{mo}(s) = (R_{mc} + R_{sw} + 2Z_{Ld}(s)) \parallel Z_{CF}(s). \tag{26}$$

Therefore, the closed-loop system output impedance can be derived as

$$Z_o(s) = \frac{Z_{mo}(s)}{1 + G_{\rm open}(s)}. \tag{27}$$

5) Verification: The small-signal frequency response of AP-MCA is measured from the laboratory prototype to verify the theoretical analysis. The calculated small-signal parameters and system operating parameters are listed in Table I.

Fig. 14 shows the calculated and measured Bode plots of the open-loop transfer function of AP-MCA, where these two plots match very well until 20 kHz, and the measured crossover frequency and phase margin are close to the calculated values. However, the measurement result shows a higher damping factor in the system. This is mainly because that the resistance of many connectors and PCB track impedance in the large output power loop are not counted during small-signal modeling for the sake of simplify.

Since the PI controller is designed for the nominal-load condition, as we know the worst operating point concerning the system stability for the buck-type derived converters is when no load is connected to the output. Therefore, we have to check the system stability for no-load condition; otherwise, the PI controller has to be modified. The measured Bode plots of $G_{\rm open}(s)$ for nominal-load and no-load conditions show that the system still fulfils the stability criteria for no-load condition.

TABLE I
SYSTEM PARAMETERS FOR SMALL-SIGNAL MODEL VERIFICATION

Name	Denotation	Value
Total on-resistance	R_{mc}	0.2 Ω
Switching energy losses	E_{sloss}	2.4 μJ
Switching frequency of PWM inverter	f_s	500 kHz
Virtual resistor representing switching losses	R_{sw}	0.1 Ω
Output voltage feedback factor	K_{FB}	0.01
Reference signal scaling factor	K_{SC}	0.4
Sampling time	T_{smp}	7 μs
DC-link voltage of PWM inverter	U_z	20 V
Output voltage	U_o	120 V
Nominal load resistor	R_L	35 Ω

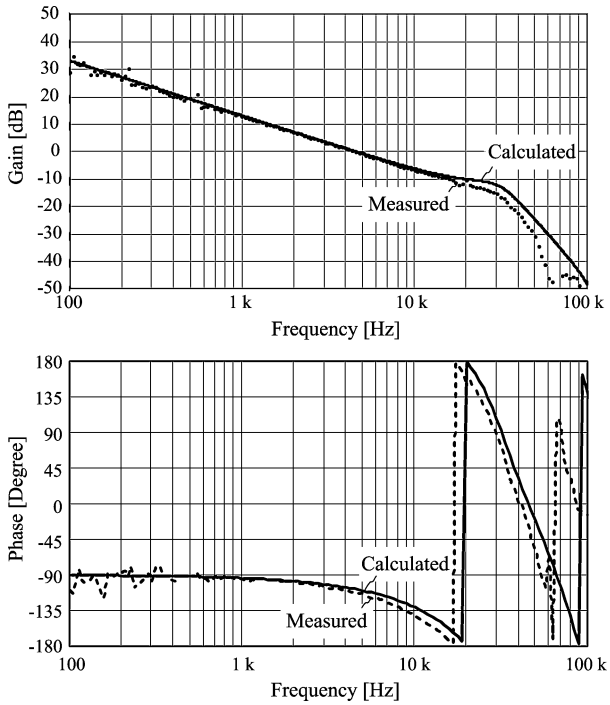

Fig. 14. Comparison of the calculated and measured Bode plots of the open-loop transfer function of AP-MCA. The controlled system has a crossover frequency of 4.5 kHz and phase margin of 70°.

The calculated and measured Bode plots of the closed-loop transfer function, as shown in Fig. 15, have good matching up to 10 kHz. The comparison of the calculated and measured Bode plots of the system output impedance are depicted in Fig. 16, where the curves are in line besides the calculated curve shows less damping factor.

IV. PWM MULTICELL AMPLIFIER

A. Operation Principle

The circuit diagram of P-MCA is shown in Fig. 17, which has exact the same power circuit as AP-MCA. However, in P-MCA all the inverters are operating in PWM mode. The switching

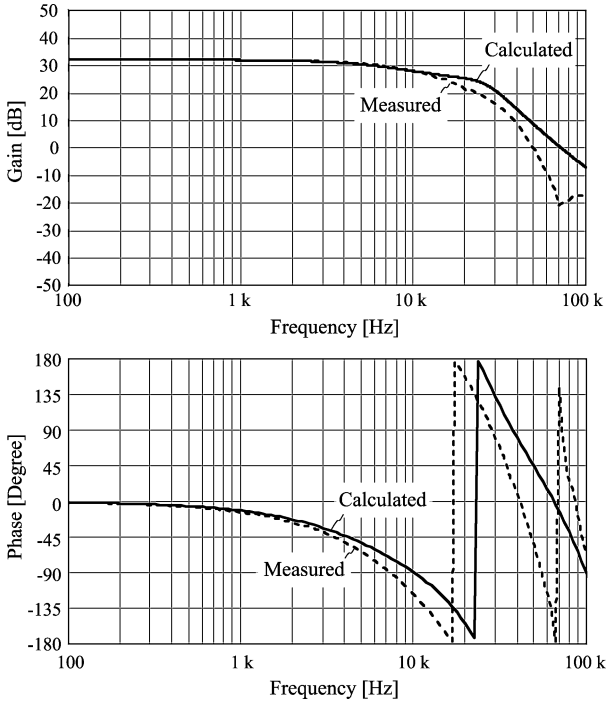

Fig. 15. Bode plots of AP-MCA closed-loop transfer function.

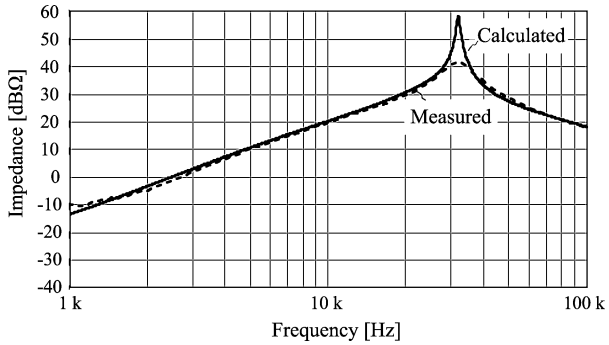

Fig. 16. Comparison of the calculated and measured Bode plots of AP-MCA output impedance $Z_o(s)$.

frequency of each cell is set to 50 kHz; therefore, the effective switching frequency of the ten-cell system is 500 kHz, which is same as the switching frequency of PWM inverter cell in AP-MCA system. This provides the fair condition to compare the system efficiency later.

Fig. 18 demonstrates the key waveforms of P-MCA. There the ten-cell series-connected inverter using sinusoidal PWM (SPWM) control produces the total output voltage u_{mo}, and the sinusoidal output voltage u_o is achieved after low-pass filtering of u_{mo}.

The phase shift between the output voltages of two adjacent inverter cells is demonstrated in Fig. 19. Since ten-cell inverter is employed in hardware and each inverter is switching at 50 kHz, the phase shift should be 2 μs and/or 36°.

B. Control Design

The only difference between AP-MCA and P-MCA is the modulation method. AP-MCA utilized a hybrid modulation that

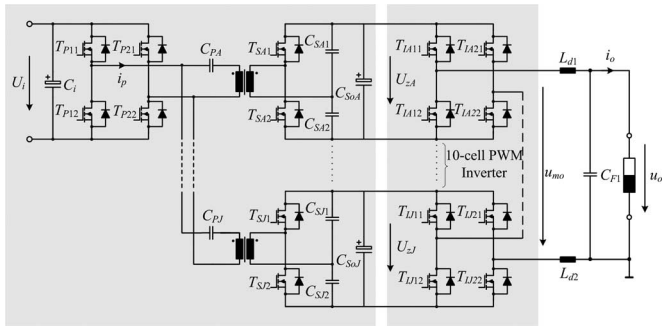

Fig. 17. P-MCA circuit diagram.

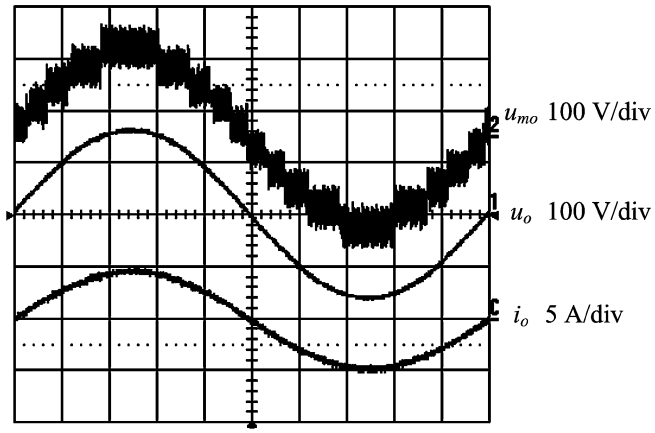

Fig. 18. Measured key waveforms of P-MCA.

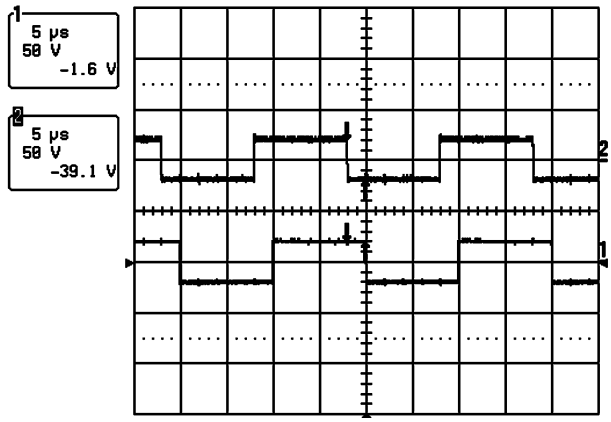

Fig. 19. Phase shift between the output voltages of two adjacent inverter cells, 36° (2 μs). Operation parameters: $U_{\rm in} = 200\,{\rm V}$, $f_{sm} = 50\,{\rm kHz}$, $U_{o,{\rm rms}} = 115\,{\rm V}$, and $f_o = 1\,{\rm kHz}$.

combines AM and PWM, while P-MCA only employs PWM modulation. The fast analog comparator arrays designed for AM modulation are not needed for P-MCA, and this makes P-MCA the only system, which is fully digitally controlled among H-MCA, AP-MCA, and P-MCA. A well-known phase-shifted scheme for generating the carrier signals are implemented that increases the system switching frequency by factor of ten for P-MCA.

The system small-signal modeling and control design are very similar to AP-MCA. Therefore, the control designing for

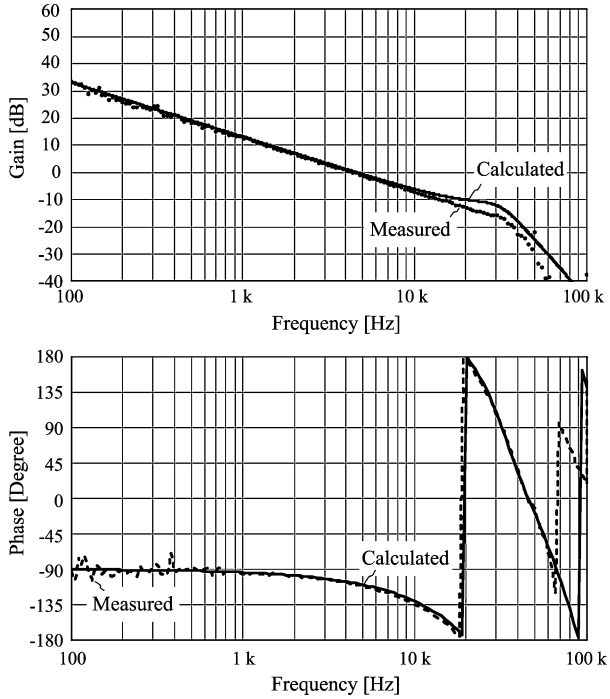

Fig. 20. Comparison of the calculated and measured Bode plots of the open-loop transfer function of P-MCA.

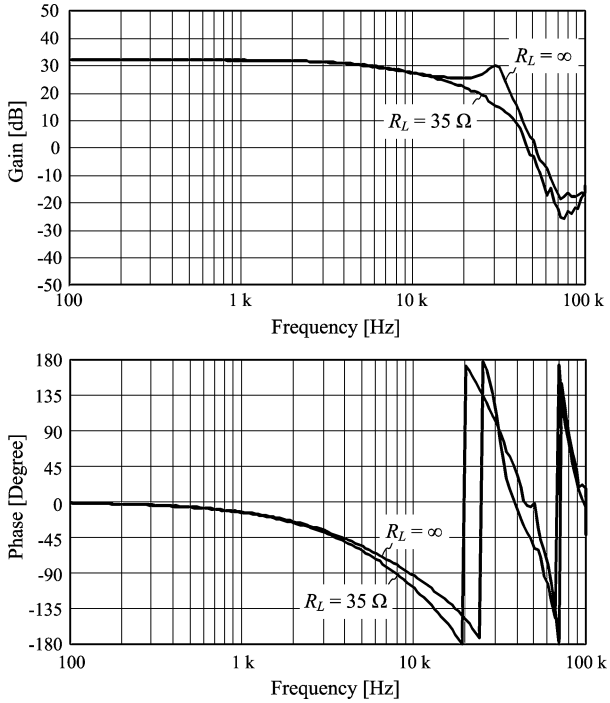

Fig. 21. Measured Bode plots of the closed-loop transfer function of P-MCA for the nominal-load and no-load conditions.

P-MCA will be not treated in detail. When designing the compensator for P-MCA, the functional block diagram of AP-MCA shown in Fig. 11(b) can be still used with few parameter modifications. These changes are as follows.

1) The disturbance voltage $\tilde{u}_{\rm AM}(s)$ is no longer presented;
2) Gain K_G is changed from U_z to $10U_z$ because all the ten cell inverter units are operating in PWM mode and this effectively increases the inverter dc-link voltage by a factor of ten.
3) The parameter $K_{\rm PI}$ of the controller is reduced to $0.1K_{\rm PI}$; therefore, the designed system crossover frequency can remain at 4.5 kHz.

After the compensation, the controlled P-MCA system has a crossover frequency of 4.5 kHz and phase margin of 70°, which are exactly same as in AP-MCA.

A series of measurements for the system small-signal frequency response have been tested and compared to the calculated models. The calculated and measured Bode plots of the open-loop transfer function of P-MCA are compared in Fig. 20, where both curves match quite well until 20 kHz. Similar as AP-MCA, the measurements show the implemented P-MCA has higher damping factor that the calculated model.

The measured Bode plots of the closed-loop transfer function of P-MCA for the nominal-load and no-load conditions are illustrated in Fig. 21. The "−3 dB frequency" is about 7 kHz.

V. Hardware and Performance Comparison

In this section, the designed laboratory prototype for verifying the three different amplifier topologies is first introduced; then, the measurements from these amplifiers are compared.

TABLE II
Specifications of Laboratory Prototype

135V Range	270V Range
U_{in} = 200 V	U_{in} = 400 V
$U_{o,rms}$ = 0 V ~ 135 V	$U_{o,rms}$ = 0 V ~ 270 V
$R_{L,nom}$ = 35 Ω	$R_{L,nom}$ = 70 Ω
P_o = 500 W @ 135 Vac	P_o = 1 kW @ 270 Vac
$I_{o,max}$ = 4.5 A (continuous)	
Power bandwidth = 5 kHz	
Load phase angle = -π/4…+π/4	

A. Hardware Realization

In order to create a common basis for comparison, the specifications applied for all the amplifiers are given in Table II, where U_in is the dc input voltage, which could be provided by a bidirectional single-phase rectifier, U_o is the rms value of the output voltage and spans the universal input voltage range, and P_o is the output power.

For both output voltage ranges, the amplifiers are able to output maximum 4.5 A continuous current. The input nominal voltage is regulated to be 200 and 400 V, respectively, for the 135 and 270 VAC output voltage ranges. This brings the benefit that the amplifiers can utilize all the levels for both output voltage ranges so that the output-voltage quality does not suffer when the amplifiers generate low-amplitude output voltage.

The power-circuit scheme of the laboratory prototype is depicted in Fig. 22. When designing the prototype, the following issues were considered.

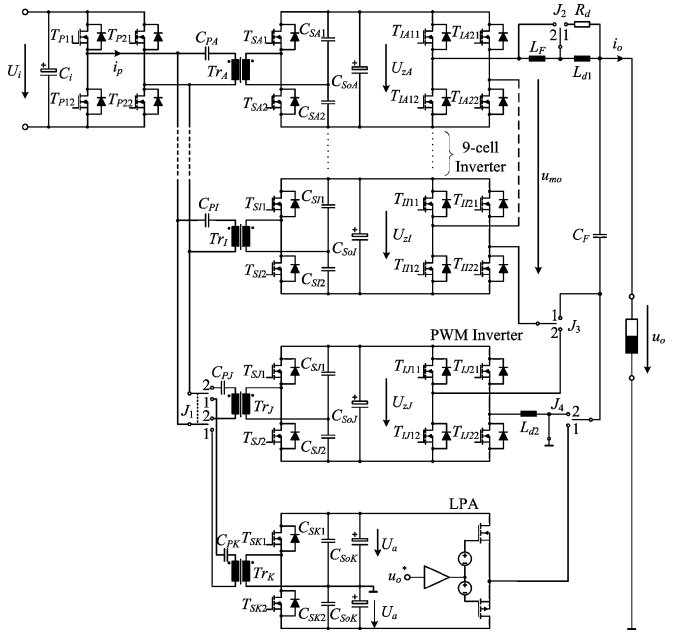

Fig. 22. Laboratory prototype power-circuit scheme. By the proper selection of the jumpers and different digital control coding, this hardware can realize three topologies: H-MCA, AP-MCA (AM+PWM), and P-MCA (PWM).

TABLE III
JUMPER TABLE FOR HARDWARE CONFIGURATION OF DIFFERENT TOPOLOGIES

Topology	J_1	J_2	J_3	J_4
H-MCA	1	1	1	1
AP-MCA (AM + PWM)	2	2	2	2
P-MCA (PWM)	2	2	2	2

1) Flexible structure that allows a single hardware to realize all the three topologies.
2) Compact and symmetric design.

By the proper selection of the jumpers and different digital control coding, this prototype is able to implement three topologies: H-MCA (nine-cell AM inverter plus LPA), AP-MCA (nine-cell AM inverter plus one-cell PWM amplifier), and P-MCA (ten-cell PWM amplifier). Table III shows the jumper configurations for realizing the different topologies, where the jumpers are realized by using connectors and 0-Ω resistors. For example, to switch the system from AP-MCA to H-MCA, one daughter board has to be plugged out and replaced by another board that can provide the dc supply voltages for the LPA, i.e., J_1 switches the position from 2 to 1. For realizing the switching of J_2, J_3, and J_4, one has to solder and/or unsolder the relevant 0-Ω resistors. The power components are listed in Table IV.

The front and rear views of the ten-cell amplifier laboratory prototype are shown in Fig. 23. This hardware comprises one motherboard, five daughter boards, five mirrored daughter boards, one FPGA/measurement board, and one DSP board. The motherboard mainly serves as interface between FPGA/measurement board and daughter boards. Besides that, the primary MOSFETs as well as their gate drivers, the current

TABLE IV
COMPONENTS LIST

Name	Denotation	Type	Manufacturer
Input Capacitor	C_i	2 X 100 µF / 450 V	nichicon
Primary MOSFETs	T_{P11}, T_{P12}, T_{P21}, T_{P22}	SPP20N60CFD	Infineon
Primary Resonant Capacitor	C_{PX} (X=A…K)	3 X 15 nF / 400 V	AVX
Transformer	Tr_X (X=A…J)	EFD 30/15/9, N87, 120:6	Epcos
Secondary MOSFETs	T_{SX1}, T_{SX2} (X=A…K)	IRF6648	IRF
Secondary Half Bridge Capacitor	C_{SX1}, C_{SX2} (X=A…J)	4 X 10 nF / 25 V	muRata
Secondary DC Link Capacitor	C_{SoX} (X=A…J)	2 X 330 µF / 50V	PANASONIC
Inverter MOSFETs	T_{IX11}, T_{IX12}, T_{IX21}, T_{IX22} (X=A…K)	IRF6648	IRF
Output Inductor	L_F	10 µH, 10 A	RENCO
Output Damping Inductor	L_{d1}, L_{d2}	68 µH, 6.2 A	C & D TECH.
Damping Resistor	R_d	2 X 10 Ω (parallel)	BI Technologies
Output Capacitor	C_F	220 nF / 500 VAC	EPCOS
Power Operational Amplifier		MP111FD	APEX

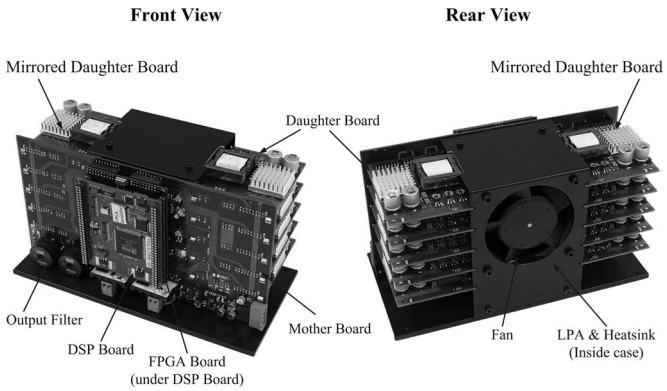

Fig. 23. Laboratory prototype with both front and rear views.

sensors, output filter, LPA, and main contactors are assembled on the motherboard as well.

The high-frequency ac-voltage bus generated by the primary full bridge provides the input voltage for all the daughter boards. Each daughter board, as shown in Fig. 24, mainly consists of the resonant capacitor, isolation transformer, and the secondary-side MOSFETs. The reason to design five mirrored daughter boards is to limit the interfering high-frequency ac voltage to a small area and to have a symmetric system design. Furthermore, four n-channel MOSFETs are used for each inverter cell. This requires the corresponding four gate drivers must have three different ground potentials. There is alternative way to form the H-bridge by using complementary p- and n-channel MOSFETs that brings the benefit to reduce the realization effort and saving of the printed circuit board space.

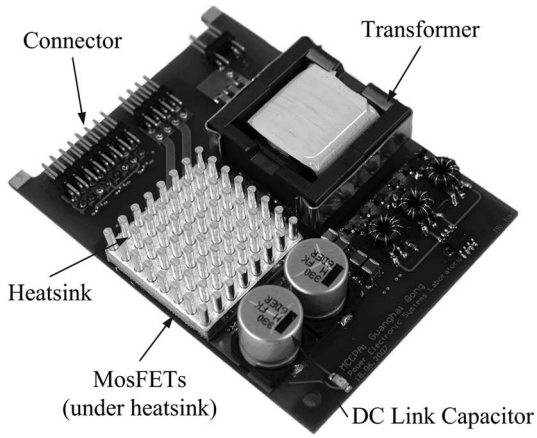

Fig. 24. Daughter board.

Fig. 26. Universal DSP control board from PES, ETH Zurich.

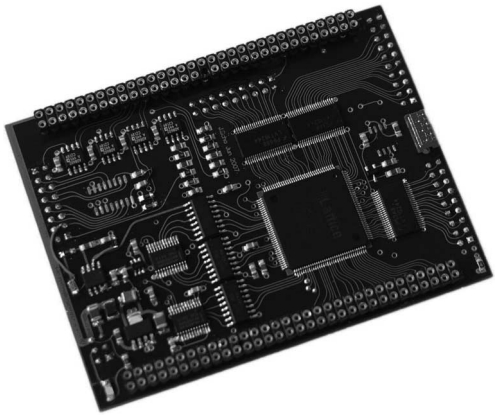

Fig. 25. FPGA and measurement board with 49 independent gate control signals.

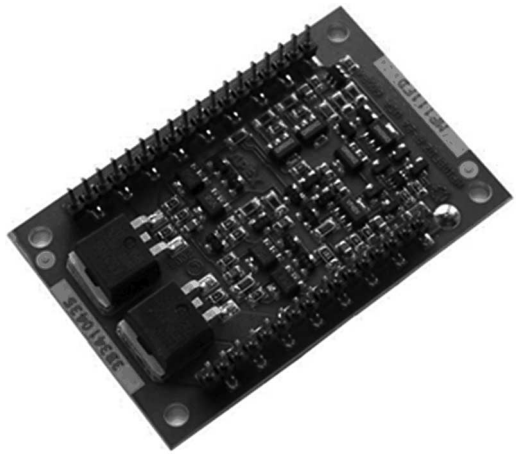

Fig. 27. Apex power operational power amplifier MP111FD. The dimension is 41.4 mm $\times$ 63.2 mm $\times$ 11.5 mm.

Because of the large number of employed MOSFETs, the system requires 49 independent gate control signals. Therefore, a 144-pin Lattice FPGA chip, LCMXO2280 C, with 2280 lookup tables (LUTs) and 113 I/Os is selected to fulfill the requirement in the FPGA/measurement board, as demonstrated in Fig. 25. This board also includes 20 fast-speed comparators, MAX964, which are used for generating the AM inverter control signals with minimized delay time in H-MCA. The control signals measurement circuits are integrated in this board as well. The DSP board shown in Fig. 26 is the universal DSP control board from power electronic systems (PES), ETH Zurich. There, the 16-bit, fixed-point DSP controller from analog devices, ADSP-21992, is equipped. This device also embeds eight-channel, 14-bit AD converters with up to 20 MSPS.

For the H-MCA, the most important requirement for the LPA is that it must have enough high slew rate to compensate for the ramp-up and ramp-down slope of the multicell inverter. In this design, the *dv*/*dt* of the step voltages from the multicell inverter is designed as 50 V/μs. Therefore, a commercial APEX power operational power amplifier MP111FD, as shown in Fig. 27, is used in the system. The main specifications of MP111FD are: SR $=$ 130 V/μs, 15 A/100 V, maximum allowed power dissipation 130 W at 60 °C. This device is assembled in the middle area of motherboard where the corresponding heatsink and fan have to be attached in addition in order to dissipate the amplifier losses. Furthermore, the fins of the heatsink are placed horizontally; therefore, the air blown by the fan can also flow to all the daughter boards, which helps to improve their thermal condition.

B. Performance Comparison of MCAs

Based on the universal prototype, the system performances of H-MCA, AP-MCA, and P-MCA are measured and compared.

Fig. 28 shows the system key waveforms at the nominal operation. In H-MCA, the sinusoidal output voltage is achieved by using a high slew rate LPA to correct the stair-shaped voltage generated by the multicell inverter. For AP-MCA and P-MCA, the output voltage is attained by low-pass filtering the 500 kHz switching ripple in u_{mo}, where AM+SPWM and phase-shifted unipolar SPWM are utilized for AP-MCA and P-MCA, respectively. Both H-MCA and P-MCA generate smooth 1 kHz sinusoidal output voltage waveforms, whereas there is notable distortion in the output voltage produced by AP-MCA. This distortion is due to that the control system does not have sufficient attenuation for the disturbance caused by the AM-modulated

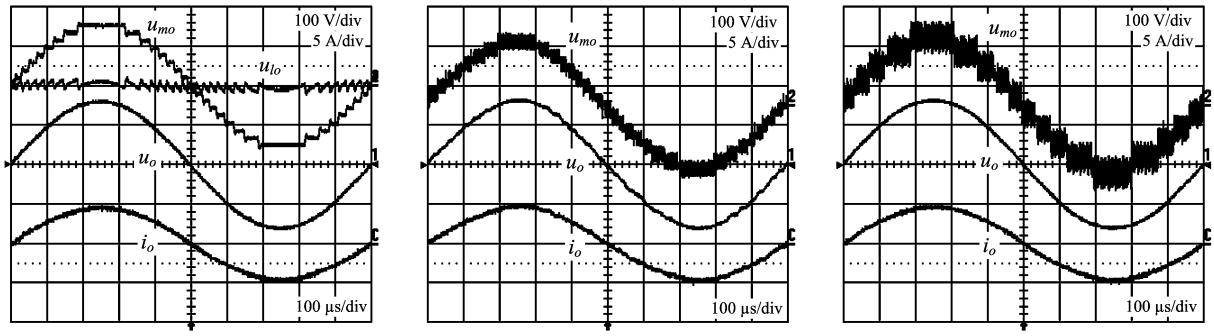

Fig. 28. Key waveforms at nominal operation: (a) H-MCA, (b) AP-MCA, and (c) P-MCA. Operation parameters: $U_{\rm in} = 200\,{\rm V}$, $f_o = 1\,{\rm kHz}$.

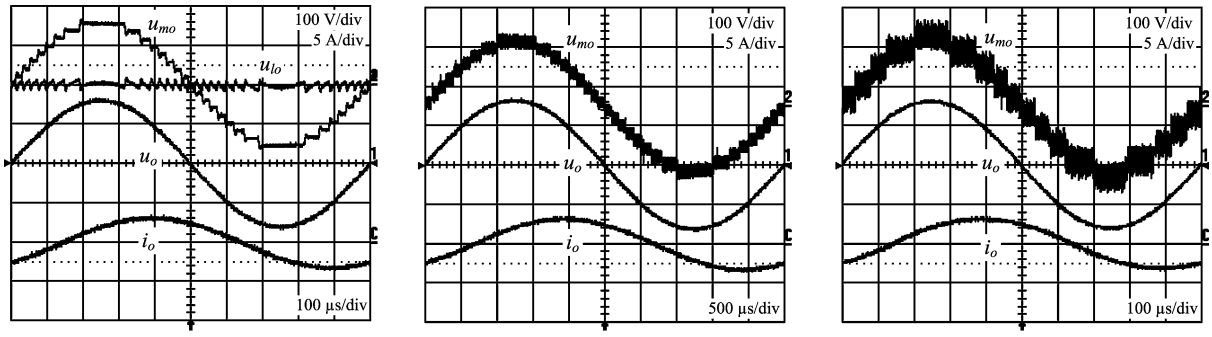

Fig. 29. System operation for an inductive load of 2.5 mH/35 Ω in series: (a) H-MCA, (b) AP-MCA, and (c) P-MCA. Operation parameters: $U_{\rm in} = 200\,{\rm V}$, $f_o = 1\,{\rm kHz}$ (200 Hz for AP-MCA).

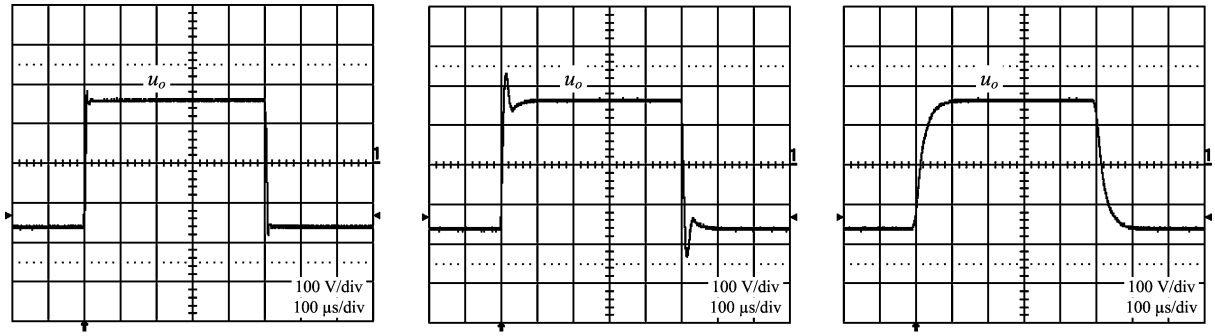

Fig. 30. Systems output rectangular waveform: (a) H-MCA, (b) AP-MCA, and (c) P-MCA. Operation parameters: $U_{\rm in} = 200\,{\rm V}$, $f_o = 1\,{\rm kHz}$.

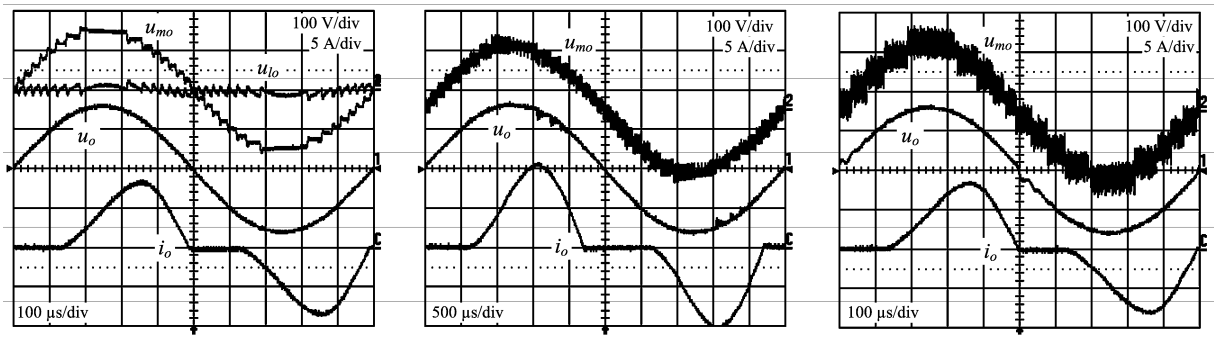

Fig. 31. Systems supplying a nonlinear load: (a) H-MCA, (b) AP-MCA, and (c) P-MCA. Operation parameters: $U_{\rm in} = 200\,{\rm V}$, $f_o = 1\,{\rm kHz}$ (200 Hz for AP-MCA).

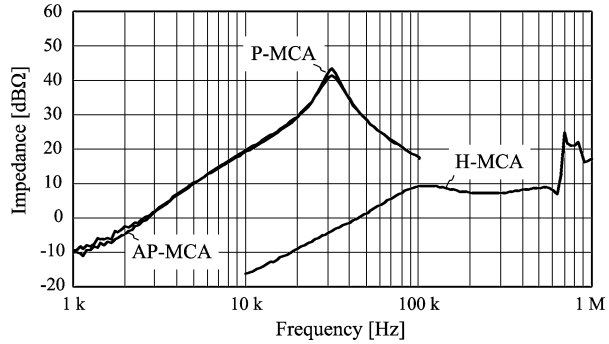

Fig. 32. System output impedance in dependency on the output frequency. DC operation parameters: $U_o = 120\,\mathrm{V}$, $R_L = 35\,\Omega$.

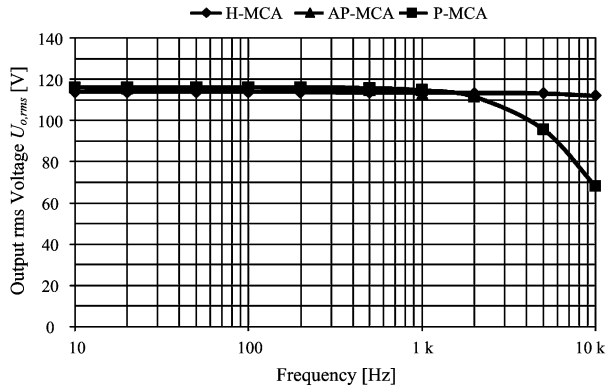

Fig. 33. Large-signal output voltage in dependency on the output frequency for a specified output voltage reference $U_{o,\mathrm{rms,ref}} = 115\,\mathrm{V}$.

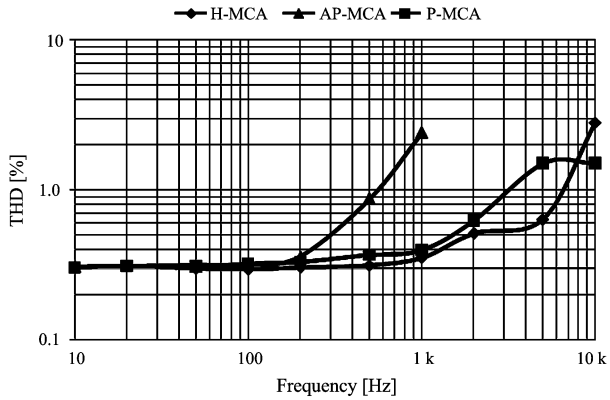

Fig. 34. THD of the output voltage in dependency on the output frequency, where $U_{o,\mathrm{rms,ref}} = 115\,\mathrm{V}$.

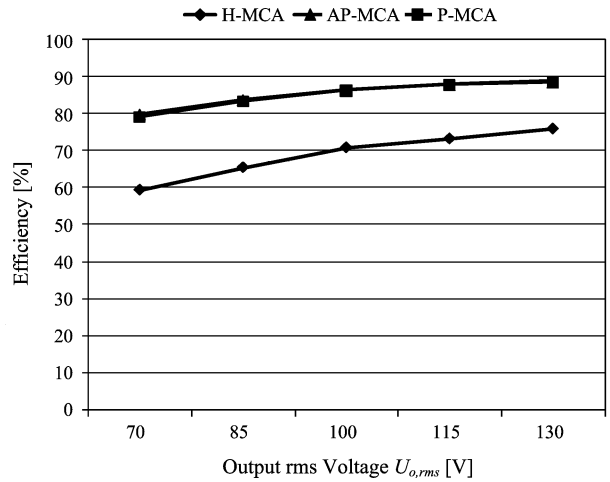

Fig. 35. Measured system efficiency in dependency on the output voltage for nominal load.

multicell output voltage. In the following measurements, the nominal output frequency is reduced to 200 Hz in order to guarantee a clean output-voltage shape for AP-MCA. Furthermore, H-MCA shows much less common-mode noise in contrast with other two systems.

The measured waveforms when the systems supply an inductive load of 2.5 mH/35 Ω in series are demonstrated in Fig. 29. The experimental results show that all the three systems are able to feed a nonresistive load as specified without any stability problem. The measurement results for supplying capacitive loads are given in [24].

Fig. 30 illustrates the experimental results when the systems generate rectangular waveforms for the nominal load. H-MCA shows the highest slew rate of 60 V/μs but with a voltage overshoot of 6%. There is no voltage overshoot for P-MCA; however, it has the slowest slew rate that is only 6.5 V/μs. AP-MCA is not suitable for generating rectangular output voltage because of the excessive overshoot.

The system performances for supplying a nonlinear load are compared in Fig. 31. For this test, a load circuit comprised of a full-bridge rectifier followed by a 2.5-mH inductor in series with a parallel-connected 100-μF capacitor and 35-Ω resistor is employed. H-MCA shows the cleanest output-voltage shape. There is small crossover distortion occurring in the output voltage of P-MCA. In AP-MCA, the peak current is larger because lower test frequency is applied. The overcurrent causes too much voltage drop in the dc supply voltages of the inverter cells, therefore we see the distortion in AP-MCA.

H-MCA has much lower output impedance in contrast to AP-MCA and P-MCA, as demonstrated in Fig. 32. The reasons are that H-MCA has much higher bandwidth, and *dv*/*dt* filter has higher corner frequency and much higher damping factor compared to the output filter of AP-MCA and P-MCA.

The large-signal output voltage with dependency on the output frequency for a specified output-voltage reference $U_{o,\mathrm{rms,ref}} = 115\,\mathrm{V}$ is measured and compared in Fig. 33, where the output-voltage amplitude of H-MCA is able to keep almost constant for the frequency range from 10 Hz to 10 kHz. However, the output-voltage amplitude of P-MCA starts to fall after 1 kHz because of the limited bandwidth.

Fig. 34 shows the measured total harmonic distortions (THDs) of the output voltage. There H-MCA and P-MCA show similar THD values from 10 Hz to 10 kHz. However, the THD of AP-MCA increases very quickly after 200 Hz because of the internal disturbance as discussed already.

The measured system efficiencies are depicted in Fig. 35, where AP-MCA and P-MCA have increased the efficiency by at least 13 percentage points in contrast to H-MCA by eliminating the LPA.

TABLE V
SYSTEM PERFORMANCE COMPARISON

Topologies	H-MCA	AP-MCA	P-MCA
Efficiency ($U_{o,rms}$ = 130 V, R_L = 35 Ω)	76%	89%	89%
Slew Rate (U_{op} = 162 V, R_L = 35 Ω)	60 V/μs	32 V/μs	6.5 V/μs
THD ($U_{o,rms}$ = 115 V, R_L = 35 Ω, f_o = 1kHz)	0.35%	2.4%	0.39%
Power Bandwidth	10 kHz	1 kHz	7 kHz
Small-signal Bandwidth	600 kHz	8 kHz	7 kHz
Output Impedance (f = 10 kHz)	0.16 Ω	10 Ω	10 Ω

The main system performances that have been compared are summarized in Table V.

VI. CONCLUSION AND OUTLOOK

Three multilevel amplifiers, H-MCA, AP-MCA, and P-MCA, for ac-test-power-source applications are presented in this paper. For each type of amplifier, its operation principle is explained and its control design is described. A universal laboratory prototype with a compact and symmetric design is built to verify the theoretical analysis. This prototype is able to realize three topologies: H-MCA, AP-MCA, and P-MCA, by the proper selection of the jumpers and different digital control coding. The performances of these three amplifiers are measured from the prototype and compared.

P-MCA shows the advantages of simple modulation/low implementation effort, high efficiency, low THD, sufficient power bandwidth, and no overshoot voltage for step response, but it has a limited slew rate of only 6.5 V/μs. This topology can be employed for low-cost ac-power-source applications that do not require very high dynamics, or the grid utility interface for renewable energy applications.

Concerning the system dynamic, H-MCA is obviously the best topology that possesses many merits like high slew rate, high power and small-signal bandwidth, low output impedance that make it have excellent performance in case of nonlinear load, and low THD. However, the system performance is impaired by the low efficiency and this system is relatively costly compared to the pure switch-mode amplifiers.

The output-voltage quality at high frequencies of AP-MCA suffers from the AM+SPWM hybrid modulation scheme. There, the control signals of the AM multicell inverter are obtained by comparing the input reference signal and a series of threshold voltages; therefore, the feedback voltage has no influence on determining the output voltage of the AM multicell. Thus, this multicell inverter acts as a disturbance voltage source for the control system.

Based on the studies of the MCAs in this study, some ideas for improving the system performance in the course of further research are listed as follows.

1) LPA design is the key to achieve better system performance. Instead of using the commercial LPA in H-MCA, a custom-designed LPA with higher power bandwidth could be employed, where the feed-forward control also could be applied as show in Fig. 3. This would further improve the output-voltage quality and dynamic behavior.
2) For some applications where the flexibility to increase or decrease the output voltage is not necessarily required, an asymmetric multicell inverter would significantly reduce the number of inverter cells needed for generating the same number of output voltage levels [27].
3) There would be several possibilities for further improvement of the system dynamics performance of P-MCA: reducing sampling time, using higher switching frequency/smaller output filter, or utilizing fast control methods, e.g., single-cycle control [28].

REFERENCES

[1] G. B. Yundt, "Series- or parallel-connected composite amplifiers," *IEEE Trans. Power Electron.*, vol. PE-1, no. 1, pp. 48–54, Jan. 1986.
[2] S. Kashiwagi, "A high-efficiency audio power amplifier using a self-oscillating switching regulator," *IEEE Trans. Ind. Appl.*, vol. IA-21, no. 4, pp. 906–911, Jul. 1985.
[3] X. Jiang, N. D. Lopez, and D. Maksimovic, "A switched mode envelope tracker for polar EDGE transmitter," in *Proc. 2006 IEEE Power Electron. Spec. Conf.*, pp. 1–7.
[4] M. Rodriguez, P. F. Miaja, A. Rodriguez, and J. Sebastian, "A multiple-input digitally-controlled buck converter for envelope tracking applications in radiofrequency power amplifiers," *IEEE Trans. Power Electron.*, vol. 24, Nov. 2009.
[5] M. Vasic, O. Garcia, J. A. Oliver, P. Alou, D. Diaz, and J. A. Cobos, "Multilevel power supply for high efficiency RF amplifiers," *IEEE Trans. Power Electron.*, vol. 24, Nov. 2009.
[6] M. Hoyerby and M. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2387–2398, Sep. 2008.
[7] F. Wang, A. H. Yang, D. F. Kimball, L. E. Larson, and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1244–1255, Apr. 2005.
[8] G. Gong, H. Ertl and J. W. Kolar, "Novel power supply for linear power amplifiers," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 684–698, Feb. 2008.
[9] N. Sano, T. Hayashi, and H. Ogawa, "High efficiency class an audio power amplifier (class A+ amplifier)," presented at the 61st Convers. Audio Eng. Soc., 1978, Preprint No. 1382.
[10] J. H. Jeong, G. H. Kim, and B. R. Min, et al., "A high efficiency class A amplifier accompanied by class D switching amplifier," in *Proc. 1997 IEEE Power Electron. Spec. Conf.*, vol. 2, pp. 1210–1216.
[11] O. M. Mueller and J. N. Park, "Quasi-linear IGBT inverter topologies," in *Proc. 1994 IEEE Appl. Power Electron. Conf.*, vol. 1, pp. 253–259.
[12] H. Ertl, J. W. Kolar, and F. C. Zach, "Basic considerations and topologies of switched-mode assisted linear power amplifiers," *IEEE Trans. Ind. Electron.*, vol. 44, no. 1, pp. 116–123, Feb. 1997.
[13] H. Ertl, J. W. Kolar, and F. C. Zach, "A novel switch-mode power amplifier with high output voltage quality employing a hybrid output voltage filter," in *Proc. 1997 Power Electron. Intell. Motion Conf.*, pp. 419–428.
[14] R. A. R. Van Der Zee and E. A. J. M. van Tuijl, "A power-efficient audio amplifier combining switching and linear techniques," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 985–991, Jul. 1999.
[15] G. R. Walker, "A Class B switch-mode assisted linear amplifier," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1278–1285, Nov. 2003.
[16] A. E. Ginart, R. M. Bass, W. M. Jr. Leach, and T. G. Habetler, "Analysis of the class AD audio amplifier including hysteresis effects," *IEEE Trans. Power Electron.*, vol. 18, no. 2, pp. 679–685, Mar. 2003.
[17] T. W. Kwak, M. C. Lee, Y. S. Yuk, K. H. Lee, H. H. Park, C. Kim, and G. H. Cho, "Hybrid switching amplifier using a novel two-quadrant wideband buffer for dynamic power supply applications," in *Proc. 2008 Power Electron. Spec. Conf.*, pp. 546–551.
[18] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[19] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.
[20] Datasheet of APEX Microtechnology Power Operational Amplifier MP 111 [Online]. Available: http://www.apexmicrotech.com.
[21] D. Self, *Audio Power Amplifier Design Handbook*, 3rd ed. London, U.K.: Newnes, 2002, pp. 247–253.
[22] K. Iwaya and T. Noguchi, "High-frequency switched mode power with small capacity filter inverters," in *Proc. 2004 IEEE Ind. Electron. Soc. Conf.*, vol. 1, pp. 35–40.
[23] P. Cooke, "Modeling average current mode control," in *Proc. 2000 IEEE Appl. Power Electron. Conf. Expo.*, vol. 1, pp. 256–262.
[24] G. Gong, "Hybrid amplifiers for AC power source applications," Ph.D. dissertation, ETH Zurich, Zurich , Switzerland, 2009.
[25] J. J. D'Azzo, *et al., "Linear Control System Analysis and Design: Conventional and Modern,"* McGraw-Hill, 1992, Chapter 15–16.
[26] G. F. Franklin, *Digital Control of Dynamic Systems*, 5th ed. Boca Raton, FL: CRC Press, 2003, p. 451.
[27] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.
[28] Z. Lai and K. M. Smedley, "A new extension of one-cycle control and its application to switching power amplifiers," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 99–105, Jan. 1996.

Guanghai Gong was born in Zhejiang, China, in 1977. He received the B.Sc. and M.Sc. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1999 and 2002, respectively, and the Ph. D. degree from the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland.

In January 2008, he joined ABB Switzerland as a Development Engineer in the Traction Converters Department. Since March 2009, he has been a Technical Project Manager for high-power traction converters. His research interests during his studies included hybrid power amplifiers, soft-switched dc-dc converters, and ac-dc converters for aircraft applications. Currently his focus is on the development of traction converters for locomotive and high-speed train applications.

Dominik Hassler received the M.Sc. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in May 2007.

He was engaged in power electronics, high-voltage technology, and embedded systems. He has been a Research Associate with the Power Electronic Systems Laboratory, ETH Zurich, with main focus on hardware development and software engineering.

Johann W. Kolar (SM'xx–F'10) received the M.Sc. and Ph.D. degrees (*summa cum laude/promotio sub auspiciis praesidentis rei publicae*) from the University of Technology Vienna, Vienna, Austria.

Since 1984, he has been engaged as an Independent International Consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics, and high-performance drives. On February 1, 2001, he was appointed as a Professor and the Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland. He has proposed numerous novel pulsewidth-modulated (PWM) converter topologies, and modulation and control concepts, e.g., the VIENNA Rectifier and the three-phase ac–ac sparse matrix converter. He has authored or coauthored more than 350 scientific papers in international journals and conference proceedings and has filed 75 patents. He also received an Erskine Fellowship from the University of Canterbury, Christchurch, New Zealand, in 2003. He initiated and/or is the founder/cofounder of four spin-off companies targeting ultrahigh-speed drives, multidomain/level simulation, ultracompact/efficient converter systems, and pulsed power/electronic energy processing. Since 2002, he has also been an Associate Editor of the *Journal of Power Electronics of the Korean Institute of Power Electronics* and has been a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*. His current research interests include ac–ac and ac–dc converter topologies with low effects on the mains, e.g., for power supply of data centers, more-electric-aircraft and distributed renewable energy systems, realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (e.g., SiC), novel concepts for cooling and electromagnetic interference (EMI) filtering, multidomain/scale modeling/simulation and multiobjective optimization, physical-model-based lifetime prediction, pulsed power, and ultrahigh-speed and bearingless motors.

Dr. Kolar is the recipient of the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the First Prize Paper Award of the IEEE IAS IPCC in 2008, and the IEEE IECON Best Paper Award of the IES PETC in 2009. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory, ETH Zurich, as the leading academic research institution in power electronics in Europe. He is a member of the IEEJ and a member of the International Steering Committees and the Technical Program Committees of numerous international conferences in the field (e.g., the Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and the Chairman of the Education Chapter of the EPE Association. From 1997 to 2000, he was an Associate Editor of the IEEE Transactions on Industrial Electronics. Since 2001, he has been an Associate Editor of the IEEE Transactions on Power Electronics.