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Comprehensive Large-Signal Performance Analysis of Ceramic Capacitors for Power Pulsation Buffers

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Abstract—In high power density single-phase PV inverter systems, active auxiliary circuits are installed, shifting the double line-frequency power pulsation away from the dc link to a dedicated buffer capacitor. Being relieved from strict voltage ripple requirements, a larger voltage ripple is allowed at the buffer capacitor, significantly reducing the capacitance requirements and consequently the overall volume of the converter system. Since the capacitance density of electrolytic capacitors must be derated because of imposed current limitations, ceramic capacitors become the preferred choice in power pulsation buffer applications. In particular, TDK's class II X6S MLCC with BaTiO₃ ceramic and the recently launched CeraLink with PLZT ceramic are promising candidates due to their high energy density. The actual prevailing capacitance of these two types of ceramics, strongly depends on the operating point, that is, a dc bias voltage and a superimposed large-signal amplitude ac voltage. Unfortunately, the large-signal behavior and performance of these ceramic capacitors is not specified by the manufacturer. In this paper, a comprehensive characterization of the X6S MLCC and the CeraLink large-signal performance is carried out by means of experimental measurements. The acquired data enables an accurate dimensioning of the power pulsation buffer capacitor and an estimate of the capacitor losses during operation. Since the device temperature has a strong impact on the ceramic properties, results for 30 °C, 60 °C and 90 °C are presented.

Index Terms—Ceramic Capacitor, CeraLink, PLZT, Class II, X6S, BaTiO₃, MLCC, Large-Signal, Power Pulsation Buffer, Active Power Decoupling

I. INTRODUCTION

In single-phase power electronic systems, typically bulky electrolytic capacitors are installed in order to cope with the intrinsic double line-frequency power pulsation. Aiming at the highest possible power density of a single-phase PV inverter, active power decoupling techniques are applied [1]–[3], shifting the double line-frequency power pulsation away from the dc link to a dedicated buffer capacitor. Being relieved from strict voltage ripple requirements, a much larger voltage swing is allowed at this buffer capacitor, resulting in drastically reduced capacitance requirements for the so called Power Pulsation Buffer (PPB) which also comprises a converter stage interfacing the buffer capacitor and the dc link. In order to identify the most suited capacitor technology for PPB applications, a benchmark of selected class II ceramic capacitors, metalized polyester (PEN), metalized polypropylene (PP) and electrolytic capacitors with rated voltages between 50 V and 450 V is presented in [4]. Since the energy density of electrolytic capacitors must be derated because of lifetime associated current limitations, the benchmark revealed that 2.2 μF/450 V class II X6S ceramic capacitors from TDK's C575 Multi Layer Ceramic Capacitor (MLCC) series features by far the highest energy density.

Not included in the benchmark in [4] but considered in this paper, is the recently launched CeraLink capacitor from TDK which is well suited for power electronic applications according to its promising properties [5], [6]. In [1], a Pareto optimal design in terms of power

density of a 2 kW PPB implemented for the Google Little Box Challenge is presented. In order to accurately dimension the employed ceramic buffer capacitor and calculate the losses associated with the power pulsation in each iteration of the optimization procedure in [1], operating point dependent large-signal performance data of the X6S MLCC and the CeraLink capacitor are needed. More specifically, the capacitance and loss density as a function of applied dc bias $V_{dc} \in [0, 400]$ and superimposed double line-frequency ac voltage $V_{ac} \in [0, 130]$ is required. Unfortunately, comprehensive large-signal capacitance and loss data of ceramic capacitors is not provided by the manufactures and is also lacking in scientific literature. In [4] only a single operating point, 225 V dc bias and 450 V_{pp} ac excitation, is provided for the X6S MLCC. Therefore, in this paper experimentally determined large-signal performance data of the two most promising capacitor candidates, 2.2 μF, 450 V class II X6S MLCC and 2 μF, 650 V 2nd generation CeraLink are presented. Since the performance of the considered ceramic materials is strongly affected by the operating temperature, the experimental results for 30 °C, 60 °C and 90 °C device temperature are provided. An introductory comparison between the two considered ceramic capacitor technologies consider herein are given in Section II. The experimental setup, similar to the one presented in [4], and the measurement principle to calculate the capacitance and loss density of the capacitors is presented in Section III. The obtained results are presented and discussed in Section IV. Furthermore, a polynomial fit to the measured data is provided in Section V, allowing design engineers to accurately dimension a buffer capacitor and estimate the occurring losses.

II. X6S MLCC VS. CERALINK

MLCCs are divided in three application classes (according to IEC/EN 60384-1), depending on the relative permittivity and the stability with respect to voltage, temperature and frequency of the ceramic material. Class II ceramics are made of ferroelectric materials such as barium titanate (BaTiO₃) and are therefore well suited for energy storage application due to the high relative permittivity. Adversely, the relative permittivity of barium titanate based ceramics is not constant but strongly depends, among several other factors, on the applied dc bias and ac excitation [7], [8]. With increasing dc bias voltage, the effective capacitance of class II ceramics drastically drops, decreasing capacitance density at operating voltage levels. Depending on the used additives in the ceramic compositions, various temperature ranges such as X5R, X6S, Y5V etc. are available. The first letter of the code specifies the minimum operating temperature, the digit defines the upper temperature and the last letter defines the deviation from the nominal capacitance over the operating temperature range. The X6S MLCC considered here can be operated from –55 °C to 105 °C with a change in capacitance of $\Delta C/C = \pm 22\%$.

By contrast, the novel CeraLink capacitor technology consists of a lead-lanthanum-zirconate-titanate (PLZT) ceramic composition

whose crystal structure is tuned such to exhibit anti-ferroelectric behavior if no voltage is applied. By applying an electrical field, it is energetically more favorable for the anti-parallel polarized domains to switch into a parallel configuration. By switching the domains, additional energy can be stored which appears as an increase of the dielectric permittivity under field. When exceeding this maximum “switching level” by even stronger electrical fields, a ferroelectric behavior with decreasing permittivity is observed [5], [6], [9]. The level of the maximum permittivity can be adjusted by variation of the dielectric layer thickness of the multilayer capacitor’s design. As a consequence, the CeraLink offers high capacitance at dc link voltage levels.

Several properties of a single capacitor X6S MLCC and CeraLink chip are compared in Tab. I, emphasizing that the CeraLink is rated for voltages up to 650 Vdc in contrast to the max. permissible operating voltage of 450 Vdc in case of the X6S MLCC. The 2nd generation CeraLink prototypes provided by TDK were tuned such to exhibit the highest rel. permittivity around a bias of 375 V. The

TABLE I
COMPARISON OF X6S MLCC AND CERALINK

	TDK X6S MLCC C5750X6S2W225M250KA	TDK CeraLink 2 nd gen. prototype PLZT
Material	BaTiO ₃	PLZT
Capacitance	2.2 μF ¹	2.0 μF ²
Dimensions	5.7 x 5 x 2.5 mm	7.3 x 8 x 2.7 mm
Volume	0.07 cm ³	0.16 cm ³
Current Rating	1 A/μF, $f > 100$ kHz	5 A/μF, $f > 100$ kHz
Max. voltage	450 Vdc	650 Vdc
Max. temperature	105 °C	125 °C

¹ Nominal capacitance at 0 Vdc bias.

² Typ. nominal capacitance at $V_{op} = 400$ Vdc.

inner electrodes of the X6S MLCC are made from Nickel (Ni), which is a standard material for inner electrodes in ceramic capacitors. CeraLink’s PLZT ceramic is able to be cofired with copper inner electrodes, which enables optimal thermal conductivity and lowers electrical losses, especially in the high-frequency regime.

The X6S MLCC comes in a monolithic SMD package where the outer terminations, a fired copper paste covered with plated Ni/Sn layers, are directly soldered onto PCBs. In case of the CeraLink, individual ceramic chips are connected to a multilayered metal lead frame consisting of copper and invar steel with silver galvanics in order to increase the robustness with respect to mechanical load (PCB bending, mismatch of thermal expansion during soldering) and decrease thermomechanical stress by matching the resulting thermal expansion coefficients of the materials involved.

A sputter layer of chromium, nickel and silver is applied to the lapped PLZT surface which is then connected to the lead-frame by means of a μ -silver sinter process. This assembly process achieves a highly reliable connection with low ESR and ESL, optimized thermal conductivity and enables the construction of large modules (up to 100 μF). By contrast, since the X6S MLCCs are only available as single chips, realizing a large capacitance value makes it necessary to mount a large number of individual capacitors onto the PCB. A lumped parameter circuit can be used to model the different loss mechanism in ceramic capacitors as presented in [6], [10]. The basic model as shown on the left in Fig. 1 includes a parasitic inductance ESL and several resistors to model the different loss mechanism in ceramic capacitors. Resistor R_{el} connected in series with the capacitor C_{er} models the losses caused by the resistance of the electrodes. The dc losses caused by the leakage current of the

dielectric material are modeled with R_{ins} connected in parallel to C_{er} . The hysteresis losses which occur in the dielectric material when excited with a large voltage swing are modeled with $R_{diel} = \frac{\alpha \cdot 2\pi}{\omega}$ with material constant α , connected in series with dc blocking capacitor C_b . According to [6], the total losses are given by

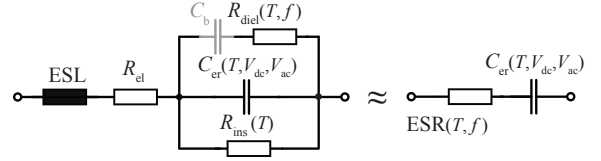


Fig. 1. Lumped parameter circuit to model the losses in ceramic capacitors.

$$P_{tot} = \frac{U_{dc}^2}{R_{ins}} + I_{ac,rms}^2 \cdot \underbrace{\left(R_{el} + \frac{1}{\omega} \frac{\alpha \cdot 2\pi}{1 + (\alpha \cdot 2\pi C_{er})^2} \right)}_{ESR} \quad (1)$$

$$\approx I_{ac,rms}^2 \cdot ESR,$$

where the losses associated with the finite insulation resistance are typically negligible. In Fig. 2 the ESR over frequency is shown for the

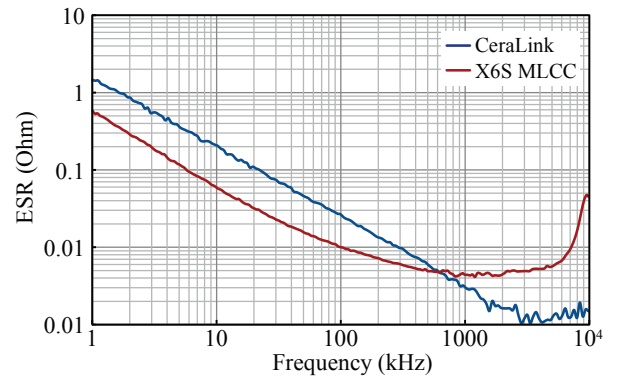


Fig. 2. Comparison of small-signal ESR over frequency measured at 25 °C with 0 V dc bias and 0.5 V rms ac excitation.

X6S MLCC and the CeraLink. At 25 °C, the X6S capacitor has lower resistance at frequencies below 1 MHz, while the CeraLink prototype shows lower values at higher frequencies. Below 1 MHz, the ESR is dominated by the dielectric resistance R_{diel} which decreases with frequency. At higher frequencies the resistance of the conductors (inner electrodes, terminations, and junction resistances) exceed the dielectric resistance. As it can be seen, the ESR starts to increase again at high frequencies which can be explained by the skin effect in the conductors of the capacitors [6]. The difference in ESR in the high frequency range are caused by the different inner electrode material of the two capacitors. As mentioned above, the CeraLink prototype uses electrodes made out of copper, whereas the X6S MLCC uses electrodes made out of nickel, and the specific resistance of copper is approx. a factor of 4 lower than nickel. Although the ESR of the CeraLink drops drastically with temperature as shown in Fig. 3, the low-frequency dielectric losses are still substantial. This is also nicely illustrated in Fig. 4 where the change in stored charge

$$\Delta Q_c(t) = \int_{t_0}^{t_0+t} i_c(\tau) d\tau \quad (2)$$

with respect to the capacitor voltage is plotted for a 120 Hz cycle at 60 °C operating temperature. Clearly visible is the pronounced

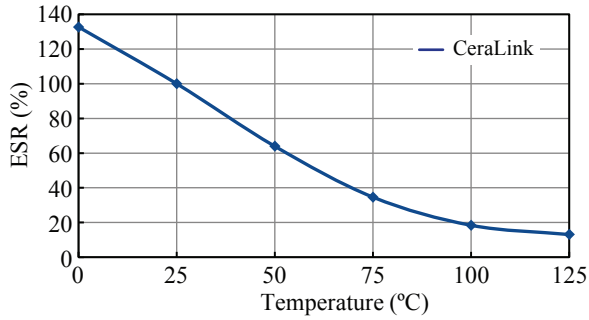


Fig. 3. ESR over temperature of the CeraLink capacitor. Measurement conditions: 400 V dc bias, 0.5 V_{rms}, 1 kHz ac excitation.

hysteresis of the CeraLink capacitor, which indicates significantly higher losses compared to the X6S MLCC which features a much smaller width of the hysteresis loop. Furthermore, Fig. 2 illustrates the change of rel. permittivity with respect to applied dc bias of both ceramic materials considered herein. At low bias voltage the ferroelectric material exhibits a higher rel. permittivity ($\epsilon_{X6S,I} > \epsilon_{Cera,I}$). Increasing the bias voltage to 350 V dc, significantly increases the rel. permittivity of the PLZT ceramic while decreases the rel. permittivity of the BaTiO₃ ($\epsilon_{Cera,II} > \epsilon_{X6S,II}$). As indicated in Fig. 1, the lumped

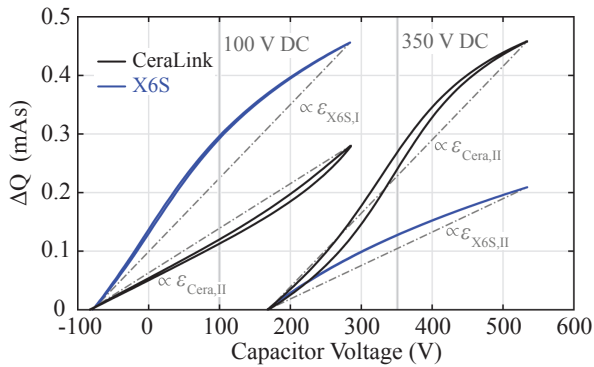


Fig. 4. Change in stored charge in a single CeraLink and X6S MLCC chip with respect to applied voltage at 60°C for 100 V and 350 V dc bias. Clearly visible is the pronounced hysteresis of the CeraLink capacitor.

parameter of the capacitor model strongly depend on temperature, applied voltage amplitude and frequency. The dielectric losses modeled with $R_{diel}(T, f)$ depend strongly on operating temperature and on the frequency of the applied ac voltage. The effective capacitance $C_{er}(T, V_{dc}, V_{ac})$ depends primarily on the applied dc bias but also on the ac voltage and the operating temperature. The experimental results presented in Section IV of this paper confirm these dependencies.

The current rating listed in Tab. I is determined by the self-heating of the capacitor

$$\Delta T = I_{ac,rms}^2 \cdot ESR \cdot R_{th},$$

where the thermal resistance R_{th} models the cooling of the capacitor and depends on the thermal resistance of the capacitor, the PCB and the applied cooling method (convection, forced-air cooling etc.). The specification of the X6S MLCC is different from the CeraLink in terms of the allowed self-heating.

The X6S MLCC is allowed to have a maximum operating temperature of 105 °C and a maximum ΔT of 20 °C [11]. The temperature

raise is limited because due to self heating by ripple currents [12] together with the comparably low thermal conductivity yield to temperature gradients within the ceramic body. As a result, the thermomechanically induced stress yield to cracking and ultimately to malfunction of the ceramic.

By contrast, the CeraLink's maximum permissible change in temperature ΔT is not restricted as long as the maximum operating temperature of 125 °C is not exceeded. Due to the good thermal conductivity of the whole module, no malfunction due to hotspot formation was observed so far.

Because of electromechanical stress inside the ceramic which can lead to increased leakage currents and possible device failure, the maximal allowed ΔT is limited to 20 °C in case of the X6S MLCC [11], [12]. The PLZT ceramic in the CeraLink features extremely small leakage currents and due to the employed copper electrodes a much better thermal spreading is achieved, therefore ΔT is not limited in case of the CeraLink, just the maximum device temperature of 125 °C.

III. EXPERIMENTAL SETUP AND MEASUREMENT PROCEDURE

As mentioned in the introduction, the performance of the device under test (DUT), here the X6S MLCC and CeraLink, must be determined under operating conditions similar to those present in power pulsation buffers. The test setup used to adjust the operating point of the ceramic capacitors is schematically shown in Fig. 5 (a). The voltage applied to the capacitor under test C_{dut} is composed of a dc bias and a superimposed ac ripple voltage. A 600 V dc laboratory source is used to charge a large 1.9 mF electrolytic decoupling capacitor C_b . The output of an ac laboratory supply is connected in series with C_b and C_{dut} by means of a 1 : 1 isolation transformer. Since C_b is much larger than C_{dut} , the voltage across the capacitor under test is given by

$$v_{dut}(t) = V_{dc} + C_b / (C_b + C_{dut}) \approx v_{ac} = V_{dc} + v_{ac}(t).$$

As shown in Fig. 5 (a), the DUT is enclosed in a laboratory oven in order to determine the performance of the DUT for several operating temperatures. In addition, a fan is used to extract the losses occurring in the ceramic capacitors during the experiments and facilitates heat distribution inside the oven. For each operating point $\{V_{dc}, V_{ac}\}$, the resulting voltage and current of the capacitor under test is measured with an oscilloscope equipped with appropriate voltage probe and current transducer. A detailed list of the used test equipment is provided in Tab. III. To increase measurement accuracy, specifically

TABLE II
LIST OF DEVICES USED IN THE TEST SETUP

Item	Type
dc source	Sorensen XHR600-1.7
ac source	Elgar SW5250A
transformer	Rusa GmbH
oven	Binder ED 53
voltage probe	Teledyne HVD3106
current probe	Teledyne CP031A
oscilloscope	Teledyne HDO4054
power meter	Yokogawa WT3000

to increase signal to noise ratio of the current measurement at low ac voltage, and to average tolerances between individual capacitors, multiple capacitors (10 or more) were connected in parallel on a custom mounting fixture as depicted in Fig. 5 (b). Given the recorded measurements, the large-signal characteristics of the capacitor under

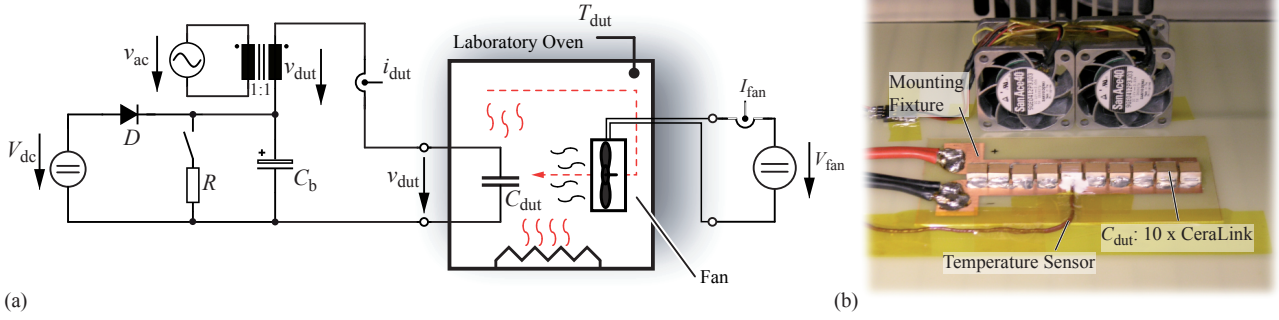


Fig. 5. (a) Experimental setup to adjust the dc bias and ac ripple voltage applied to the ceramic capacitors under test. C_{dut} is enclosed in a laboratory oven in order to emulate different operating temperatures. (b) Picture of the test fixture with installed CeraLink capacitors inside the laboratory oven.

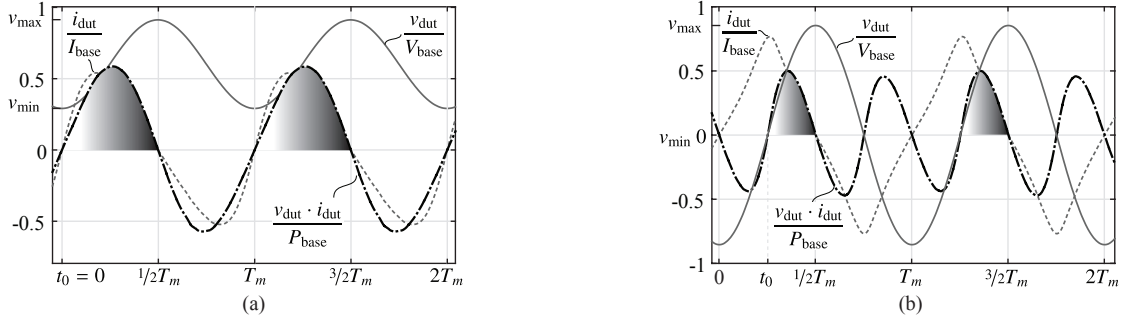


Fig. 6. Measured voltage v_{dut} and current i_{dut} waveforms and calculated instantaneous power of the DUT, where v_{dut} exhibits a dc bias and superimposed ac voltage in (a) and solely an ac voltage in (b).

test are calculated in *MATLAB*. Fig. 6 shows typical voltage and current waveforms and the calculated instantaneous power $p_{\text{dut}}(t) = u_{\text{dut}} \cdot i_{\text{dut}}$ of a measurement performed with X6S capacitors at 30°C . In Fig. 6 (a) an operating point with significant dc bias and ac excitation such that $v_{\text{dut}}(t) > 0, \forall t$, is depicted. The difference in stored energy

$$\Delta E_{\text{dut}} = 1/2 \cdot C_{\text{er,dut}} (\max(|v_{\text{dut}}|)^2 - \min(|v_{\text{dut}}|)^2), \quad (3)$$

is delivered by the ac source within the time interval $t_0 = 0$ and $T_m/2$

$$E_{\text{src}} = \int_{t_0}^{T_m/2} p_{\text{dut}}(t) dt = \int_{t_0}^{T_m/2} u_{\text{dut}} \cdot i_{\text{dut}} dt. \quad (4)$$

Expression (4) also includes the energy which is dissipated during the charging process. The total occurring power loss within one cycle is calculated according to

$$P_{\text{loss,dut}} = \frac{1}{T_m} \int_0^{T_m} u_{\text{dut}} \cdot i_{\text{dut}} dt. \quad (5)$$

Assuming that the total power loss is equally distributed over the charging and discharging interval, the energy related large-signal capacitance at a given operating point is calculated by means of

$$C_{\text{er,dut}} = \frac{2 \cdot \left(\int_{t_0}^{T_m/2} u_{\text{dut}} \cdot i_{\text{dut}} dt - \frac{1}{2} T_m P_{\text{loss,dut}} \right)}{\max(|u_{\text{dut}}|)^2 - \min(|u_{\text{dut}}|)^2}. \quad (6)$$

The integration of the power is started at t_0 when the capacitor voltage reaches minimum in case of $v_{\text{dut}}(t) > 0, \forall t$ (Fig. 6 (a)). If the applied ac voltage is large enough that the voltage across the DUT also becomes negative, then the start of integration t_0 is postponed to coincide with the zero crossing of the capacitor voltage as shown

in Fig. 6 (b). Note, that in this case $\min(|u_{\text{dut}}|) = 0$. The power loss computed with equation (5) includes the ohmic losses in the electrodes and terminals of the capacitor, the losses caused by the leakage current and the losses in the dielectric material due to the large-signal voltage swing. It is essential to carefully deskew voltage and current probes before the measurement, since just a small error in phase-shift can lead to arbitrary wrong results when evaluating (5). In order to check the accuracy of the numerical loss calculation, the losses of the capacitor under test were also measured by means of a Yokogawa WT3000 power analyzer connected at the secondary side of the isolation transformer (not shown in Fig. 5 (a)). Fig. 7 shows the excellent accordance between between directly measured and calculated losses obtained for a single CeraLink capacitor at 60°C operating temperature.

IV. LARGE-SIGNAL CAPACITANCE AND POWER LOSS

The measurement principle outlined in the previous section was carried out for a large number of discrete operating points. For each applied dc bias voltage in the discrete set $\{0, 100, 150, 200, 250, 300, 350, 400\}$ V, measurements at 120 Hz sinusoidal ac voltages with amplitudes in the set $\{10, 30, 50, 70, 90, 110, 130\}$ V rms were performed. These measurements were carried out at 30°C , 60°C and 90°C operating temperature. To refine the coarse grid of measurement point, a two-dimensional piecewise cubic interpolation was performed in *MATLAB*.

A contour plot of the interpolated large-signal capacitance obtained for the CeraLink and the X6S MLCC is shown in Fig. 8. Since the capacitors considered differ in volume, the capacitance per volume is plotted to allow a direct comparison. In the right column of

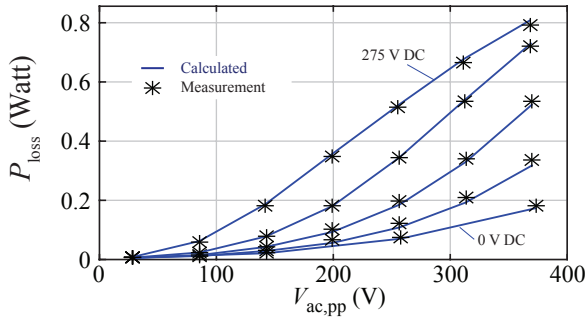


Fig. 7. Comparison between calculated losses according to (5) and measured losses with Yokogawa power analyzer. Depicted are the losses that occur in a single CeraLink chip with respect to applied ac excitation and several dc bias voltages at 60° operating temperature.

Fig. 8 the capacitance density of the X6S MLCC, which strongly reduces with increasing dc bias as expected from a class II ceramic. At 30 °C operating temperature, a maximum capacitance density of 24.87 $\mu\text{F}/\text{cm}^3$ occurs at zero dc bias and small ac amplitude. Given the volume of a single X6S chip of 0.07 cm^3 , the capacitance of 24.87 $\mu\text{F}/\text{cm}^3 \cdot 0.07 \text{ cm}^3 = 1.77 \mu\text{F}$ per chip was measured. The capacitance density is almost constant with respect to the applied ac voltage up to 100 V_{pp} , and then reduces significantly with increasing ac amplitude. However, if a dc bias larger than 250 V is applied, then the capacitance density becomes almost independent of the large-signal ac excitation. The elevated operating temperatures have only a small effect on the X6S MLCC, but it can be noticed that for dc bias levels greater 150 V the capacitance density increases.

The contour plot of the capacitance density of the CeraLink, shown in the left column in Fig. 8, illustrates the unique feature of increasing capacitance with dc bias as described earlier in Section II. At 30 °C operating temperature, the maximal capacitance density of 10 $\mu\text{F}/\text{cm}^3$ occurs at $V_{\text{dc}} = 350 \text{ V}$ and $V_{\text{ac,pp}} = 140 \text{ V}$. Given the volume of a single CeraLink chip of 0.16 cm^3 (roughly twice the volume of a single X6S chip), a maximal capacitance of 1.6 μF per single chip was measured. Increasing the dc bias above 350 V reduces the effective capacitance again. Up to $V_{\text{dc}} \approx 280 \text{ V}$, the capacitance density of the CeraLink increases steadily with the amplitude of the applied ac voltage. Increasing the dc bias voltage further, an optimal ac amplitude in terms of capacitance emerges at $V_{\text{ac,pp}} = 140 \text{ V}$ in case of 30 °C operating temperature. Increasing the operating temperature of the CeraLink, shifts the maximum capacitance density to both smaller dc bias and ac amplitude. Furthermore, the peak of the capacitance density is slightly flattened when the operating temperature increases, clearly visible in the transition from 60 °C to 90 °C temperature. The power loss per chip volume occurring in the CeraLink and X6S MLCC during continuous operation with the respective applied dc bias and ac excitation is shown in Fig. 9. Naturally, the highest loss density occurs in the region of the $\{V_{\text{dc}}, V_{\text{ac}}\}$ space where the combination of large prevailing capacitance and large applied ac voltage is present. At around zero dc bias, the dielectric loss density of the X6S MLCC increases quadratically with applied ac voltage reaching its maximum of 3.9 W/cm^3 at the largest applied ripple voltage (400 V_{pp}). Since the reactive power reduces with increasing dc bias due to the lower effective capacitance, the associated power losses reduce accordingly. Increasing the operating temperature of the X6S MLCC has just a minor impact on the power losses. The peak loss density reduces by a factor of 0.89 to 3.5 W/cm^3 at 90 °C

operating temperature. In case of the CeraLink capacitor, shown in the left column in Fig. 8, the domain of high power loss shifts to larger dc bias voltages. At 30 °C device temperature, a maximal loss density of 9 W/cm^3 occurs at $V_{\text{dc}} = 300 \text{ V}$, $V_{\text{ac,pp}} = 400 \text{ V}$. It can be clearly seen that the power losses strongly decrease with device temperature, which was anticipated from the behavior of the ESR with respect to temperature as depicted earlier in Fig. 3. Increasing the temperature to 90 °C, decreases the peak power loss density by a factor of 0.38 to 3.42 W/cm^3 .

In order to directly compare the performance of both capacitors in a realistic active power decoupling application, the buffer capacitor operating point presented in [1] is studied. The buck-type PPB presented in [1] is equipped with a 150 μF buffer capacitor. The buffer capacitor is operated with a dc bias of 300 V and a superimposed ac voltage with 130 V_{pp} amplitude. The steady-state temperature at rated power of the converter dimensioned in [1] is close to 60 °C. Considering the experimental results in Fig. 8, the X6S MLCC features a capacitance density of 8.4 $\mu\text{F}/\text{cm}^3$, as opposed to the slightly higher 9.5 $\mu\text{F}/\text{cm}^3$ of the CeraLink. The loss density of the X6S MLCC at the considered operating point amounts to just 56 mW/cm^3 . By contrast, the CeraLink dissipates 1.15 W/cm^3 in the very same operating point, which would reduce to 0.6 W/cm^3 if a device temperature of 90 °C would be feasible. It can be concluded, that although the CeraLink features a higher capacitance density, the power losses caused by the 120 Hz voltage ripple are much higher than those of the X6S MLCC.

V. POLYNOMIAL FIT TO EXPERIMENTAL DATA

In order to make the large-signal characterization of the ceramic capacitors available to the interested reader, a polynomial fit to the experimental data is provided. For a given dc bias voltage V_{dc} , a 3rd order polynomial in V_{ac} is fitted to the experimental capacitance and loss density data. The coefficients of the polynomials

$$c_{\text{er}}(\tilde{v}_{\text{ac}}) \Big|_{V_{\text{dc}}} = p_0 + p_1 \cdot \tilde{v}_{\text{ac}} + p_2 \cdot \tilde{v}_{\text{ac}}^2 + p_3 \cdot \tilde{v}_{\text{ac}}^3, \quad (7)$$

$$p(\tilde{v}_{\text{ac}}) \Big|_{V_{\text{dc}}} = p_0 + p_1 \cdot \tilde{v}_{\text{ac}} + p_2 \cdot \tilde{v}_{\text{ac}}^2 + p_3 \cdot \tilde{v}_{\text{ac}}^3, \quad (8)$$

are listed in Tab. III for 60 °C and 90 °C operating temperature. For the sake of brevity of this manuscript, the coefficients at 30 °C operating temperature are omitted. In order to obtain well conditioned polynomials, the peak to peak ac amplitude is normalized with 400 V,

$$\tilde{v}_{\text{ac}} = V_{\text{ac,pp}}/400 \text{ V}.$$

Note that the physical unit of the polynomials are $[c] = \mu\text{F}/\text{cm}^3$, $[p] = \text{W}/\text{cm}^3$. The quality of the polynomial fits are indicated by means of the statistical measures R^2 and RMSE in Tab. III. In order to obtain a finer resolution in direction of V_{dc} , interpolation can be performed between the polynomials obtained from adjacent V_{dc} entries in Tab. III. In order to prevent possible negative losses to result from the polynomial (8) at very low ac amplitude, $\tilde{v}_{\text{ac,pp}}$ should only be chosen in the interval $[0.1, 1]$.

In the following it is exemplified how to use the provided data to dimension a buffer capacitor and estimate the losses. From a circuit simulation or an analytical calculation it is known that if 100 μF are installed and a dc bias of $V_{\text{dc}} = 250 \text{ V}$ is maintained, a double line-frequency ac ripple of 200 V_{pp} results. Due to the imposed operating temperature of 60 °C and the relatively low double line-frequency, the CeraLink's performance potential can not be fully exploited, therefore it was decided to realize the buffer capacitor with X6S MLCCs in this example. From Fig. 8 and Fig. 9 or

from equation (7)-(8) with the coefficients in Tab. III, the prevailing capacitance and loss density of the X6S MLCC in the given operating point turns out to be $9.6 \mu\text{F}/\text{cm}^3$ and $0.4 \text{W}/\text{cm}^3$, respectively. Given the volume of a single X6S chip (cf. Tab. I), the prevailing capacitance per chip is $9.6 \mu\text{F}/\text{cm}^3 \times 0.07 \text{cm}^3 = 0.67 \mu\text{F}$. Thus, in order to actually realize the needed $100 \mu\text{F}$, $\lceil 100 \mu\text{F}/0.67 \mu\text{F} \rceil = 150$ X6S chips must be mounted in parallel. Given the loss density, the total power loss of the buffer capacitor during operation is $0.4 \mu\text{F}/\text{cm}^3 \times 0.07 \text{cm}^3 \times 150 = 4.2 \text{W}$.

VI. CONCLUSION

In single-phase high power density converter systems, active auxiliary circuits (PPBs) are installed to mitigate the double line-frequency voltage ripple at the dc link. The employed auxiliary converters feature a dedicated buffer capacitor which is operated with a large voltage swing superimposed to a constant dc bias. Because of their high energy density, TDK's X6S MLCC and CeraLink capacitors

were identified to be the most promising candidates for realizing an ultra compact PPB. The prevailing capacitance of these two types of ceramics, BaTiO₃ and PLZT, strongly depends on the operating point, that is dc bias voltage and superimposed large-signal amplitude, double line-frequency ac voltage. In Section II the basic properties of both capacitor technologies were compared. Despite the fact that the CeraLink was developed to be primarily used as dc link snubber, and thus was optimized to feature a very low ESR at high frequency, high capacitance at dc link voltage levels and a high current capability, it was chosen as a candidate for a power pulsation buffer.

In this particular case, the ESR of the CeraLink at double line-frequency is significantly larger than that of the X6S MLCC. Class II ceramics, BaTiO₃ in case of the X6S, exhibit a reduction in capacitance with increase in bias voltage. By contrast, the PLZT ceramic used in the CeraLink exhibits an increase in capacitance with applied dc voltage. Besides the dc bias, also the applied ac voltage affects the actual available capacitance of both ceramic capacitors.

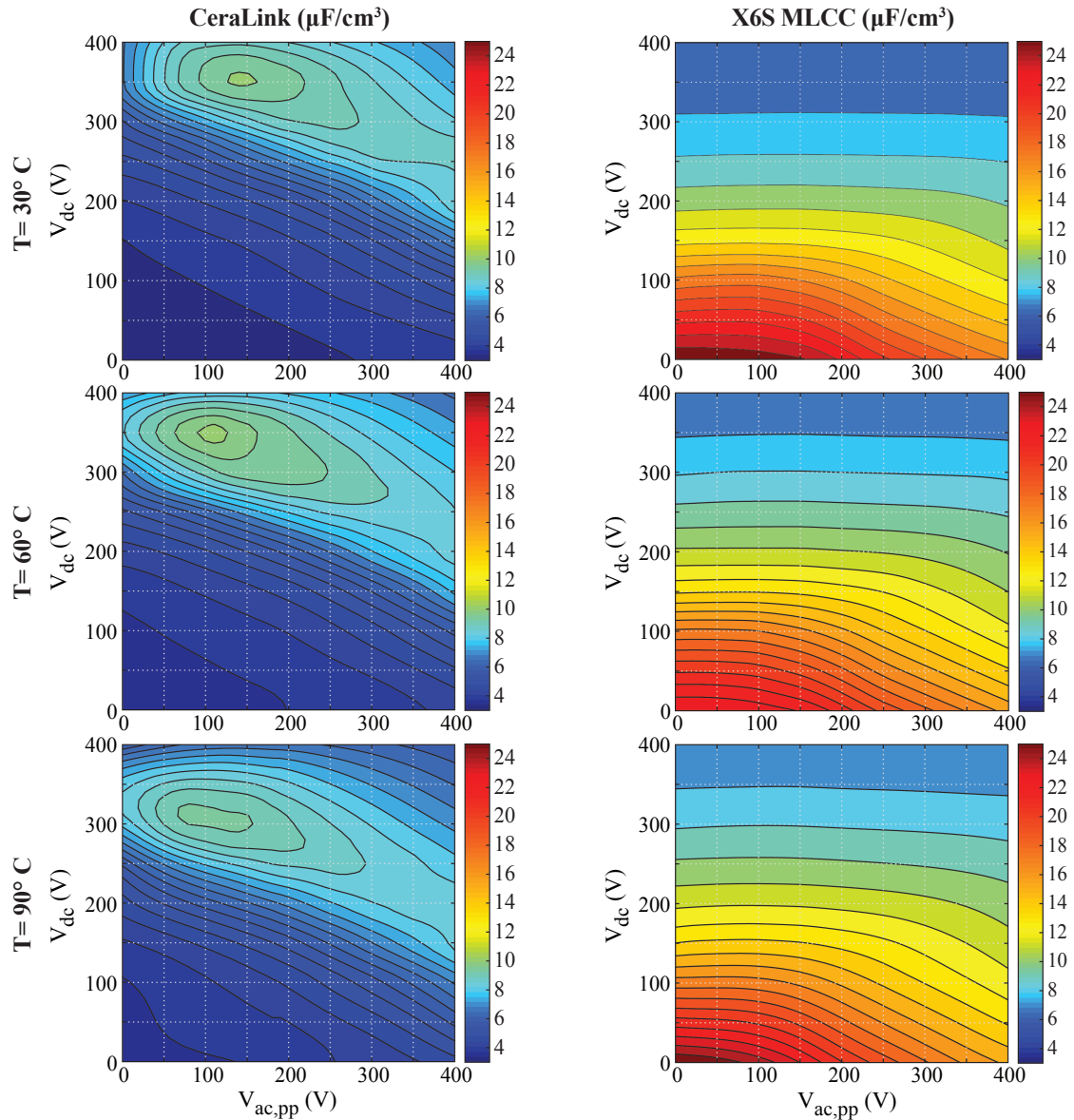


Fig. 8. Contour plot of capacitance density with respect to dc bias V_{dc} and 120Hz ac excitation $V_{ac,pp}$ at 30 °C, 60 °C and 90 °C operating temperature.

In order to accurately dimension a buffer capacitor in practice, the large-signal performance of the X6S MLCC and CeraLink was experimentally determined in this paper. Both the energy related capacitance density and the power loss density with respect to applied dc bias and superimposed ac voltage was determined for 30 °C, 60 °C and 90 °C operating temperature. The coefficients of 3rd order polynomials fitted to the measured performance data are provided, allowing design engineers to dimension buffer capacitors in practice. Direct comparison at a typical operating point occurring in a PPB application revealed that the capacitance density of the CeraLink is just slightly higher compared to the X6S MLCC, while the power losses associated with the double line-frequency voltage ripple are significantly higher in case of the CeraLink (factor 10 higher at 90 °C). Based on the measured large-signal performance, the X6S MLCC is the preferred choice in 400 V PPB applications if the operating temperature is < 105 °C and frequencies are kept low. It should be pointed out again, that the CeraLink has been developed particularly for applications with frequencies higher than

several 10 kHz and was never intended to be used for low-frequency power pulsation buffering. However, due to the maximum rated temperature of 125 °C and the strong improvement of performance with temperature, the CeraLink might be the preferred choice in PPB applications with high ambient temperatures (f. i. > 85 °C), if a very high power density is demanded.

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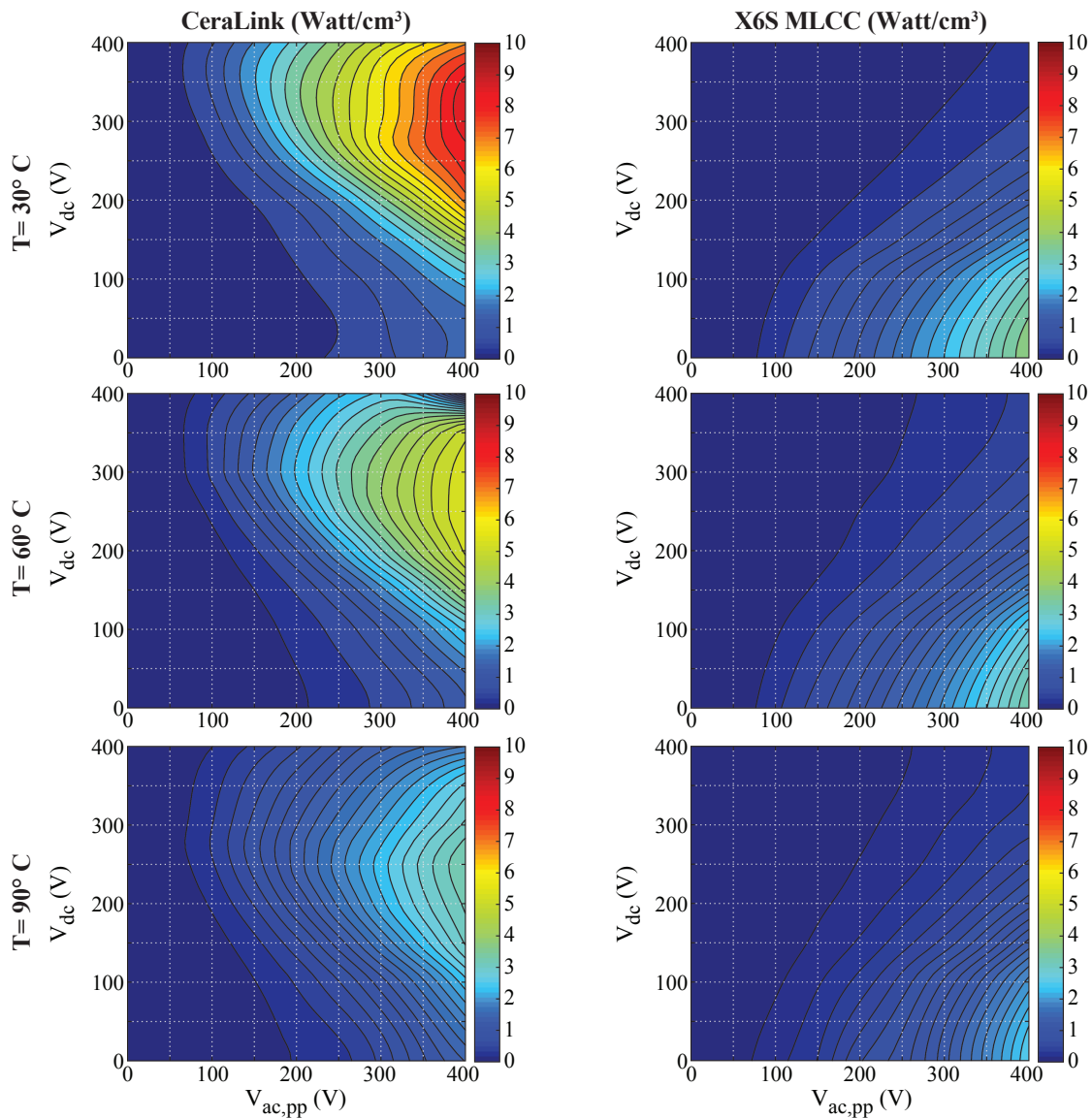


Fig. 9. Contour plot of loss density with respect to dc bias V_{dc} and 120 Hz ac excitation $V_{ac,pp}$ at 30 °C, 60 °C and 90 °C operating temperature.

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TABLE III

3RD ORDER POLYNOMIAL FIT TO MEASURED CAPACITANCE AND LOSS DENSITY ($\mu\text{F}/\text{cm}^3$) DATA AT 60 °C AND 90 °C OPERATING TEMPERATURE FOR DIFFERENT DC BIAS VOLTAGES.

	V_{dc}	CeraLink						X6S MLCC						
		p_0	p_1	p_2	p_3	R^2	RMSE	p_0	p_1	p_2	p_3	R^2	RMSE	
60 °C	Cap. Density ($\mu\text{F}/\text{cm}^3$)	0	3.50	0.94	-1.26	1.21	1.000	0.013	23.11	8.82	-34.62	19.14	1.000	-
	100	3.70	1.22	-1.50	2.67	1.000	0.010	17.31	4.68	-21.72	12.19	1.000	0.044	
	150	3.92	1.42	-0.74	3.21	1.000	0.018	13.54	2.14	-6.30	1.62	1.000	0.021	
	200	4.57	-0.28	9.20	-4.74	0.999	0.057	11.23	0.22	-0.13	-1.19	0.999	0.014	
	250	5.23	5.76	1.62	-4.10	0.996	0.094	9.60	0.27	-0.20	-0.49	0.995	0.020	
	275	5.91	11.26	-11.47	2.63	0.996	0.073	-	-	-	-	-	-	
	300	6.63	14.85	-22.56	9.09	0.998	0.041	8.35	0.40	-0.50	-0.04	0.968	0.023	
	350	8.36	12.52	-28.14	14.95	0.993	0.105	7.40	0.44	-0.87	0.40	0.966	0.008	
60 °C	Loss Density (W/cm^3)	0	-0.03	0.48	-0.72	1.69	1.000	0.027	-0.07	1.07	2.05	0.36	1.000	-
	100	-0.02	0.27	-0.32	2.77	1.000	0.009	-0.03	0.41	1.32	0.99	1.000	0.009	
	150	0.01	-0.12	1.05	3.36	1.000	0.010	-0.03	0.33	0.28	1.33	1.000	0.009	
	200	0.18	-2.88	11.70	-3.55	0.999	0.063	-0.06	0.48	-0.35	1.19	1.000	0.005	
	250	0.09	-2.35	16.28	-8.44	1.000	0.057	-0.01	0.16	0.10	0.59	0.999	0.012	
	275	-0.07	-0.18	12.94	-7.13	0.999	0.079	-	-	-	-	-	-	
	300	-0.19	1.80	9.00	-5.14	0.999	0.075	0.01	0.05	0.22	0.33	1.000	0.005	
	350	-0.15	1.73	7.92	-4.56	0.999	0.059	0.01	-0.10	0.58	-0.04	0.999	0.007	
90 °C	Cap. Density ($\mu\text{F}/\text{cm}^3$)	0	3.64	1.12	-1.07	1.30	0.998	0.064	26.01	-1.32	-24.40	15.75	0.999	0.152
	100	3.90	1.15	0.42	1.64	1.000	0.019	17.23	5.32	-22.64	12.76	1.000	0.054	
	150	4.33	0.56	5.33	-1.80	0.999	0.045	13.94	3.04	-8.97	3.29	1.000	0.013	
	200	5.06	2.74	5.92	-5.37	0.999	0.042	11.71	1.17	-2.67	0.25	1.000	0.008	
	250	5.94	10.75	-12.32	3.59	1.000	0.016	10.10	0.45	-0.99	-0.09	0.998	0.015	
	275	7.00	11.89	-19.34	8.08	0.996	0.051	-	-	-	-	-	-	
	300	8.02	9.81	-19.70	9.15	0.991	0.103	8.80	0.71	-1.62	0.70	0.994	0.011	
	350	8.02	6.91	-17.15	9.03	0.998	0.043	7.82	0.45	-1.03	0.46	0.993	0.007	
90 °C	Loss Density (W/cm^3)	0	0.08	-1.07	2.79	-0.42	0.993	0.151	-0.10	1.44	0.66	1.45	0.997	0.078
	100	0.02	-0.32	1.46	1.34	1.000	0.013	-0.01	0.17	1.67	1.03	1.000	0.008	
	150	0.09	-1.47	6.17	-1.63	1.000	0.031	-0.03	0.36	0.16	1.57	1.000	0.013	
	200	0.10	-1.80	10.05	-5.08	1.000	0.016	-0.02	0.28	0.02	1.10	1.000	0.009	
	250	-0.05	0.22	6.77	-3.51	1.000	0.030	-0.01	0.15	0.09	0.73	1.000	0.009	
	275	-0.07	0.84	5.19	-2.65	1.000	0.031	-	-	-	-	-	-	
	300	-0.09	0.97	4.37	-2.14	1.000	0.028	0.01	-0.05	0.56	0.17	1.000	0.006	
	350	-0.04	0.45	4.24	-1.96	1.000	0.020	0.02	0.24	-0.35	0.64	0.999	0.006	