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Design Aspects of Three-Phase Current-Source Converter Commutation Cells with Monolithic Bidirectional GaN Transistors

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***Abstract*—The recent availability of novel monolithic bidirectional GaN switches (MBDSs) renders current-source converters (CSCs) with their inherently sinusoidal output voltages an interesting alternative to voltage-source converters (VSCs) for future motor-friendly variable-speed drives (VSDs). However, CSC commutation cells contain three MBDSs and hence obtaining low-inductance and symmetric PCB layouts is more challenging. Furthermore, CSCs employing MBDSs require special multi-step commutation sequences that rely on current-direction and/or voltage-polarity information. In this paper, we provide an overview of these challenges, and, employing Ansys Q3D simulations, comparatively evaluate CSC commutation cell PCB layouts with first-generation 600 V, 140 mΩ GaN MBDSs regarding commutation inductances and parasitic capacitances. Whereas clearly all available packages are optimized for VSC half-bridges, the identified CSC commutation cell layouts facilitate a compact realization of a full AC-AC VSD prototype (3D CAD model). Still, concepts such as PCB-embedding or chip-level integration of the MBDSs, gate drives, etc. could greatly benefit future high-performance CSC realizations, and ultimately lead to an intelligent power module (IPM) concept for CSCs.**

***Index Terms*—Current-source converter, monolithic bidirectional GaN transistor, commutation cell, commutation sequence, voltage-source converter.**

I. Introduction

Variable-speed drives (VSDs) with sinusoidal output voltages reduce harmonic motor losses and prevent issues arising from switched output voltages with, especially in case wide-bandgap (WBG) power semiconductors are used, high dv/dt values (reflections on motor cables and transient overvoltages, common-mode bearing currents, etc.). Voltage-source converters (VSCs, see Fig. 1a) achieve this with the integration of an output filter [1]. Alternatively, current-source converters (CSCs, see Fig. 1b) inherently feature continuous motor voltages. Because the higher switching frequencies enabled by WBG devices mitigate concerns regarding the physical size of the required DC-link inductors, in the last years CSCs have been increasingly considered also for VSDs with lower power ratings [2]–[8], and also for PFC rectifiers applications e.g. for EV chargers [9]. However, CSCs require switches with bipolar voltage blocking capability [2], i.e., advantageously an anti-series connection of *two* transistors, which is a significant structural drawback compared to VSCs regarding chip area usage. This drawback is removed by recently available first-generation GaN 600 V, 140 mΩ dual-gate monolithic bidirectional switches (MBDSs) [5], [10], which use the same chip region for blocking either voltage polarity (see Fig. 1c).

Furthermore, in contrast to a VSC's half-bridge (two-switch) commutation cell (see Fig. 1a), a CSC commutation cell involves *three* switches connected to a common switch-node and *three* (AC-side) capacitors (see Fig. 1b). This paper provides an overview of the implications on PCB layouts, commutation sequences, and the main fault scenarios. For example, CSC

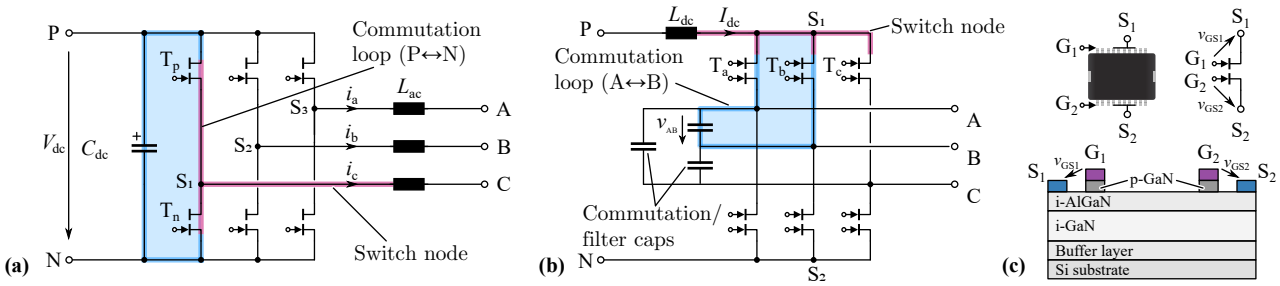

Fig. 1. Commutation loops (blue) and switch nodes (pink) of (a) a voltage-source converters (VSCs) and (b) current-source converters (CSCs). Note that the CSC's commutation cell consists of *three* transistors that are connected to a common switch node. (c) Cross section of a first-generation dual-gate monolithic bidirectional GaN transistor.

PCB layouts with discrete switches tend to be more intricate compared to half-bridge layouts for VSCs. Therefore, Section II discusses first a baseline CSC commutation cell hardware realization with available bottom-cooled MBDS samples, which is used to experimentally verify Quasi-static (QS) electromagnetic (EM) Ansys-Q3D-simulation-based estimations of the commutation loop inductances. Achievable improvements of CSC commutation cell layouts employing MBDSs with top-cooled packages can thus be quantified and compared to reference layouts of VSC half-bridge commutation cells. We then explore potential improvement vectors such as PCB integration and chip-level integration of gate drive circuitry and MBDSs in a common package, which could be considered for next-generation MBDS-based CSC commutation cell units. Similarly, whereas a VSC's commutation logic is relatively simple (interlock delay time between gate signals), CSCs employing MBDS require special multi-step commutation sequences, which depend on current-direction or voltage-polarity information; this is addressed in Section III. Finally, Section IV discusses the most important fault scenarios for CSC and VSC commutation cells, before the paper concludes with an outlook on two hardware prototypes of CSC-based and VSC-based AC-AC VSDs.

II. Commutation Cells

This section first discusses the structural differences between the CSC and VSC commutation cells and briefly touches on RRC gate drives for GaN gate-injection transistors (GITs). Then, based on measurements and Q3D simulations, commutation inductances, layout capacitances, and PCB area requirements of CSC commutation cells with bottom-cooled and top-cooled GaN MBDS samples are evaluated and compared to well-known VSC half-bridge layouts. Finally, we explore improvement vectors for future integrated CSC commutation cells.

A. Structural Differences of VSC and CSC Commutation Cells

The fundamental difference between three-phase VSC and CSC switching stages lies in the number of commutation cells and the number of switches per commutation cell. As shown in Fig. 1ab, a three-phase VSC consists of three commutation cells with two transistors each (i.e., three half-bridges) that thus form three switched voltage nodes. In contrast, the CSC consists of only two commutation cells with three transistors each, and thus two switched voltage nodes. The voltage at the switched node of a VSC switches between a constant DC-link voltage and zero (with respect to N), whereas the voltage of a CSC's switch node changes between the three phase voltages (v_A, v_B, v_C) with respect to an artificial output voltage star point. The CSC's switches are blocking the line-to-line AC voltages and thus must provide bipolar voltage blocking capability.

As in a VSC, any commutation of a CSC directly involves two transistors, **and all three** AC-side capacitors (in Fig. 1b, only the current path over the capacitor mainly involved in the current commutation is highlighted with the capacitors connected in delta configuration, which ultimately enables more compact commutation loops). Note that the commutation loop capacitors and external filter capacitors could also be arranged in star connection. In this case, a star point would directly be available for advantageous EMI filter realizations [10]. Note further that in grid-connected CSC stages, both, the filter capacitors and the commutation capacitors must be safety-certified (Class-X), as they are exposed to the grid voltage.

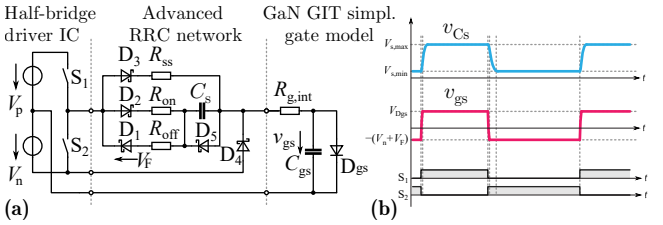

Fig. 2. (a) Employed RRC gate drive, which is based on [11] and (b) exemplary key waveforms [12]. The advanced RRC network ensures a fixed negative gate voltage in the off-state and duty-cycle independent switching behavior.

In a VSC, each half-bridge can be equipped with its own commutation capacitor, and hence all three commutation loops can be made equal. The three switches connected to a common switch node in the CSC, however, result in three overlapping commutation loops (per CSC commutation cell), and hence challenges in obtaining a symmetric layout (three equal commutation loop inductances), see Section II-C below. Furthermore, even though also in a CSC only two switches are actively involved in a given commutation, the voltage across the third switch connected to the common switch note changes as well. First, the resulting charging currents incur additional C_{oss} switching losses in the hard-turned-on switch [5], similar to three-level T-type brige-legs [13]. Second, it is in general[1] desirable to permanently tie the gate of the third switch to a negative bias voltage, thereby mitigating the risk for parasitic turn-on. For the considered GaN gate-injection transistors (GITs), this can be achieved with an extended RRC network as discussed in the following.

B. RRC Gate Drive for GaN Gate-Injection Transistors (GITs)

Standard MOSFETs have capacitive gates and thus draw gate current only during turn-on and turn-off transients. In contrast, GaN GITs (such as the available MBDS samples) show a diode-like behavior between gate and source and require a continuous gate input current of a few mA while in the on-state [15]. Therefore, a standard gate drive IC must be extended by a so-called RRC network[2] see, e.g., [11], [15]. The essential idea is to employ a series capacitor C_s that transiently provides a low-impedance path to charge/discharge the gate capacitance C_{gs}, and a parallel high-impedance path that supplies the small steady-state current required by the

[1]Note that certain FETs with a high-enough ratio C_{gs}/C_{gd} may be virtually immune against parasitic turn-on [14].

[2]Note that there are dedicated, integrated GaN GIT driver ICs; but typically these can only provide a negative bias during a (half-bridge) commutation and not continuously as is desirable in a CSC due to the third turned-off switch across which the blocking voltage is forced to change during any commutation between the other two switches.

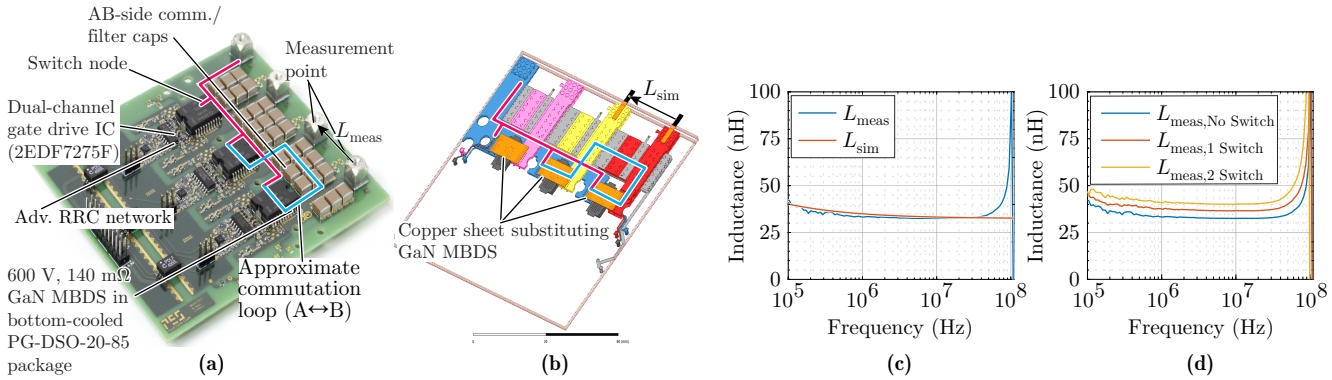

Fig. 3. (a) PCB containing one commutation cell of a CSC with bottom-cooled first-generation 600 V,140 mΩ GaN MBDSs and (b) Q3D simulation of the PCB from (a), whereby the switches are replaced by copper foils. (c) Comparison of simulated and measured inductances between the indicated measurement points, demonstrating a good matching between simulation and measurement. (d) Measured contribution of the switch packages to the commutation loop inductance (the copper foil used before is substituted by actual switches).

GIT in the on-state. To ensure a fixed negative gate bias in the off-state, and to eliminate the duty-cycle dependent transient behavior observed with standard RRC networks, we employ the circuit shown in Fig. 2, which is closely based on the approach proposed in [11]. During the turn-on transition, the gate current is supplied via R_{on} and C_s and since $R_{on} << R_{ss}$ the gate voltage quickly rises with a time constant of $\tau \approx R_{on}C_{gs}$ until the GIT's gate diode clamps at V_{Dgs}. The voltage across the series capacitor increases to $v_{Cs} = V_{s,max} = V_p - V_{Dgs}$. During turn-off, the gate voltage quickly reduces to $-(V_n + V_F)$ (V_F is the forward-voltage drop of the Schottky diodes employed in the gate drive network) via C_s and R_{off} with a time constant of $\tau \approx R_{off}C_{gs}$ until D_4 clamps the gate to the negative supply voltage. Furthermore, D_4 provides a fast discharge path for C_s via D_1 and R_{off}, such that v_{Cs} quickly reaches (almost) zero. Note that without the extension of the RRC network by the additional diode D_4, the voltage across the gate in the off-state would depend on v_{Cs}, which would slowly discharge via D_1, D_3 and R_{ss}. Thus, the gate voltage could ultimately increase to zero (i.e., the desired negative gate bias would be lost), and the initial conditions for the next turn-on would inherently depend on the duty cycle.

C. CSC Commutation Cell Layout

This section comparatively evaluates the commutation loop inductances of CSC commutation cell layouts employing first-generation 600 V, 140 mΩ GaN MBDSs [5], [16], which come in DSO-20-85 (bottom-cooled) or DSO-20-87 (top-cooled) packages.

Since a CSC commutation cell contains three switches and thus three commutation loops (see Section II-A), it is challenging to achieve a symmetric layout having equal commutation inductances between all three phases. Symmetric arrangements would place the three switches in a star or delta configuration [17]. However, at least considering the given discrete packages, such arrangements result in high PCB area usage, e.g., because of the necessity to separate the low-voltage side and the high-voltage side of the gate driver circuitries.

Considering in a first step the 600 V, 140 mΩ bottom-cooled GaN MBDS samples, a characterization PCB containing one CSC commutation cell has been realized (see Fig. 3a) to verify their switching performance [5] with the conceptual layout arrangement shown in Fig. 4a (with the commutation capacitors configured in a star arrangement). To evaluate the commutation loop inductances L_{comm} of other configurations, e.g., with top-cooled devices, the quasi-static (QS) electromagnetic (EM) simulation tool *Ansys Q3D* is used. Thus, first, the accuracy of the simulation setup is verified against measurements using the said prototype PCB. Since the internal structure of the novel GaN MBDSs is not known (and therefore, cannot be modeled in the simulation), the GaN devices were substituted by a copper sheet during measurement and simulation (see Fig. 3b). We compare the measured (with a Keysight 4294A precision impedance analyzer) and simulated inductances of the BC loop, considering the measurement terminals at the edge of the PCB as marked in Fig. 3a. These points were chosen for the verification of the simulation due to the good repeatability of the setup in the simulation environment. Fig. 3c demonstrates a precise matching between the measured and simulated inductances. The resonance of the PCB that is observed in the measurement is not modeled in Ansys Q3D due to known difficulties of modeling high frequency effects [18]. Further, the contribution of the DSO-20-85 package to the total commutation loop inductance was evaluated by measuring the PCB inductance between the same measurement points (marked in Fig. 3a) while substituting the copper sheets used in the earlier measurement with the (turned-on) switches. Fig. 3d shows the comparison of the measured PCB inductance with both the switches short-circuited by copper sheet, with one switch present, and with both the switches present. The contribution of the two DSO-20-85 packages is found to be around 8 nH (i.e., about 4 nH per package).

With the simulation setup successfully verified, further layout options for the CSC commutation cell can be evaluated. Note that the main purpose of the simulation is a comparative study between different layout options rather than the accurate extraction of frequency dependent EM models of the PCB layouts (this would require detailed internal models of the switch packages). As the baseline option, the CSC commutation cell with MBDSs in bottom-cooled DSO-20-85 packages

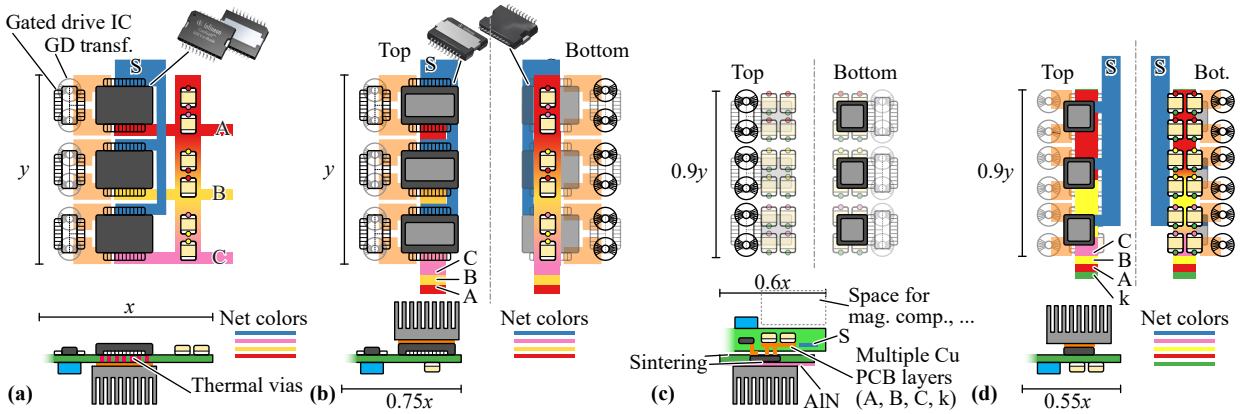

Fig. 4. Conceptual illustrations of exemplary CSC commutation cell layouts (see Fig. 1b) and improvement vectors. Note that all variants feature commutation caps arranged in delta configuration (see Fig. 1b). (a) Existing first-generation 600 V, 140 mΩ GaN MBDS with bottom-cooled package (PCB area ≈ 20 cm^2). (b) An otherwise identical but top-cooled package facilitates a more compact realization (PCB area ≈ 15 cm^2), largely vertical commutation loops, and improved cooling. (c) PCB-embedding of pre-packaged switches (package size estimated from IGLD60R070D1) and other low-height electronics (gate drive ICs, commutation capacitors) as proposed in [19] enables compact 3D-stacked realizations (PCB area ≈ 11 cm^2). (d) Integration of gate drive and MBDS in a common package (package size estimated from the integrated half-bridge IGI60F1414A1L) simplifies design and layout (PCB area ≈ 10 cm^2) (k denominates a commutation and/or filter capacitor star point available in case of star connection).

(see Fig. 4a and Fig. 5a) was considered; the commutation capacitors are connected in delta arrangement (see Fig. 1b). The thermal vias needed below the bottom-cooled DSO-20-85 package force a mostly lateral commutation loop and therefore relatively large commutation loop inductances result (see Table I; the inductances are extracted for a broad frequency range as, e.g., in Fig. 3c, but the table summarizes the values at 100 MHz). Note that there are two small loops (AB and BC) and one larger loop (AC), with a corresponding difference in the simulated inductances (17 nH vs. 21 nH, not including the packages[3]).

A clear improvement in terms of lower commutation loop inductance, lower thermal resistance[4], reduced PCB area usage (e.g., because of the possibility to place the commutation capacitors below the switches instead of next to them) can be achieved with MBDSs in a top-cooled (but otherwise identical) DSO-20-87 package. The conceptual arrangement of Fig. 4b shows a first layout option that aims at minimizing the overlap of the switch node and the phase layers (see Fig. 5b), i.e., minimizes the parasitic capacitance C_{par} of the PCB, which contributes to the hard-switching losses (in parallel to the switches' output capacitances C_{oss}). The resulting commutation loop is thus still partly lateral but much smaller, which is reflected by the simulation results from Table I (the simulated inductances of the small and of the large commutation loop reduce to 7.2 nH and 11 nH, respectively, not including the packages; without a significant increase of the parasitic capacitance, C_{par}). The parasitic capacitance C_{par} is obtained as the sum of the three capacitances between each phase and the switch node, which can be obtained with the Q3D CG solver (without placing the commutation capacitors on the simulated PCB).

The commutation inductance can be further reduced by accepting a larger overlap between switch node and phase layers (i.e., a higher parasitic capacitance C_{par}). The second layout option shown in Fig. 5c moves the switch node beneath the transistors, but still assigns all (inner) PCB layers to the switch node, i.e., there is no full overlap of switch-node and phase planes. This results in slight reduction of the commutation inductances to 6.9 nH and 9.5 nH, but in an increased parasitic capacitance of 33 pF. Finally, the third layout option of Fig. 5d fully overlaps the switch node plane with the phase planes, resulting in a fully vertical commutation loop and thus minimal and especially almost fully symmetric commutation inductances of 6.4 nH and 6.9 nH. However, the parasitic capacitance further increases to 68 pF due to significantly higher overlap of phase and switch-node planes. All in all, the layout option from Fig. 5b seems to provide the most favorable trade-off between commutation inductances (20 % to 50 % higher than that of an optimized half-bridge layout, see below) and parasitic capacitance.

D. VSC Commutation Cell Layout

Since the VSC commutation cell has only two switches (considering the top-cooled DSO-20-87 package), the commutation cell layout can be quite compact with a completely vertical commutation loop (see Fig. 6). Thus, a low commutation inductance of 4.6 nH is found (see Table I). Note further that the overlap of switch-node and the DC planes can be kept relatively small, i.e., C_{par} (7.8 pF) remains low even for a fully vertical commutation loop (see Table I). These results confirm that currently available packages are optimized for VSC half-bridge layouts and possibly a higher degree of integration would be required to achieve further improvements of CSC commutation cells.

[3]In the simulation, the switch is replaced with a copper sheet; the measured additional inductance contribution of the DSO-20-85 package has been measured at about 8 nH for two packages, see above, and we assume the same contribution for the top-cooled DSO-20-87 package.

[4]For the bottom-cooled package, the heat extraction through thermal vias in the PCB adds an extra contribution of $R_{\text{th,PCB}} \approx 2.8$ K/W which accordingly increases the total thermal resistance from junction to heatsink.

[5]All values are extracted from Ansys Q3D simulations for a broad frequency range; the table lists the represntative values at 100 MHz

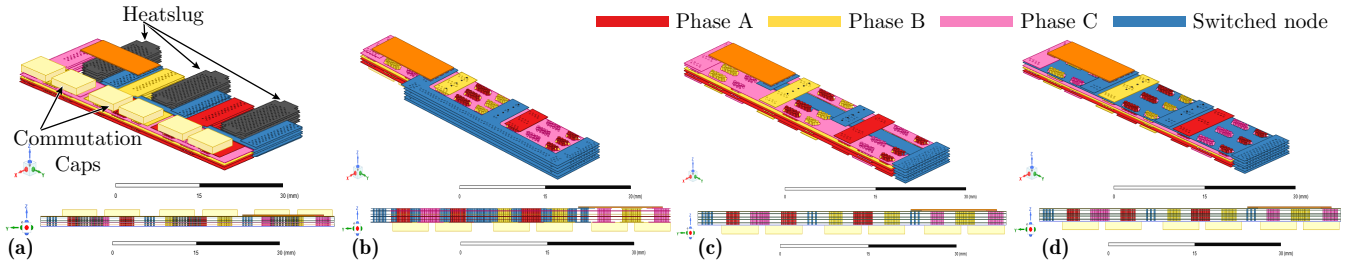

Fig. 5. Q3D layouts for CSC commutation cells with MBDSs in (a) bottom-cooled DSO-20-85 packages that force lateral commutation loops, and in top-cooled DSO-20-87 packages, considering three different variants, i.e., (b) laterally displaced switch-node to minimize the parasitic capacitance, (c) switch-node beneath the switches but without overlapping the phase planes, and (d) completely vertical layout arrangement of phase and switch-node connections.

TABLE I
COMMUTATION INDUCTANCES WITHOUT (L_{PCB}) AND WITH (L_{comm}) THE MEASURED CONTRIBUTION OF THE PACKAGES (+8 nH FOR TWO SWITCHES), AND PARASITIC SWITCH-NODE CAPACITANCES OF THE CONSIDERED LAYOUTS[5]. BC: BOTTOM-COOLED PACKAGES, TC: TOP-COOLED PACKAGES.

			L_{PCB} (nH)	L_{comm} (nH)	Rel. (-)	C_{par} (pF)
CSC BC	Fig. 5a	BC	17.0	25.0	1.99	18
		AC	21.1	29.1	2.32	
CSC TC	Fig. 5b	BC	7.2	15.2	1.21	22
		AC	11.0	19.0	1.52	
	Fig. 5c	BC	6.9	14.9	1.19	33
		AC	9.5	17.5	1.40	
	Fig. 5d	BC	6.4	14.4	1.15	68
		AC	6.9	14.9	1.19	
VSC TC	Fig. 6ab	PN	4.6	12.6	1.00	7.8

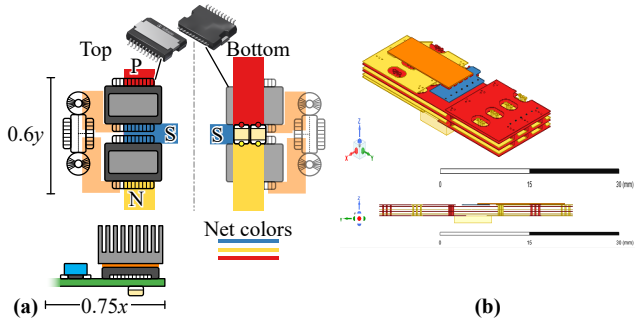

Fig. 6. (a) Conceptual illustration of a VSC half-bridge commutation cell and (b) Q3D layout used for the simulations.

E. Improvement Vectors

The dual-gate GaN MBDS devices are four terminal common-drain devices with two source and two gate terminals (see Fig. 1c). This implies the need for two separate isolated gate driver ICs (or one dual-channel driver IC) and two isolated gate-drive power supplies per MBDS, which contributes significantly to the total required PCB area[6] of the commutation cell. Therefore, as suggested for example in [19], pre-packaged switches, gate drive ICs (and other components, e.g., gate drive power supply transformers [20] and commutation capacitors) could be embedded in PCBs, which are then joined by means of sintering techniques. Such 3D-stacking approaches enable more compact realizations, especially because the additional space on the bare top surface of the PCB can be utilized for additional components (see Fig. 4c). However, whereas corresponding manufacturing processes do exist [19], they involve several additional and non-standard steps compared to conventional PCB production lines. Furthermore, circuit debugging may become challenging due to limited accessibility of the embedded components.

Alternatively, (chip-level, monolithic) integration of gate-driver, switches, and even sensing elements and protection functionality, which has been demonstrated for GaN transistors and half-bridge power ICs [21]–[23], could be considered (see Fig. 4d). Even if the isolated gate drive power supply might not be included on-chip or in the package, it could reside on a second, stacked PCB, and facilitate more flexible layouts of the power stage, e.g., aiming for a symmetric commutation cell layout (e.g., star or delta arrangements of the commutation cell's three switches as suggested in [17] for SiC power modules) without sacrificing extra PCB area. Such far-reaching integration concepts, i.e., intelligent power module (IPM) approaches for CSC commutation cells, could enable significantly more compact, and possibly fully symmetric, CSC commutation cells in the future.

[6]Considering a CSC commutation cell layout as in Fig. 4b, the gate-drive circuits including the RRC networks and the isolated power supplies occupy almost the same area (7.5 cm^2) as the switches (8.6 cm^2).

III. Commutation Sequences

The structural differences of VSC and CSC commutation cells also necessitate different commutation sequences to ensure safe operation. These are briefly outlined in the following.

To prevent a short-circuit of the DC-link during the commutation of a VSC bridge-leg, it is necessary to insert an interlock delay time t_{IL} between the turn-off and turn-on gate signals as shown in Fig. 7. Note that the sequence of the applied gate signals is fixed and independent of the switched current direction. As a result, the applied voltage at the switch node during the interlock delay time depends on the current direction (and, to a lesser extent, on the current magnitude), i.e., voltage time area errors $\Delta v \cdot t$ occur. These distortions may eventually degrade the THD of the output current, which can, however, be mitigated by accounting for t_{IL} in the duty cycle calculation based on the feed-forward (and/or measured) current direction, i.e., by compensating t_{IL} [24].

In contrast, during the commutation of the DC-link current between any two of the three phases of a CSC commutation cell, *two* conditions must be fulfilled at all times:

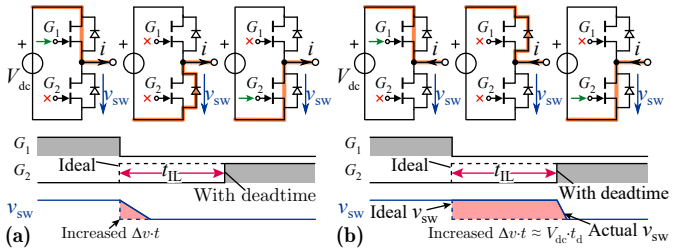

Fig. 7. Impact of the interlock delay time t_{IL} on the effective switch node voltage v_{sw} of a VSC commutation cell during a commutation P → N for (a) positive output current i, where the voltage-time area error $\Delta v \cdot t$ depends on the current magnitude (soft-switched transition), and (b) for negative output current i, where the voltage-time area error is mostly defined by t_{IL} (hard-switched transition).

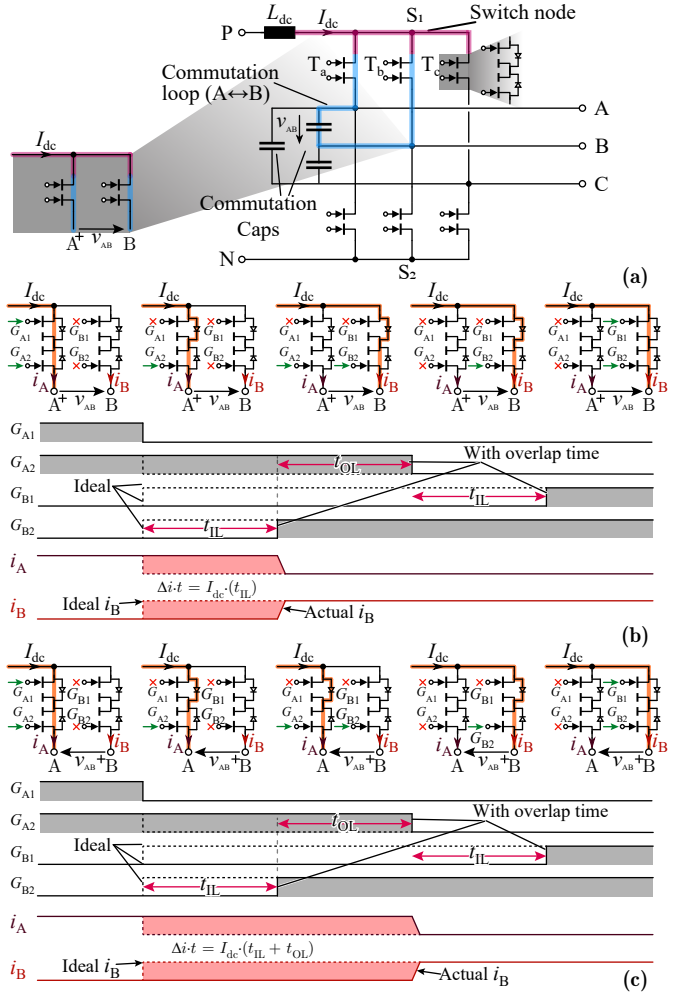

Fig. 8. Current-direction-based four-step commutation sequence of a CSC commutation cell for a current commutation from A → B. (a) Overview schematic and inner equivalent circuit of the MBDS (common-drain connection of two transistors). The time of the actual current commutation depends on the polarity of the involved line-to-line voltage, i.e., (b) $v_{ab} > 0$ (hard-switched transition) or (c) $v_{ab} < 0$ (soft-switched transition). The time intervals t_{IL} (interlock delay time as in a VSC) prevent a short-circuit of the AC-side commutation capacitors, and the time interval t_{OL} (overlap time) is needed to ensure the continuous availability of a path for the DC-link current. The commutation sequence results in current-time area errors $\Delta i \cdot t$ that depend on the voltage polarity.

- At least one device in the commutation loop must be capable of blocking the involved line-to-line voltage to prevent a short circuit of the AC-side capacitors (see Fig. 8a); note that in contrast to a VSC, the commutation voltage can have either polarity.
- There must always be a conduction path for the DC-link current I_{dc}.

This is possible with either voltage-polarity-dependent (considering the line-to-line voltage involved in the commutation) or current-direction-dependent multi-step commutation sequences, which have been previously described in literature [4], [25].[7] Since CSCs typically operate with a fixed current direction (but inherently with bipolar commutation voltages), it may be advantageous to consider current-direction-dependent commutation sequences, as it is then in principle possible to always employ the same commutation sequence.[8] Thus, Fig. 8bc show the current-direction-dependent four-step commutation sequence for a fixed direction of the current I_{dc}, and the resulting behavior for the two polarities of the voltage v_{AB}, respectively. The four-step commutation sequence modifies the four gate signals of the two involved dual-gate MBDSs with two types of delays: an interlock delay time t_{IL}, which, as in a VSC half-bridge, is responsible for avoiding a short-circuit of the AC-side capacitors, and an overlap delay time t_{OL} that ensures the continuous availability of a current flow path for I_{dc}. As a consequence of the required commutation sequences, differences in the applied current time areas at the phase terminals appear, which depend on the polarity of the switched line-to-line voltage. Considering Fig. 8bc, there is a constant part (the first t_{IL} delay that is present independent of the voltage polarity), which can easily be accounted for in the duty cycle generation. The remaining distortion then originates from the overlap delay time, but could be compensated based on the feed-forward (and/or measured) voltage polarity information, i.e., similar as in a VSC.

As the described four-step commutation sequence is valid only for a given DC-link current direction, a restriction on the allowed DC-link current ripple and/or the minimum average DC-link current arises, i.e., these values must be selected such that a (even temporary) change of the current direction is not possible (otherwise one of the two above-mentioned conditions would be violated, with potentially fatal consequences for the semiconductors). This is specifically relevant at low-load conditions where it is advantageous to reduce the DC-link current for efficiency reasons. There are basically three options to meet this challenge: (1) Limit I_{dc} to a minimum value that is sufficiently higher than the worst-case current ripple amplitude, which, however reduces the low-load efficiency of the system; (2) employ voltage-polarity-dependent commutation sequences [4], [25] for low-load operation; or (3) operate the

[7]Note that direct matrix converters essentially consist of three CSC commutation cells, and hence the same conditions apply for their commutation sequences. Therefore, various options for such multi-step commutation sequences have been proposed since the 1980s, and are summarized in [25].

[8]Note, however, that the two commutation cells in a three-phase inverter or rectifier see *different* current directions, i.e., must employ different commutation sequences.

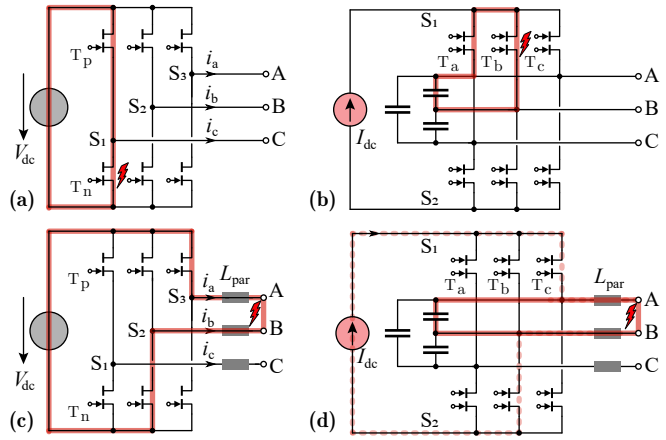

Fig. 9. Internal short-circuit faults in (a) VSC and (b) CSC commutation cells, and external short-circuit faults at the converter terminals again for (c) VSC and (d) CSC. L_{par} represents the parasitic inductance from the terminals and connections.

CSC in the discontinuous conduction mode (DCM) (one of the gates of MBDS is turned-off, making the switch operate in an anti-series connection of switch and diode ensuring only unidirectional flow of current), either with adapted space-vector modulation schemes [26], [27] or based on charge control, which inherently allows a seamless transition into DCM [28].

IV. Fault Scenarios

Finally, the most important fault scenarios for CSC and VSC commutation cells will be discussed.

A. Short-Circuit Faults

In a VSC, bridge-leg short circuits (see Fig. 9a) can occur due to, e.g., parasitic turn-on, insufficient interlock delay t_{IL} or device failures, whereby the DC-link capacitor feeds energy into the fault. Earlier, the bipolar voltage blocking capability required by switches in CSCs was typically realized by a series connection of a transistor and a diode. In such a configuration, the likelihood of failures is much lower, as any possible short-circuit path, regardless of the voltage polarity, always comprises a robust diode. However, when modern MBDSs are employed, identical short-circuit events as discussed above for VSCs can occur, see Fig. 9b, with the AC-side commutation/filter capacitors serving as the energy reservoir. Thus, the same protection concepts should be implemented in CSC and VSC commutation cells. Recently, approaches to overcurrent protection of GaN transistors based on the desaturation detection concept [29] or relying on sensing of the gate-source voltage [30] have been analyzed, amongst others.

In contrast, low-impedance faults at the AC-side terminals affect VSCs and CSCs differently. In a VSC, the fault current path involves two transistors (see Fig. 9c), i.e., if the fault impedance is small, similar conditions as during a bridge-leg short circuit arise. In case of a CSC, a fault at the terminals can only lead to a high current in the AC-side commutation and filter capacitors (see Fig. 9d); the transistors are not part of the fault current path and the switching stage would be capable of feeding the fault with a limited current once the energy stored in the capacitors has been dissipated into the fault (note that this cannot be prevented, as no switching element is in that path). Thus, to be robust against this type of faults, a VSC needs fast-acting overcurrent protection of the transistors, whereas the CSC does not.

B. Open-Circuit Faults

A typical, simple trip reaction to the detection of any fault in a converter is to turn-off all switching devices. In a VSC, the current impressed by the AC-side inductors then always finds a path through either of the two diodes in a bridge-leg. However, due to the bipolar voltage/current blocking capability of the switches employed in CSC commutation cells, situations where there is no path for the impressed DC-link current may arise, e.g., if all transistors are turned-off instantly, or in case of a wrongly selected current-direction-dependent multi-step commutation sequence. The impressed DC-link current would then quickly charge the small output capacitances of the switches, leading to destructive overvoltages.[9] Therefore, CSCs (and also matrix converters that face the same challenge) are often equipped with overvoltage protection circuits, such as described, e.g., in [31]–[33], which essentially divert the energy stored in the DC-link inductor into a capacitive buffer equipped with a dissipation element, thus clamping the overvoltage and protecting the switches.

V. Conclusion

Available samples of first-generation 600 V, 140 mΩ GaN monolithic bidirectional switches (MBDSs) pave the way for competitive current-source converter (CSC) realizations. In this paper, we provide an overview of the conceptual differences, i.e., regarding the circuit structure, commutation sequences, and fault scenarios, between CSC commutation cells (employing the dual-gate GaN MBDSs) and well-known half-bridge commutation cells used in voltage-source converters (VSCs) (employing GaN transistors as well). Using Ansys Q3D simulations (experimentally verified for one example), we evaluate various layout options for CSC commutation cells with GaN MBDSs in both, bottom-cooled and top-cooled packages. In general, about 20 % to 50 % higher commutation loop inductances (compared to half-bridge VSC layouts) and asymmetries among the three commutation loops are difficult to avoid, unless a relatively large additional parasitic switch-node capacitance would be accepted. The analyzed VSC and CSC (variant shown in Fig. 4b) commutation cells are being implemented in full hardware demonstrators of all-GaN 1.4 kW, 200 V (line-to-line rms) AC-AC variable-speed drives. Design details can be found in [10] and Fig. 10 shows the 3D CAD renderings and volume breakdowns of the converter prototypes. All in all, even though suitable layouts for CSC commutation cells based on available GaN MBDS samples have been identified, we believe that CSCs could strongly benefit from further integration, e.g., of MBDSs, gate drives,

[9]Note that this implies that the trip reaction of a CSC must ideally follow a sequence of steps to bring the converter into a safe state.

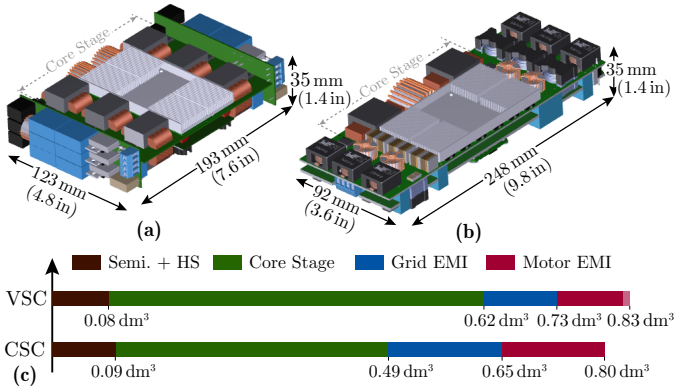

Fig. 10. 3D CAD renderings of all-GaN 1.4 kW, 200 V (line-to-line rms) AC-AC VSD prototypes with 97 % target efficiency at nominal load, using (a) VSC (power density $\rho \approx 1.7\,\mathrm{kW/dm^3}$) and (b) CSC ($\rho \approx 1.8\,\mathrm{kW/dm^3}$) topologies, the latter employing 600 V, 140 mΩ GaN MBDSs. (c) Volume breakdowns. Both systems feature full EMI filters towards the grid and towards the motor; design details are given in [10].

possibly sensing circuitry, etc. into the switch packages or even monolithically on-chip. Such efforts could ultimately aim for an intelligent power module (IPM) for high-performance, highly compact CSCs.

References

[1] K. Shirabe, M. M. Swamy, J.-K. Kang, M. Hisatsune, Y. Wu, D. Kebort, and J. Honea, "Efficiency comparison between Si-IGBT-based drive and GaN-based drive," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 566–572, Jan. 2014.

[2] T. Friedli, S. D. Round, D. Hassler, and J. W. Kolar, "Design and performance of a 200-kHz All-SiC JFET current DC-link back-to-back converter," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1868–1878, Sep. 2009.

[3] T. M. Jahns and B. Sarlioglu, "The incredible shrinking motor drive: Accelerating the transition to integrated motor drives," *IEEE Power Electron Mag.*, vol. 7, no. 3, pp. 18–27, Sep. 2020.

[4] R. Amorim Torres, H. Dai, W. Lee, B. Sarlioglu, and T. Jahns, "Current-source inverter integrated motor drives using dual-gate four-quadrant wide-bandgap power switches," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 5183–5198, Sep. 2021.

[5] N. Nain, D. Zhang, J. Huber, J. W. Kolar, K. K. Leong, and B. Pandya, "Synergetic control of three-phase AC-AC current-source converter employing monolithic bidirectional 600 V GaN transistors," in *Proc. 22nd IEEE Control Modeling Power Electron. Workshop (COMPEL)*, Cartagena, Colombia, Nov. 2021.

[6] M. Guacci, D. Zhang, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Three-phase two-third-PWM buck-boost current source inverter system employing dual-gate monolithic bidirectional GaN e-FETs," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 4, pp. 339–354, Dec. 2019.

[7] D.-T. Do, H. Cha, and F. Akbar, "Switching-cell four-leg current source inverter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10 349–10 359, Nov. 2021.

[8] H. Dai, R. A. Torres, J. Gossmann, W. Lee, T. M. Jahns, and B. Sarlioglu, "A seven-switch current-source inverter using wide bandgap dual-gate bidirectional switches," *IEEE Trans. Ind. Appl.*, vol. 58, no. 3, pp. 3721–3737, May 2022.

[9] D. Zhang, M. Guacci, M. Haider, D. Bortis, J. W. Kolar, and J. Everts, "Three-phase bidirectional buck-boost current DC-link EV battery charger featuring a wide output voltage range of 200 to 1000V," in *Proc. Energy Conversion Congr. Expo. (ECCE USA)*, Detroit, MI, USA, Oct. 2020, pp. 4555–4562.

[10] N. Nain, J. Huber, and J. W. Kolar, "Comparative evaluation of three-phase AC-AC voltage/current-source converter systems employing latest GaN power transistor technology," in *Proc. Int. Power Electron. Conf. (IPEC/ECCE Asia)*, Himeji, Japan, May 2022, pp. 1726–1733.

[11] D. Bortis, O. Knecht, D. Neumayr, and J. W. Kolar, "Comprehensive evaluation of GaN GIT in low- and high-frequency bridge leg applications," in *Proc. 8th IEEE Int. Power Electron. Motion Ctrl. Conf. (IPEMC/ECCE Asia)*, Hefei, China, May 2016, pp. 21–30.

[12] J. Huber, J. W. Kolar, N. Nain, and F. Vollmaier, "Experimental analysis of 1st gen. 600 V GaN M-BDSs," in *Pt. 4 of Tutorial on Emerging Bidirectional Switches presented at ECCE USA*, Vancouver, Canada, Oct. 2021.

[13] D. Cittanti, C. Gammeter, J. Huber, R. Bojoi, and J. W. Kolar, "A simplified hard-switching loss model for fast-switching three-level T-type SiC bridge-legs," *Electronics*, vol. 11, no. 11, p. 1686, Jan. 2022.

[14] D. Graovac, "Parasitic turn-on of power MOSFET – How to avoid it?" Dec. 2008, Infineon Technologies Application Note. [Online]. Available: https://tinyurl.com/mpbz9bw3

[15] D. Varajao and B. Zojer, "Gate drive solutions for CoolGaN 600V HEMTs," Dec. 2020, infineon Technologies White Paper. [Online]. Available: https://tinyurl.com/yh75wf8d

[16] B. Pandya, "600V GaN dual gate bidirectional switch," 2019, PowerAmerica Institute. [Online]. Available: https://tinyurl.com/2aumzc59

[17] L. G. Alves Rodrigues, "Design and characterization of a three-phase current source inverter using 1.7kV SiC power devices for photovoltaic applications," Ph.D. dissertation, Université Grenoble Alpes, Grenoble, France, 2019.

[18] I. Kovacevic-Badstuebner, D. Romano, G. Antonini, J. Ekman, and U. Grossner, "Broadband circuit-oriented electromagnetic modeling for power electronics: 3-D PEEC solver vs. RLCG-solver," *Energies*, vol. 14, no. 10, p. 2835, Jan. 2021.

[19] T. Li, C. Voigt, A. Lindemann, L. Boettcher, and E. Erhardt, "An embedded power section with GaN HEMTs," in *Proc. 12th IEEE Energy Conv. Congr. Expo. (ECCE Asia)*, Singapore, May 2021, pp. 26–31.

[20] B. Sun, R. Burgos, and D. Boroyevich, "Ultralow input–output capacitance PCB-embedded dual-output gate-drive power supply for 650 V GaN-based half-bridges," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1382–1393, Feb. 2019.

[21] R. Vartanian, D. Veereddy, and A. Medina-Garcia, "GaN based integrated power stages (IPS) for low power adapter/charger applications," in *Proc. Power Conversion and Intelligent Motion Conf. (PCIM)*, Nuremberg, Germany, May 2021.

[22] C. Kuring, M. Wolf, X. Geng, O. Hilt, J. Böcker, J. Würfl, and S. Dieckerhoff, "GaN-based multichip half-bridge power module integrated on high-voltage AlN ceramic substrate," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 11 896–11 910, Oct. 2022.

[23] J. Stevens, T. Ribarich, and S. Oliver, "Practical realization of GaN's capability: GaN Fast power ICs introduce lossless sensing and autonomous protection," *IEEE Power Electron Mag.*, vol. 9, no. 2, pp. 30–38, Jun. 2022.

[24] T. Sukegawa, K. Kamiyama, K. Mizuno, T. Matsui, and T. Okuyama, "Fully digital, vector-controlled PWM VSI-fed AC drives with an inverter dead-time compensation strategy," *IEEE Trans. Ind. Appl.*, vol. 27, no. 3, pp. 552–559, May 1991.

[25] J. W. Kolar, T. Friedli, J. Rodriguez, and P. W. Wheeler, "Review of three-phase PWM AC-AC converter topologies," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 4988–5006, Nov. 2011.

[26] B. Guo, F. Wang, R. Burgos, and E. Aeloiza, "Control of three-phase buck-type rectifier in discontinuous current mode," in *Proc. IEEE Energy Conv. Congr. Expo. (ECCE USA)*, Denver, CO, USA, Sep. 2013, pp. 4864–4871.

[27] D. Drews, R. Cuzner, and G. Venkataramanan, "Operation of current source inverters in discontinuous conduction mode," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4865–4877, Nov. 2016.

[28] D. Zhang, D. Cao, J. Huber, J. Everts, and J. W. Kolar, "Advanced synergetic charge control of three-phase PFC buck-boost current DC-link EV chargers," in *Proc. 23rd IEEE Control Modeling Power Electron. Workshop (COMPEL)*, Tel Aviv, Israel, Jun. 2022.

[29] R. Hou, J. Lu, Z. Quan, and Y. W. Li, "A simple desaturation-based protection circuit for GaN HEMT with ultrafast response," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6978–6987, Jun. 2021.

[30] E. A. Jones, P. Williford, and F. Wang, "A fast overcurrent protection scheme for GaN GITs," in *Proc. 5th IEEE Wide Bandgap Power Devices Appl. Workshop (WiPDA)*, Albuquerque, NM, USA, Oct. 2017, pp. 277–284.

[31] T. Ando, K. Nakamura, T. Mine, H. Inaba, T. Kurosawa, M. Nakazato, and Y. Sakai, "Current source power converting apparatus with overvoltage protection," U.S. Patent 4 884 182A, Nov. 28, 1989.

[32] B. Guo, F. Xu, F. Wang, L. M. Tolbert, and B. J. Blalock, "Overvoltage protection scheme for three-phase current source converter built with SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Fort Worth, TX, USA, Mar. 2014, pp. 3469–3476.

[33] L. A. L. d. A. C. Costa, B. Fan, R. Burgos, D. Boroyevich, W. Chen, and V. Blasko, "The fast overvoltage protection consideration and design for SiC-based matrix converters," *IEEE Trans. Ind. Appl.*, vol. 57, no. 6, pp. 6145–6154, Nov. 2021.