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***Abstract*—For Voltage Regulator Modules (VRM), integrating the power converter with the load in an advanced integration process is a method to deliver power at higher voltage levels, and thereby overcome the high supply current requirements predicted by the 2009 International Technology Roadmap for Semiconductors (ITRS). The most conventional converter type used is the buck or step-down converter. For this converter, the output inductor is recognized as the performance limiting component with respect to efficiency and area requirements. This paper details an inductor optimization procedure for Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC) applications. Targeting the highest possible efficiency for a specified area-related power density, the optimization procedure determines the best inductor dimensions given the buck converter operating conditions. The optimization procedure is verified using experimental data obtained from a PCB inductor realization. According to the results, the most favorable inductor achieves an efficiency of 94.5% and an area-related power density of $1.97\,\mathrm{W/mm^2}$ at a switching frequency of $170\,\mathrm{MHz}$.**

I. Introduction

From the 2009 International Technology Roadmap for Semiconductors (ITRS) [1], the supply voltage of deep sub-micron integrated circuits is expected to decrease from around $1.0\,\mathrm{V}$ in 2009 to around $0.6\,\mathrm{V}$ in 2025. However, the power density is expected to remain almost constant during that period, indicating an increase in supply current requirements. Power delivery at low voltage and high current by an external Point Of Load (POL) converter is troublesome since path inductances and resistances cause supply instability and power loss, respectively, and the required number of Controlled Collapse Chip Connections (C4) for power delivery to the chip increases [2]. An increased external supply voltage of kV_{DD} and an internal k:1 POL converter with an efficiency of η_{POL} facilitates a reduction of the supply current by a factor of $k\eta_{\mathrm{POL}}$ for a desired power delivery to the on-chip load, e.g. a microprocessor.

We distinguish between two types of power supply integration: Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC) [3]. For PSiP, separate chips containing switches, drivers, controllers, etc. are within the same package but with external passives. For PwrSoC, a single chip contains the switches, drivers, controllers, etc. and the passives are integrated. Possibly, PwrSoC can be implemented on the same die as the load.

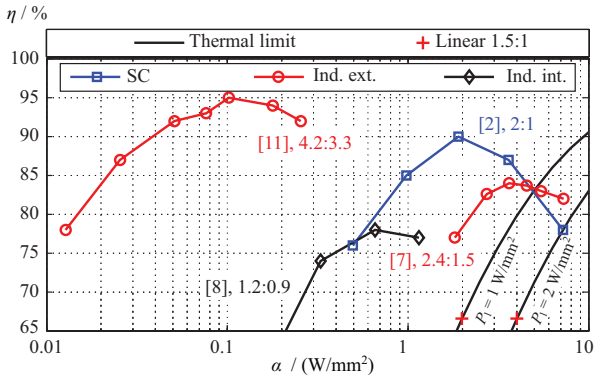

Fig. 1. Efficiency, η, vs. area-related power density, α, of published integrated power converters. Each citet converter represents one specific design operated at various load levels. The shown efficiency is the total converter efficiency, and the depicted power density is scaled with respect to the surface area of the main energy storage component, i.e. the power inductor for inductor based converters and the capacitors for switched capacitor converters. The appertaining conversion ratio is given next to the citation.

Circuit topologies suited for PSiP and PwrSoC conversion can be categorized as linear regulators, inductor based converters, and switched capacitor (SC) converters. Linear regulators, also known as Low Drop-Out (LDO) regulators, are found impractical since their theoretically achievable efficiency equals the conversion ratio; e.g. a 1.5:1 linear regulator has a theoretical efficiency limit of 67%. The switched capacitor approach has lately shown promising results for fixed operating conditions, but it still lacks good regulation capabilities such as regulation of load and line variations [2, 4]. The inductor based buck-type converter, shown in Fig. 2, is a widely known converter topology with high regulation capabilities, and it is considered an enabling technology for PSiP and PwrSoC applications [5, 6].

Fig. 1 shows the efficiencies of published integrated power converters and the area-related power densities of the main energy storage component of the related converters,[1] i.e. the capacitors of a SC converter or the inductor of a buck converter. Very high power densities are achieved with the SC converter ($\eta_{\max} = 90\%$) and for the buck converter with

[1] Ind. int.: buck converter with integrated inductor; Ind. ext.: buck converter with external inductor.

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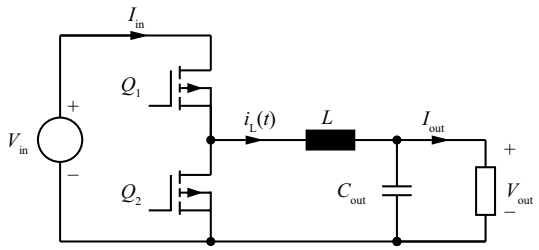


Fig. 2. Classical buck converter implemented with two switches Q_1 and Q_2 driven in antiphase with duty cycle D. The output filter consists of the inductor L and the capacitor C which set the output current ripple and the output voltage ripple, respectively.

external inductors ($\eta_{\max} = 84\%$) [2, 7], whereas the power density and efficiency achieved with internal inductors are considerably lower ($\alpha < 1.2\,\mathrm{W/mm^2}$; $\eta_{\max} = 77.9\%$) [8]. The 1.5:1 linear regulated is also shown in Fig. 1. The limit in power density is determined by a thermal limit, which is depicted as black lines.

The switches Q_1 and Q_2 in the buck converter shown in Fig. 2 need to withstand the input voltage. The output capacitance is determined from voltage ripple requirements, and it may be reduced by using an interleaved design [6]. The inductor of an integrated buck converter is the most challenging component to design since inductors consume a large amount of total converter area and have high losses compared to discrete inductors. This results in low converter power density and efficiency [9, 10]. Furthermore, the inductance of integrated inductors is low compared to discrete inductors, and therefore the switching frequency is chosen to be high to accommodate the low inductance requirements [6, 9].

In this paper, we distinguish between three types of inductor integration: on-chip inductors, on-top-of-chip inductors, and Printed Circuit Board (PCB) inductors. For on-chip inductors, the inductor is implemented using metal layers available in the semiconductor manufacturing foundry. For on-top-of-chip inductors, the inductor is fabricated on top of the silicon die in a post-processing manufacturing step. For PCB inductors, the inductor is external to the chip die. Both on-chip and on-top-of-chip inductors are considered PwrSoC implementations whereas the PCB inductor is considered a PSiP implementation [3]. For inductors in PwrSoC applications, the stray field generated by the inductor can cause eddy currents in the silicon substrate giving rise to substrate losses. A solution to this problem is the patterned ground shield, which reduces this effect on behalf of a slightly increased parasitic capacitance to the substrate [12].

Investigated inductor geometries are the spiral and racetrack inductors. The spiral inductor is readily available in most semiconductor manufacturing processes. The racetrack inductor has been used and studied in the literature, especially with magnetic materials [5] or as a coupled inductor for a tapped inductor buck converter [13]. In this paper, only coreless inductors are considered since adding magnetic materials in an integrated circuit foundry requires additional specialized manufacturing steps [10]. A third inductor geometry, the toroid inductor, which is often used in discrete buck converters, becomes impractical for PSiP and PwrSoC because of its three-dimensional structure.

The subject of this paper is an inductor optimization procedure for designing inductors with the lowest possible power loss for a desired inductor surface area. The output of the procedure is the so-called $\alpha - \eta$ Pareto front [14], which represents the set of inductors characterized by their geometry parameters that give the best performance with respect to both α and η. The proposed inductor optimization procedure applies equally for PSiP and PwrSoC applications. Experimental evaluation of practical inductors to verify the procedure are performed on a macroscopic level owing to the simpler manufacturing process of PCBs. Manufacturing on-chip and on-top-of-chip inductors to verify the procedure will be the subject of future research.

In **Section II**, the operating modes of the buck converter are discussed in order to determine the inductance value needed for a desired inductor current waveform and converter switching frequency. **Section III** details the geometrical models for spiral and racetrack inductors. A Finite Element Method (FEM) simulator uses these geometrical models to calculate the inductor parameters: inductance, dc resistance, and ac resistance. The optimization procedure is presented in **Section IV** and it utilizes the results obtained from the FEM simulation to determine the $\alpha - \eta$ Pareto front. The Pareto fronts of two case studies are presented and discussed in **section V**. Based on these results, the most promising inductor realizations are selected and manufactured on PCB for verification of the proposed inductor optimization procedure. **Section VI** concludes the paper.

II. Buck Converter operation

The output voltage of the classical buck converter shown in Fig. 2 is $V_{\mathrm{out}} = DV_{\mathrm{in}}$, where D is the duty cycle and V_{in} is the input voltage. The inductance L for a given peak-peak inductor current ripple $\Delta I_{L\mathrm{pp}}$ is

$$L = V_{\mathrm{out}} \frac{1-D}{f_{\mathrm{sw}} \Delta I_{L\mathrm{pp}}}, \tag{1}$$

where f_{sw} is the switching frequency. We define the Peak to Average Ratio PAR of the inductor current as

$$PAR = \frac{I_{L\mathrm{p}}}{I_{\mathrm{out}}} = 1 + \frac{\Delta I_{L\mathrm{pp}}}{2 I_{\mathrm{out}}}, \tag{2}$$

where $I_{L\mathrm{p}}$ is the peak inductor current and I_{out} is the dc output current. It can be shown that for $1 < PAR < 2$, the buck converter of Fig. 2 operates in Continuous Conduction Mode (CCM1) with solely positive inductor currents $i_L(t) > 0$, for $PAR > 2$ in Continuous Conduction Mode (CCM2) with positive and negative inductor currents, and for $PAR = 2$ in Boundary Conduction Mode (BCM) with $i_L(t) \geq 0$.

It follows from (1) and (2) that the inductance L, the inductor rms current $I_{L(\mathrm{rms})}$, and the peak energy $W_{L\mathrm{p}}$ stored

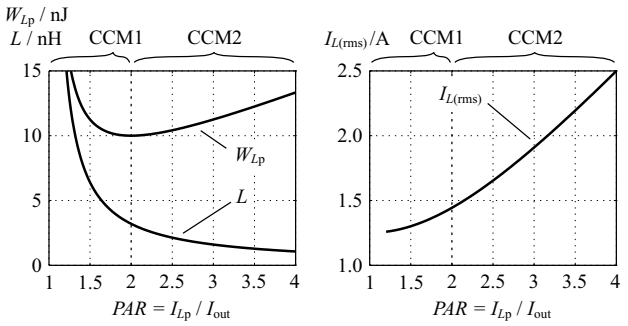


Fig. 3. Inductance and peak energy stored in the inductor of a buck converter plotted against PAR (left); inductor rms current, $I_{L(\mathrm{rms})}$, plotted against PAR (right). The selected operating conditions of the buck converter is: $V_{\mathrm{in}} = 1.6\,\mathrm{V}$, $V_{\mathrm{out}} = 0.8\,\mathrm{V}$, $I_{\mathrm{out}} = 1.25\,\mathrm{A}$, and $f_{\mathrm{sw}} = 50\,\mathrm{MHz}$.

in the inductor can be expressed in terms of PAR as

$$L = \frac{V_{\mathrm{in}} - V_{\mathrm{out}}}{2 f_{\mathrm{sw}} I_{\mathrm{out}} (PAR - 1)} \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}, \tag{3}$$

$$I_{L(\mathrm{rms})} = \sqrt{I_{\mathrm{out}}^2 \left(1 + \frac{1}{3}(PAR - 1)^2\right)}, \text{ and} \tag{4}$$

$$W_{L\mathrm{p}} = \frac{1}{2} L I_{L\mathrm{p}}^2 = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{4 f_{\mathrm{sw}}} \left(1 - \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}\right) \frac{PAR^2}{PAR - 1}, \tag{5}$$

respectively. For the $I_{L(\mathrm{rms})}$ calculation, the inductor current waveform is assumed to be triangular.

From Fig. 3, we see that the inductance decreases with PAR, the rms inductor current increases with PAR, and that the energy stored in the inductor is minimum in BCM when $PAR = 2$. It is not straight forward to determine the best PAR value based on these observations. Designing for CCM1, the inductance and the energy storage requirement are high and this yields a relatively large inductor resulting in a low power density. Designing for CCM2, the inductance is low, however, because of high peak currents, the peak stored energy is larger than for BCM. Furthermore, high rms and peak currents in the semiconductor switches Q_1 and Q_2 result in increased conduction and switching losses of the transistors, thereby reducing efficiency. Overall ripple for the design of the output capacitor can be reduced by interleaving several stages. Thus, BCM is typically considered a good design starting point as a trade-off between efficiency and power density.

III. Inductor modeling

A. Spiral inductor

The spiral inductor model is setup as shown in Fig. 4, where the geometry parameters are defined in Tab. I. The model considers each winding as a concentric circle of wire [15].

From [16], the inductance of a spiral inductor can be approximated as

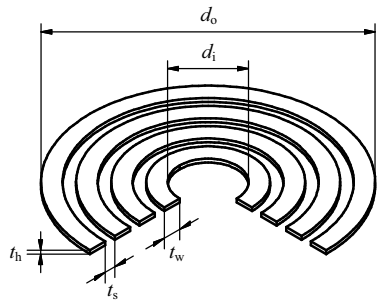


Fig. 4. Spiral inductor modeled as concentric circles of wire. The geometry parameters describing the spiral inductor are defined in the figure.

TABLE I
Geometry parameters for the spiral and racetrack inductors.

Geometry parameter	Description
N	Number of windings
d_{i}	Inner diameter
d_{o}	Outer diameter
t_{w}	Winding width
t_{h}	Winding height
t_{s}	Space between windings
cl	Length of middle extensions (racetrack only)

$$L_{\mathrm{spiral}} \approx \frac{\mu_0 N^2 d_{\mathrm{avg}}}{2} \left[\ln\left(\frac{c_1}{k}\right) + c_2 k^2\right], \tag{6}$$

$$d_{\mathrm{avg}} = \frac{d'_{\mathrm{o}} + d'_{\mathrm{i}}}{2},\ k = \frac{d'_{\mathrm{o}} - d'_{\mathrm{i}}}{d'_{\mathrm{o}} + d'_{\mathrm{i}}},\ c_1 = 2.46,\ c_2 = 0.20,$$

$$d'_{\mathrm{i}} = \max\left(0,\ d_{\mathrm{i}} - \frac{t_{\mathrm{w}} + t_{\mathrm{s}}}{2}\right),\ d'_{\mathrm{o}} = d_{\mathrm{o}} + \frac{t_{\mathrm{w}} + t_{\mathrm{s}}}{2}.$$

The dc resistance can be estimated by

$$R_{\mathrm{dc,spiral}} = \sum_{j=1}^{N} \frac{2\pi\rho}{t_{\mathrm{h}} \ln\left(\frac{r_{\mathrm{o},j}}{r_{\mathrm{i},j}}\right)}, \tag{7}$$

$$r_{\mathrm{i},j} = \frac{1}{2} d_{\mathrm{i}} + (j-1)(t_{\mathrm{w}} + t_{\mathrm{s}}),\ r_{\mathrm{o},j} = r_{\mathrm{i},j} + t_{\mathrm{w}},$$

where $\rho = 0.0172 \cdot 10^{-6}\,\Omega\mathrm{m}$ is the resistivity of copper. The ac resistance of a spiral inductor is difficult to estimate analytically, so instead, the ac resistance at the switching frequency and its n harmonics considered is obtained from FEM simulations as discussed in section IV. The area of the spiral inductor is

$$A_{L,\mathrm{spiral}} = \pi \left[\frac{1}{2} d_{\mathrm{i}} + N(t_{\mathrm{s}} + t_{\mathrm{w}}) - t_{\mathrm{s}}\right]^2. \tag{8}$$

B. Racetrack inductor

The racetrack inductor model is shown in Fig. 5 and it also has the geometry variables in Tab. I. The racetrack can be considered as two concentric half-spirals with the windings connected by straight middle extensions of length cl.

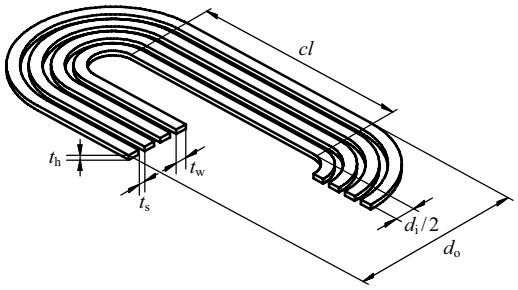


Fig. 5. Racetrack inductor model, which has the same geometry parameters as the spiral with the addition of cl to describe the length of the middle extensions.

The dc resistance of the racetrack inductor can be estimated from the dc resistance of the spiral inductor in (7) with an additional term that takes the middle extensions into account

$$R_{\mathrm{dc,racetrack}} = R_{\mathrm{dc,spiral}} + \frac{2\,\rho\,cl}{t_\mathrm{h}} \sum_{j=1}^{N} \frac{1}{r_{\mathrm{o},j} - r_{\mathrm{i},j}}. \qquad (9)$$

There is no analytical expression for the inductance nor for the ac resistance of racetrack inductors available, so both are estimated by the FEM simulations. The area of the racetrack inductor is

$$A_{L,\mathrm{racetrack}} = A_{L,\mathrm{spiral}} + cl\big[d_\mathrm{i} + 2N(t_\mathrm{s} + t_\mathrm{w}) - t_\mathrm{s}\big]. \quad (10)$$

IV. Inductor Optimization Procedure

The inductor optimization procedure presented in this paper is illustrated by the flowchart shown in Fig. 6. The procedure input is the converter operating conditions: input voltage V_in, output voltage V_out, output current I_out, and inductor current peak to average ratio PAR. Next, the inductor type is chosen and the design space of inductors to be simulated is defined by the minimum and maximum value of each geometry parameter from Tab. I. Additionally, an incremental step size can be set for each geometry parameter.

The first set, $i = 1$, of geometry parameters is loaded into a generic inductor model in a FEM simulator and a dc simulation is run to extract the dc inductance $L_{\mathrm{dc},i}$ and the dc resistance $R_{\mathrm{dc},i}$. The surface area $A_{L,i}$ is also determined using (8) or (10), depending on which inductor type is being simulated. The switching frequency $f_{\mathrm{sw},i}$ is calculated based on $L_{\mathrm{dc},i}$ and the converter operating conditions. A FEM simulation is run at the switching frequency and each of the n harmonics considered, and an ac resistance $R_{\mathrm{ac},ij}$ for each harmonic, $j = 1 \ldots n$, is extracted. From the initial operating conditions, the inductor current waveform, which is assumed to be triangular, can be determined. The rms value of the inductor current at each harmonic $I_{L(\mathrm{rms}),ij}$ is found from the Fourier series expansion of the a priori known current waveform. The total power loss $P_{\mathrm{l},i}$ in the inductor can then be estimated by

$$P_{\mathrm{l},i} = I_\mathrm{out}^2 R_{\mathrm{dc},i} + I_{L(\mathrm{rms}),i1}^2 R_{\mathrm{ac},i1} + \ldots + I_{L(\mathrm{rms}),in}^2 R_{\mathrm{ac},in}. \qquad (11)$$

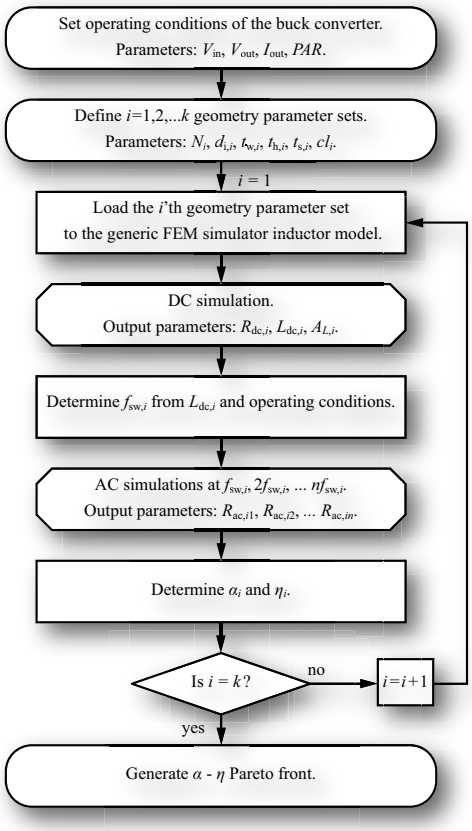


Fig. 6. Flowchart of optimization procedure.

Finally, the efficiency η_i and area-related power density α_i for the i'th geometry parameter set are calculated as

$$\eta_i = \frac{P_{\mathrm{o},i}}{P_{\mathrm{o},i} + P_{\mathrm{l},i}} \text{ and} \qquad (12)$$

$$\alpha_i = \frac{P_{\mathrm{o},i}}{A_{L,i}}, \qquad (13)$$

respectively.

After having determined η_i and α_i of the first geometry set, the next set, $i = i + 1$, is loaded into the model and the procedure is repeated. The entire inductor optimization procedure is completed when all predefined sets of geometry variables have been processed. Thereafter, the highest efficiency inductor given an area-related power density is found by searching the simulated data, and the $\alpha - \eta$ Pareto front is generated. The geometry parameters for the inductors forming the Pareto front can then be extracted for practical realizations. The optimization procedure is repeated for each investigated inductor type, which requires its own generic FEM simulator model.

V. Evaluation and Verification of the Inductor Optimization Procedure

The inductor optimization procedure described in the previous section is performed with the following example buck converter operating conditions:

TABLE II
GEOMETRY PARAMETER LIMITS AND STEP SIZES FOR THE SPIRAL PCB INDUCTOR OPTIMIZATION PROCEDURE CASE STUDY USING (6) AND (7).

Implementation	Geometry parameter	Range	Step size
Spiral inductor			
PCB	N	$1 \ldots 20$	1
	d_i	$0.30\,\mathrm{mm} \ldots 1.80\,\mathrm{mm}$	$0.25\,\mathrm{mm}$
	t_w	$0.15\,\mathrm{mm} \ldots 1.95\,\mathrm{mm}$	$0.05\,\mathrm{mm}$
	t_s	$0.15\,\mathrm{mm} \ldots 1.95\,\mathrm{mm}$	$0.05\,\mathrm{mm}$
	t_h	$35\,\mu\mathrm{m}$	–

TABLE III
GEOMETRY PARAMETER LIMITS AND STEP SIZES FOR THE SPIRAL AND RACETRACK PCB INDUCTOR OPTIMIZATION PROCEDURE CASE STUDY USING THE RESULTS OBTAINED FROM THE FEM SIMULATIONS.

Implementation	Geometry parameter	Range	Step size
Spiral inductor			
PCB	N	$1 \ldots 10$	1
	d_i	$0.30\,\mathrm{mm} \ldots 1.80\,\mathrm{mm}$	$0.50\,\mathrm{mm}$
	t_w	$0.15\,\mathrm{mm} \ldots 1.95\,\mathrm{mm}$	$0.15\,\mathrm{mm}$
	t_s	$0.15\,\mathrm{mm} \ldots 0.9\,\mathrm{mm}$	$0.15\,\mathrm{mm}$
	t_h	$35\,\mu\mathrm{m}$	–
Racetrack inductor			
PCB	N	$1 \ldots 10$	1
	d_i	$0.30\,\mathrm{mm}$	–
	t_w	$0.15\,\mathrm{mm} \ldots 1.95\,\mathrm{mm}$	$0.15\,\mathrm{mm}$
	t_s	$0.15\,\mathrm{mm}$	–
	t_h	$35\,\mu\mathrm{m}$	–
	cl	$0.20\,\mathrm{mm} \ldots 2.00\,\mathrm{mm}$	$0.20\,\mathrm{mm}$

- Input and output voltage: $V_\mathrm{in} = 1.6\,\mathrm{V}$, $V_\mathrm{out} = 0.8\,\mathrm{V}$.
- Output currents and output power levels:
  - PCB: $I_\mathrm{out} = 1.25\,\mathrm{A}$, $P_\mathrm{out} = 1\,\mathrm{W}$.
  - On-top-of-chip: $I_\mathrm{out} = 0.5\,\mathrm{A}$, $P_\mathrm{out} = 0.4\,\mathrm{W}$.
  - On-chip: $I_\mathrm{out} = 50\,\mathrm{mA}$, $P_\mathrm{out} = 40\,\mathrm{mW}$.
- Operating mode: $PAR = 2$.

These operating conditions represent a buck converter operated in BCM with duty cycle $D = 50\%$.

A. PCB inductor optimization procedure case study

Running the optimization procedure presented in the previous section, the output is a set of inductance and resistance values; one for each inductor's geometry parameter set. The performance of each inductor is mapped into an $\eta - \alpha$ plane as a single point. The upper part of the envelope around all resulting points defines the Pareto front.

The optimization is performed for the PCB spiral inductor using the analytical expressions for the dc inductance and resistance given in (6) and (7), respectively. The geometry parameters are selected according to the limits given by the PCB manufacturer listed in Tab. II. Since the computational effort needed to evaluate the analytical equations is considerably less than the effort needed to conduct FEM simulations, more than 80,000 single inductor designs are used to generate the plot presented in Fig. 7; there, each point represents a single design result. Only inductors, which result in a switching frequency less than $100\,\mathrm{MHz}$, are mapped to the $\eta - \alpha$ plane in order to avoid exceedingly high switching frequencies. The points located on the Pareto front shown in Fig. 7 represent the inductor designs which yield the highest efficiency at a given area-related power density.

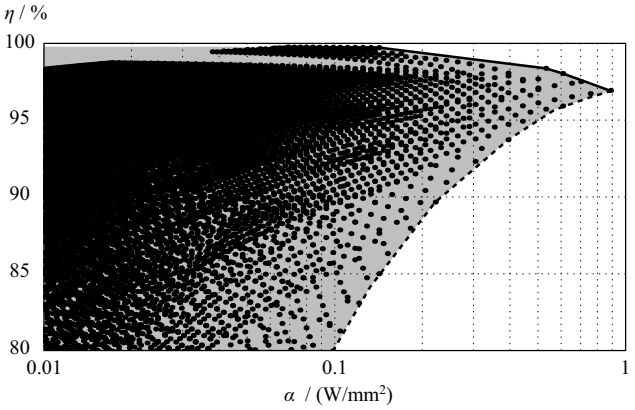


Fig. 7. Results of the optimization procedure for spiral PCB inductors using the analytical expressions (6), (7), and (8). The upper part of the envelope is the Pareto front, which represents the inductors with the highest achievable efficiencies for given area-related power densities. Points representing inductors with low N generally achieve high efficiencies, whereas the efficiency reduces with increasing N due to increased resistances. The inward bend of the lower part of the envelope (dashed line) is caused by the minimum spacing requirement, which become more profound for higher number of windings.

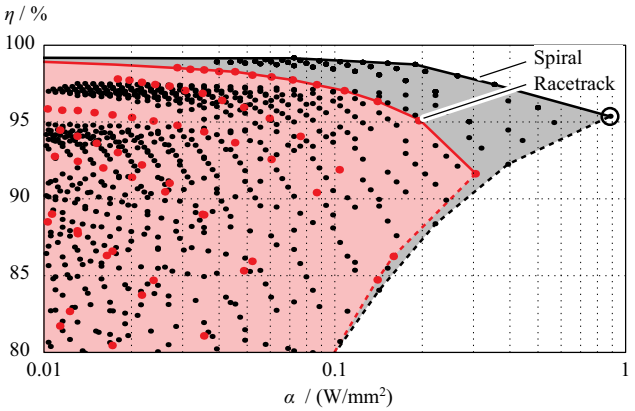


Fig. 8. Results of the optimization procedure for PCB inductors. Black points represent spiral inductors and red points represent racetrack inductors. For each inductor type, the upper part of the envelope is the Pareto front. The optimum point, marked with a circle, correspond to the inductor with the geometry parameters listed in Tab. IV.

Fig. 8 depicts the Pareto fronts for spiral inductors (black) and racetrack inductors (red), which are obtained from the optimization procedure with FEM simulations. The used geometry parameter limits are listed in Tab. III and only inductors where $f_\mathrm{sw} < 100\,\mathrm{MHz}$ are considered. The model of the spiral inductor can be implemented in a 2D FEM simulation because of its axial symmetry. The racetrack inductor is implemented as a 3D FEM simulation model. Since 3D simulations are far more time consuming than 2D simulations, a reduced number

TABLE IV
GEOMETRY PARAMETERS AND SIMULATION RESULTS FOR THE OPTIMUM SPIRAL PCB INDUCTOR.

Geometry parameter	Value	Output parameter	Simulation value
N	2	L	2.7 nH
d_i	0.30 mm	η	95.4%
d_o	1.20 mm	α	0.88 W/mm^2
t_w	0.15 mm	f_sw	58 MHz
t_h	35 µm	R_dc	15mΩ
t_s	0.15 mm	R_ac @ f_sw	43mΩ

TABLE V
GEOMETRY PARAMETER LIMITS AND STEP SIZES FOR THE ON-TOP-OF-CHIP AND ON-CHIP SPIRAL INDUCTOR OPTIMIZATION PROCEDURE CASE STUDY.

Implementation	Geom. par.	Range / Points	Step size
On-top-of-chip	N	1 . . . 10	1
	d_i	{40 µm, 70 µm, 120 µm, 200 µm}	–
	t_w	10 µm . . . 100 µm $\wedge$ $t_\mathrm{w}/t_\mathrm{h} \geq 1$	18 µm
	t_s	10 µm . . . 100 µm $\wedge$ $t_\mathrm{s}/t_\mathrm{h} \geq 1$	18 µm
	t_h	10 µm . . . 100 µm	18 µm
On-chip	N	1 . . . 35	1
	d_i	{20 µm, 40 µm, 100 µm, 200 µm, 400 µm}	–
	t_w	{2 µm, 4 µm, 6 µm, 8 µm, 10 µm, 12 µm, 15 µm, 20 µm, 30 µm, 50 µm}	–
	t_s	{1.8 µm, 3 µm, 5 µm}	–
	t_h	3 µm	–

of geometry parameter sets is used for the racetrack inductor optimization. The optimization results obtained from the FEM simulations consider ac losses, and therefore the efficiencies shown in Fig. 8 are less than the calculated efficiencies based on (7) and depicted in Fig. 7.

From a direct comparison between the two inductor types, the spiral is found to outperform the racetrack with respect to both efficiency and area-related power density. A close inspection of the results reveals that the best performing racetrack inductors have minimum cl; that is, they are close to being spiral inductors. Still, the racetrack inductor remains attractive for inductors with a magnetic core.

The selected optimized PCB inductor is marked with a circle in Fig. 8, and data for this particular inductor is summarized in Tab. IV. The power loss of this inductor is $p_\mathrm{l} = 42\,\mathrm{mW/mm^2}$, and active cooling is required; however, p_l is considerably less than typical losses of advanced microprocessors, which are in the range of $500\,\mathrm{mW/mm^2}$.

B. On-top-of-chip and on-chip spiral inductor optimization procedure case study

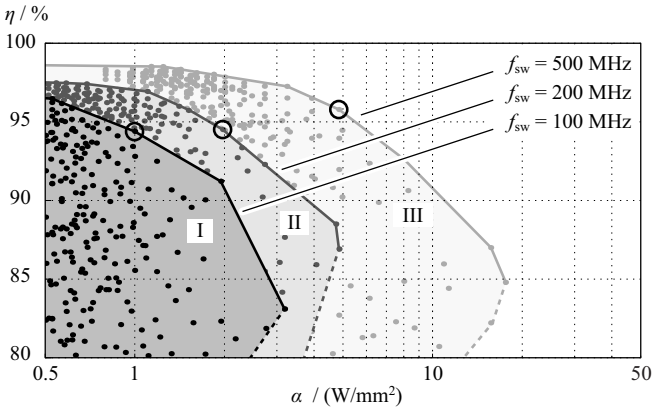
For the on-top-of-chip and on-chip implementations, only the spiral inductor is considered since the results obtained from the PCB inductor in section V-A showed that the coreless racetrack inductor is inferior to the spiral inductor. The geometry parameter limits, listed in Tab. V, are considered to be representative for practical realizations. For the on-top-of-chip implementation, the wire width and spacing are restricted to be greater than or equal to the wire thickness for practical reasons. The resulting Pareto fronts are shown in Fig. 9, where the dark gray, medium gray, and light gray domains, I, II, and III, represent various maximum converter switching frequencies. The increase in allowable switching frequency, compared to 100 MHz for the PCB implementation, shows the inductor's performance gain in power density. The on-top-of-chip Pareto front in Fig. 9(a) has higher area-related power density compared to the PCB implementation in Fig. 8. Since the converter

TABLE VI
GEOMETRY PARAMETERS AND SIMULATION RESULTS FOR THE SELECTED INDUCTORS FOUND WITH THE INDUCTOR OPTIMIZATION PROCEDURE FOR THE ON-TOP-OF-CHIP REALIZATION.

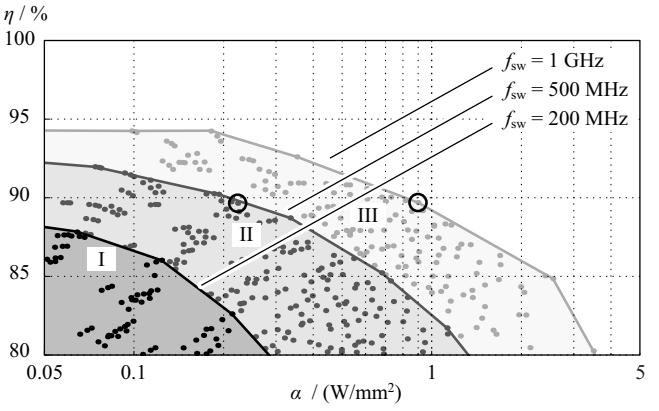
Geometry parameter	Value	Output parameter	Simulation value
On-top-of-chip realization, domain I ($f_\mathrm{sw} \leq 100\,\mathrm{MHz}$)			
N	4	L	4.3 nH
d_i	70 µm	η	94.4%
d_o	714 µm	α	1.0 W/mm^2
t_w	46 µm	f_sw	91 MHz
t_h	46 µm	R_dc	40mΩ
t_s	46 µm	R_ac @ f_sw	124mΩ
On-top-of-chip realization, domain II ($f_\mathrm{sw} \leq 200\,\mathrm{MHz}$)			
N	3	L	2.3 nH
d_i	120 µm	η	94.5%
d_o	508 µm	α	1.97 W/mm^2
t_w	46 µm	f_sw	170 MHz
t_h	28 µm	R_dc	40mΩ
t_s	28 µm	R_ac @ f_sw	132mΩ
On-top-of-chip realization, domain III ($f_\mathrm{sw} \leq 500\,\mathrm{MHz}$)			
N	2	L	0.81 nH
d_i	120 µm	η	95.8%
d_o	324 µm	α	4.85 W/mm^2
t_w	28 µm	f_sw	480 MHz
t_h	28 µm	R_dc	31mΩ
t_s	46 µm	R_ac @ f_sw	109mΩ

TABLE VII
GEOMETRY PARAMETERS AND SIMULATION RESULTS FOR THE SELECTED INDUCTORS FOUND WITH THE INDUCTOR OPTIMIZATION PROCEDURE FOR THE ON-CHIP REALIZATION.

Geometry parameter	Value	Output parameter	Simulation value
On-chip realization, domain II ($f_\mathrm{sw} \leq 500\,\mathrm{MHz}$)			
N	6	L	9.1 nH
d_i	100 µm	η	89.6%
d_o	478 µm	α	0.22 W/mm^2
t_w	30 µm	f_sw	410 MHz
t_h	3 µm	R_dc	1.0Ω
t_s	1.8 µm	R_ac @ f_sw	1.9Ω
On-chip realization, domain III ($f_\mathrm{sw} \leq 1\,\mathrm{GHz}$)			
N	6	L	4.1 nH
d_i	40 µm	η	89.7%
d_o	238 µm	α	0.90 W/mm^2
t_w	15 µm	f_sw	907 MHz
t_h	3 µm	R_dc	1.0Ω
t_s	1.8 µm	R_ac @ f_sw	1.9Ω



(a)



(b)

Fig. 9. Spiral inductor Pareto fronts for (a) on-top-of-chip implementation and (b) on-chip implementation. The shadings correspond to a specified maximum switching frequency of the buck converter.

operating conditions are fixed, then the inductance required decreases with frequency from (3). Because of the less coarse geometry parameter limits of the on-top-of-chip inductor compared to the PCB inductor, the required inductance can be implemented using less area, thereby increasing the power density. According to the Pareto front, the reduced area has only a slight impact on efficiency compared to the Pareto front of the PCB inductor. However, transistor switching losses increase with switching frequency, and therefore surface and loss models of the complete buck converter are needed to determine the optimal switching frequency with respect to maximum efficiency and / or power density.

The on-top-of-chip implementation in Fig. 9(a) is seen to perform better than the on-chip implementation in Fig. 9(b). This is mainly due to the thin metal layers available in advanced submicron semiconductor processes being a very limiting geometry parameter. Only for very high switching frequencies does the on-chip implementation perform well, but such frequencies are typically not feasible due to increased switching losses of the transistors.

As an example, the optimized inductors are selected based on a predefined efficiency, which is chosen to be $\eta = 95\%$ for the on-top-of-chip implementation and $\eta = 90\%$ for the on-chip implementation. The best fitting inductors are marked with circles in Fig. 9(a) and 9(b); the data of these inductors are summarized in Tab. VI and Tab. VII, respectively. The most favorable inductor is the on-top-of-chip implementation that achieves an efficiency of 94.5% and an area-related power density of $1.97\,\mathrm{W/mm^2}$ at a switching frequency of $170\,\mathrm{MHz}$. This selection is based on the assumption that a maximum switching frequency of $200\,\mathrm{MHz}$ represents a reasonable value for an on-top-of-chip realization.

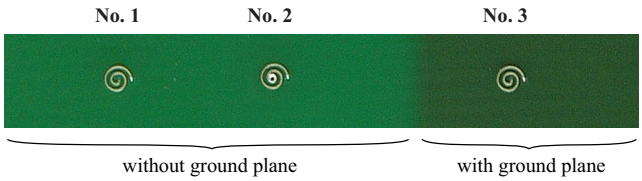


Fig. 10. Printed Circuit Board (PCB) spiral inductors produced to verify the inductor optimization procedure. The surface of each inductor is $1.5\,\mathrm{mm^2}$.

TABLE VIII
COMPARISON OF CALCULATED, SIMULATED, AND MEASURED INDUCTANCES OF THE OPTIMUM SPIRAL PCB INDUCTOR FROM TABLE IV.

Calculated Value	Simulated Value	No. 1 Measured	No. 2 Measured	No. 3 Measured
2.4 nH	2.7 nH	3.1 nH	2.8 nH	3.1 nH

C. Experimental verification of spiral PCB inductors

The optimum inductor with geometry parameters from Tab. IV are produced on the PCB shown in Fig. 10 to verify the presented inductor optimization procedure. The inductor labeled No. 1 is the practical realization of the optimum inductor. No. 2 inductor realization is the same inductor but with a via included in the center point, and No. 3 inductor realization is equivalent to No. 1, but with a ground plane underneath to investigate whether this influences the impedance within the considered frequency range.

The inductor measurements are performed with an Agilent 4395A impedance analyzer using a model 40A, $1\,\mathrm{mm}$ pitch Picoprobe from GGB Industries, Inc. The calculated, simulated, and measured inductances are compared in Tab. VIII. Moreover, the resistances over frequency have been measured; however, these measurement results are not considered to be meaningful due to a distinctive scattering caused from the contact resistance of the probe, which changes depending on contact pressure, and due to the inductors' impedance angles, $\varphi = \arg(R + \mathrm{j}\omega L)$, being close to $90°$.

The calculated inductance is obtained with the parameters of the optimum inductor given in Tab. IV being inserted into (6). The error between the calculated and simulated inductance is due to the FEM simulation model, which considers the spiral inductor as concentric circles; this simplification yields reduced accuracy if a low number of turns is used together with a small inner diameter.

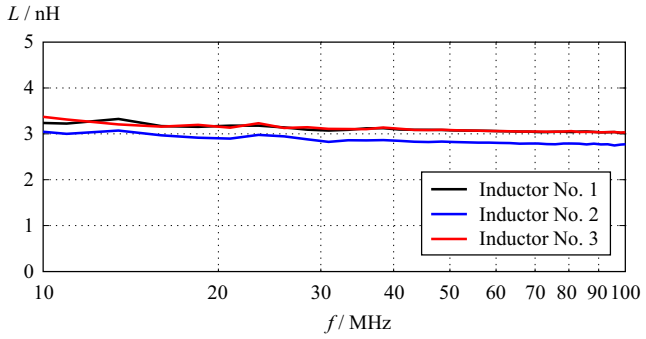


Fig. 11. Measured inductance over frequency of the three PCB inductors.

The measured inductance values are higher than the calculated and simulated values. However, also the surface area of the realized inductors, which is $1.5\,\mathrm{mm}^2$, is higher than the calculated value of $1.1\,\mathrm{mm}^2$. With some tuning of the PCB layout, e.g. using $N = 1.85$ turns, the inductance is expected to approach the desired value of $2.7\,\mathrm{nH}$ and the surface is reduced to $1.3\,\mathrm{mm}^2$. The remaining difference in surface area is due to the simplification of concentric circles used.

The measured inductances over frequency are shown in Fig. 11. It is seen that the ground plane in No. 3 has no influence within the measured frequency band compared to No. 1. For No. 2, the center via eff shortens the wire length resulting in a slightly lower inductance value compared to No. 1 and No. 3. All inductances decrease by approximately 5% within the measured frequency range due high frequency effects.

VI. Conclusions

This paper presents an inductor optimization procedure for Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC) applications. Inductor implementations considered are Printed Circuit Board (PCB) inductors, on-top-of-chip inductors, and on-chip inductors. Inductor types investigated are the coreless spiral and coreless racetrack inductors. The optimization procedure uses a Finite Element Method (FEM) simulator environment to compute efficiency and area-related power density of an inductor given a set of geometry parameters. Based on the simulations, the most efficient inductor design for a given area-related power density is determined.

The inductor optimization procedure is performed on two case studies: spiral and racetrack PCB inductors, and spiral on-top-of-chip and on-chip inductors. For PCB inductors, the spiral inductor is found to outperform the racetrack inductor in both efficiency and area-related power density for PSiP applications. For on-top-of-chip and on-chip inductors, the on-top-of-chip solution is found to be better suited for PwrSoC applications since the metal layers used for on-chip inductors are too thin, and thereby too resistive, to give sufficiently high efficiency at feasible operating frequencies.

The most promising spiral PCB inductor was fabricated and measured to verify the proposed inductor optimization procedure.

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References

[1] "International technology roadmap for semiconductors," 2009. [Online]. Available: www.itrs.net

[2] L. Chang, R. K. Montoye, B. L. Ji, A. J. Weger, K. G. Stawiasz, and R. H. Dennard, "A fully-integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3 A/mm^2," in *IEEE Symposium on VLSI Circuits (VLSIC 2010)*, Honolulu, Hawaii, 16–18 June 2010, pp. 55–56.

[3] R. Foley, F. Waldron, J. Slowey, A. Alderman, B. Narveson, and S. C. O'Mathuna, "Technology roadmapping for power supply in package (psip) and power supply on chip (pwrsoc)," in *Proc. of the 25th IEEE Annual Applied Power Electronics Conference and Exposition (APEC 2010)*, Palm Springs, CA, 21–25 Feb. 2010, pp. 525–532.

[4] V. W. Ng, M. D. Seeman, and S. R. Sanders, "High-efficiency, 12V-to-1.5V dc-dc converter realized with switched-capacitor architecture," in *Symposium on VLSI Circuits*, Kyoto, Japan, 16–18 June 2009, pp. 168–169.

[5] S. Mathúna, T. O'Donnell, N. Wang, and K. Rinne, "Magnetics on silicon: an enabling technology for power supply on chip," *IEEE Trans. on Power Electron.*, vol. 20, no. 3, pp. 585–592, May 2005.

[6] P. Hazucha, G. Schrom, J. Hahn, B. A. Bloechel, P. Hack, G. E. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233 MHz 80%-87% efficient four-phase dc-dc converter utilizing air-core inductors on package," *IEEE Trans. on Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, April 2005.

[7] G. Schrom, P. Hazucha, F. Paillet, D. J. Rennie, S. T. Moon, D. S. Gardner, T. Kamik, P. Sun, T. T. Nguyen, M. J. Hill, K. Radhakrishnan, and T. Memioglu, "A 100MHz eight-phase buck converter delivering 12A in 25mm^2 using air-core inductors," in *Proc. of the 22nd IEEE Annual Applied Power Electronics Conference (APEC 2007)*, Anaheim, CA, 25 Feb.–1 March 2007, pp. 727–730.

[8] J. Wibben and R. Harjani, "A high-efficiency dc–dc converter using 2 nH integrated inductors," *IEEE Trans. on Solid-State Circuits*, vol. 43, no. 4, pp. 844–854, April 2008.

[9] R. Meere, T. O'Donnell, H. Bergveld, N. Wang, and S. O'Mathuna, "Analysis of microinductor performance in a 20-100 MHz dc/dc converter," *IEEE Trans. on Power Electron.*, vol. 24, no. 9, pp. 2212–2218, Sept. 2009.

[10] C. R. Sullivan, "Integrating magnetics for on-chip power: Challenges and opportunities," in *Proc. of the IEEE Custom Integrated Circuits Conference (CICC 2009)*, San Jose, CA, 13–16 Sept. 2009, pp. 291–298.

[11] Texas Instruments, "TPS3002 datasheet," 2008. [Online]. Available: http://focus.ti.com/docs/prod/folders/print/tps63002.html

[12] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*. Cambridge University Press, 2004.

[13] J. Qiu and C. R. Sullivan, "Inductor design for VHF tapped-inductor dc-dc power converters," in *Proc. of the 26th IEEE Annual Applied Power Electronics Conference and Exposition (APEC 2011)*, Fort Worth, TX, 6–11 March 2011, pp. 142–149.

[14] J. W. Kolar, J. Biela, and J. Miniböck, "Exploring the Pareto front of multi-objective single-phase PFC rectifier design optimization-99.2% efficiency vs. 7kW/dm^3 power density," in *Proc. of the 6th International Power Electronics and Motion Control Conference (IPEMC 2009)*, Wuhan, China, 17–20 May 2009.

[15] R. Rodriguez, J. Dishman, F. Dickens, and E. Whelan, "Modeling of two-dimensional spiral inductors," *IEEE Trans. on Components, Hybrids, and Manufacturing Technology*, vol. 3, no. 4, pp. 535–541, Dec 1980.

[16] S. S. Mohan, M. del Mar Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Trans. on Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.