Motor-Integrated Power Factor Corrected Single-to-Three-Phase AC/AC Converter Concepts

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VDE "Elektromechanische Antriebssysteme 2023"

November 9th, 2023

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Motivation

- **Reduction of Global Carbon Emissions Required**
- **Transportation Sector Responsible for 14 %** of CO_2 Emissions

- Transportation in **Europe** Approx. **25 %** of All Emissions
- Transportation in **US** Approx. **29 %** of All Emissions

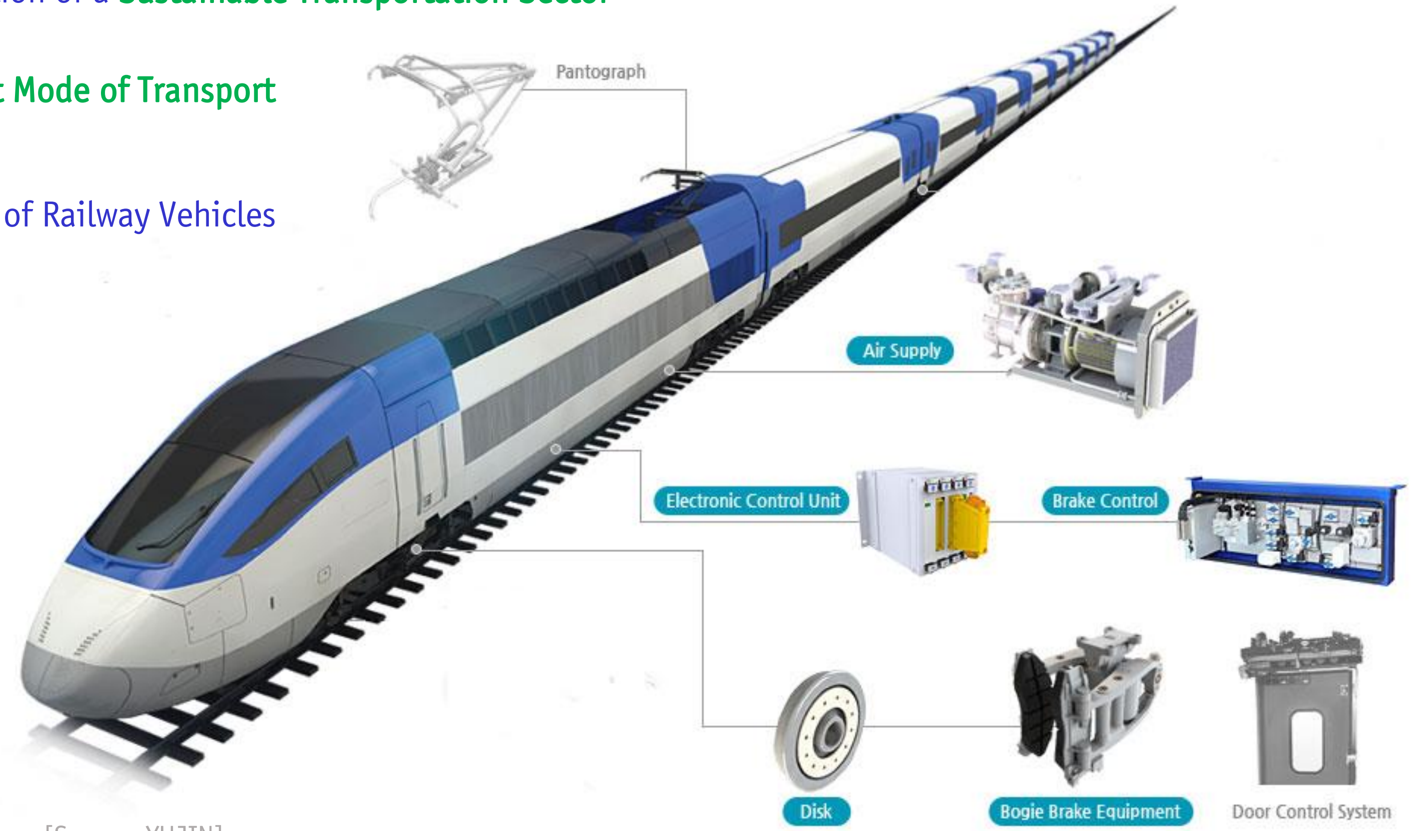
→ **Goal:** Decarbonization and Implementation of a **Sustainable Transportation Sector**

- **Railway Systems: Greenest and Cleanest Mode of Transport**
  - Performance Improvements Demanded

- Focus on **Pressurized Air Supply System** of Railway Vehicles
  - **Air Brake System**
  - Door Control System
  - Pantograph Lifting

- **General Requirements**
  - **Compactness**
  - High Efficiency
  - Reliability
  - Redundancy

→ **Unique Operating Conditions**

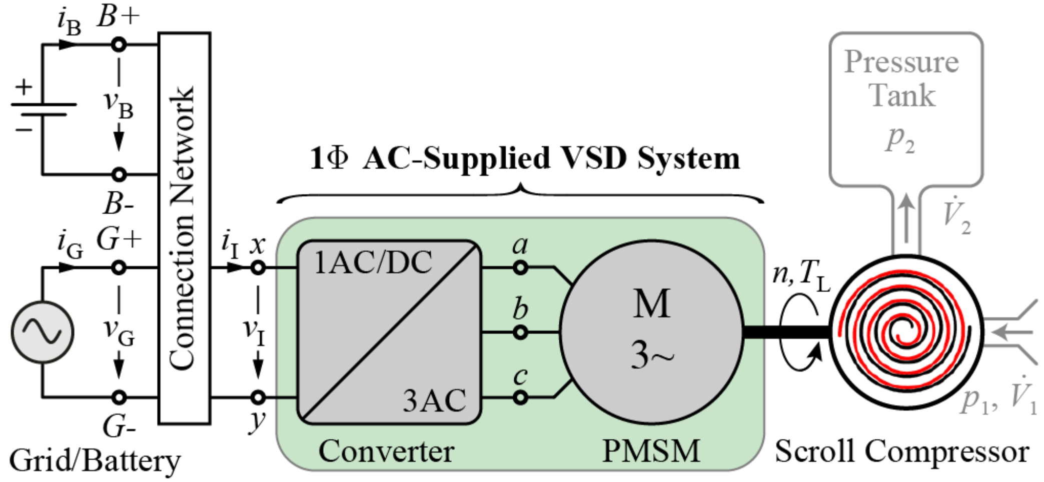


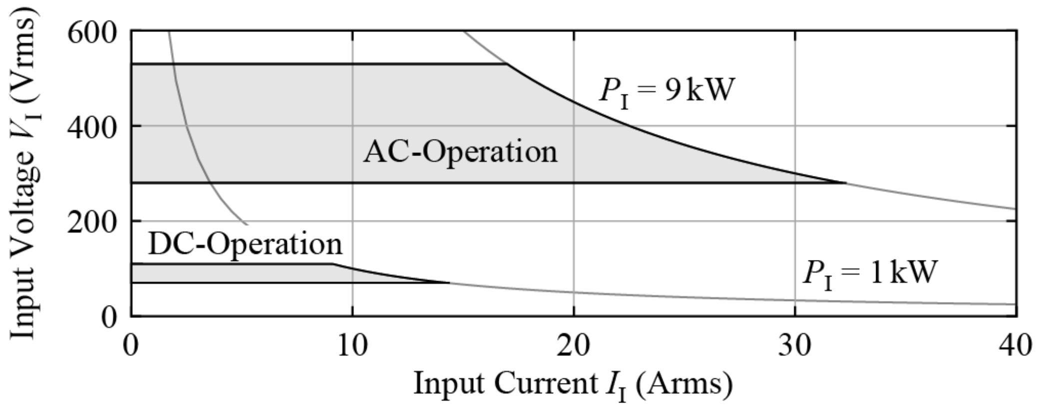
[Source: YUJIN]

Application

- **Oil-Free Scroll Compressor** 7.5 kW @ 3700 rpm
  - Charge Pressure Tank
- **Variable Speed Operation**
  - Maximum System Performance
- **AC-Operation (Grid)** 280…530 Vrms
  - Nominal Voltage 400 Vrms @ 50 Hz
  - Tertiary Traction Transformer Winding
  - Ensure Unity Power Factor Operation
- **DC-Operation (Battery)** 70….110 Vdc
  - On-Board Battery
  - Startup and Grid Interruption
- **1Φ AC/DC-to-3Φ AC Converter System**
  - Wide-Input Voltage Range
  - Survive Grid Disturbances and Interruptions

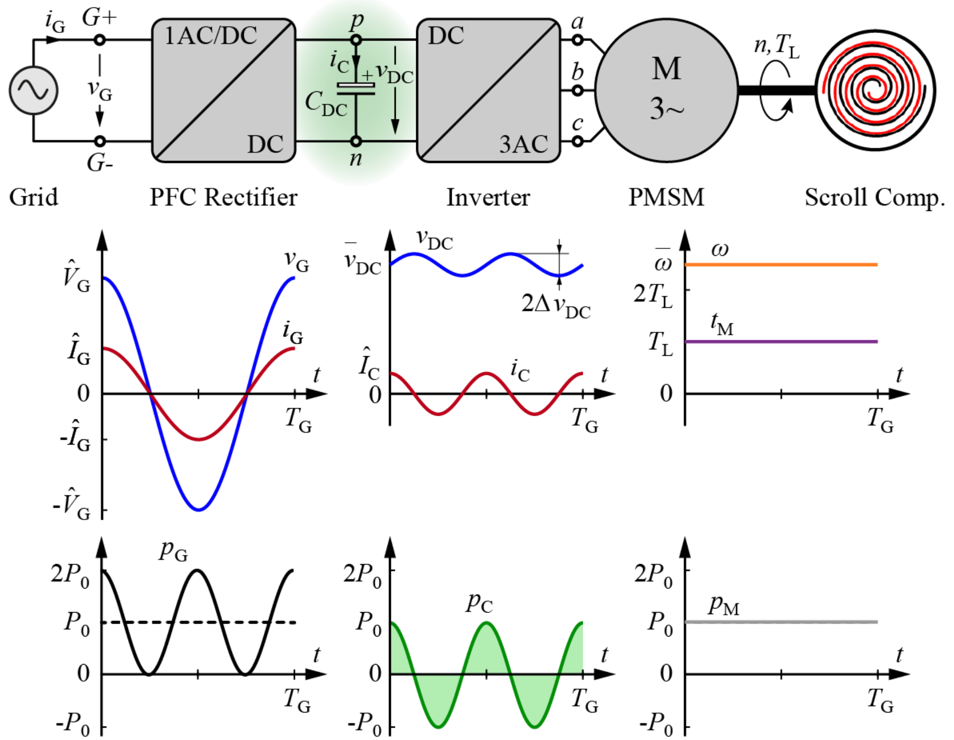
→ Ultra Compact 1Φ AC-Supplied VSD System





Challenge

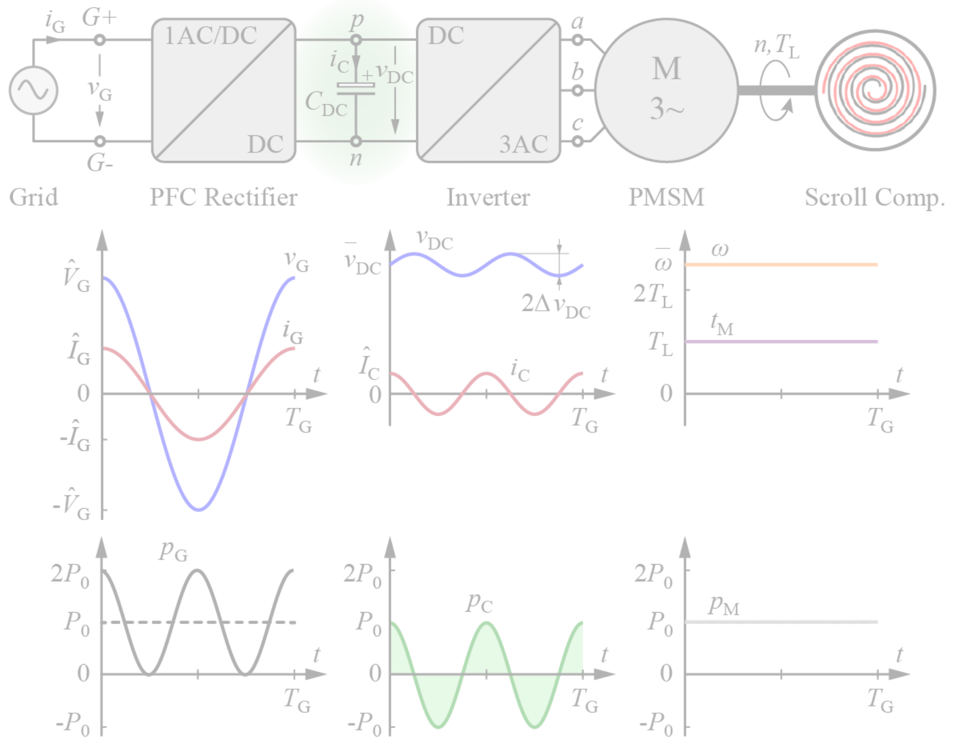
- **State-of-the-Art**
  - Electrical Energy Storage C_{DC} $\qquad \Delta v_{DC} = \frac{P_0}{2\pi\, 2 f_G} \frac{1}{\bar{v}_{DC}\, C_{DC}}$



- **Avoid Electrolytic Capacitors (1 ltr.)** → Increased Lifetime

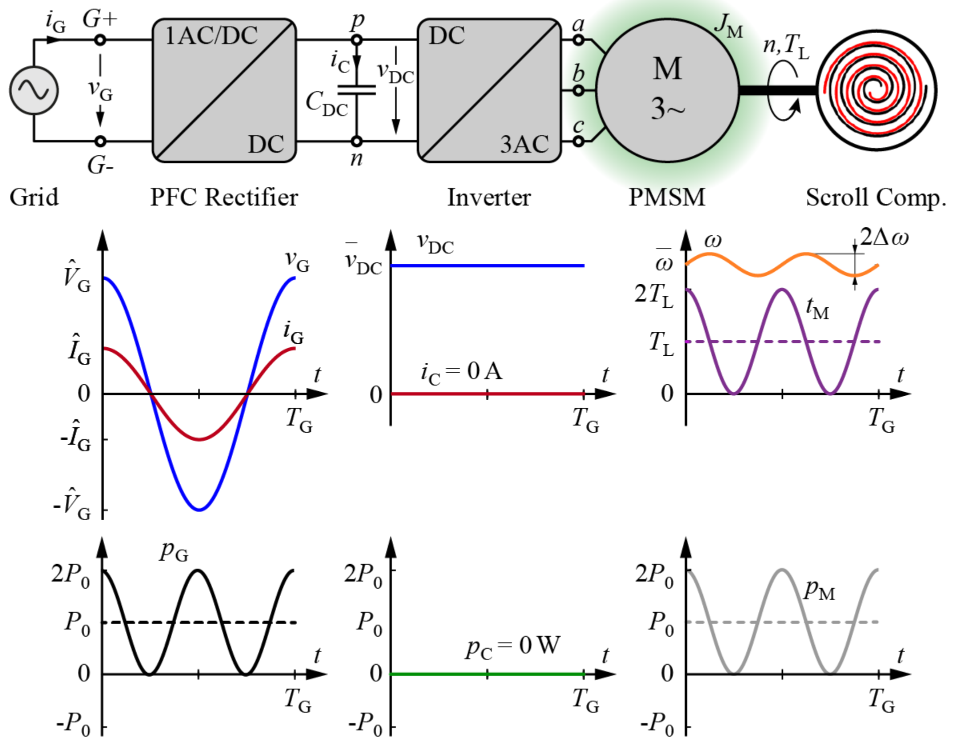
Motor-Integrated Power Pulsation Buffer (MPPB)

- State-of-the-Art
  - Electrical Energy Storage C_{DC} $\quad \Delta v_{DC} = \frac{P_0}{2\pi\, 2f_G} \frac{1}{\bar{v}_{DC}\, C_{DC}}$



- Avoid Electrolytic Capacitors (1 ltr.) → Increased Lifetime

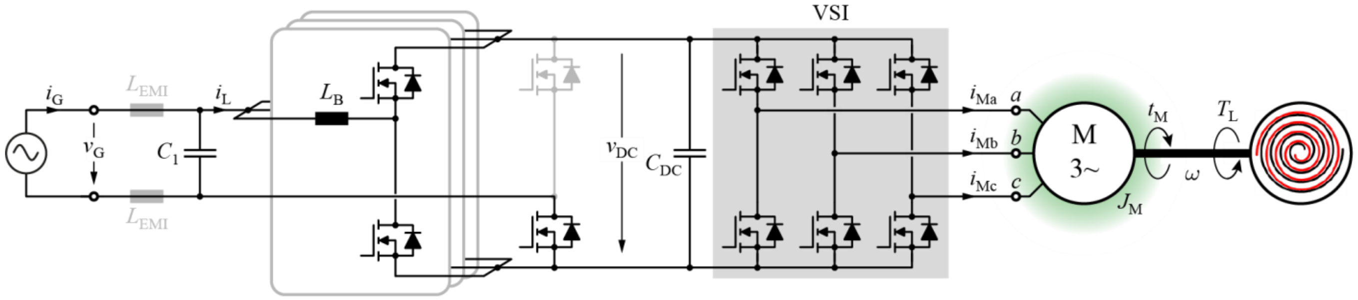
- Proposed MPPB Concept
  - Mechanical Energy Storage J_M $\quad \Delta\omega = \frac{P_0}{2\pi\, 2f_G} \frac{1}{\bar{\omega}\, J_M}$



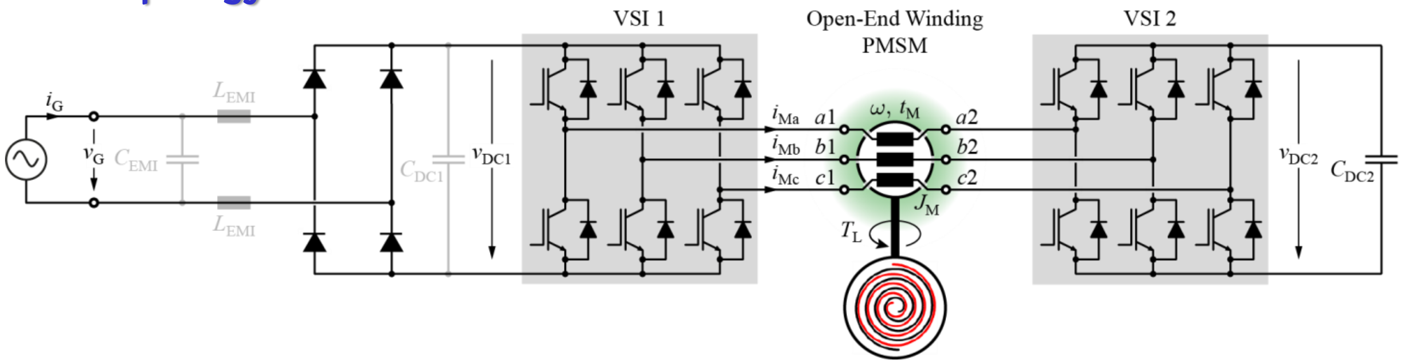
→ Electrolytic-Less 1Φ AC-Supplied VSD System

Outline

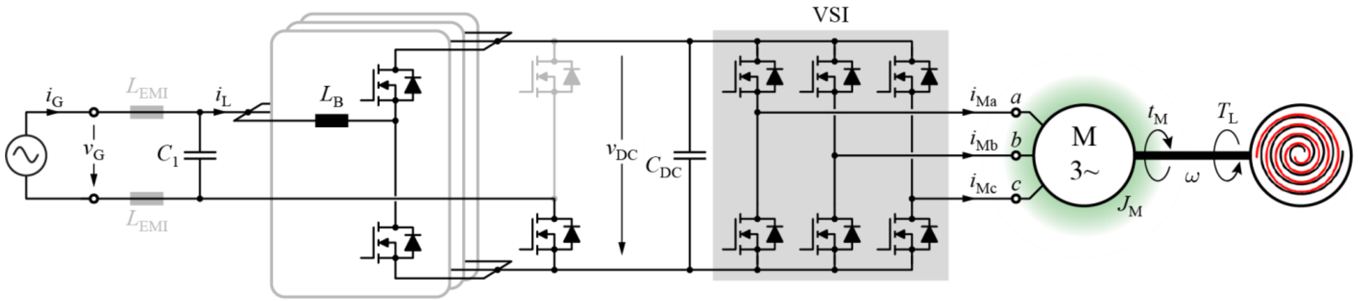
Part I: Single-Inverter Topology



Part II: Dual-Inverter Topology



Part I
Single-Inverter (SI) Topology



SI – Topology

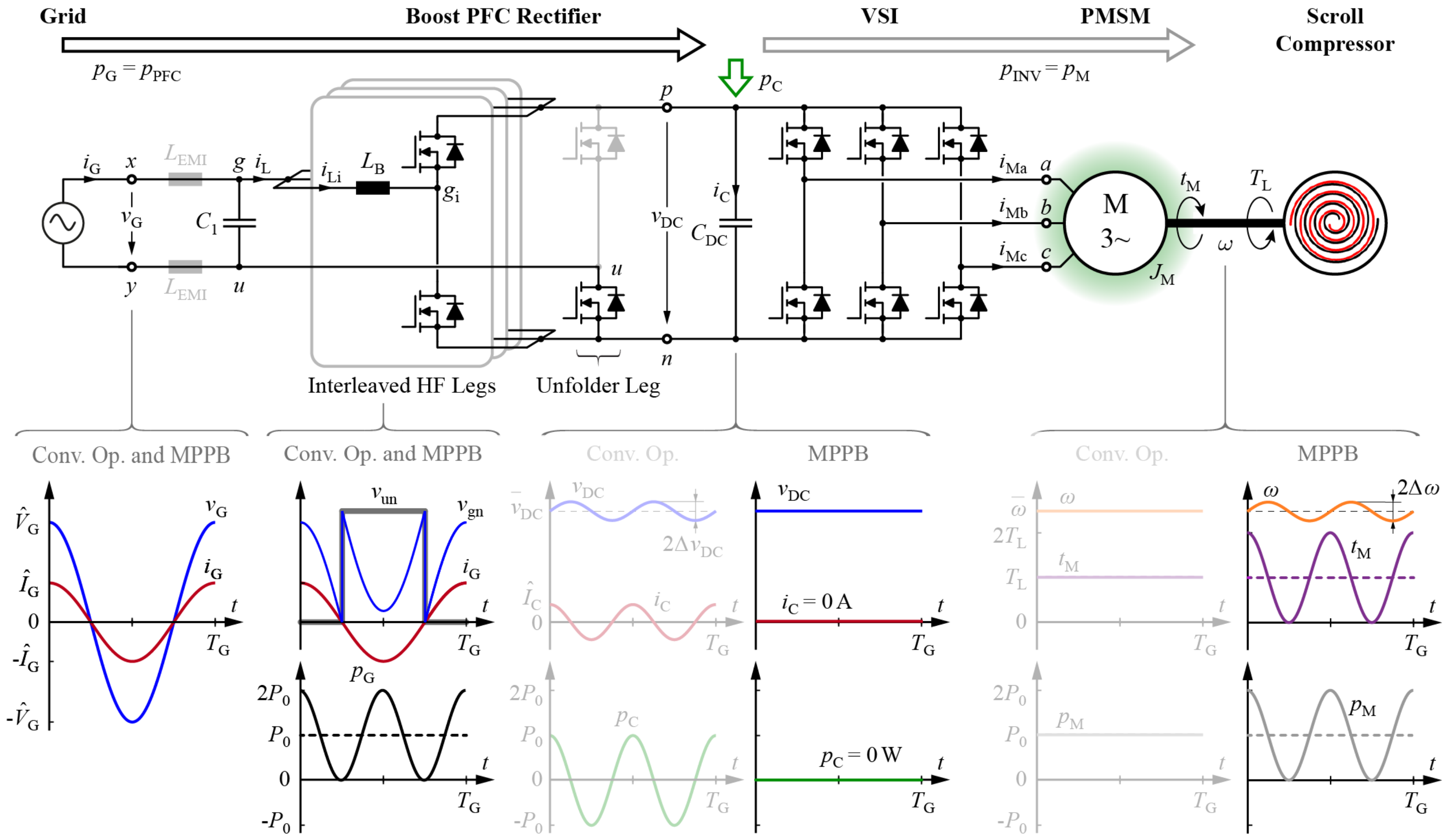
- **Two-Stage Implementation**

- **I. PFC Rectifier**
  - Boost-Type
  - Totem-Pole with Unfolder Leg
  - Three Interleaved HF Legs

- **Intermediate DC-Link**
  - Electrolytic-Less
  - Nominal: 650 Vdc
  - Maximum: 800 Vdc

→ 1.2 kV SiC MOSFETs

- **II. Three-Phase Inverter**
  - Two-Level
  - Voltage Source Inverter (VSI)

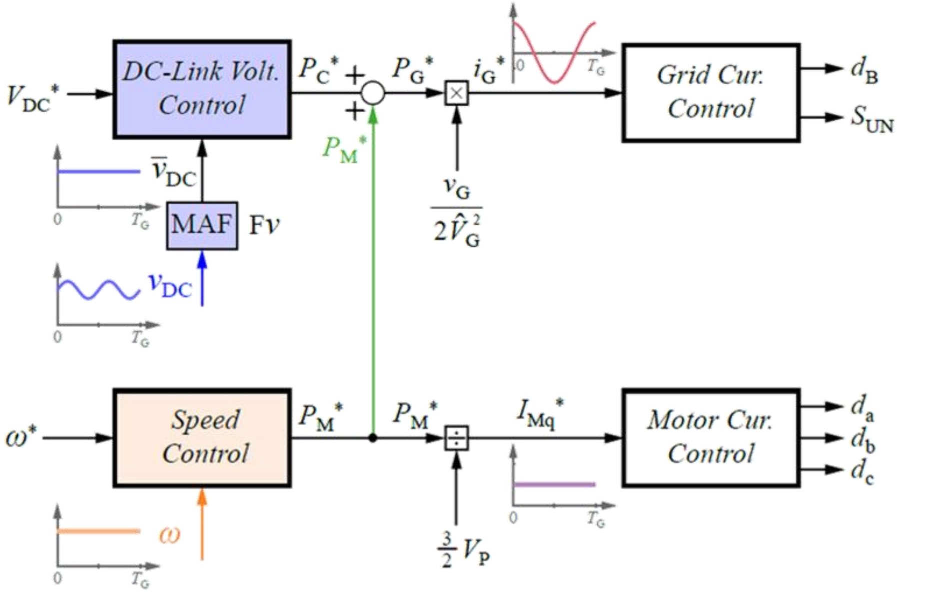


→ How to Control?

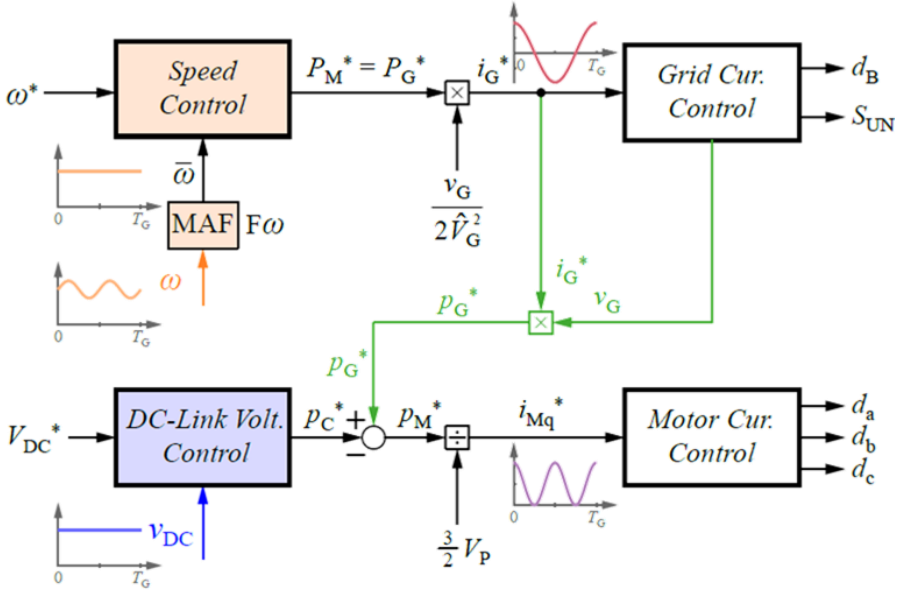
SI – Control (1)

- **Control Objectives: PFC Operation, DC-Link Voltage and Average Speed Control**
  - Implemented in Cascaded Fashion
  - Based on **Grid Power Feedforward** and **Inner Current Control Loops**

- **Conventional Operation**
  - Electrical Energy Storage C_{DC} $\quad \Delta v_{DC} = \frac{P_0}{2\pi\, 2 f_G} \frac{1}{\bar{v}_{DC}\, C_{DC}}$



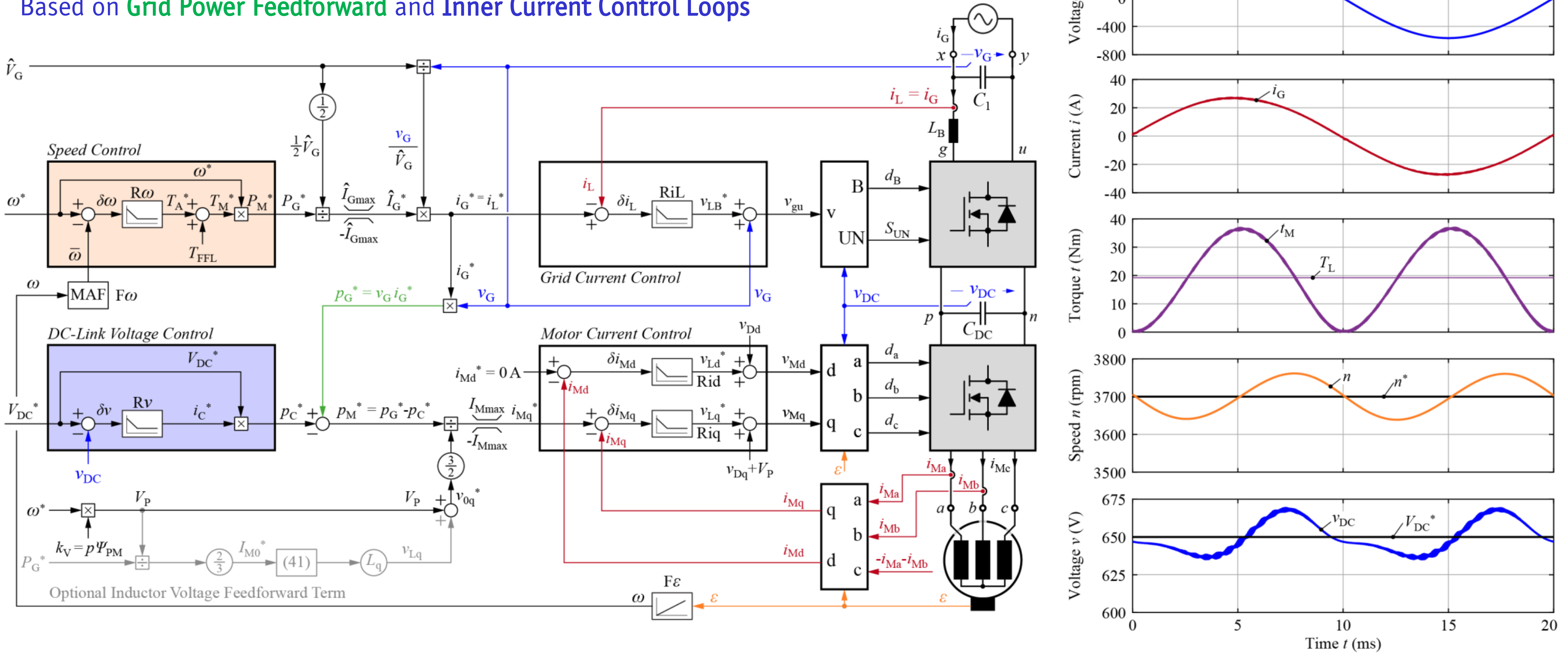
- **Proposed MPPB Operation**
  - Mechanical Energy Storage J_M $\quad \Delta\omega = \frac{P_0}{2\pi\, 2 f_G} \frac{1}{\bar{\omega}\, J_M}$



→ MPPB Operation: Achieved by High-Level Control Scheme Modifications

SI – Control (2)

- **Control Objectives:** PFC Operation, DC-Link Voltage and Average Speed Control
- Implemented in Cascaded Fashion
- Based on **Grid Power Feedforward** and **Inner Current Control Loops**



→ Verified by Circuit Simulation for C_{DC} = 60 µF - only 8 µF/kW

→ Voltage / Speed Ripple $34\,V_{pkpk}$ / $120\,rpm_{pkpk}$

Performance Analysis

Source: Siemens

SI – Comparative Phase Current Analysis

- **Conventional System** ($i_{\mathrm{Md}} = 0$ A)
  - Torque-Generating Current

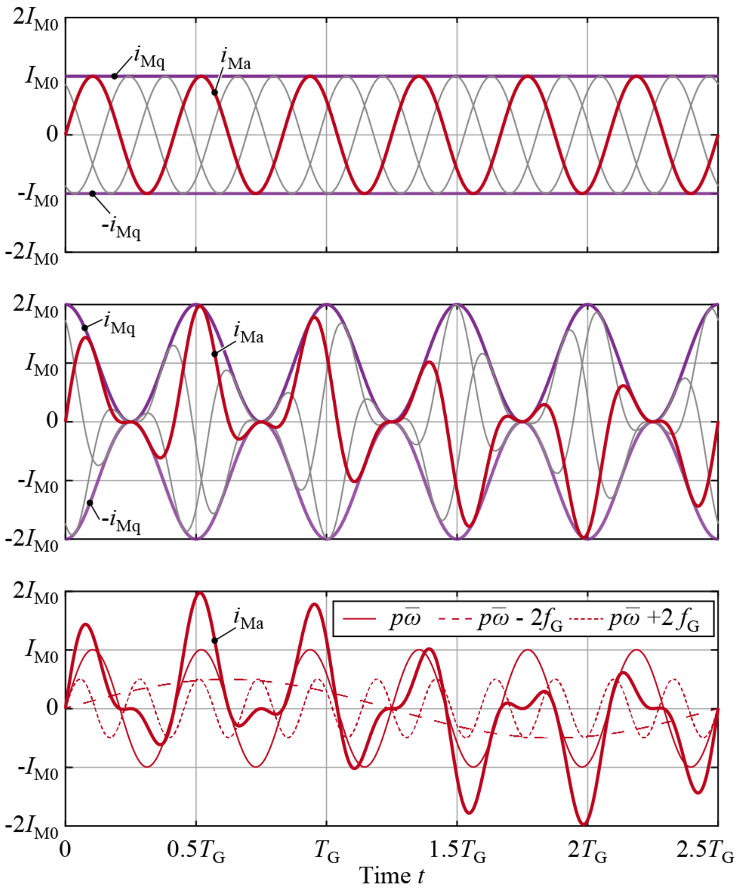
$$i_{\mathrm{Mq}} = I_{\mathrm{M0}} = \frac{2P_0}{3V_\mathrm{P}} \sim T_\mathrm{L}$$

- **Electrolytic-Less MPPB** ($i_{\mathrm{Md}} = 0$ A)
  - Torque-Generating Current

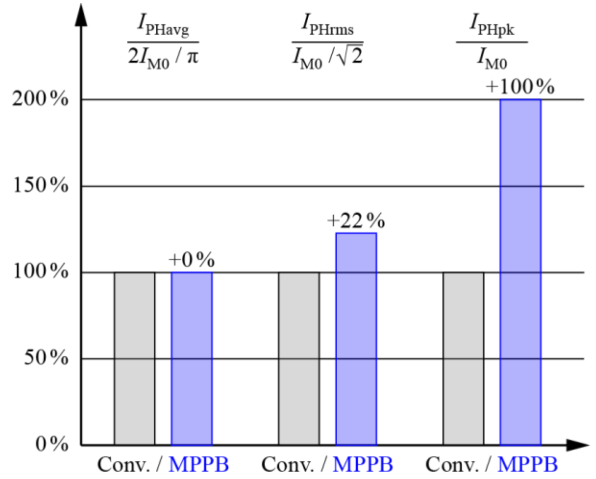
$$i_{\mathrm{Mq}} = I_{\mathrm{M0}}\,[1 + \cos(4\pi f_\mathrm{G}\, t)] \sim t_\mathrm{M}$$

- **dq-Transformation** with $\varepsilon = p\varpi\, t$

$$\begin{bmatrix} i_{\mathrm{Ma}} \\ i_{\mathrm{Mb}} \\ i_{\mathrm{Mc}} \end{bmatrix} = \begin{bmatrix} \cos(\varepsilon) & \sin(\varepsilon) \\ \cos(\varepsilon - 2\pi/3) & \sin(\varepsilon - 2\pi/3) \\ \cos(\varepsilon + 2\pi/3) & \sin(\varepsilon + 2\pi/3) \end{bmatrix} \cdot \begin{bmatrix} i_{\mathrm{Md}} \\ i_{\mathrm{Mq}} \end{bmatrix}$$



- **Comparison**



Source: Siemens

- **Superposition:** $i_{\mathrm{Ma}} = -I_{\mathrm{M0}}\left[\sin(p\varpi\, t) + \frac{1}{2}\sin(p\varpi\, t + 4\pi f_\mathrm{G}\, t) + \frac{1}{2}\sin(p\varpi\, t - 4\pi f_\mathrm{G}\, t)\right]$

→ **Harmonic Components @ $p\varpi$, $p\varpi + 4\pi f_\mathrm{G}$ and $p\varpi - 4\pi f_\mathrm{G}$**

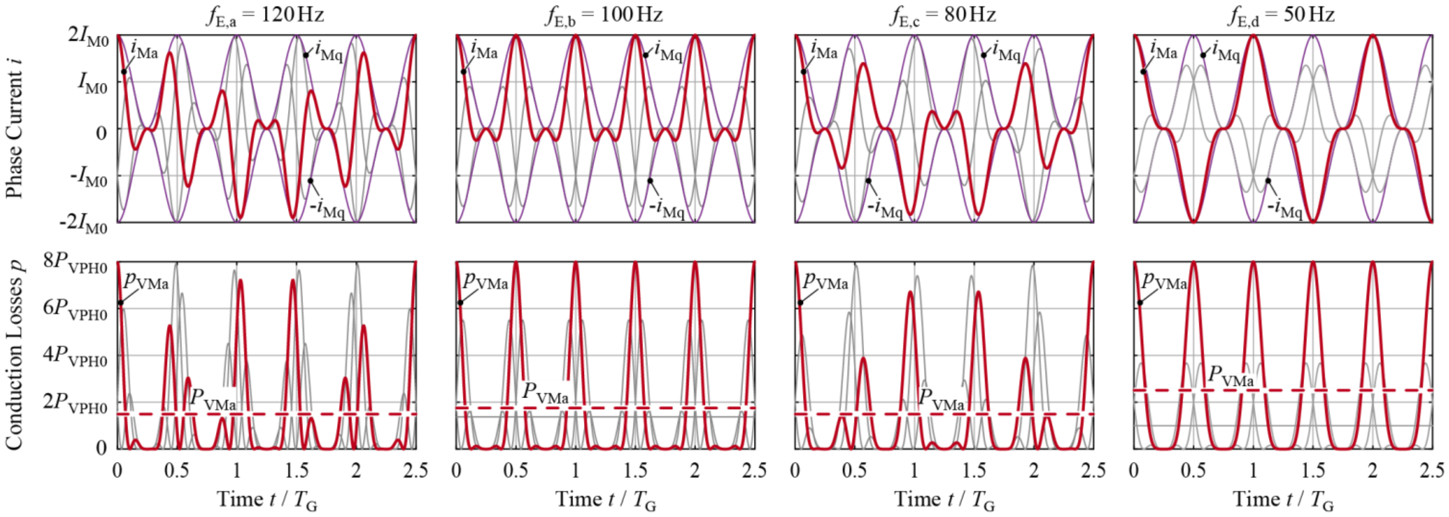
SI – Phase Conduction Losses

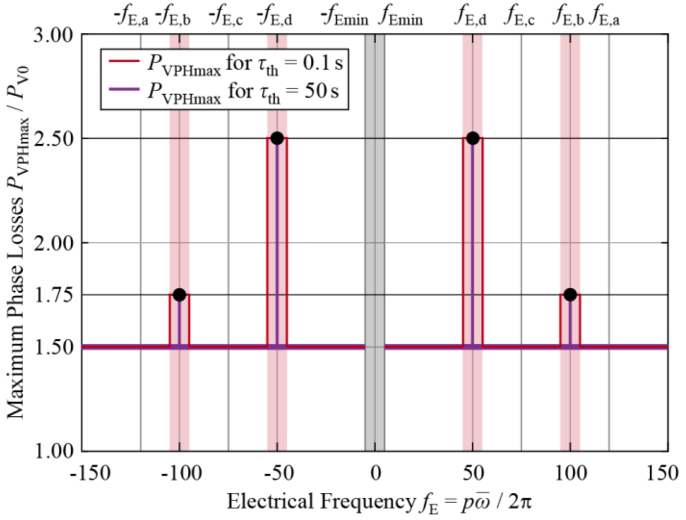
- Harmonic Components: $p\bar{\omega}$, $p\bar{\omega} + 4\pi f_G$ and $p\bar{\omega} - 4\pi f_G$

- **Standing Waves** for $p\bar{\omega} = 4\pi f_G$ (100 Hz) and $p\bar{\omega} = 2\pi f_G$ (50 Hz)
- Similar to Startup

- Asymmetric Phase Stresses

→ Restricted Frequency Ranges





- Total Conduction Losses Remain

→ **Degree of Freedom: Number of Pole Pairs p**

SI – Performance Analysis: Motor and Inverter

- **M. Motor**
  - Conventional System $P_{\mathrm{VM0}} = P_{\mathrm{VMnl}} + \frac{3}{2} R_s I_{\mathrm{M0}}^2$
  - Electrolytic-Less MPPB $P_{\mathrm{VM}} = P_{\mathrm{VMnl}} + \frac{9}{4} R_s I_{\mathrm{M0}}^2$
  - Relative Loss Increase + 25 %

- **I. IGBT Inverter**

  $$P_{\mathrm{VI}} = 3 V_{\mathrm{f}} I_{\mathrm{PHavg}} + 3 f_{\mathrm{Isw}} k_1 I_{\mathrm{PHavg}}$$

  - No Additional Losses - High Total Losses

- **II. MOSFET Inverter with dv/dt-Limitation (Miller Capacitor)**

  $$P_{\mathrm{VI}} = 3 R_{\mathrm{on}} I_{\mathrm{PHrms}}^2 + 3 f_{\mathrm{Isw}} \left(k_0 + k_1 I_{\mathrm{PHavg}}\right)$$

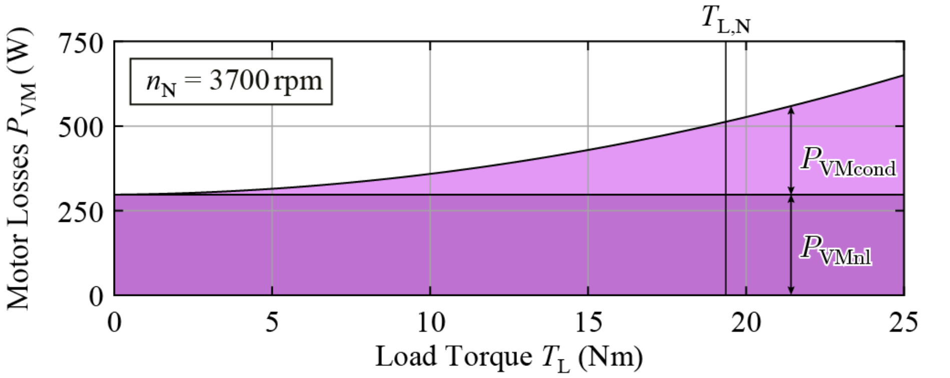
  - Relative Loss Increase + 17 %

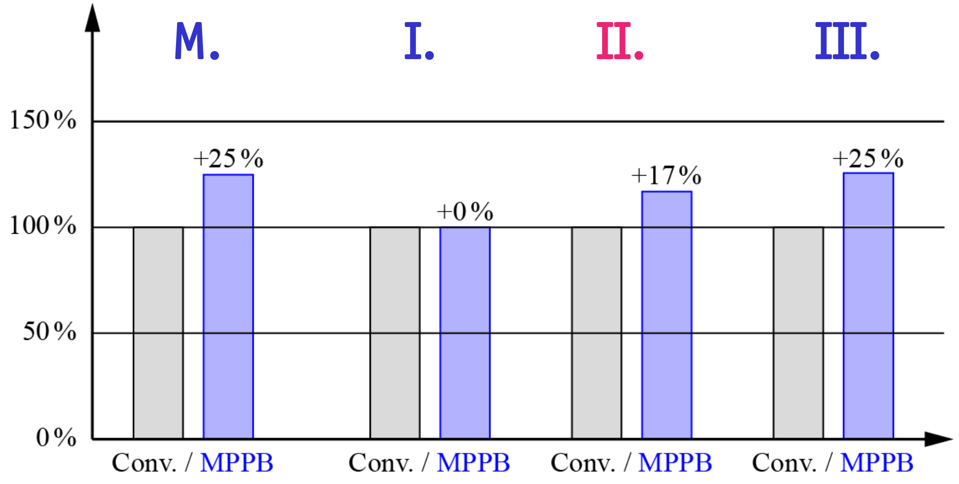
- **III. MOSFET Inverter with LC-Output-Filter**

  $$P_{\mathrm{VI}} = 3 R_{\mathrm{on}} I_{\mathrm{PHrms}}^2 + 3 f_{\mathrm{Isw}} \left(k_0 + k_1 I_{\mathrm{PHavg}} + k_2 I_{\mathrm{PHrms}}^2\right)$$

  - Relative Loss Increase + 25 %
  - Peak Phase Current + 100 %

→ Implement and Verify Hardware Demonstrator

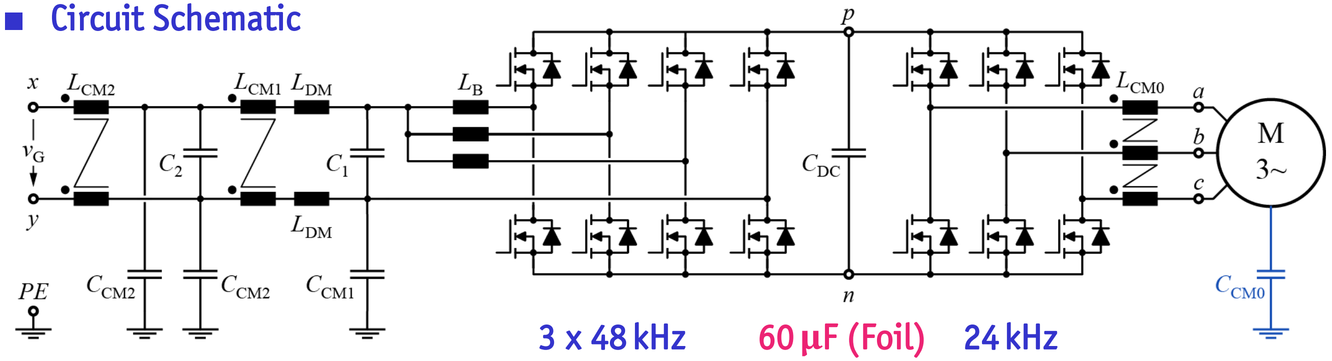




Implementation and Verification

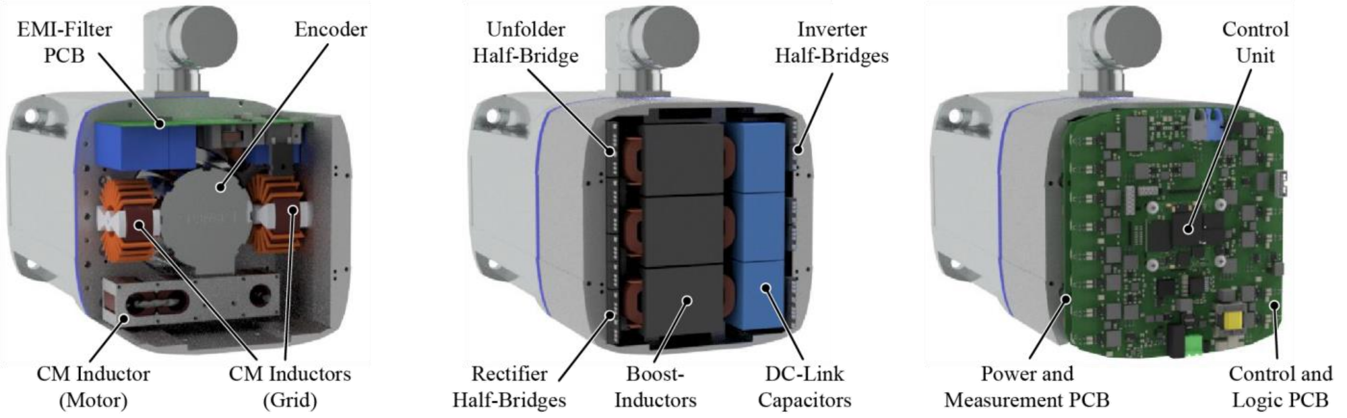
SI – Implementation

■ Circuit Schematic

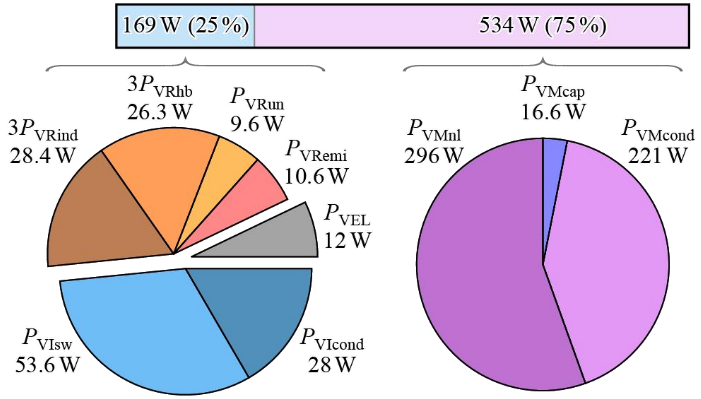


3 x 48 kHz   60 µF (Foil)   24 kHz

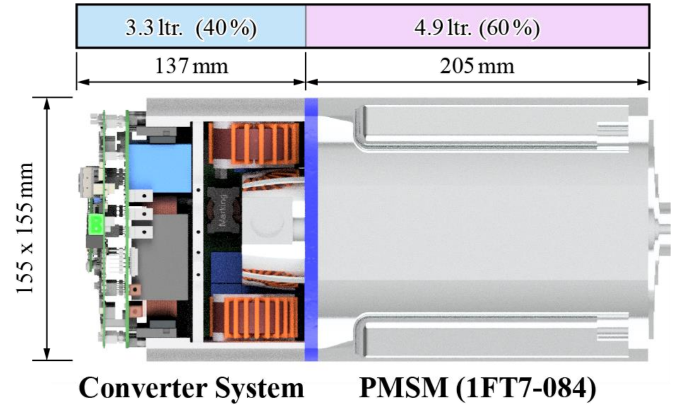
■ Motor Integration in Three Layers



■ Losses: 703 W (91.4 %)



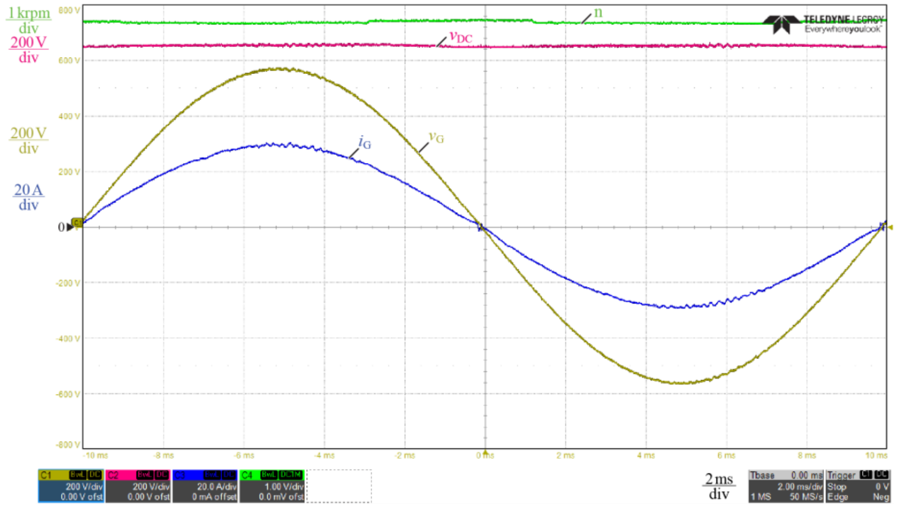
■ Volume: 8.2 ltr. (0.91 kW/ltr.)

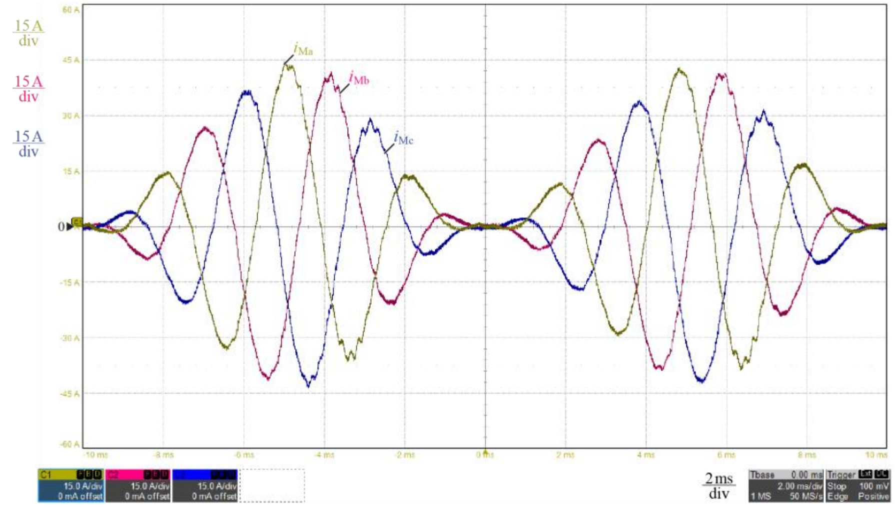


→ Drive System Performance: 0.91 kW/ltr. and 91.4 % @ 7.5 kW - IES2 Compliant

SI – Hardware Demonstrator

- Motor-Integrated Electrolytic-Less 1Φ AC-Supplied VSD System
- Time-Domain Waveforms at Nominal Operating Point
- Verification on Motor Test Bench (Specifically Developed)



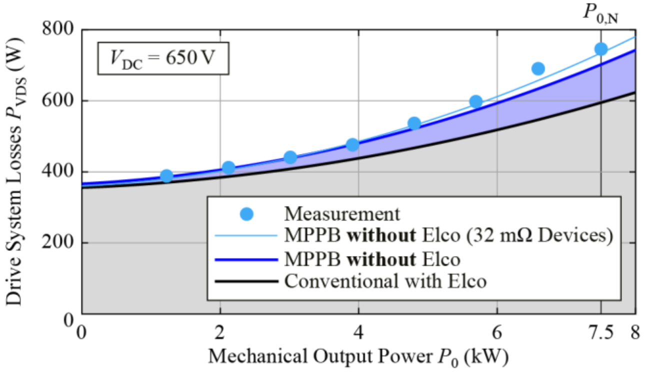


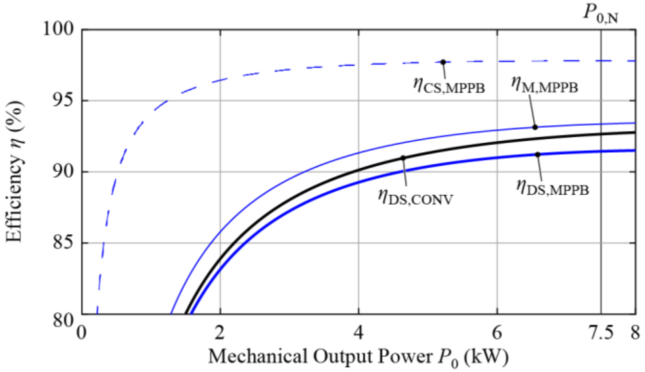
→ Demonstrator Matches Expected System Behavior

→ Verify Design Models

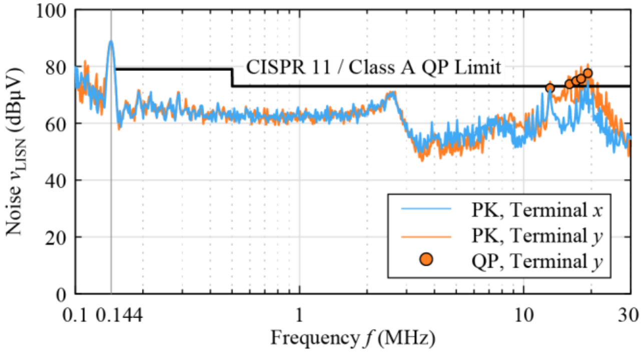
SI – Design Models

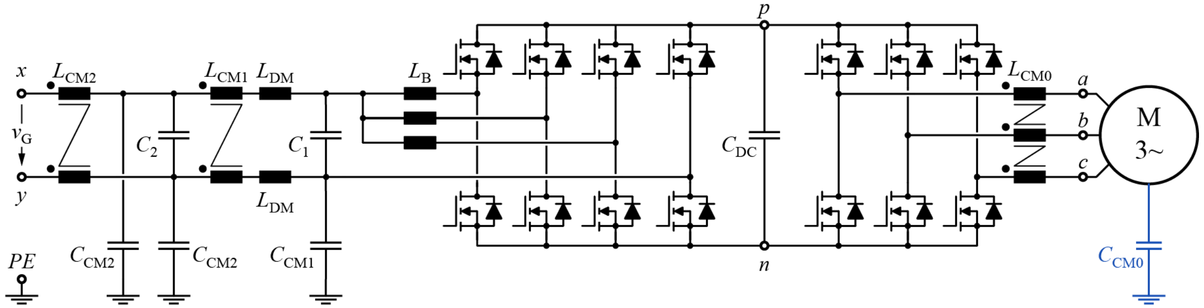
- **Loss Model**
- Conventional System 600 W (92.6 %)
- Electrolytic-Less MPPB 703 W (91.4 %)
- Drive System Efficiency >90 % for P_0 > 5 kW





- **EMI-Model**
- CISPR 11 / **Class A**
- DM-Noise: PFC Rectifier @ 144 kHz
- CM-Noise: Inverter @ 168 kHz

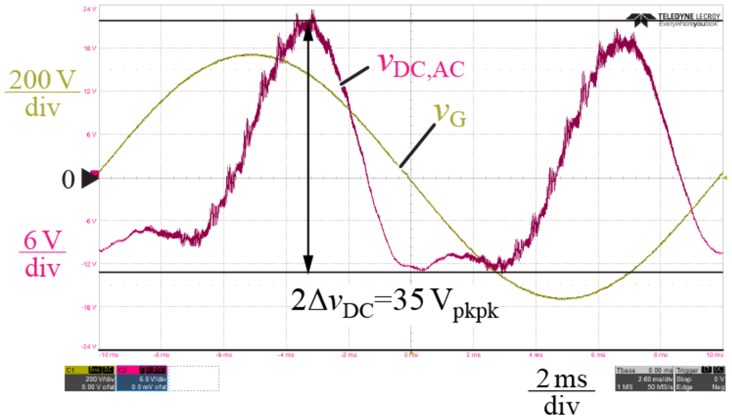




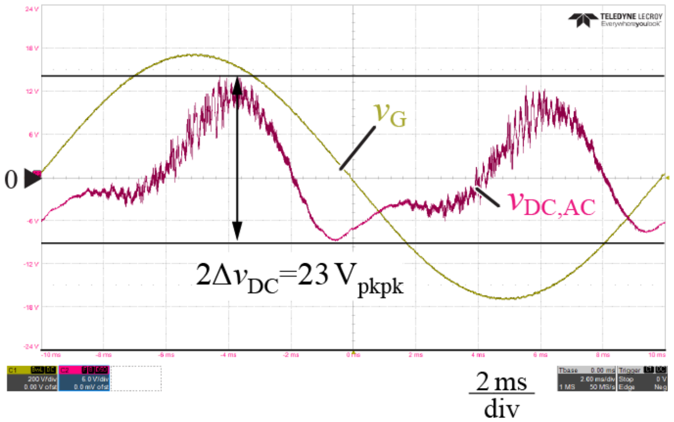
→ In-Depth Model Verification - 103 W of Additional Losses to Eliminate 1 ltr. of Electrolytic Capacitors

SI – DC-Link Voltage Ripple

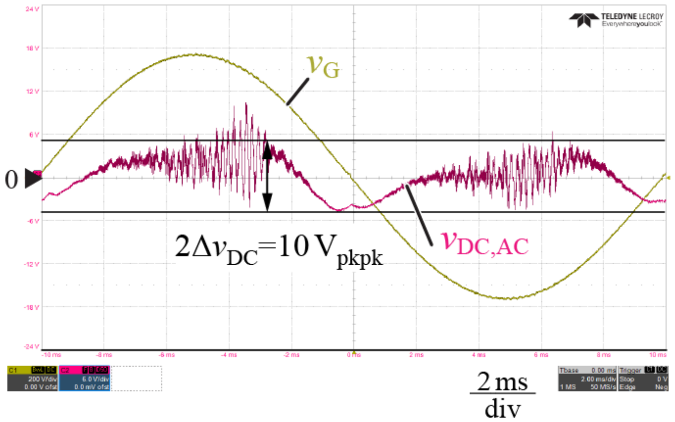
■ **LF DC-Link Voltage Fluctuations: 35 V**
- Caused by Disturbances



■ **Delay Time Reduction: 23 V**
- **Improve Controller Bandwidth**

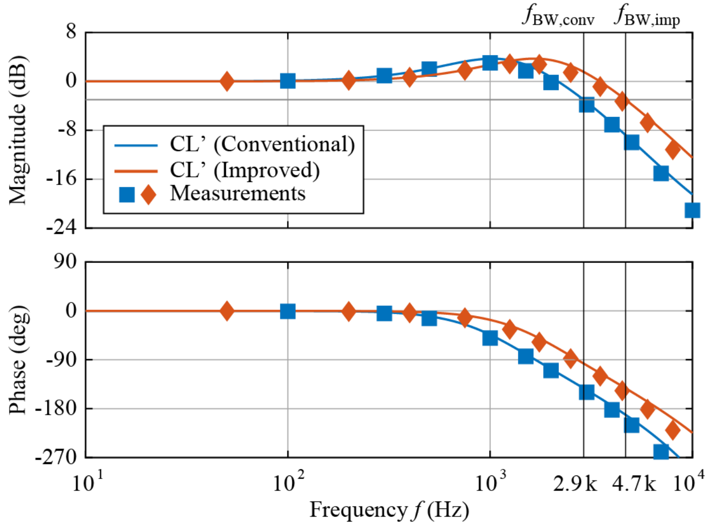


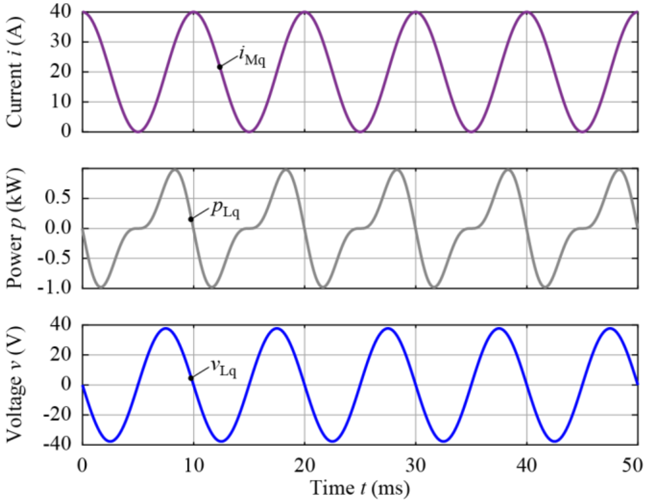
■ **Feedforward Term: 10 V**
- **Counteract Motor Magnetization Power**



- DC-Link Voltage Ripple matches Simulation
- Increase C_{DC} = 60 µF
- Increase f_{sw} = 24 kHz

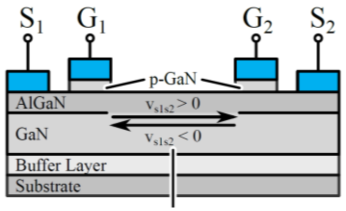
→ **Efficiency, Power Density or Cost Penalty**





→ **Analyze Grid Interruption Sustainability**

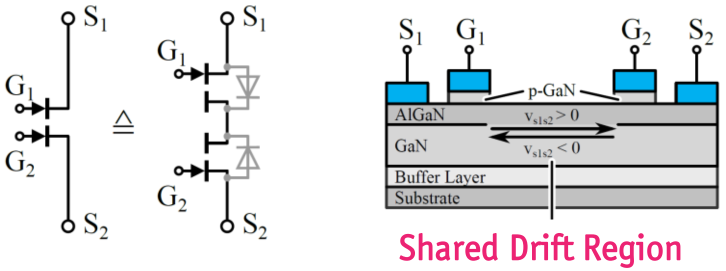
Current Source Based System



Shared Drift Region

SI – Current DC-Link: Topology

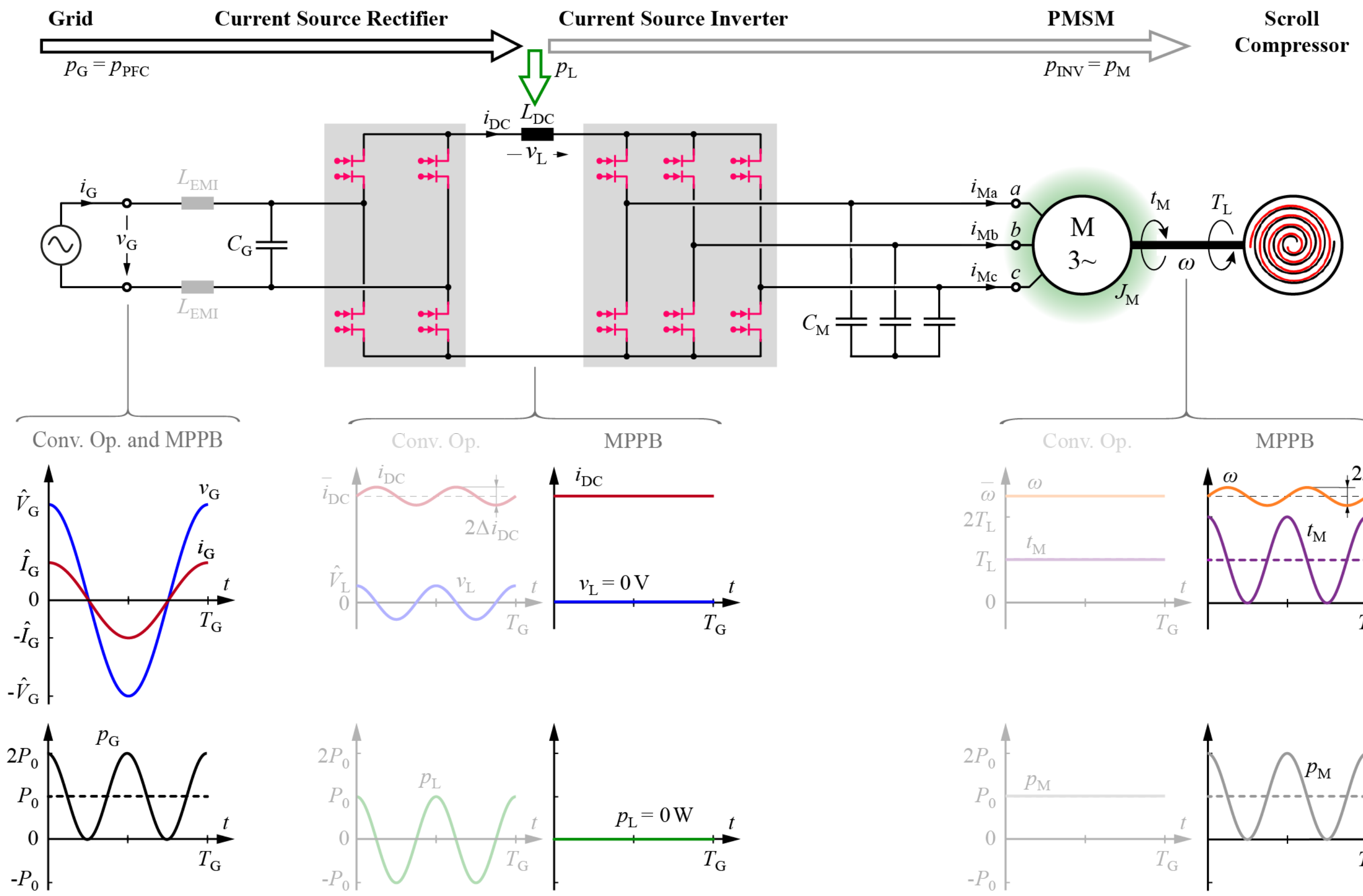
■ Monolithic Bidirectional GaN Transistor



■ Two-Stage Implementation
- Current DC-Link
- 1AC PFC Current Source Rectifier (CSR)
- Three-Phase Current Source Inverter (CSI)

■ Specifications
- 1AC: 230V/50Hz
- Motor: 2.5kW @ 300rad/s

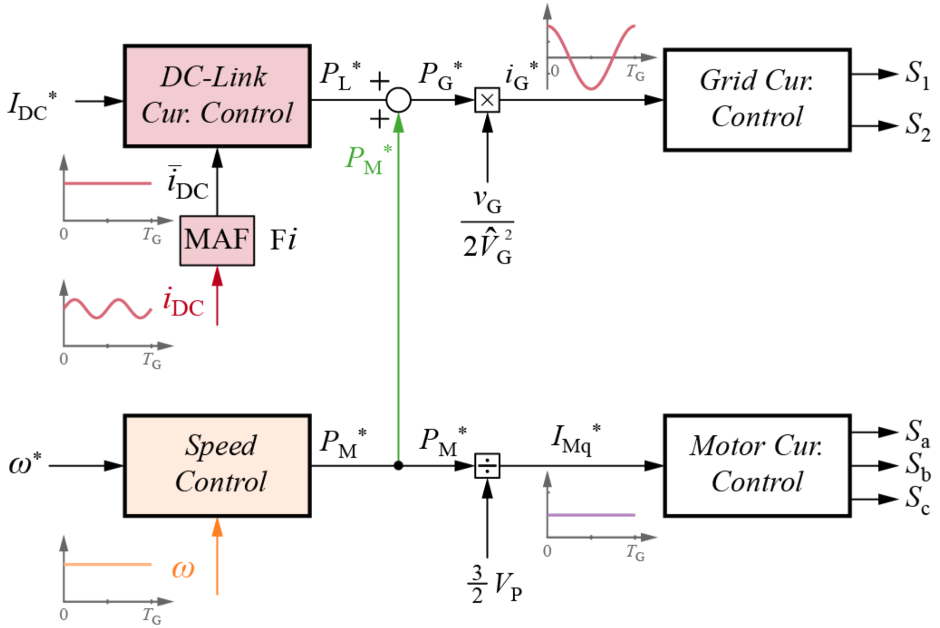
→ How to Control?



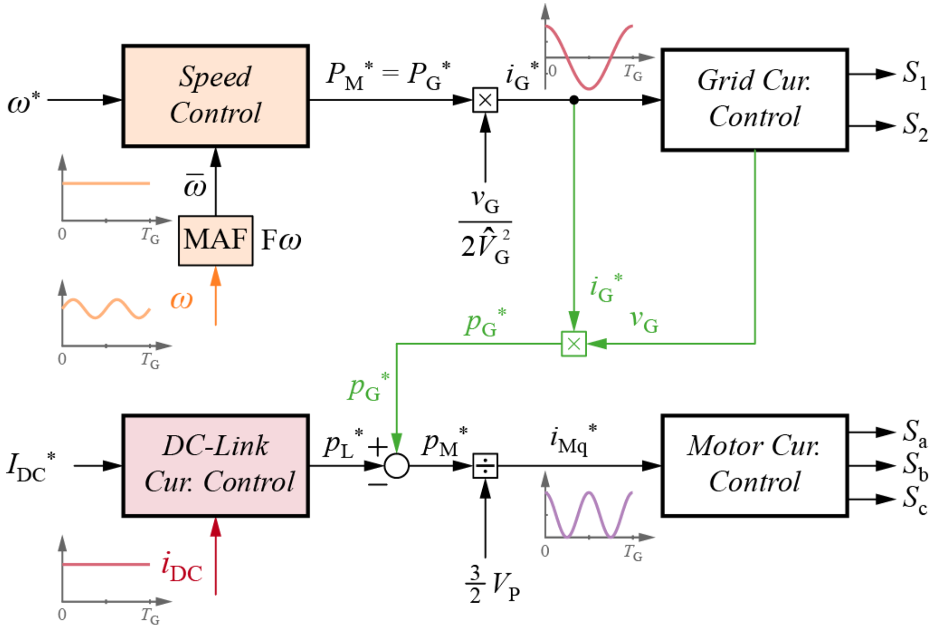
SI – Current DC-Link: Control (1)

- **Control Objectives: PFC Operation, DC-Link Current and Average Speed Control**
  - Implemented in Cascaded Fashion
  - Based on **Grid Power Feedforward** and **Inner Current Control Loops**

- **Conventional CSI Operation**
  - Electrical Energy Storage L_{DC} $\quad \Delta i_{DC} = \frac{P_0}{2\pi\, 2f_G} \frac{1}{\bar{i}_{DC} L_{DC}}$



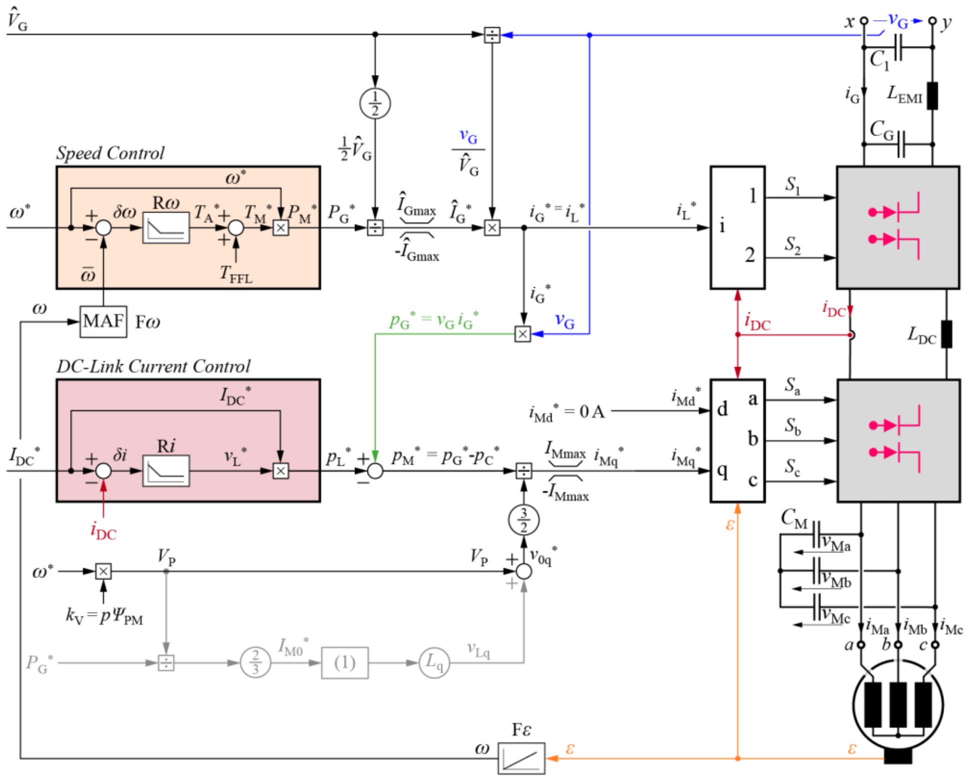
- **Proposed MPPB CSI Operation**
  - Mechanical Energy Storage J_M $\quad \Delta\omega = \frac{P_0}{2\pi\, 2f_G} \frac{1}{\bar{\omega}\, J_M}$

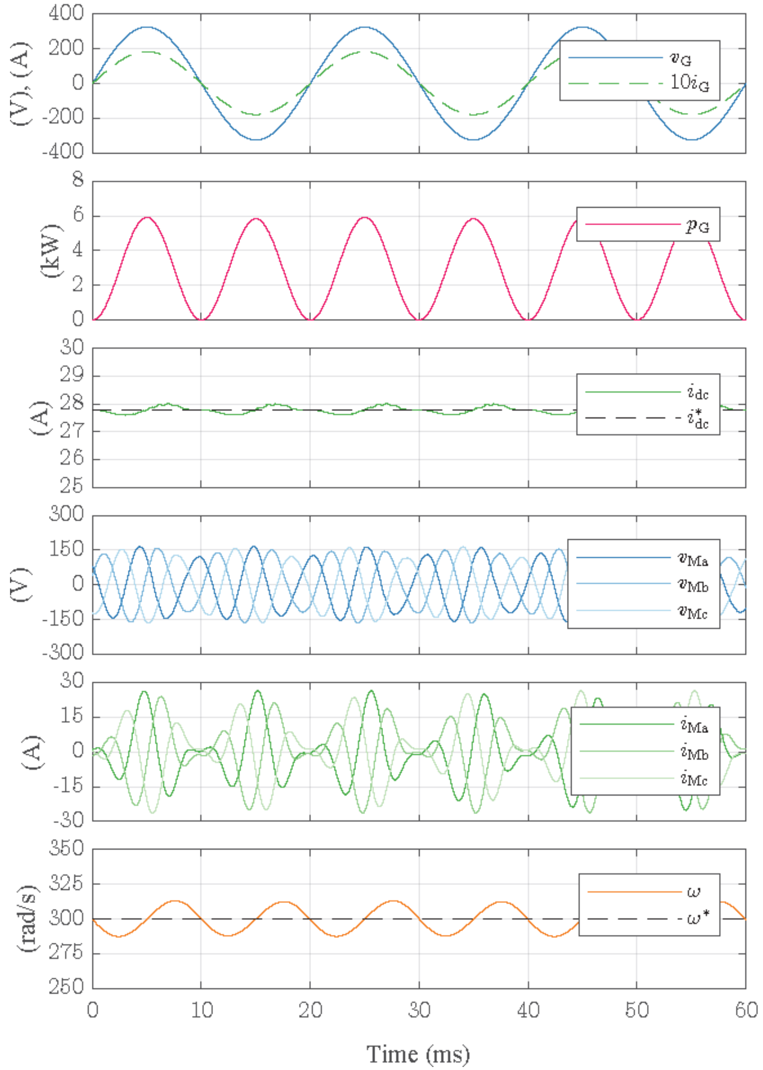


→ **MPPB CSI Operation: Achieved by High-Level Control Scheme Modifications**

SI – Current DC-Link: Control (2)

- Control Objectives: PFC Operation, DC-Link Current and Average Speed Control
  - Implemented in Cascaded Fashion
  - Based on Grid Power Feedforward and Inner Current Control Loops

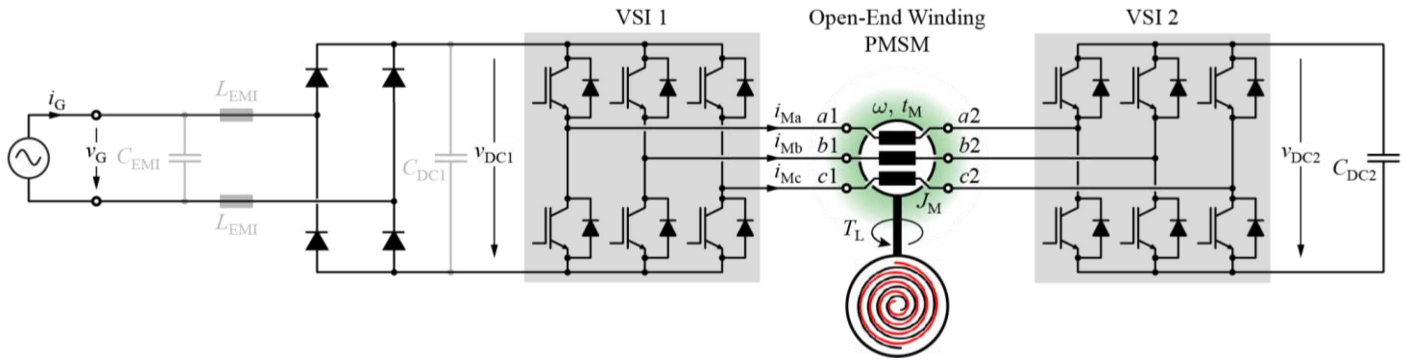




→ MPPB Concept Enables CSI for 1AC Supplied Drives: L_{DC} = 1mH - only 0.4 mH/kW (Conventional Operation Requires Unrealistic 700mH)

Part II

Dual-Inverter (DI) Topology



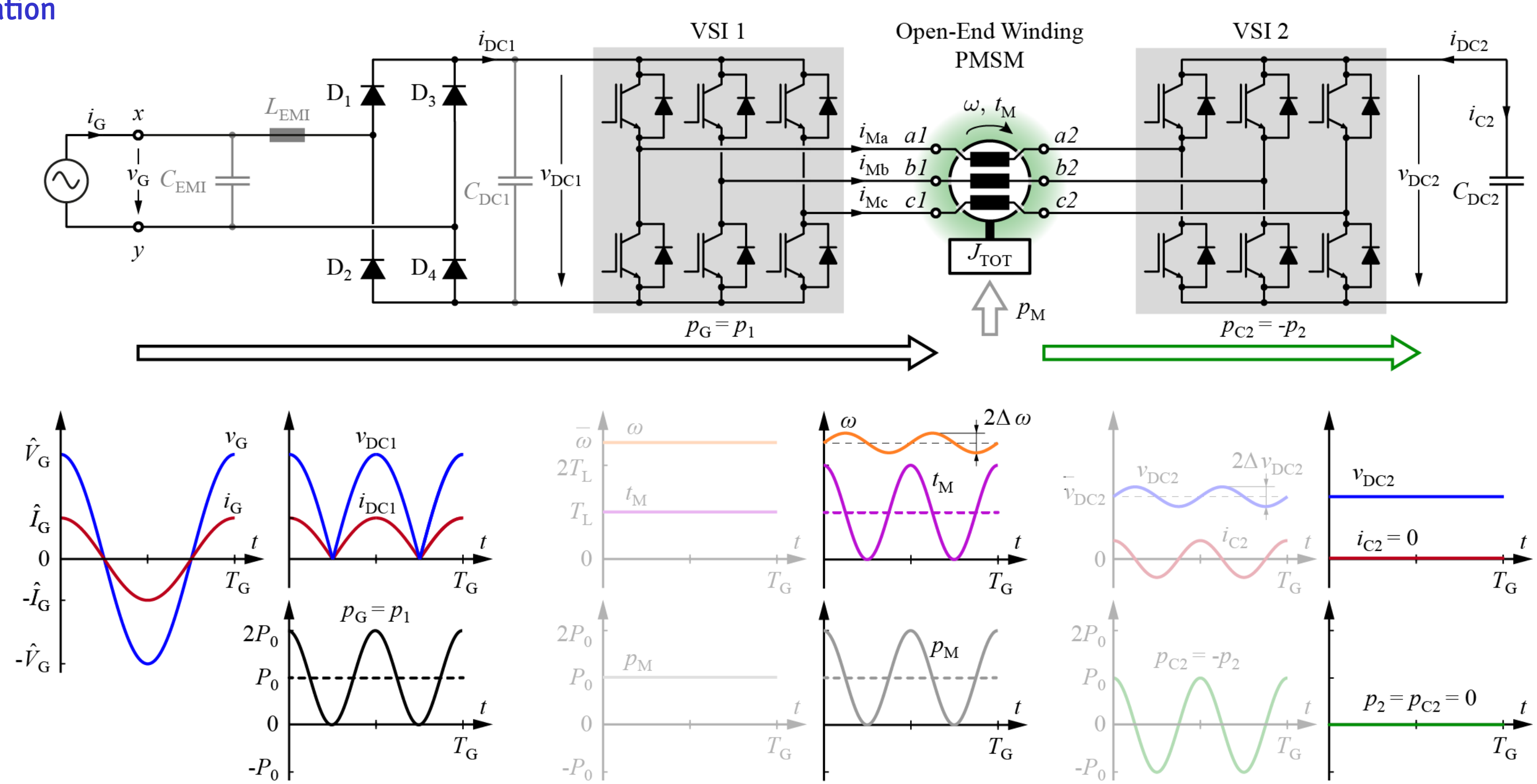
DI – Topology

- **Dual-Inverter Implementation**

- **Avoids Boost Stage**
  - No Boost Inductor
  - No HF Bridge-Legs
  - Power Buffer Required

- **Apply MPPB Concept**
  - Electrolytic-Less

- **Implementation Effort**
  - Diodes
  - IGBT Six-Pack Modules
  - Film Capacitors
  - OEW PMSM

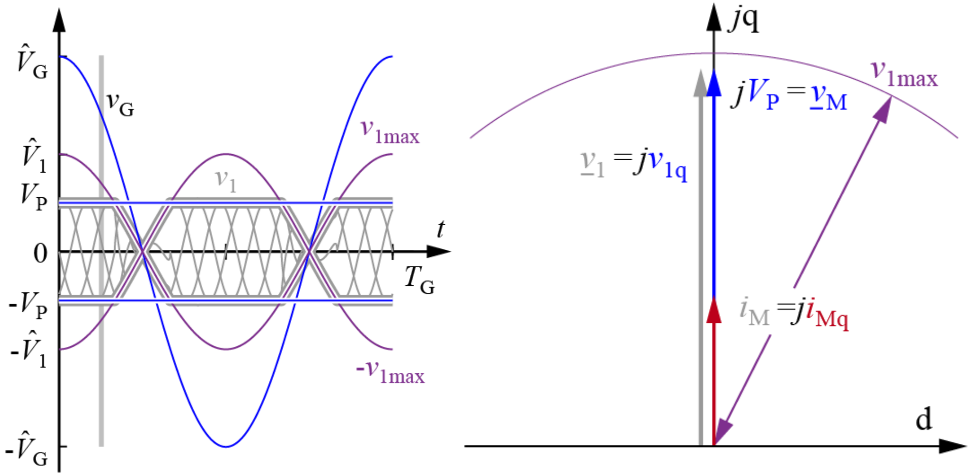


→ **Investigate Operation to Ensure $p_2(t) = 0\ \mathrm{W}$**

DI – Operation

- Ensure $p_2(t) = \underline{v}_2 \cdot \underline{i}_\mathrm{M} = 0\ \mathrm{W}$ (Space Vector Representation)

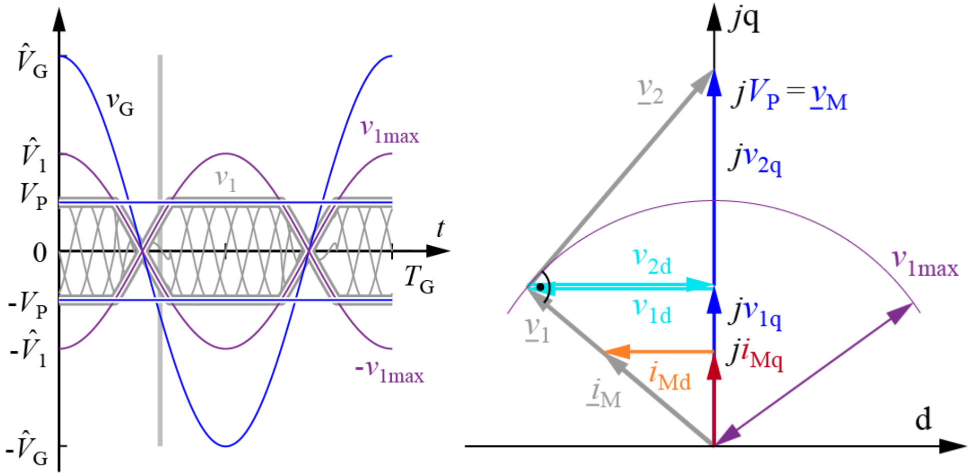
- Case I: $V_\mathrm{P} < v_{1\mathrm{max}}(t) = 0.5\,|v_\mathrm{G}(t)|$
- Ensure $\underline{v}_2 = 0\ \mathrm{V}$ and $\underline{v}_1 = \mathrm{j}\,V_\mathrm{P}$



- VSI 2 Provides No Voltage
- Zero d-Current Component

→ Performance Analysis

- Case II: $V_\mathrm{P} \geq v_{1\mathrm{max}}(t) = 0.5\,|v_\mathrm{G}(t)|$
- Ensure $\underline{v}_2 \perp \underline{i}_\mathrm{M}$ and $\underline{v}_1 = \mathrm{j}\,V_\mathrm{P} - \underline{v}_2$

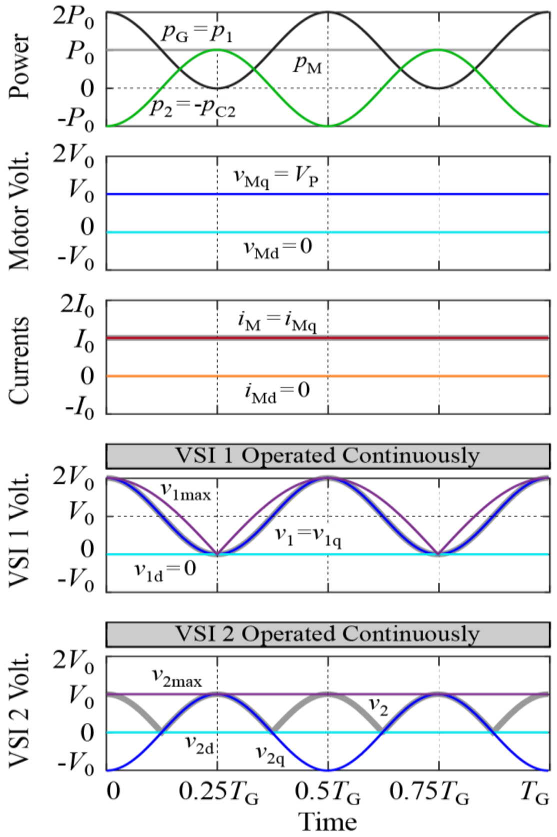


→ Select $|\underline{v}_1| = v_{1\mathrm{max}}$ and $\underline{v}_1 \parallel \underline{i}_\mathrm{M}$
- VSI 2 Provides Required Voltage Difference but No Active Power
- Non-Zero d-Current Component

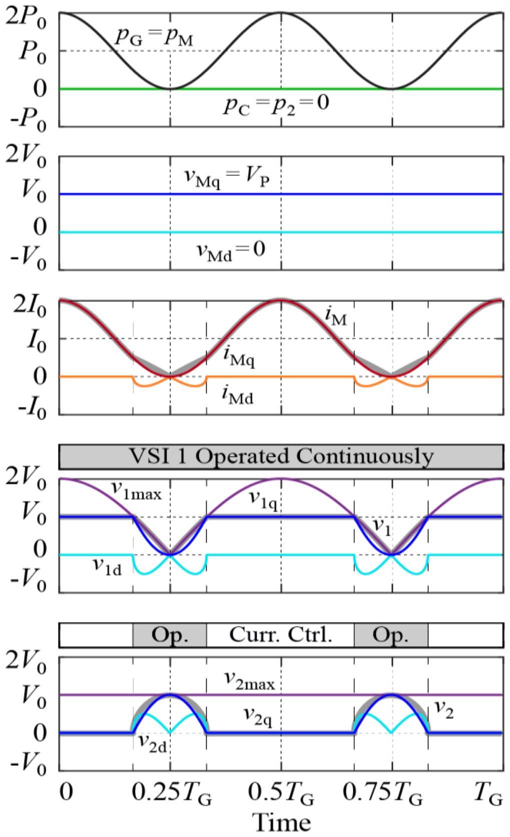
DI – Phase Current Stress

For V_{Gmin} = 360 Vrms

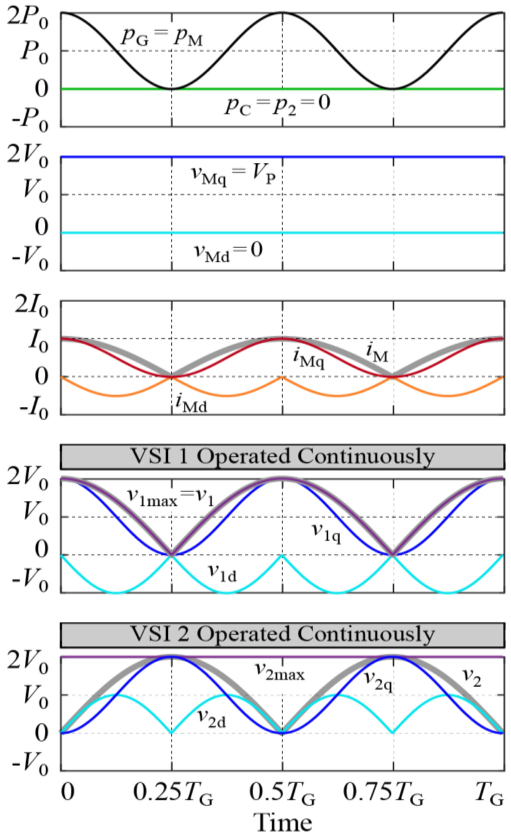
- **Implementation With Electrolytic Capacitors**
  - For $V_{\mathrm{P}} = V_0 = 125\,\mathrm{V}$ - **Grid Voltage Limit**
  - $I_{\mathrm{PH0rms}} = 33\,\mathrm{A}$



- **Electrolytic-Less MPPB Implementation**
  - For $V_{\mathrm{P}} = V_0 = 125\,\mathrm{V}$
  - $I_{\mathrm{PHrms}} = 41\,\mathrm{A}$

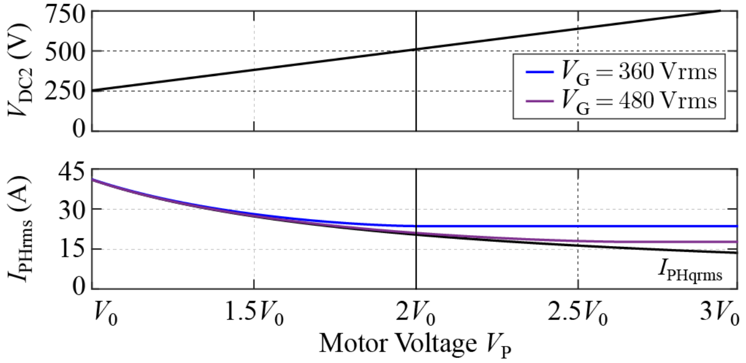


- **Electrolytic-Less MPPB Implementation**
  - For $V_{\mathrm{P}} = 2V_0 = 250\,\mathrm{V}$
  - **$I_{\mathrm{PHrms}} = 24\,\mathrm{A}$**



DI – Performance Evaluation

- **Degree of Freedom: Motor Voltage V_P**
- Influence on
  - **Secondary DC-Link Voltage V_{DC2}**
  - **Phase Current Stress I_{PHrms}**



- **System Specifications**
  - Mech. Output Power 7.5 kW
  - Mech. Speed 3700 rpm
  - Grid Voltage 360…480 Vrms
  - Grid Frequency 50 Hz
  - Switching Frequency 16 kHz

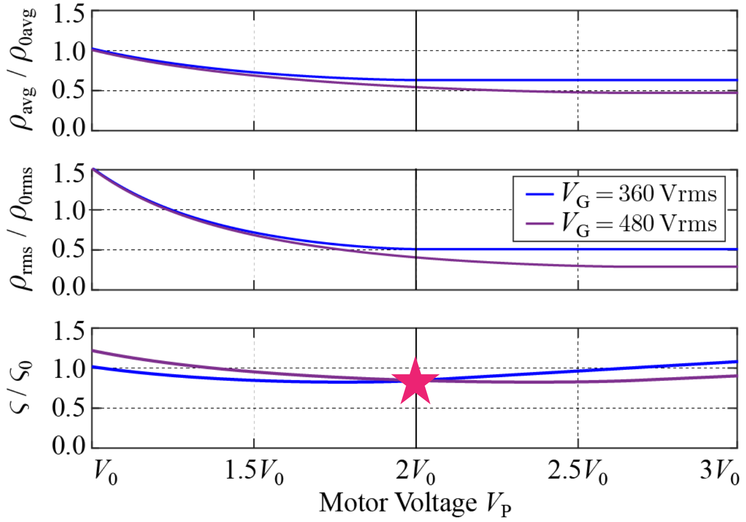
- **Performance Indices**
  - Conduction Losses

$$\rho_{avg} = \sum_k (I_{Davg,k} + I_{Tavg,k})$$

$$\rho_{rms} = \sum_k (I^2_{Drms,k} + I^2_{Trms,k})$$

  - Switching Losses

$$\varsigma = \sum_k \langle v_{T,k} + i_{T,k} \rangle_{T_G}$$

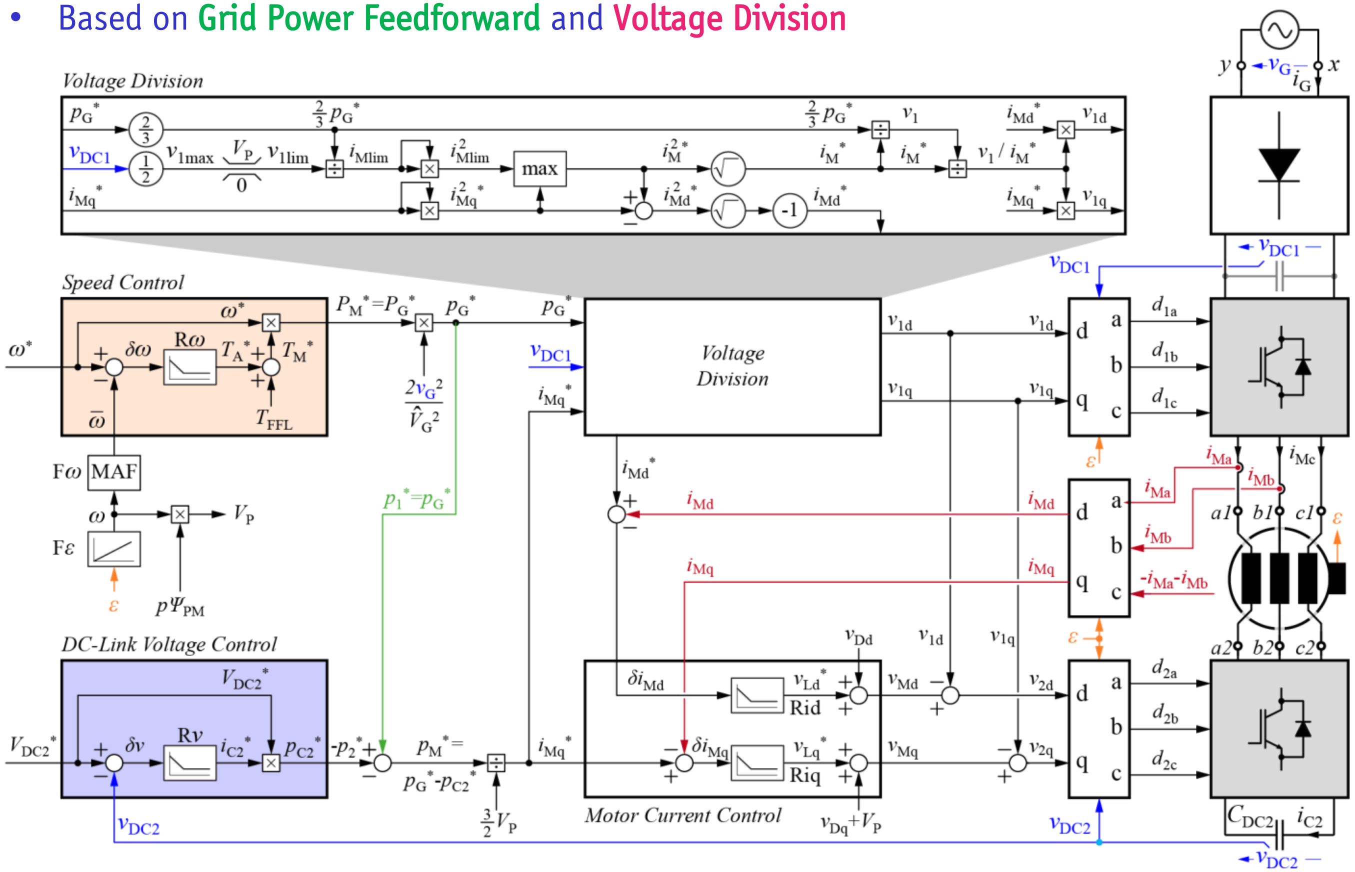


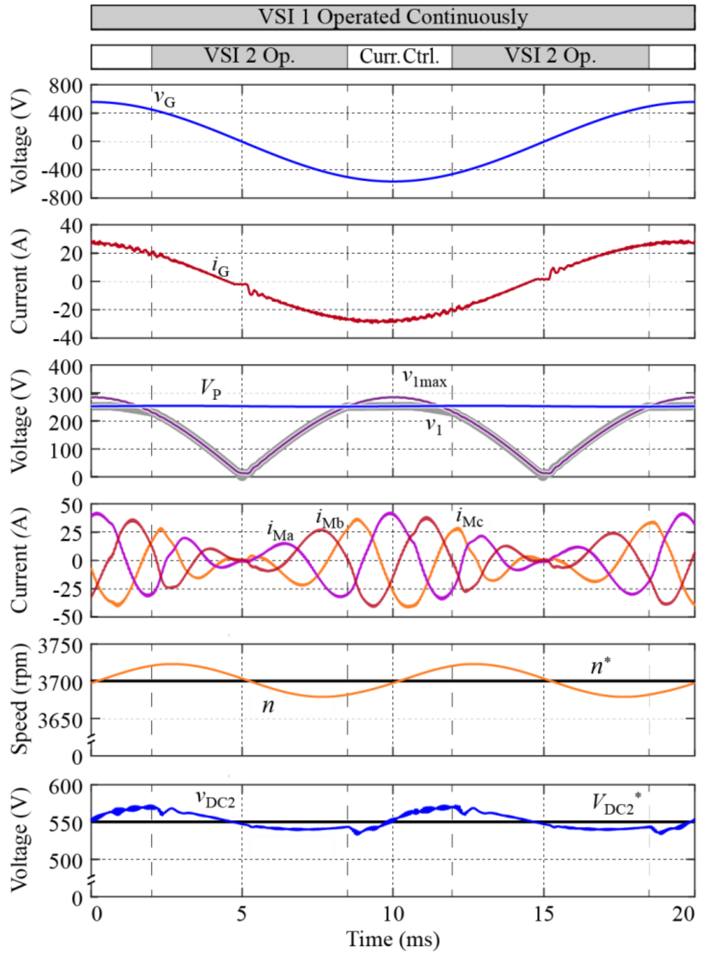
- Normalized to State-of-the-Art (with Electrolytic Capacitor)
  - **AVG Conduction Losses: -45 %**
  - **RMS Conduction Losses: -45 %**
  - **Switching Losses: -15 %**

→ **Semiconductor Loss Reduction up to 30 % @ $V_P = 2V_0$**

DI – Control

- **Control Objectives:** PFC Operation, DC-Link Voltage and Average Speed Control
  - Implemented in Cascaded Fashion
  - Based on Grid Power Feedforward and Voltage Division





→ Verified by Circuit Simulation for $C_{DC2} = 50\ \mu F$ - only $6.7\ \mu F/kW$

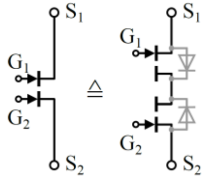
Results & Conclusions

Part I: Single-Inverter Topology

- **MPPB Concept**
  - Elim. Electrolytic Capacitors in 1Φ AC-Supplied VSD Systems
  - Performance Analysis: Motor and Inverter

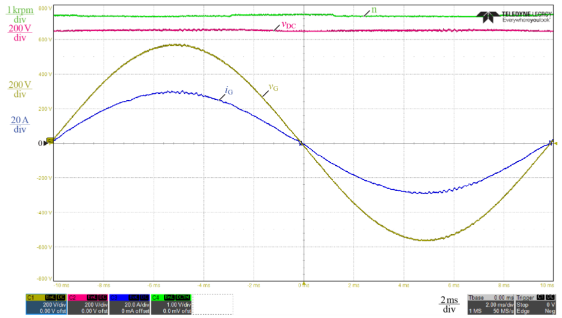
- **Motor-Integrated Hardware Demonstrator**
  - Achieving 8 µF/kW within the DC-Link
  - Drive System Perf.: 0.91 kW/ltr. and 91.4 % @ 7.5 kW
  - In-Depth Validation

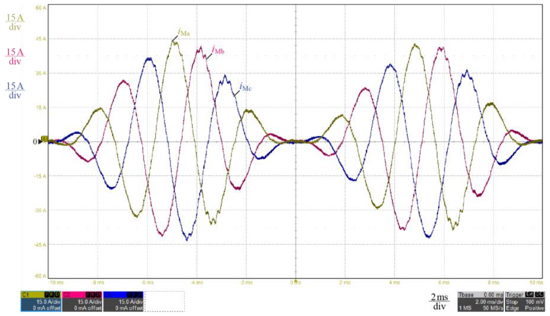
- **Current-Source Based System**
  - Monolithic Bidirectional GaN Transistor
  - Protection of Motor Winding System

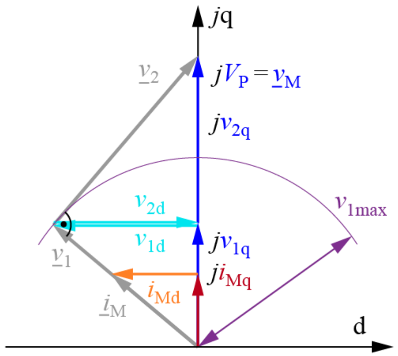


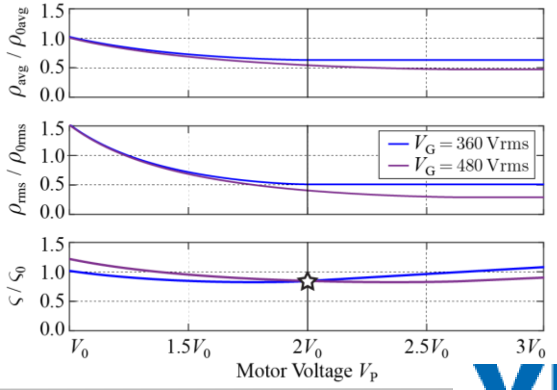
Part II: Dual-Inverter Topology

- **Dual-Inverter Employing the MPPB Concept**
  - Low Effort Implementation
  - Analysis of Operation and Control Structure
  - Semiconductor Loss Reduction of up 30 %









Thank You!

November 9th, 2023