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X-Technologies → Power Electronics 4.0

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“X-Technologies” Driving Power Electronics 4.0

Abstract — Power Electronics is a key technology for all forms of generation and utilization of electric power in modern societies, ranging from renewable energy generation and all types of power supply applications including fast-charging of EVs and hyperscale datacenters to actuator systems like variable speed drives that consume 60% of all electric energy used in industry.

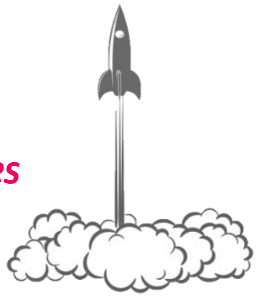
The progress in the area has been driven over the past 40 years by new power semiconductor concepts and corresponding circuit topologies and modulation/control concepts. After a 1st main step initiated by the introduction of the thyristor in 1958 and a 2nd step around 1985 triggered by the availability of Si bipolar and unipolar turn-off devices finally built as IGBTs and superjunction MOSFETs, lately a 3rd disruptive development step introduced wide bandgap devices, e.g. GaN power semiconductors dominating the low voltage arena and zero-recovery SiC diodes and power MOSFETs, which are offering exceptionally low on-resistance and high switching speeds up to unprecedented high voltages. Moreover, power electronics has massively benefitted from the parallel breathtaking development of digital signal processing which was adopted early for variable speed drive systems and since around 2005 is also regularly used in switch-mode power supplies.

Now we are at the beginning of a fascinating and even more dynamic 4th step of power electronics development and it is interesting to contemplate on the driving forces, in other words to identify the “X-technologies” and/or “moonshot technologies” of power electronics over the next decade. Starting from basic scaling laws, the talk identifies 4 core technologies potentially driving the disruption towards Power Electronics 4.0, namely wide-bandgap power semiconductors, multi-cell/level converter concepts, functional association and synergetic multi-stage converter control and finally advanced modelling and simulation and/or multi-objective design automation including digital twins, which are a key prerequisite for the introduction of Industry 4.0 concepts in Power Electronics.

Future power electronics converters have to be seen as intelligent systems, which are actively monitoring and diagnosing their source and load environment based on different types of models and actuations, aggregating data and distilling information, receiving data/updates from and reporting status information to the cloud, a type of system best denominated as *Cognitive Power Electronics 4.0*. Accordingly, we are at the advent of a fascinating next phase of highly dynamic development in power electronics, which will also fully conquer the very low voltage/power and the medium/high voltage domains.

Outline

- ► *Introduction*
- ► *X-Concepts /"Moon-Shot" Technologies*
- ► *Power Electronics 4.0*
- ► *Conclusions*



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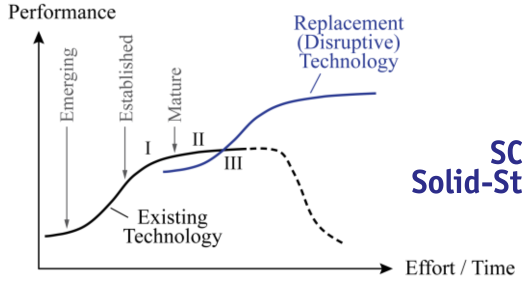
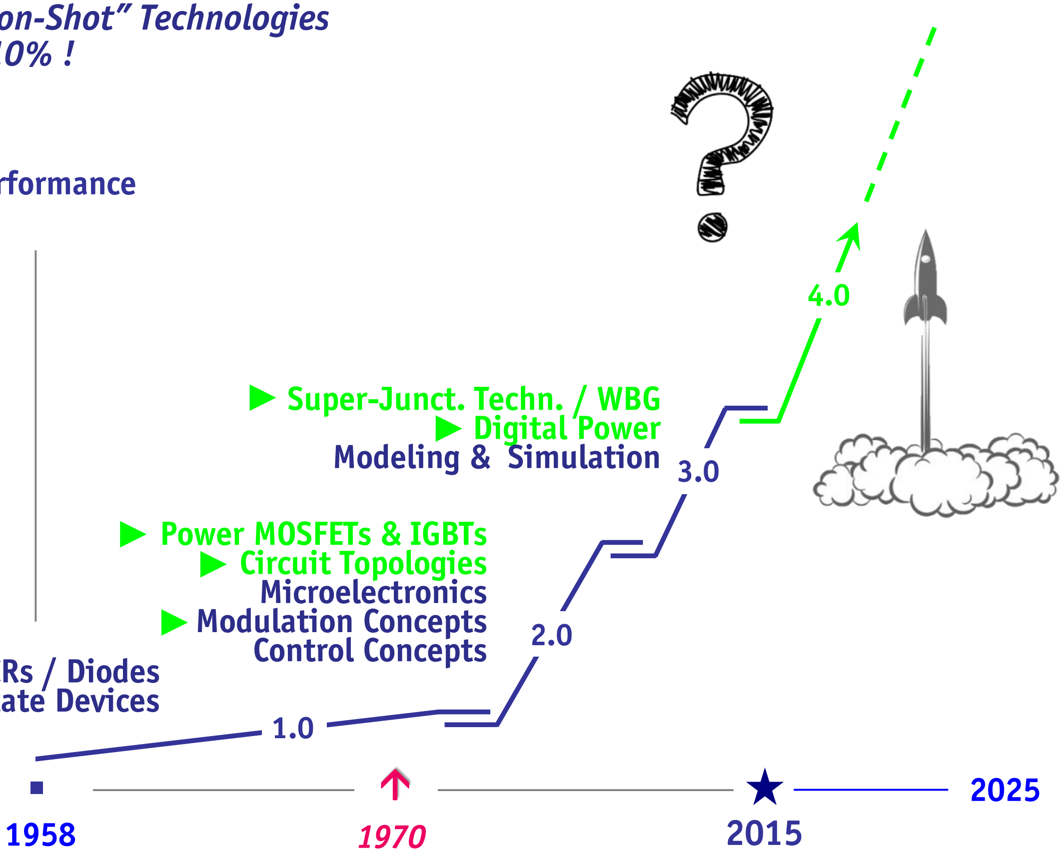
Introduction

Power Electronics
Development Steps

S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify "X-Concepts" / "Moon-Shot" Technologies*
- *10 x Improvement NOT Only 10% !*





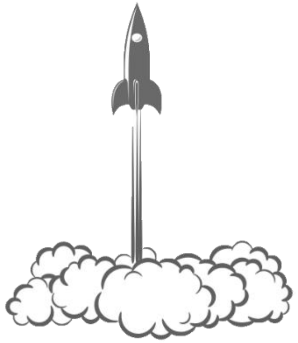
SCRs / Diodes
Solid-State Devices

▶ Power MOSFETs & IGBTs
▶ Circuit Topologies
Microelectronics
▶ Modulation Concepts
Control Concepts

▶ Super-Junct. Techn. / WBG
▶ Digital Power
Modeling & Simulation

1970
1st PEMC in
Budapest

X-Technology #1



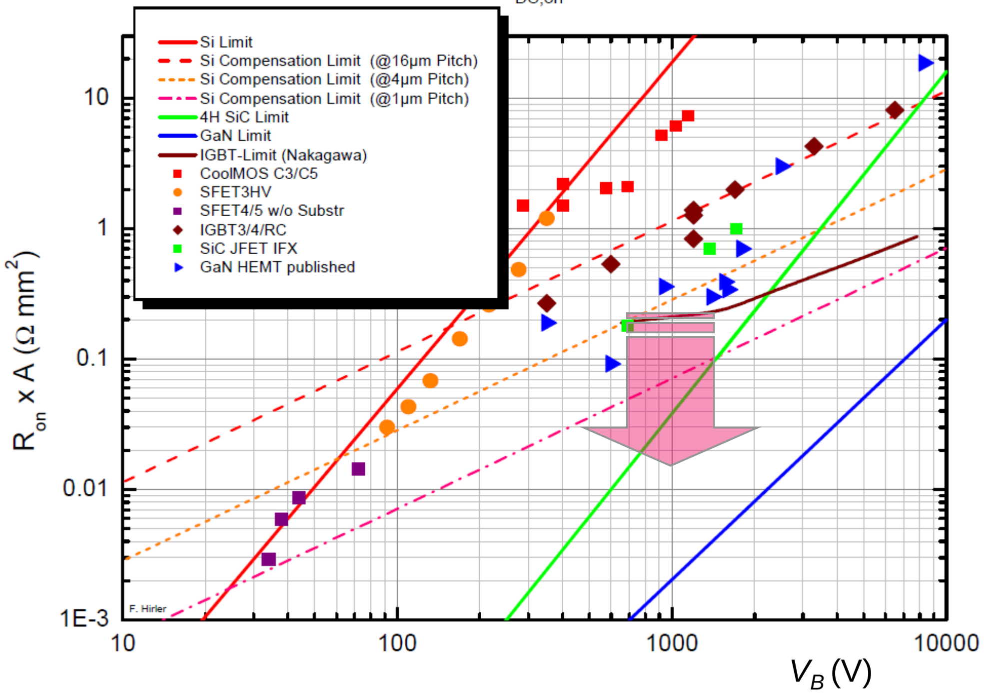
Wide Bandgap Power Semiconductors

Low $R_{DS(on)}$ High-Voltage Devices

- *SiC MOSFETs / GaN HEMTs (Monolithic AC-Switch)*
- *Low Conduction Losses & ZVS*
- *High Efficiency*

Source: Infineon

typical Cell $R_{DS,on}$ x A @25°C



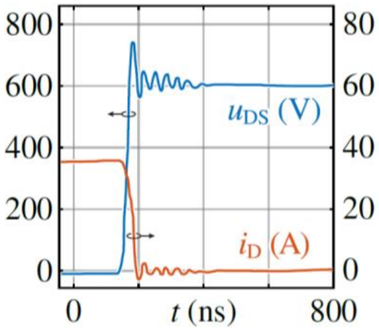
$$R^*_{on} = \frac{4V_B^2}{\varepsilon\mu_n E_C^3} \leftarrow$$

$$R^*_{on,SiC} \approx \frac{1}{300} R^*_{on,Si}$$

- *High Voltage Unipolar (!) Devices → Excellent Switching Performance*

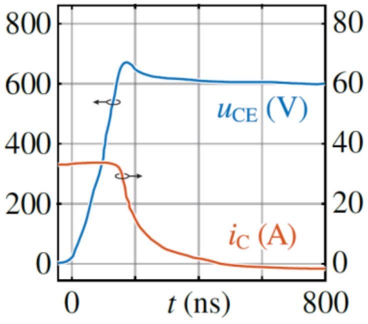
SiC vs. Si Switching Behavior

- **SiC-MOSFETs** → Resistive On-State Behavior / Factor 10 Higher Sw. Speed
- **Si-IGBT** → Const. On-State Voltage Drop / Rel. Low Switching Speed

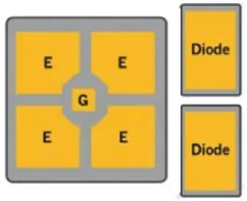


1200V 100A
Die Size: 25.6 mm²

Source: Cree



Source: Fuji Electric

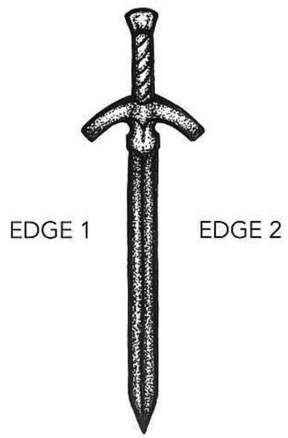


1200V 100A
Die Size: 98.8 mm² + 39.4 mm²

Source: Infineon

- Extremely High di/dt & dv/dt → Challenges in Packaging / EMI / Insulation Stress

Challenges

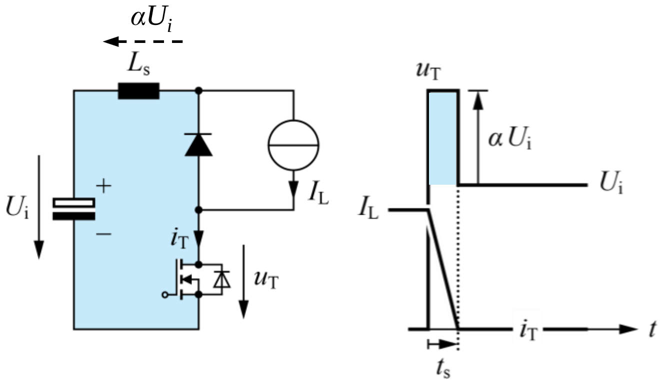


Circuit Parasitics

$$L\frac{di}{dt}=u_L$$

- *Extremely High di/dt*
- *Commutation Loop Inductance L_s*
- **Allowed L_s Directly Related to Switching Time t_s** →

$$L_s \le \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \underset{Z}{\frac{U_i}{I_L}}$$



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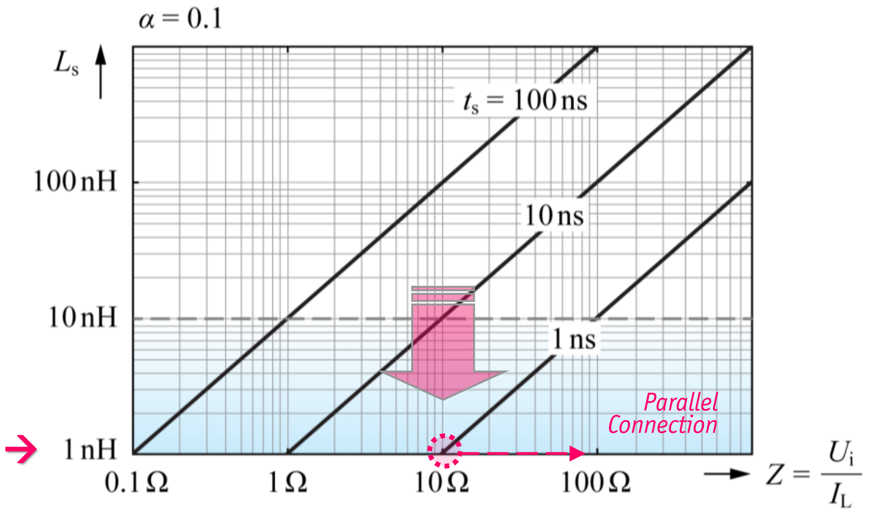


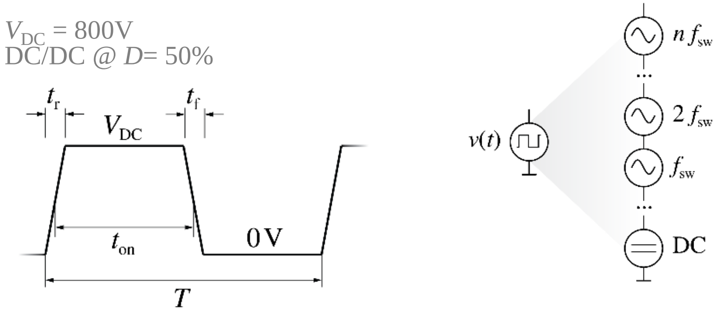
- *Advanced Packaging & Parallel Interleaving for Partitioning of Large Currents*

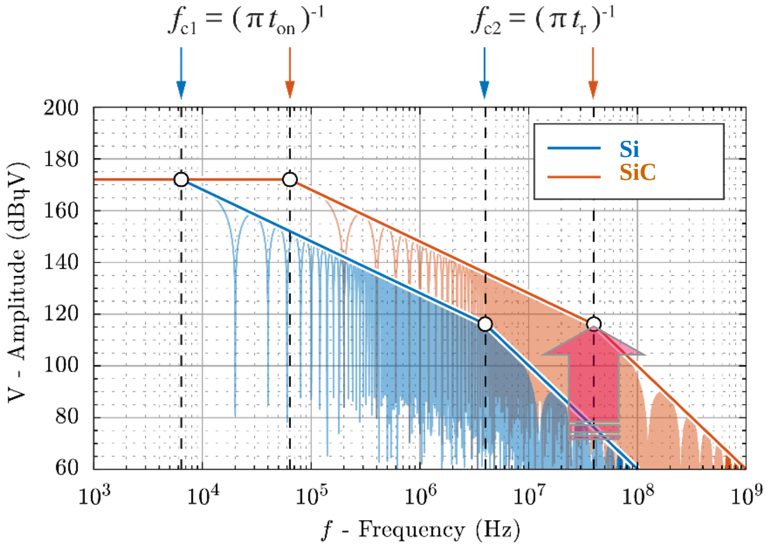
SiC vs. Si EMI Emissions

- *Higher dv/dt* → *Factor 10*
- *Higher Switching Frequencies* → *Factor 10*
- *EMI Envelope Shifted to Higher Frequencies*

f_S= 10kHz & 5 kV/us for (Si IGBT)

f_S= 100kHz & 50 kV/us for (SiC MOSFET)

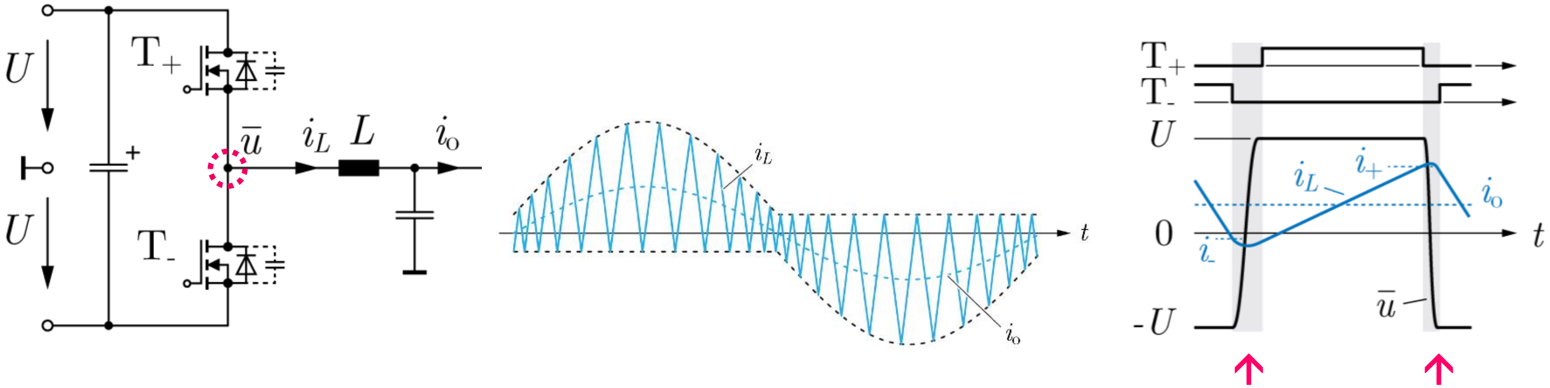




- *Higher Influence of Filter Component Parasitics & Couplings* → *Advanced Design*

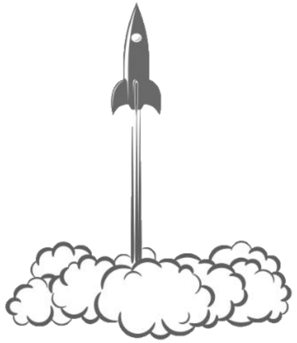
SiC MOSFETs — Soft Switching

- TCM — Triangular Current Mode → *Zero Voltage Turn-Off* & *Zero Voltage Turn-On (ZVS)*
- *Variation of Sw. Frequ.* → Spreading of EMI Noise



- Only 33% Increase of Conduction Losses
- Requires Certain Voltage Headroom for Avoiding Very Low Sw. Frequencies

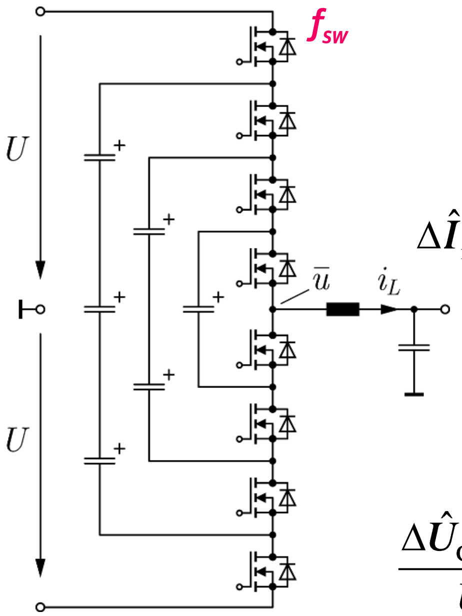
X-Technology #2



Multi-Level / -Cell Converters & Modularity

Scaling of Multi-Level Concepts

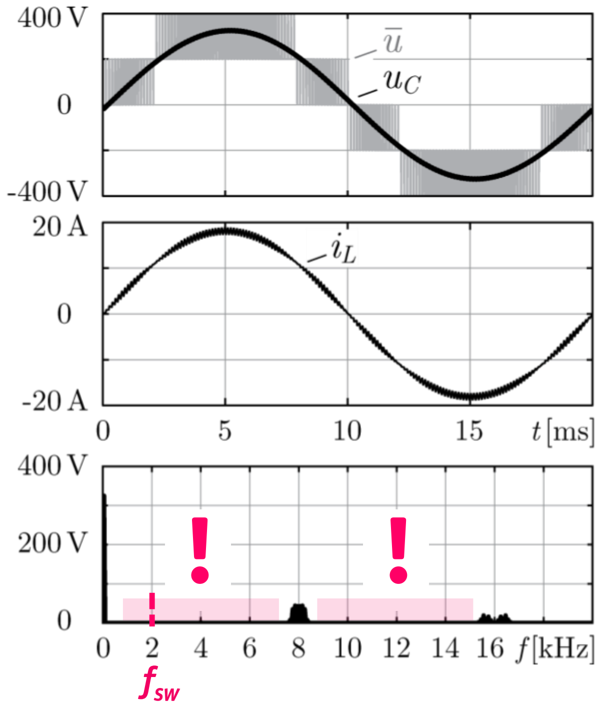
- *Reduced Ripple @ Same (!) Switching Losses*
- *Lower Overall On-Resistance @ Given Blocking Voltage*
- *Application of LV Technology to HV*



$$\frac{U}{8 f_s L}$$

$$\Delta\hat{I}_{\max,N} = \frac{1}{N^2}\,\Delta\hat{I}_{\max,N=1}$$

$$\frac{\Delta\hat{U}_{C,\max,N}}{U} = \frac{\pi^2}{32}\left(\frac{f_O}{f_S}\right)^2\frac{1}{N^3}$$

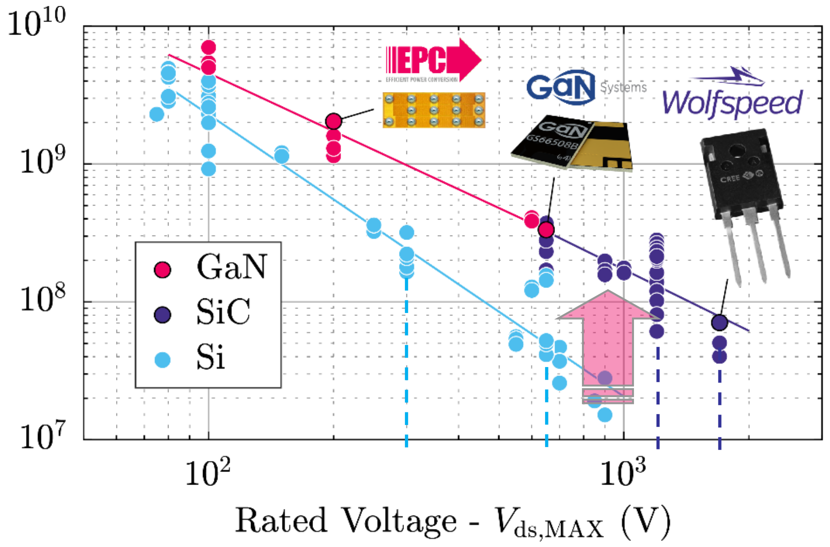


- *Scalability / Manufacturability / Standardization / Redundancy*

SiC/GaN Figure-of-Merit

- *Figure-of-Merit (FOM) Quantifies Conduction & Switching Properties*
- *FOM Identifies Max. Achievable Efficiency @ Given Sw. Frequ.*

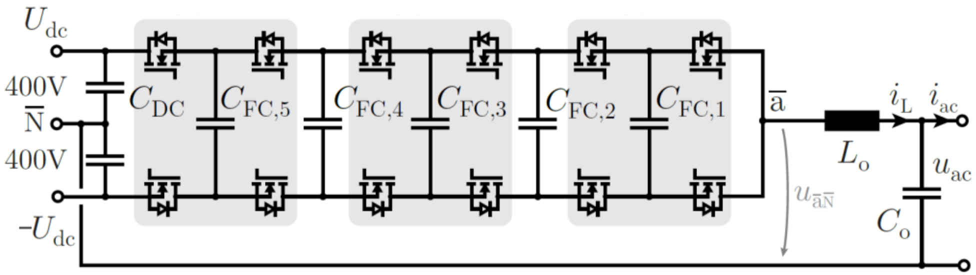
$$\mathrm{FOM} = \frac{1}{R_{\mathrm{ds,on}} Q_{\mathrm{oss}}}$$



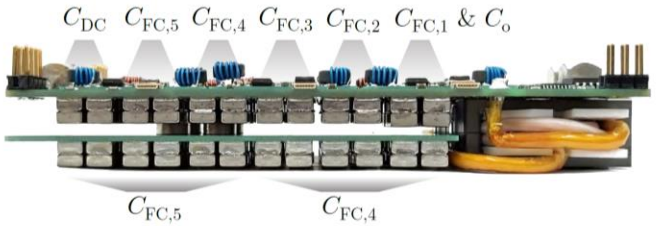
- *Advantage of Multi-Level over 2-Level Converter Topologies*

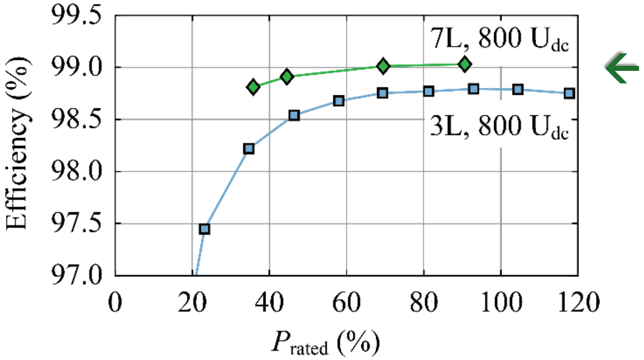
7-Level Flying Cap. 200V GaN Inverter

- DC-Link Voltage 800V
- Rated Power 2.2 kW / Phase
- 99% Efficiency → Natural Convection Cooling (!)



★ 260 W/in^3





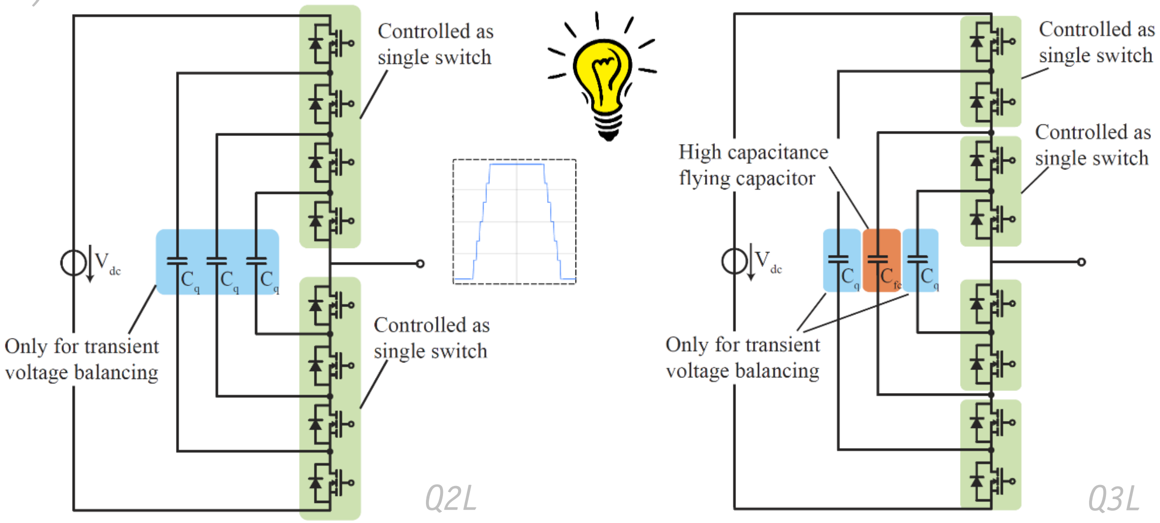
- High Effective Sw. Frequency (6 x 30kHz = 180kHz) → Small Filter Inductor L_0

Quasi-2L & Quasi-3L Inverters

- *Operation of N-Level Topology in 2-Level or 3-Level Mode*
- *Intermediate Voltage Levels Only Used During Sw. Transients*

- Schweizer (2017)

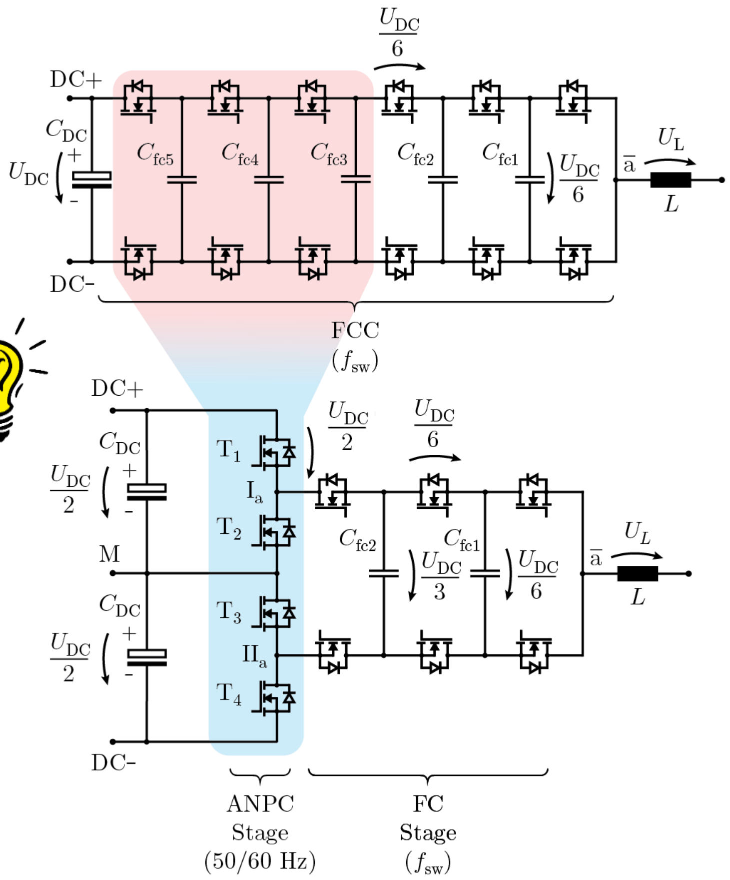
ABB

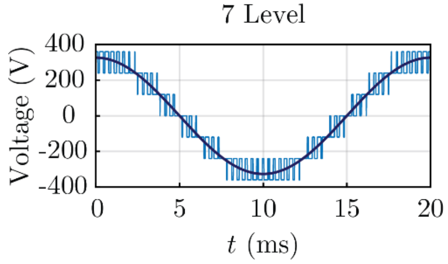


- *Clear Partitioning of Overall Blocking Voltage & Small Flying Capacitors*
- *Low Voltage/Low $R_{DS(on)}$/Low \$ MOSFETs → High Efficiency / No Heatsinks / SMD Packages*

3-Φ Hybrid Multi-Level Inverter

- *Realization of a 99%++ Efficient 10kW 3-Φ 400$V_{rms,ll}$ Inverter System*
- *7-Level Hybrid Active NPC Topology / LV Si-Technology*





★ *99.35%*
2.6kW/kg
56 W/in^3

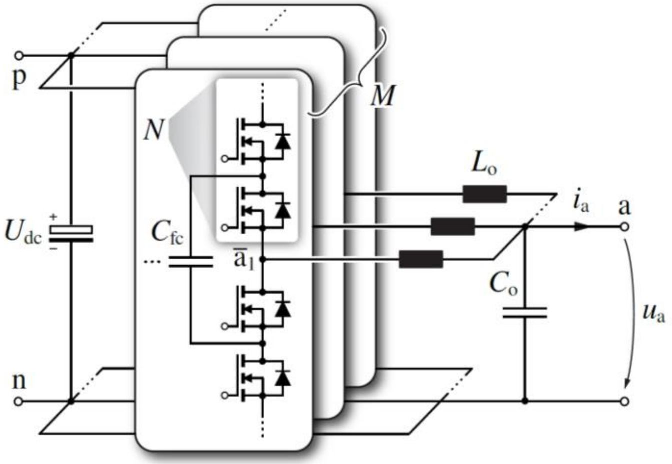
- *200V Si → 200V GaN Technology Results in 99.5% Efficiency*

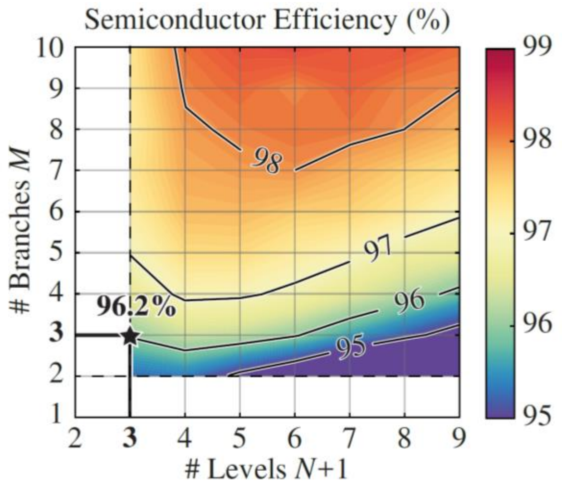
4.8MHz GaN Half-Bridge Module

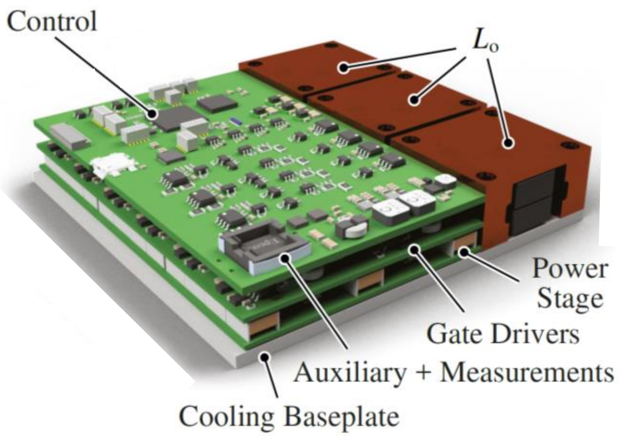
- *Combination of Series & Parallel Interleaving*

— *600V GaN Power Semiconductors, f_{sw}= 800kHz*
— *Volume of ≈180cm^3 (incl. Control etc.)*
— *H_2O Cooling Through Baseplate*

★ *≈ 820 W/in^3*

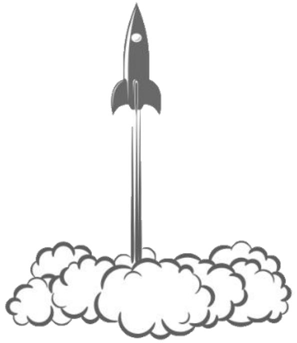






- *Operation @ f_{out}=100kHz / $f_{S,eff}$= 4.8MHz, 10kW, U_{dc}=800V*

X-Technology #3

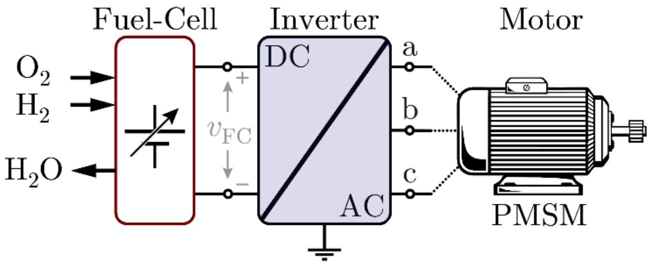


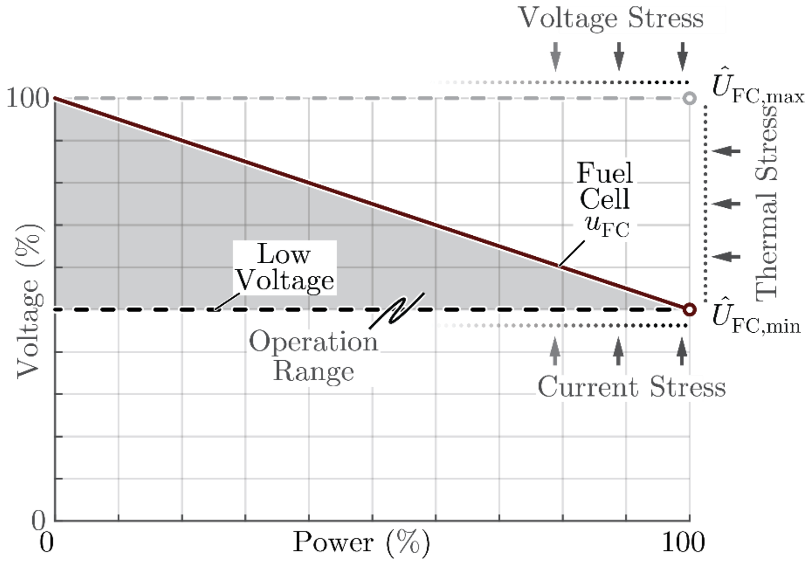
Functional Integration & Synergetic Association

Motivation

- *General / Wide Applicability*

— *Adaption to Load-Dependent Battery | Fuel Cell | Solar Panel Supply Voltage*
— *VSDs → Wide Output Voltage / Speed Range*

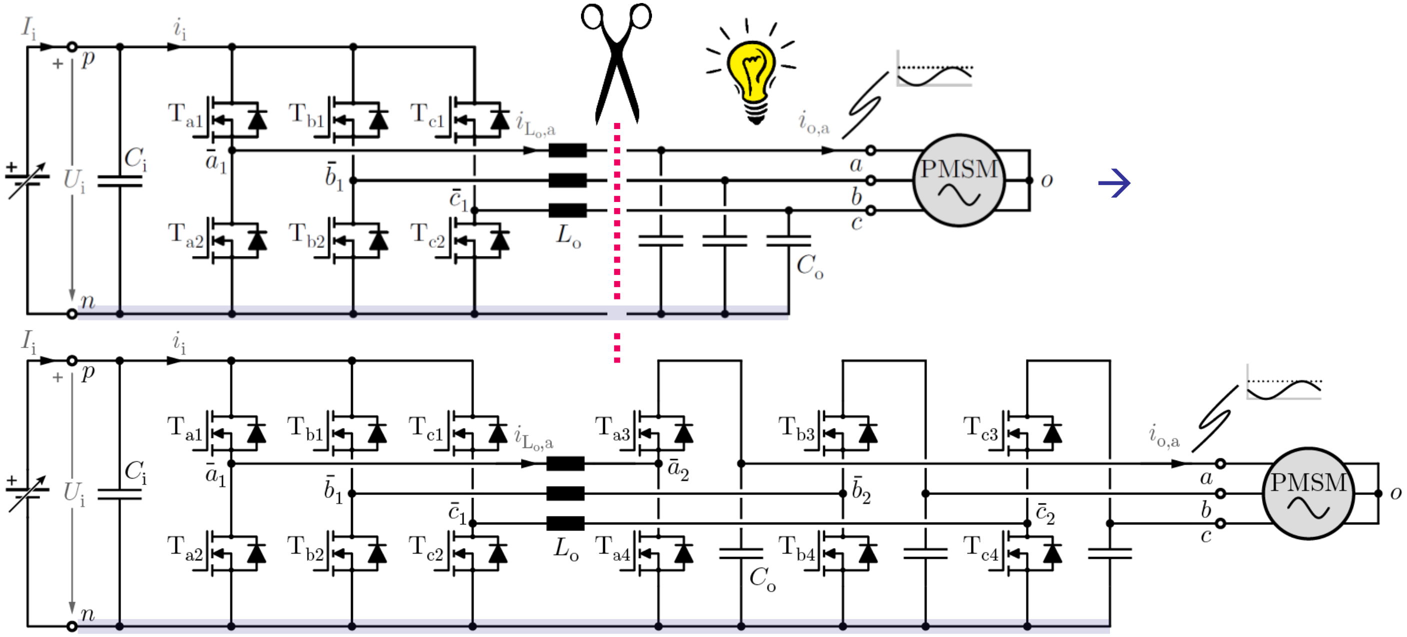




- *No Additonal Converter for Voltage Adaption → Single-Stage Energy Conversion*

Example — Buck-Boost 3-Φ Inverter

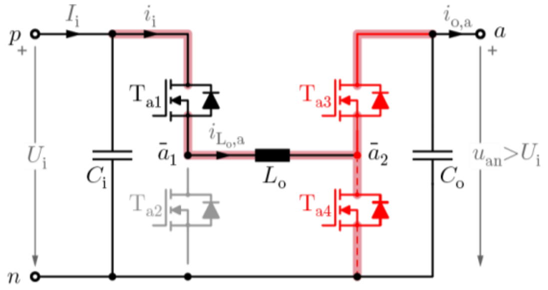
- *Generation of AC-Voltages Using Unipolar Bridge-Legs*



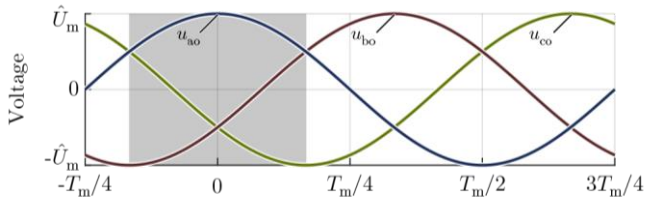
- *Switch-Mode Operation of Buck OR Boost Stage → Single-Stage Energy Conversion (!)*
- 3-Φ Continuous Sinusoidal Output / Low EMI → *No Shielded Cables / No Insul. Stress*

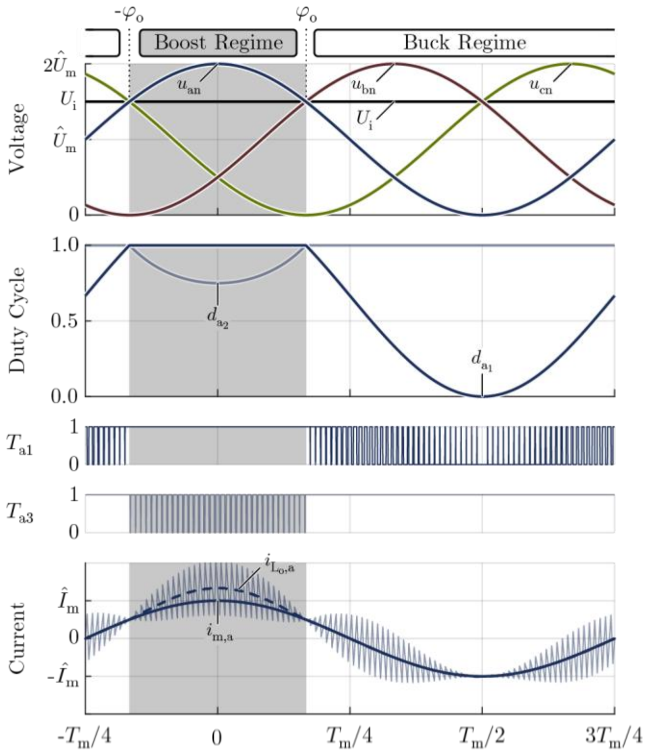
Boost-Operation $u_{an} > U_i$

- *Phase-Module*



- *Motor Phase Voltages*

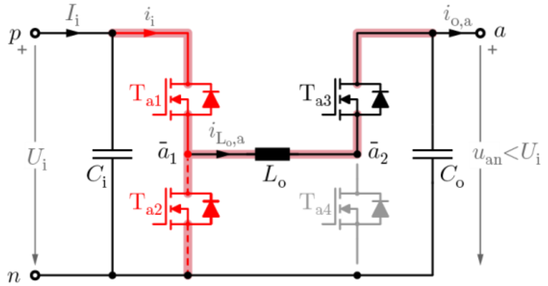




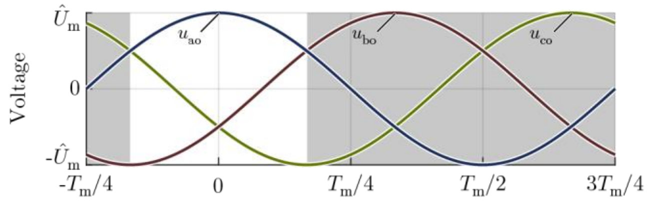
- *Current-Source-Type Operation*
- *Clamping of Buck-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion*

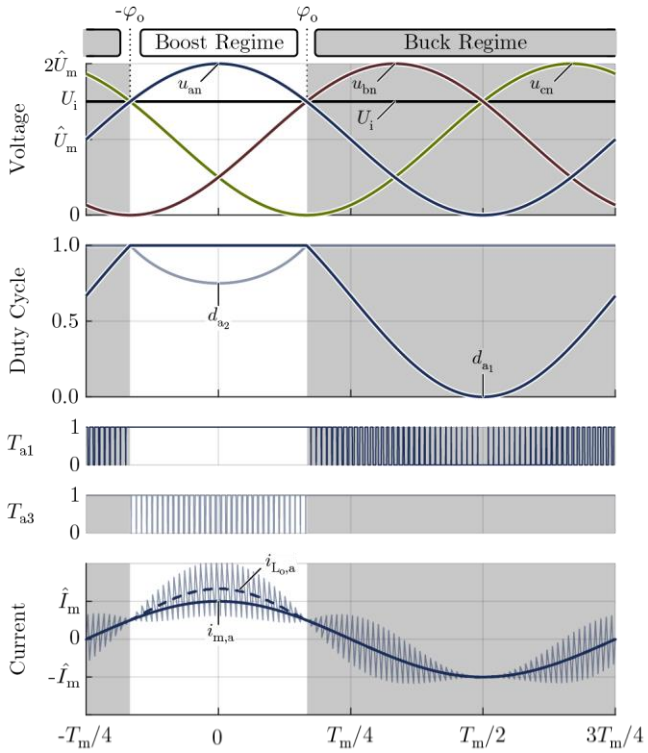
Buck-Operation $u_{an} < U_i$

- **Phase-Module**



- **Motor Phase Voltages**

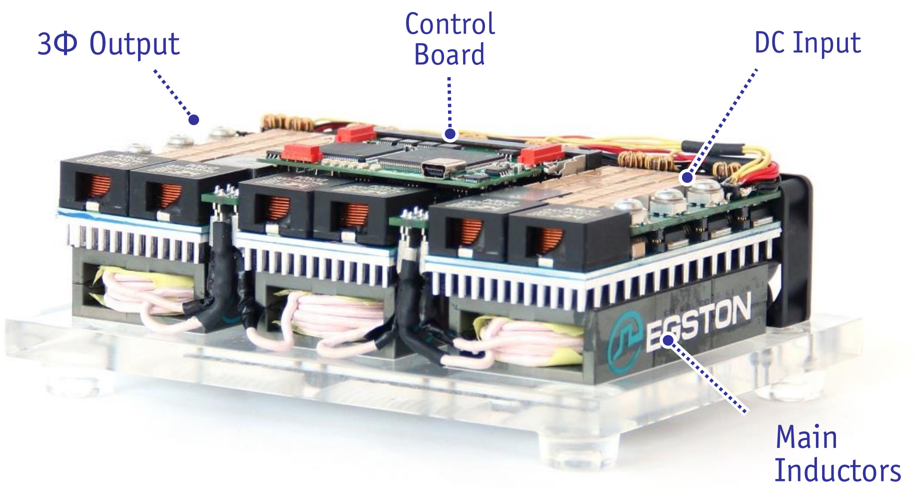


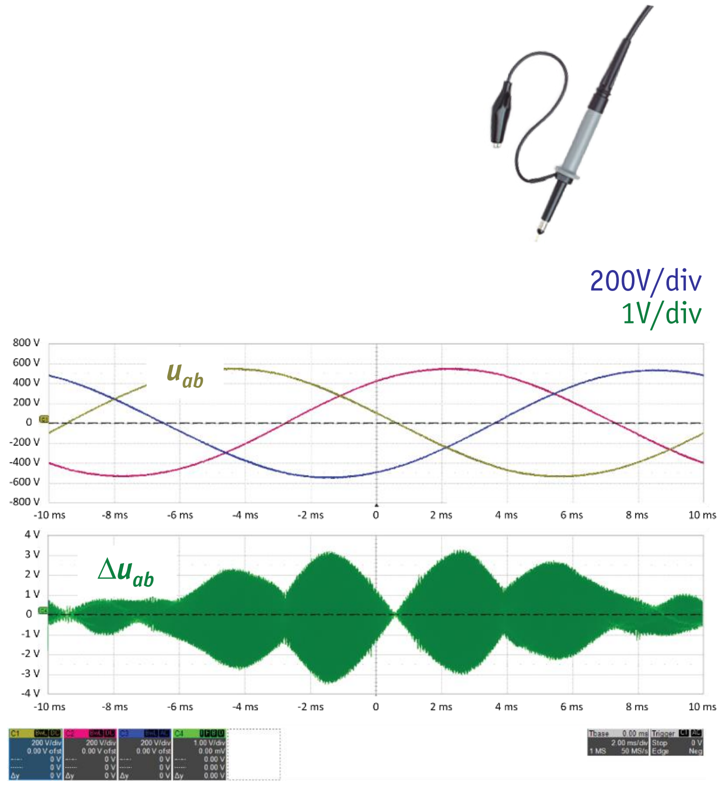


- Voltage-Source-Type Operation
- Clamping of Boost-Bridge High-Side Switch → Quasi Single-Stage Energy Conversion

SiC 3-Φ Buck-Boost Inverter Demonstrator

- DC Voltage Range 400…750V_{DC}
- Max. Input Current ± 15A
- Output Voltage 0…230V_{rms} (Phase)
- Output Frequency 0…500Hz
- Sw. Frequency 100kHz



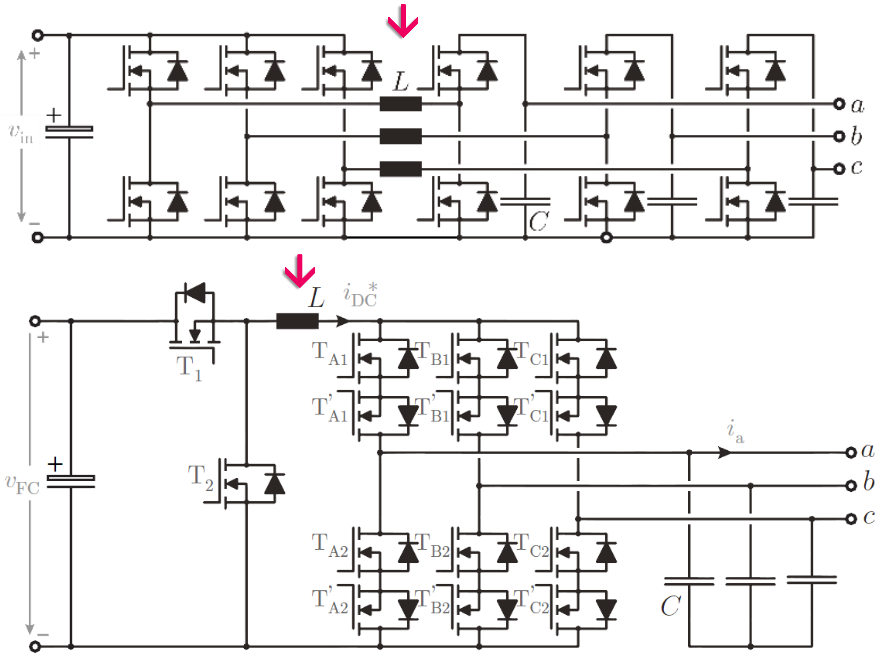


- Dimensions → 160 x 110 x 42 mm^3

★ ≈ 245 W/in^3

3-Φ Modular → 3-Φ-Integrated Buck-Boost CSI

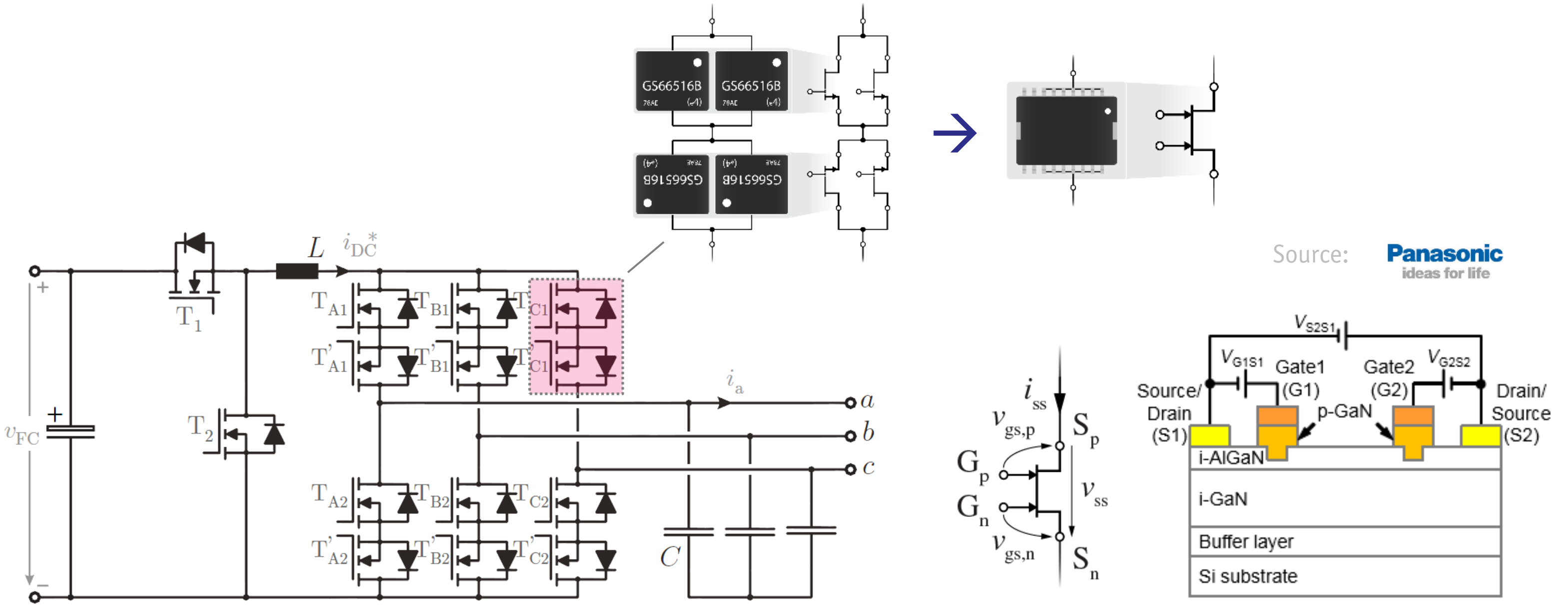
- *Modular-Inverter → Phase Modules w/ Buck-Stage | Current Link | Boost-Stage*
- *3-Φ CSI → Buck-Stage V-I-Converter | Current DC-Link DC/AC-Stage*



- *Single Inductive Component & Utilization of Monolithic (!) Bidirectional GaN Switches*

3-Φ Current Source Inverter (CSI) Topologies

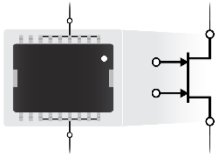
- *Bidirectional/Bipolar Switches → Positive DC-Side Voltage for Both Directions of Power Flow*



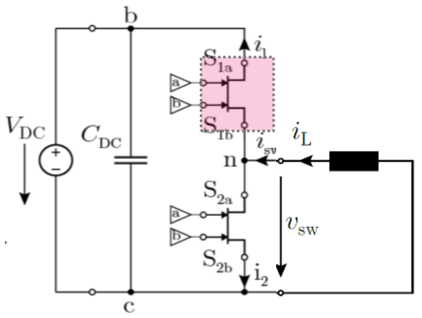
Source: Panasonic ideas for life

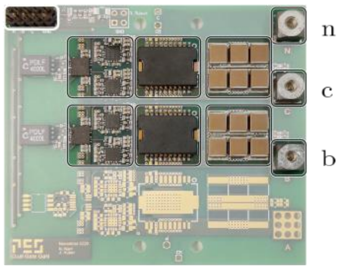
- *Monolithic Bidir. GaN Switches → Factor 4 (!) Reduction of Chip Area Comp. to Discrete Realization*

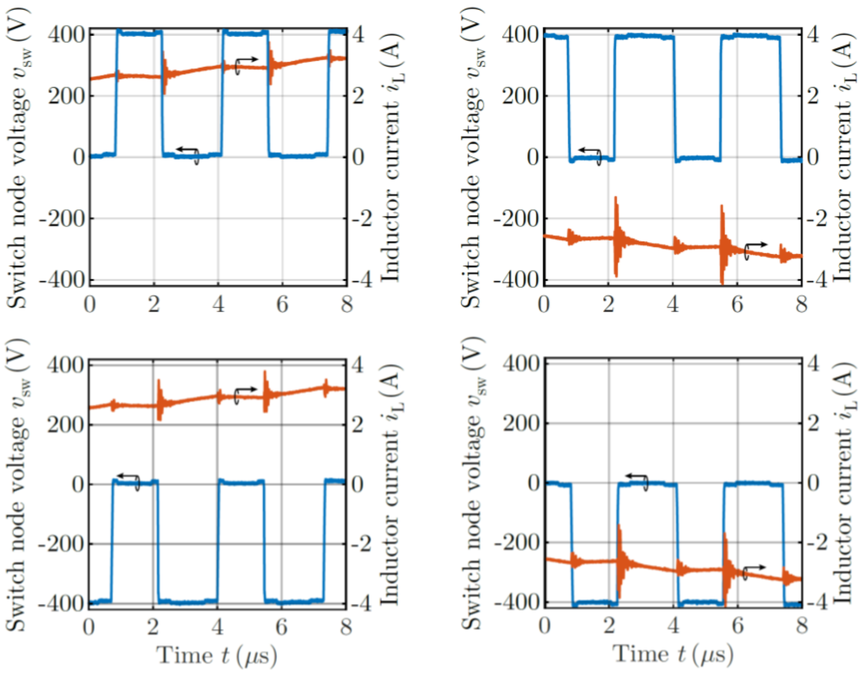
600V GaN Monolithic Bidir. Switch



- Power America Project — Based on Infineon's CoolGaN™ HEMT Technology ($R_{DS(on)}$= 70mΩ)
- Dual-Gate Device / Controllability of Both Current Directions
- Bipolar Voltage Blocking Capability | Normally On or Off



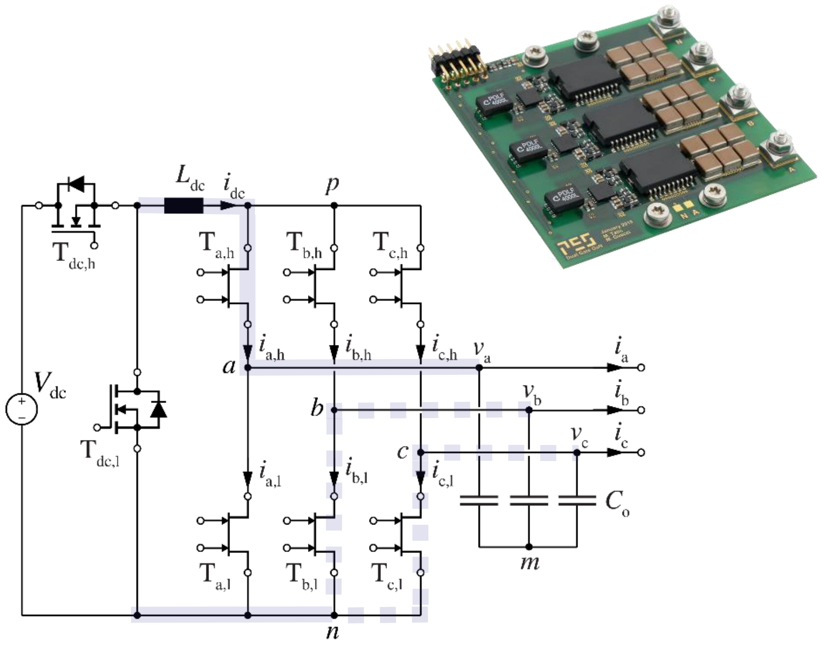


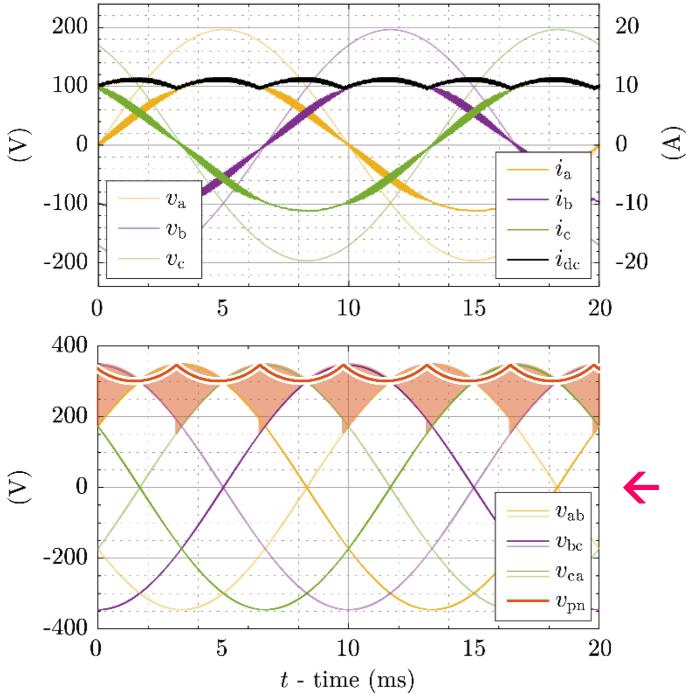


- Analysis of 4-Quardant Operation of $R_{DS(on)}$= 140mΩ Sample @ ±400V

3-Φ-Integrated Buck-Boost CSI

- *"Synergetic" Control of Buck-Stage & CSI Stage*
- *6-Pulse-Shaping of DC Current by Buck-Stage → Allows Clamping of a CSI-Phase*



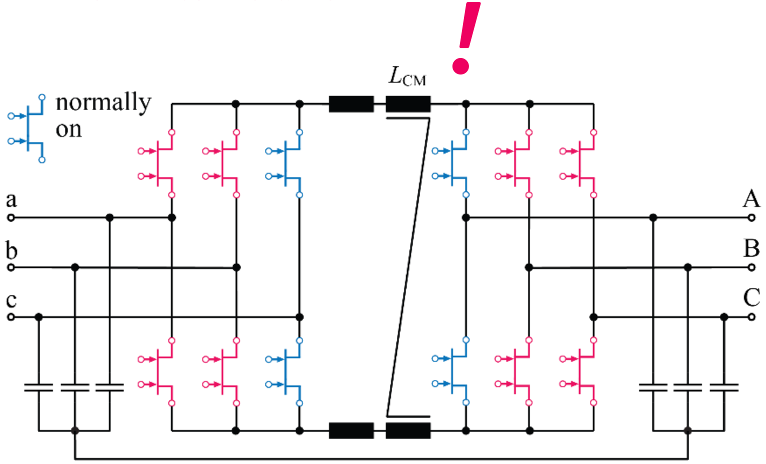


- *Switching of Only 2 of 3 Phase Legs → Reduction of Sw. Losses by ≈ 86% (!)*

3-Φ AC/AC Converter Topologies

■ Current DC-Link Topology

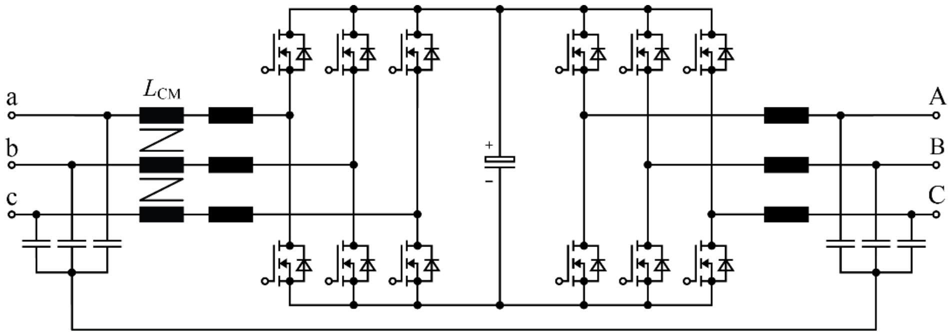
- *Application of M-BDSs*
- *Complex 4-Step Commutation*
- *Advantageous Over Matrix Converters*
- *Low Filter Volume*



- *Challenging Overvoltage Protection*
- *Limited Control Dynamics*

■ Voltage DC-Link Topology

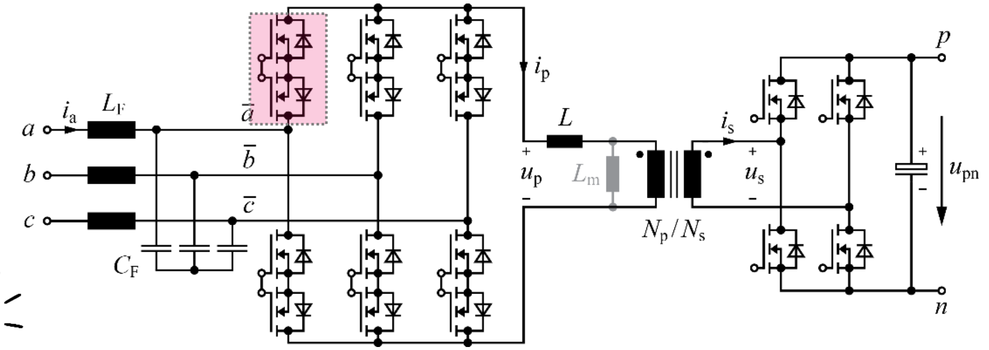
- *Standard Commutation*
- *Defined Semiconductor Voltage Stress*
- *Low-Complexity Bridge-Legs*
- *Facilitates DC-Link Energy Storage*

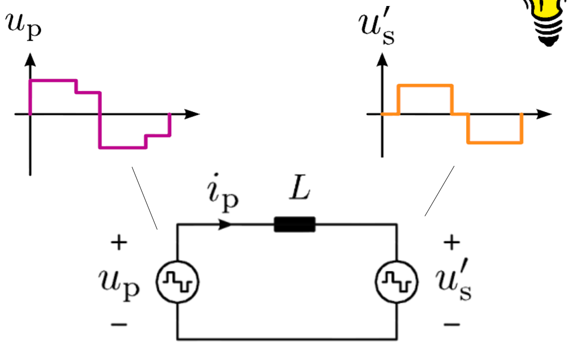


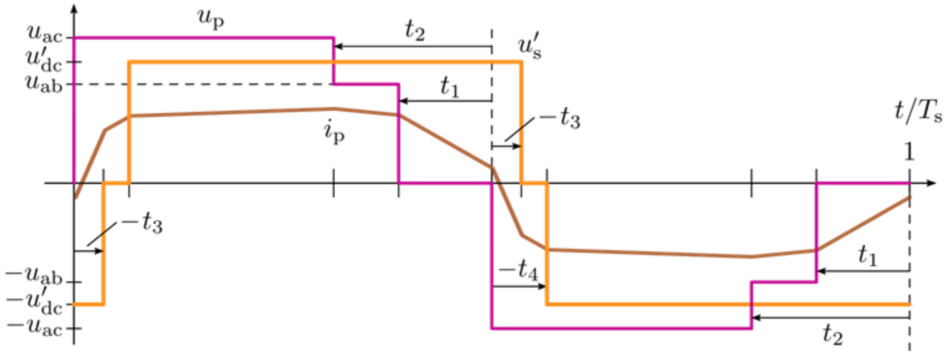
- *High Input / Output Filter Volume*

Isolated 3-Φ Matrix-Type PFC Rectifier

- *Based on Dual Active Bridge* (DAB) Concept
- *Optimal Modulation* (t_1...t_4) for Min. Transformer RMS Curr. & ZVS or ZCS
- Allows Buck-Boost Operation







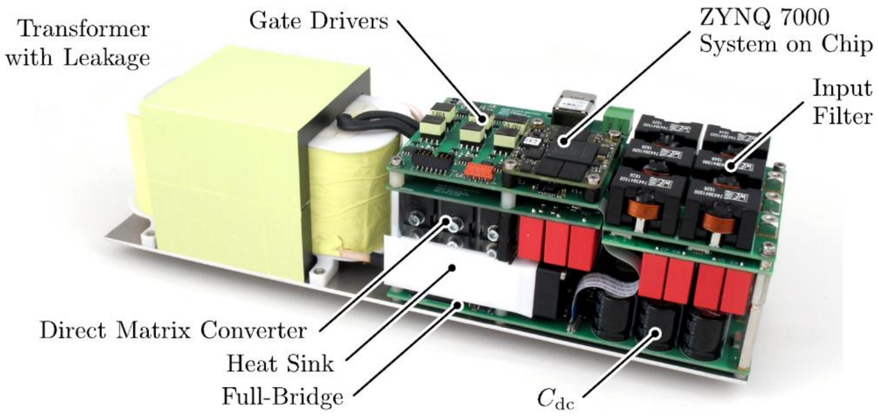
▶ Equivalent Circuit

▶ Transformer Voltages / Currents

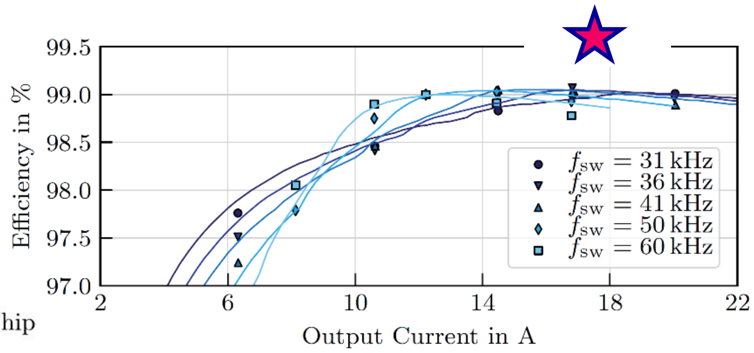
Isolated 3-Φ Matrix-Type PFC Rectifier

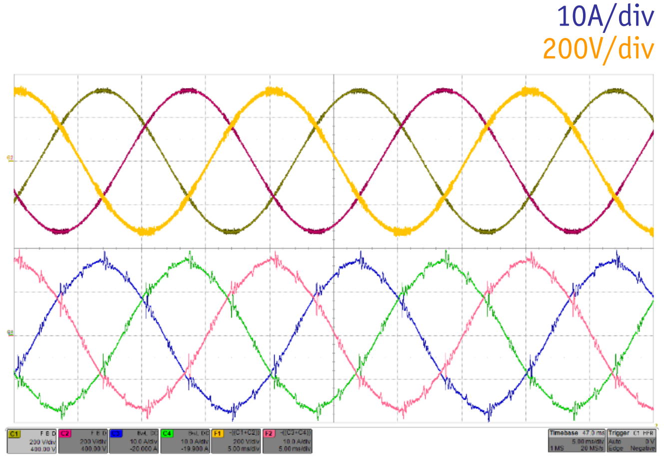
- Efficiency η = 98.9% @ 60% Rated Load (ZVS)
- Mains Current $THD_I \approx 4\%$ @ Rated Load
- Power Density $\rho \approx 4 \mathrm{kW/dm}^3$

P_O = 8 kW
U_N = 400V_{AC} → U_O = 400V_{DC}
f_S = 36kHz



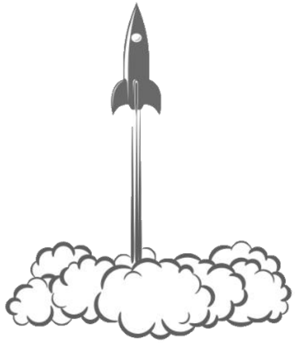
≈ 99%





- ▶ 900V / 10mΩ SiC Power MOSFETs
- ▶ Opt. Modulation Based on 3D Look-Up Table

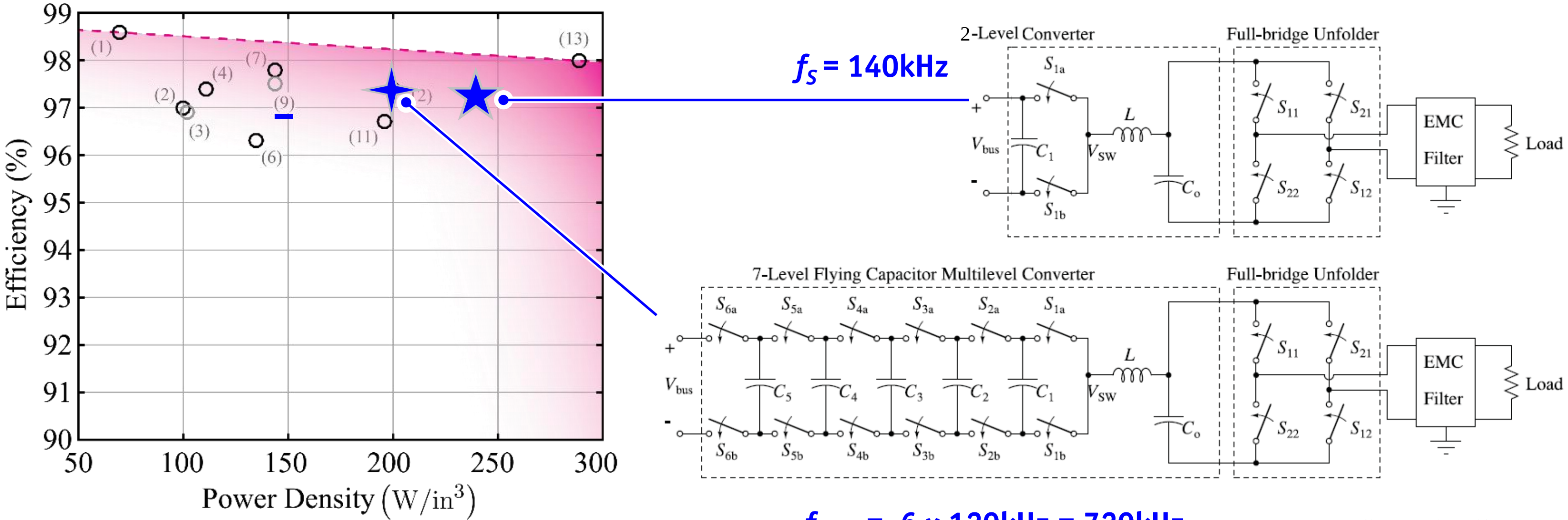
X-Technology #4



3D-Packaging
Automated Manufacturing

Multi-Level vs. 2-Level Inverter

- *Example of Google Little Box Challenge*
- Target: *2kW 1-Φ Solar Inverter with Worldwide Highest Power Density*
- *Comparative Analysis of Approaches of the Finalists*



f_S = 140kHz

$f_{S,eff}$ = 6 x 120kHz = 720kHz

Source: R. Pilawa-Podgurski

- *3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)*

Multi-Level vs. 2-Level Inverter

- *Example of Google Little Box Challenge*
- Target: *2kW 1-Φ Solar Inverter with Worldwide Highest Power Density*
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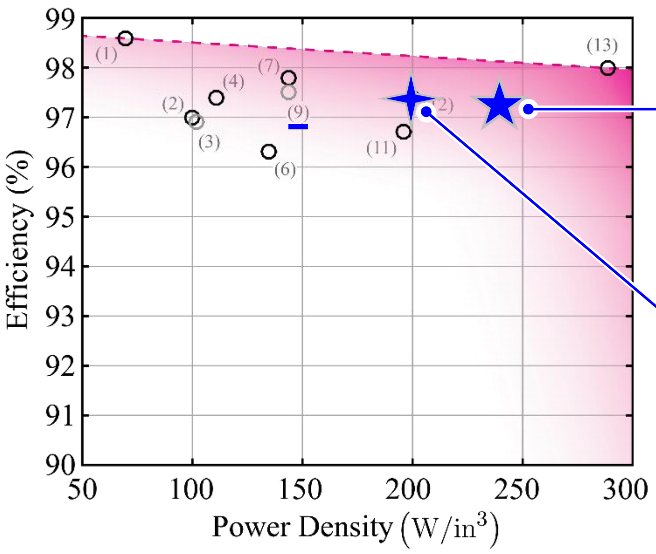
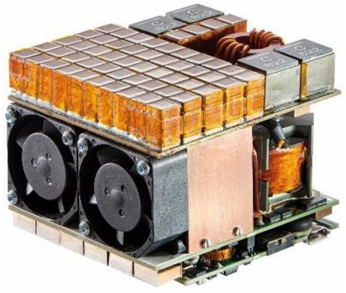
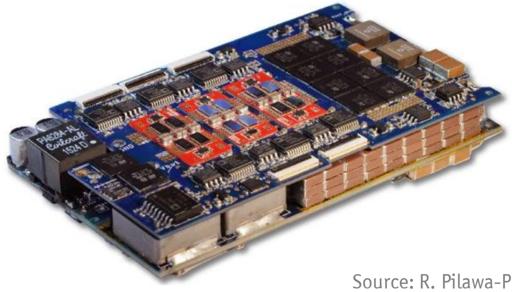


ETH zürich
Little-Box 2.0
240 W/in^3
97.4%



ILLINOIS
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN
215 W/in^3
97,6%



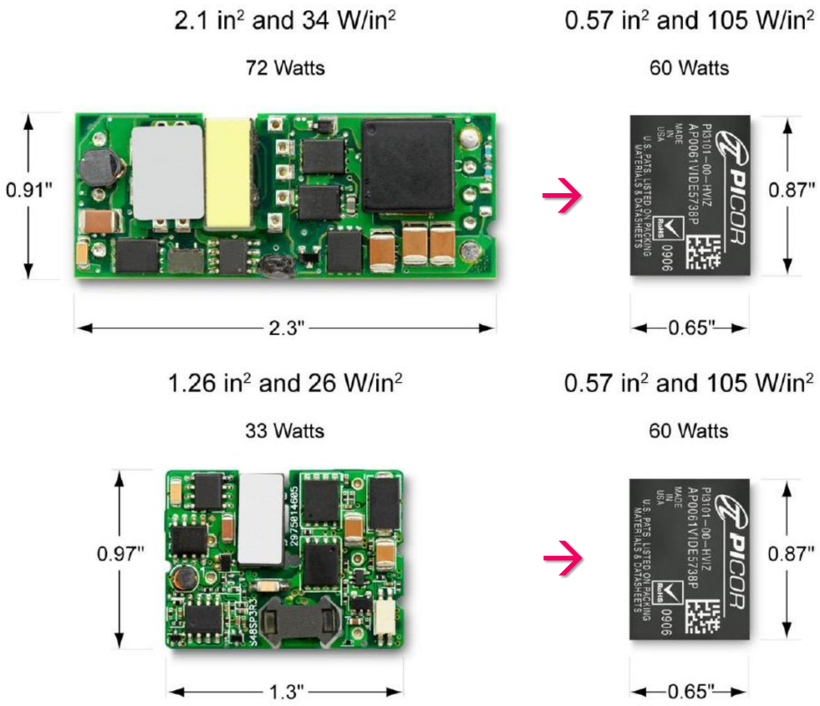
Source: R. Pilawa-Podgurski

- *3D-Packaging / Integration Highly Crucial for Utilizing Multi-Level Advantages (!)*

3D-Packaging / Heterogeneous Integration

- *System in Package (SiP) Approach*
- *Minim. of Parasitic Inductances / EMI Shielding / Integr. Thermal Management*
- *Very High Power Density (No Bond Wires / Solder / Thermal Paste)*
- *Automated Manufacturing*

Source: VICOR



- *Future Application Up to 100kW (!)*
- *New Design Tools & Measurement Systems (!)*
- *University / Industry Technology Partnership (!)*

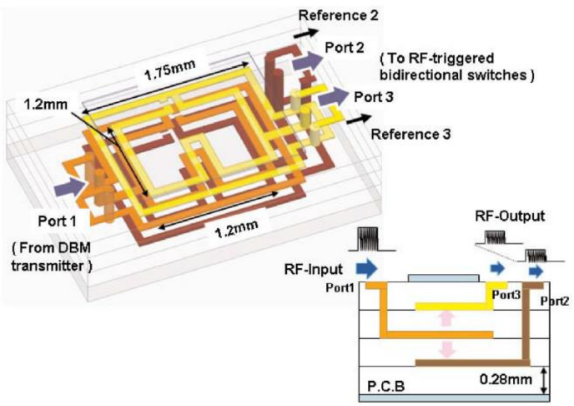
Monolithic 3D-Integration

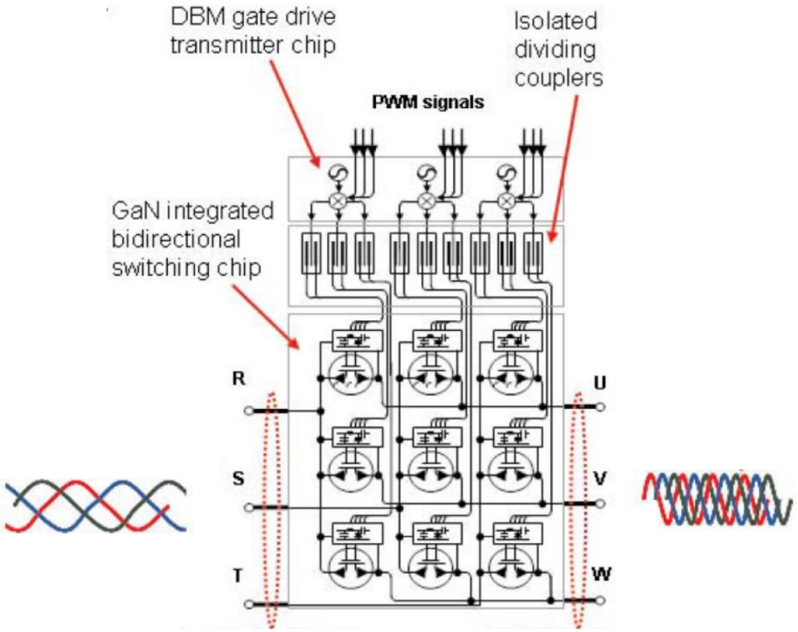
Source: **Panasonic** ISSCC 2014

- *GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology*

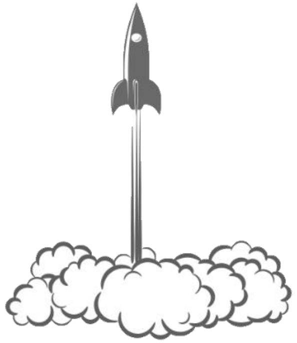
  - *9 Dual-Gate GaN AC-Switches*
  - *DBM Gate Drive Transmitter Chip & Isolating Couplers*
  - *Ultra Compact → 25 x 18 mm^2 (600V, 10A – 5kW Motor)*

5.0GHz Isolated (5kVDC) Dividing Coupler





X-Technology #5

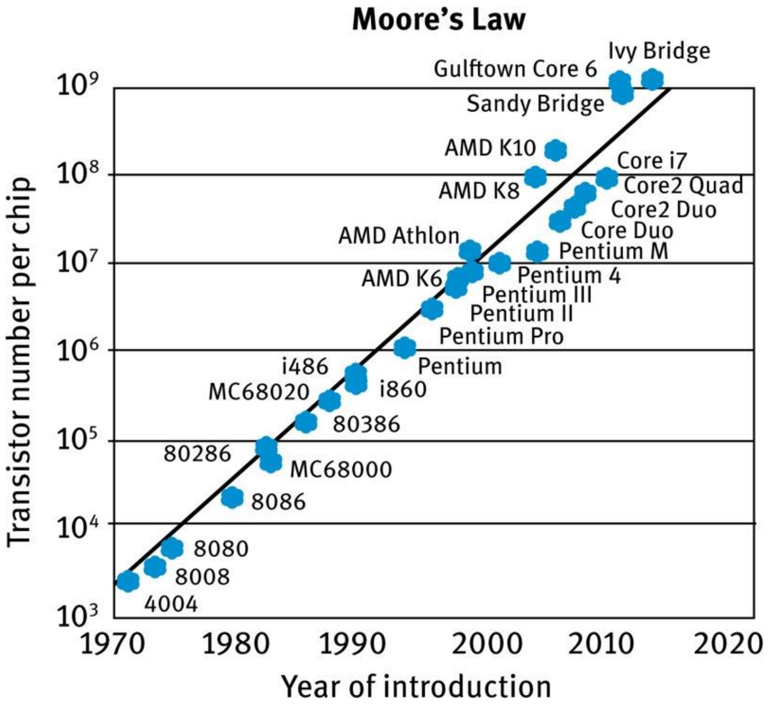


Automated Design
Digital Twin / Industry 4.0

Digital Signal & Data Processing

- *Exponentially Improving uC / Storage Technology (!)*

— *Extreme Levels of Density / Processing Speed*
— *Software Defined Functions / Flexibility*
— *Cont. Relative Cost Reduction*

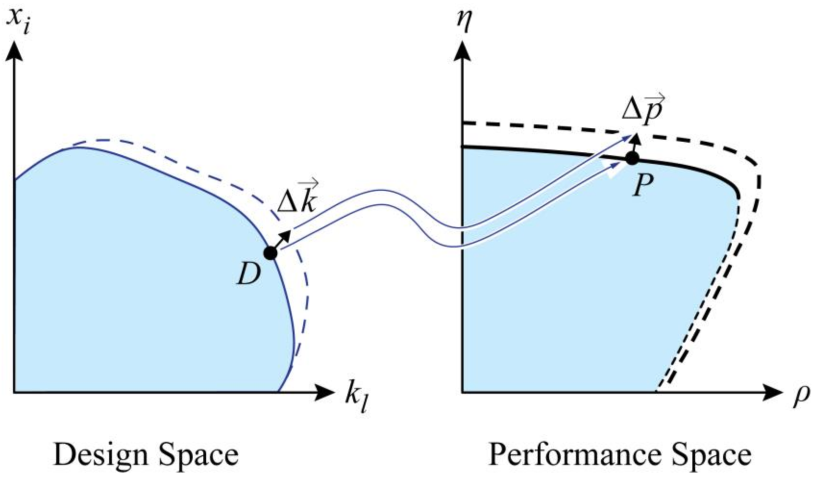


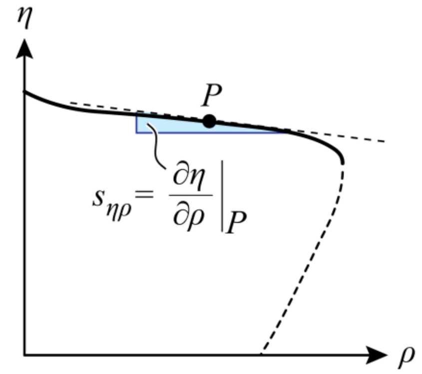
Source: Ostendorf & König / DeGruyter

- *Fully Digital Control of Complex Systems*
- *Massive Computational Power → Fully Automated Design & Manufacturing / Industrial IoT (IIoT)*

Automated Design

- *Based on Mathematical Model of the Technology Mapping*
- *Multi-Objective Optimization → Best Utilization of the "Design Space"*
- *Identifies Absolute Performance Limits → Pareto Front / Surface*

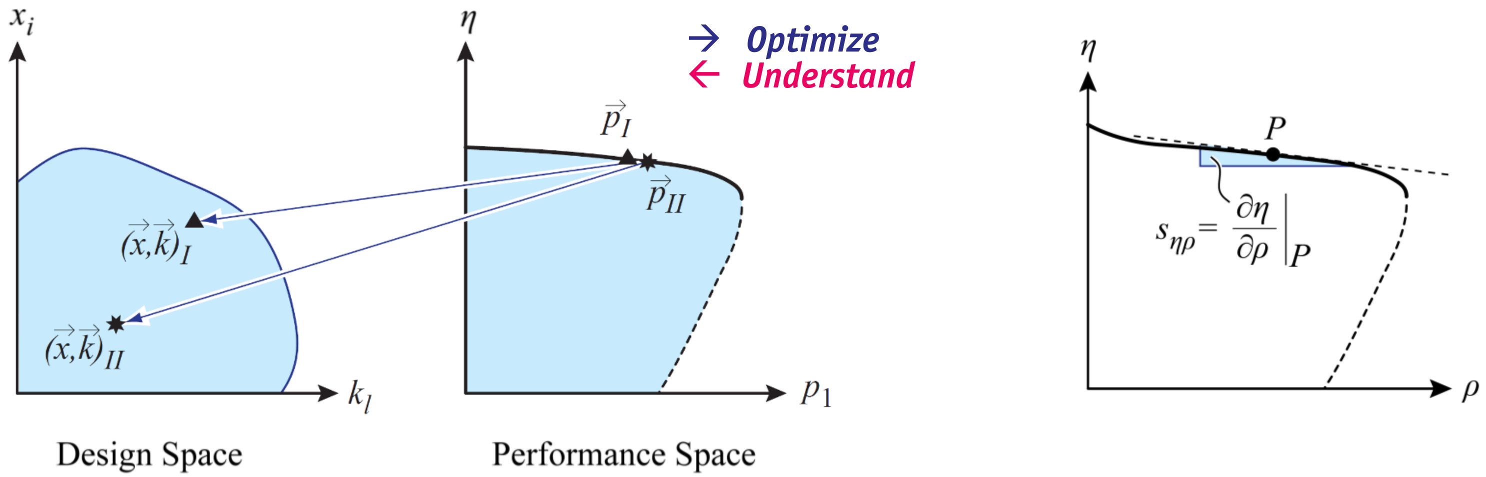




- Clarifies *Sensitivity* $\Delta\vec{p}\,/\,\Delta\vec{k}$ to Improvements of Technologies
- *Trade-Off Analysis*

Automated Design

- Design Space Diversity
- Equal Performance for Largely Different Sets of Design Parameters (!)

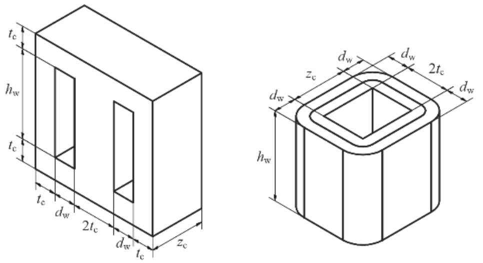


→ Optimize
← Understand

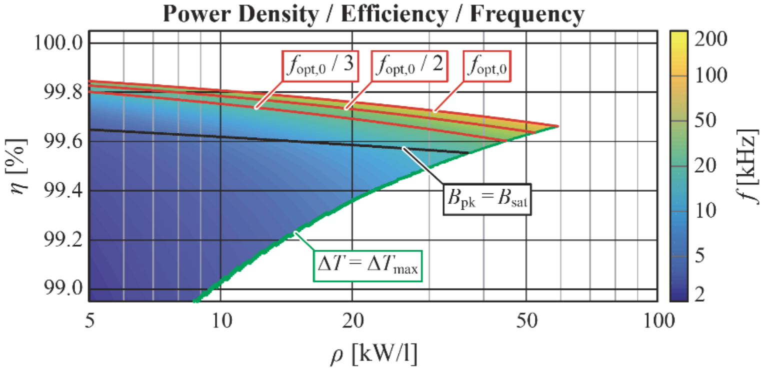
- E.g. Mutual Compensation of Volume and Loss Contributions (e.g. Cond. & Sw. Losses)
- Allows Optimization for Further Performance Indices (e.g. Costs)

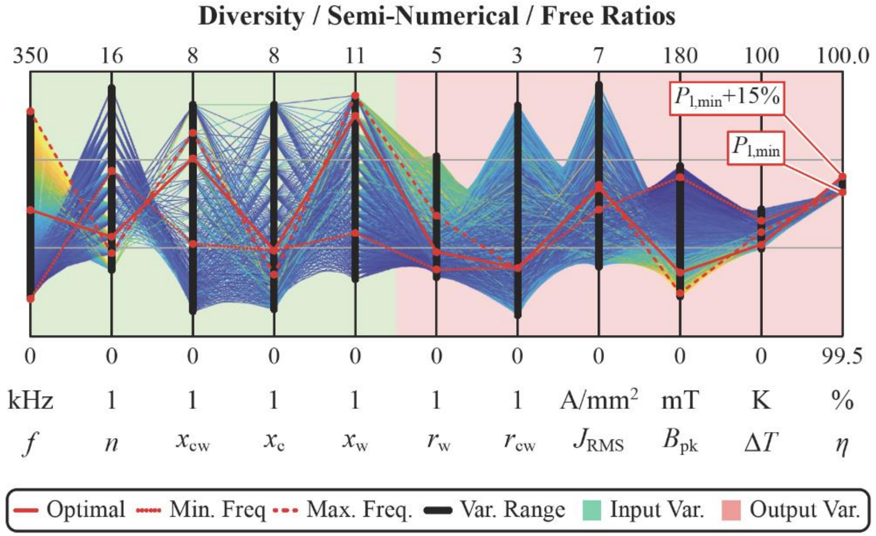
Design Space Diversity - Example

- *Design of a Medium-Frequency Transformer*
- *Wdg./Core Loss Ratio, Geometry, n etc. as Design Parameters*
- *Power Level & Power Density = const.*



Source: T. Guillod / ETH





$x_{cw} = A_c / A_w, \quad x_c = z_c / 2\,t_c, \quad x_w = h_w / d_w$

- *Mutual Compensation Core & Winding Losses Changes*
- *Limit on Part Load Efficiency / Costs / Fixed Geometry → Restricts Diversity*

Automated Design Roadmap

- *End-to-End Horizon of Modeling & Simulation*
- *Design for Cost / Volume / Efficiency Target / Manufacturing / Testing / Reliability / Recycling*

State-of-the-Art
- *User Defined* Models and Simulation / Fragmented

Assisted Design ←
- *Support* of the User with Abstracted Database of Former Designs

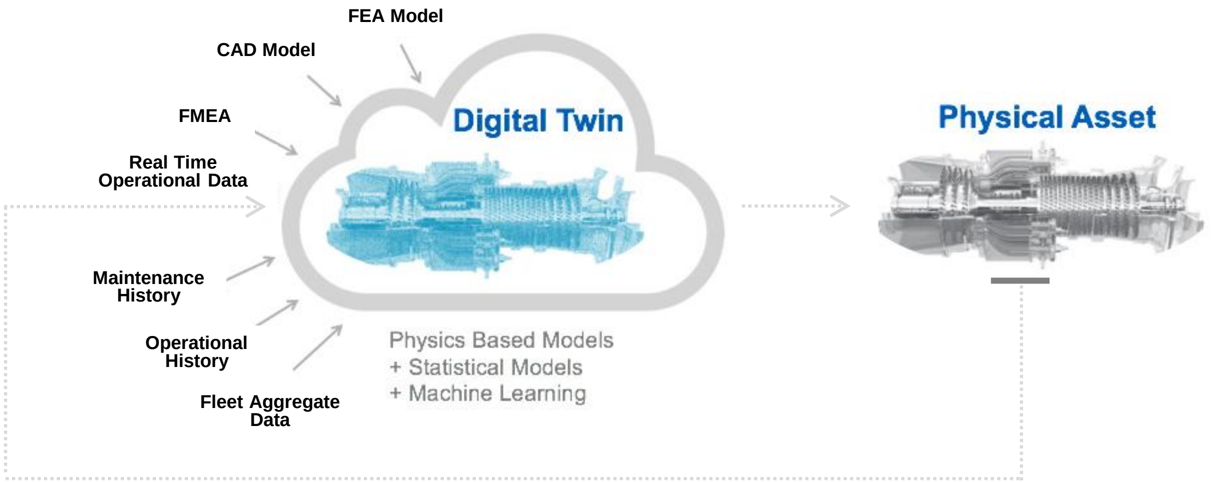
Augmented Design
- *Suggestion* of Design Details Based on Previous Designs

Autonomous Design → Design 4.0
- *Independent* Generation of Full Designs for Final Expert Judgement

- *AI-Based Summaries → No Other Way to Survive in a World of Exp. Increasing # of Publications (!)*

IIoT in Power Electronics

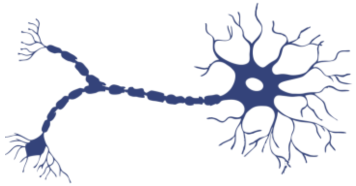
- *Digital Twin* → *Physics-Based “Digital Mirror Image”*
- *Digital Thread* → *“Weaving“ Real/Physical & Virtual World Together*



Source: www.railwayage.com

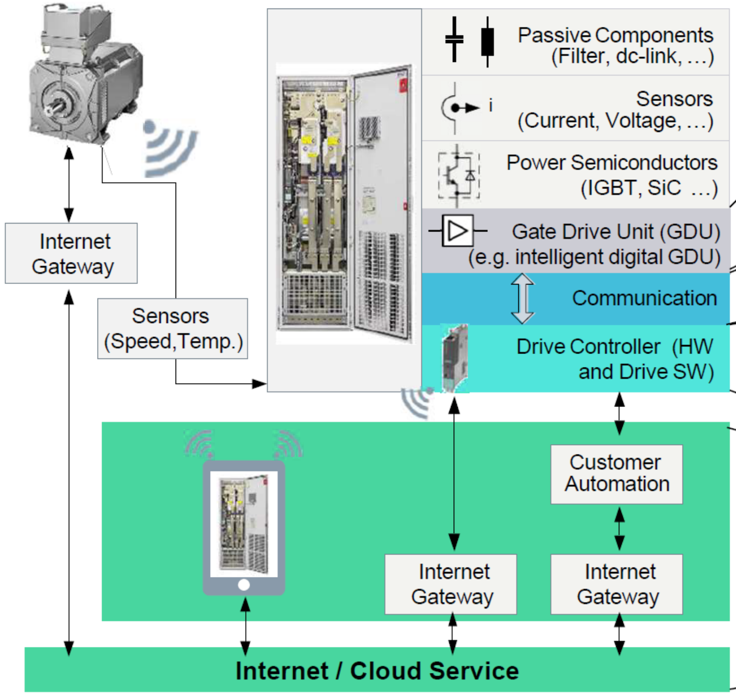
- *Requires Proper Interfaces for Models & Automated Design*
- *Model of System´s Past/Current/Future State → Design Corrections / Prev. Maintenance etc.*

Smart Inverter Concept



- *Utilize High Computing Power and Network Effects in the Cloud*

Source: R. Sommer
SIEMENS



Intelligent Gate Drive Unit
- Semiconductor protection (overcurrent, overvoltage, …)
- Collecting and preprocessing of sensor data (current, voltage, temperature, …)
- Semiconductor specific condition monitoring functions

Communication
- Communication protocol instead of on/off signals

Drive Controller
- Observer based condition monitoring functions
- Predictive maintenance functions
- Data Processing and data compression
- Communication to customer automation and/or internet

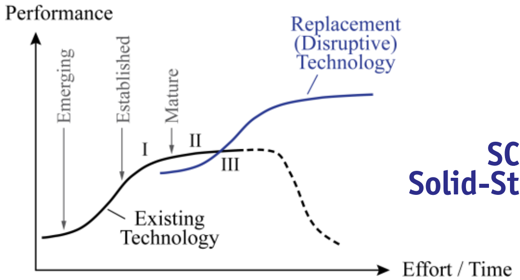
Internet / Cloud
- Service and commissioning tools
- Algorithms for „Big Data“ analysis
- Smart documentation (e.g. video to support service)
- …

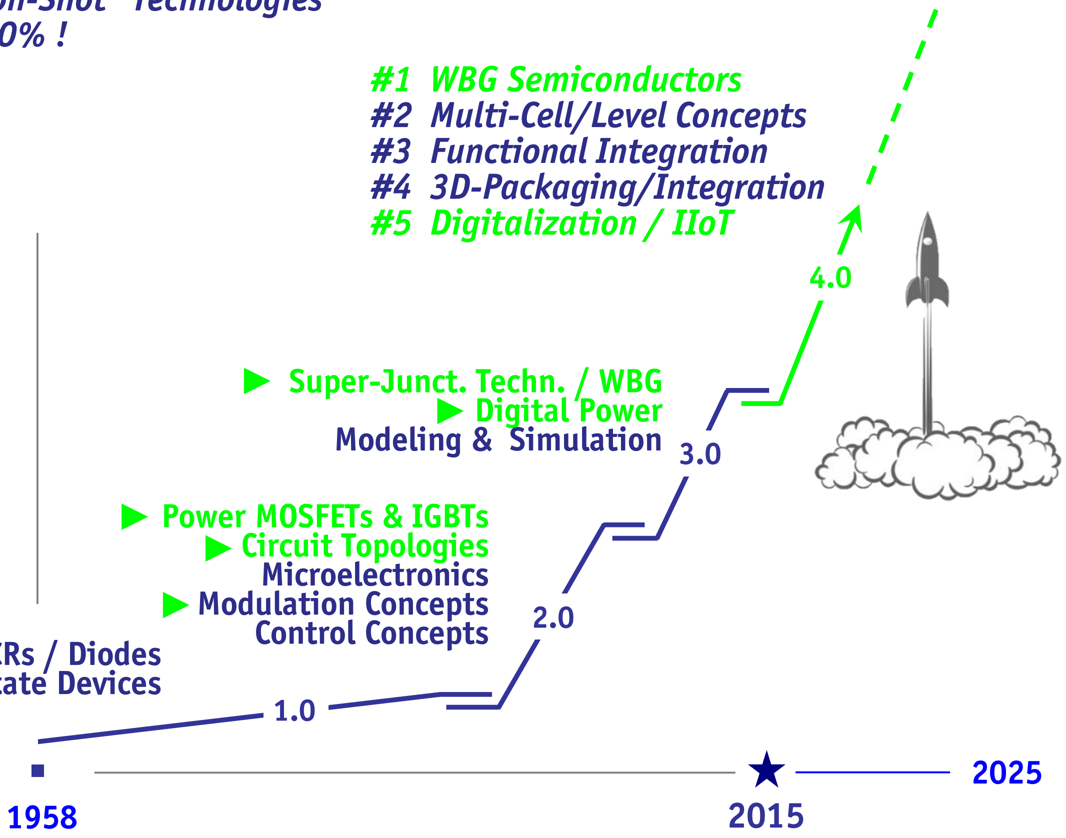
- *Component — Converter — System — Application Level*

Conclusion

S-Curve of Power Electronics

- *Power Electronics 1.0 → Power Electronics 4.0*
- *Identify “X-Concepts” / “Moon-Shot” Technologies*
- *10 x Improvement NOT Only 10% !*




#1 WBG Semiconductors
#2 Multi-Cell/Level Concepts
#3 Functional Integration
#4 3D-Packaging/Integration
#5 Digitalization / IIoT

▶ Super-Junct. Techn. / WBG
▶ Digital Power
Modeling & Simulation

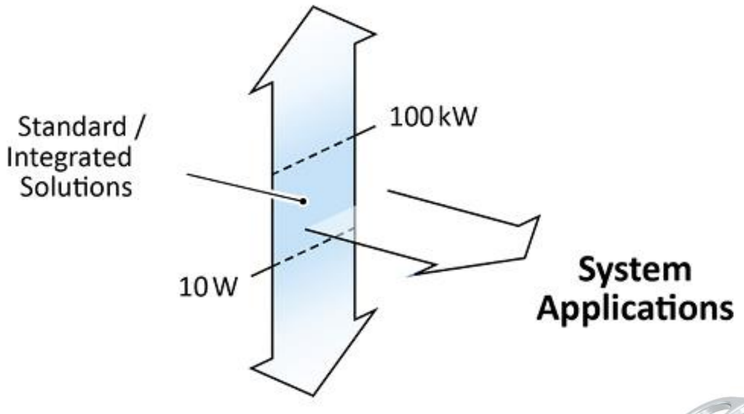
▶ Power MOSFETs & IGBTs
▶ Circuit Topologies
Microelectronics
▶ Modulation Concepts
Control Concepts

SCRs / Diodes
Solid-State Devices

Future Development

- Commoditization / Standardization
- Extreme Cost Pressure (!)
- Power → „Energy“
- Converter → System
- Time → Life Cycle

“There is Plenty of Room at the Top” → *Medium Voltage/Frequency Solid-State Transformers*



Power-Supplies on Chip ← **“There is Plenty of Room at the Bottom”**

- Key Importance of Technology Partnerships of Academia & Industry

PEMC

My Sincere
Congratulations !

Thank you!