Power Electronic Systems
Laboratory

Proceedings of the 17th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2016), Trondheim, Norway, June 27-30, 2016

Analysis and Design of a Multi-Tapped High-Frequency Auto-Transformer Based Inverter System

M. Guacci,
D. Neumayr,
D. Bortis,
J. W. Kolar,
G. Deboy

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Analysis and Design of a Multi-Tapped High-Frequency Auto-Transformer Based Inverter System

Mattia Guacci*, Dominik Neumayr*, Dominik Bortis*, Johann W. Kolar* and Gerald Deboy†
*Power Electronic System Laboratory, Swiss Federal Institute of Technology ETH Zürich, Zürich, Switzerland
e-mail: guacci@lem.ee.ethz.ch
†Infineon Technologies Austria AG, Villach, Austria

***Abstract*—The Google Little Box Challenge, an open competition to build the world smallest 2 kW Photo-Voltaic (PV) inverter, triggered a trend in the power electronic community to design PV inverter systems with a very high power density. In particular, in this paper, a novel single-phase non-isolated PV inverter topology is presented, achieving both high efficiency and high power density.**
The proposed solution takes advantage of a highly efficient resonant DC-DC stage to generate multiple intermediate DC voltage levels; these levels are then modulated by means of a high-frequency operating tap-selector and the resulting waveform is filtered and unfolded to obtain a low-frequency sinusoidal voltage at the output. Only a fraction of the full DC-link voltage is switched in every commutation of the tap-selector, consequently the occurring switching losses are reduced with respect to single-stage PWM inverters.
At the core of the DC-DC stage, a high-frequency auto-transformer with multiple output taps is employed. Since it is realized only with a single winding and a fraction of the input current directly flows to the output, its utilization increases the efficiency and reduces the volume with respect to an equivalent transformer based solution.
A detailed analysis of the working principle of the investigated inverter is presented in this paper together with a Pareto optimal design, focusing in particular on the resonant operation and on the modeling of the auto-transformer. The performance in terms of losses and volume is finally provided for the optimal solution.

***Index Terms*—PV Inverter, High Efficiency, High Power Density, Auto-Transformer, Multi-Tapped Inductor, Google Little Box Challenge.**

I. Introduction

With the aim of pushing the frontier in power density of today's Photo-Voltaic (PV) inverter systems and promoting the advantages of modern wide band-gap semiconductor devices, Google and IEEE launched the Google Little Box Challenge (LBC) [1], an open competition to build the world smallest $2\,\mathrm{kW}$ PV inverter. At the official drop-off event, all invited finalists presented their technical approaches [2] and the majority of the submissions relied on a single-stage non-isolated full-bridge based PWM inverter topology, herein schematically represented in Fig.1 (a). Generally, single-phase PV inverter systems without galvanic isolation exhibit higher efficiency (up to $98\,\%$) and reduced volume and weight compared to solutions with isolation [3]. However, in single-stage inverters, the full DC-link voltage is continuously switched and the occurring losses limit the switching frequency and, to a large extend, the power density of the system. In fact, an increase of the switching frequency reduces the volume of the components in the output filter but, if the switching losses are prevailing, it also leads to a substantially larger volume requirements for the heat-sink. In case soft-switching modulation techniques, such as triangular current mode (TCM), are applied, switching losses are reduced at the expense of increased conduction losses in power switches and in filter inductors, due to higher ripple currents [4].
At the final LBC event, a very unconventional approach, proposed by one of the participants, caught everyones attention, claiming astonishing $99.5\,\%$ efficiency at a remarkable power density of $17.4\,\mathrm{kW/dm^3}$ ($285\,\mathrm{W/in^3}$) [5]. At the core of this solution, an auto-transformer based DC-DC stage generates intermediate DC voltage levels; then, a tap-selector alternately connects to these levels in order to approximate a staircase-shaped sinusoidal voltage waveform at the output. Increasing the number of DC voltage levels, the voltage switched by the tap-selector decreases, as opposed to conventional

978-1-5090-1815-4/16/$31.00 ©2016 IEEE

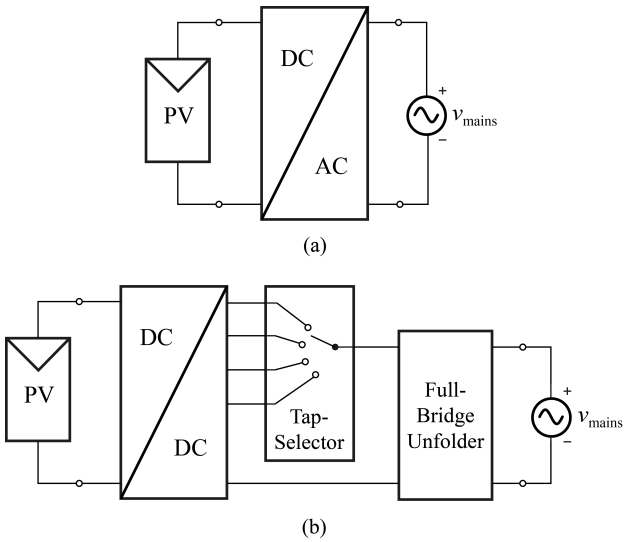

Fig. 1. Single-phase non isolated PV inverter systems: (a) conventional single-stage solution (b) auto-transformer based DC-DC stage solution with tap-selector and full-bridge unfolder.

PWM inverters where the full DC-link voltage is always switched. Moreover, the utilization of an auto-transformer offers the advantage of reduced copper losses with respect to a conventional transformer since a portion of the primary current flows directly to the connected output tap. Furthermore, since the auto-transformer is realized just with a single winding with multiple taps, a higher power density can be achieved [6] but galvanic isolation is not provided.
With the purpose of verifying the claimed performance and the advantages in terms of efficiency and power density of an auto-transformer based PV inverter, several topologies, schematically summarized in Fig.1 (b), have been investigated and compared; the resulting most promising approach is presented in this paper.
The main advantage of the proposed solution is the reduction of switching losses, in fact, as described in Section II, the multi-level DC-DC stage is operated in resonant fashion achieving Zero Voltage Switching (ZVS) in every load condition. Additionally, the switching losses in the tap-selector are reduced since only a fraction of the full DC-link voltage is switched. Finally, a full-bridge unfolder is employed to generate an AC voltage and as a consequence of its low-frequency operation, switching losses are negligible and the chip area can be increased to reduce conduction losses.
The structure of the multi-tapped high-frequency auto-transformer employed in the DC-DC stage and its advantages are described in Section III. Transparent estimates of the claimed improvement in efficiency and power density are provided in Section IV, together with a detailed description of the adopted design parameters and the associated simulated waveforms.

II. Working Principle and Resonant Operation

The proposed inverter topology is illustrated in Fig.2 with four DC voltage levels considered. The DC-link voltage and the $0\,\mathrm{V}$ reference are available from the source, while two intermediate DC voltage

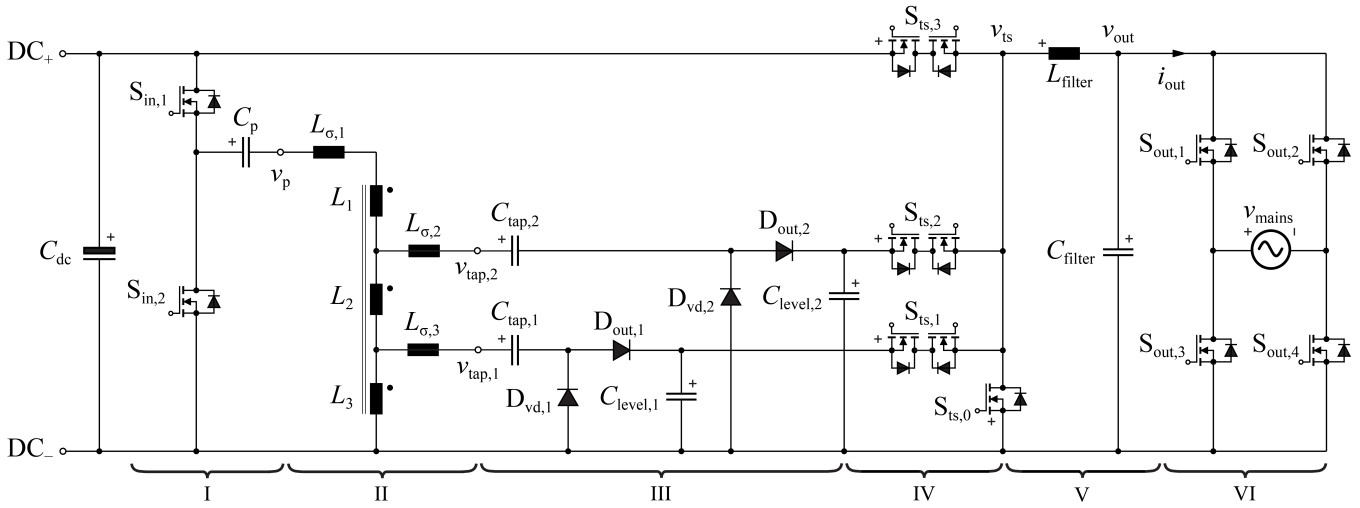

Fig. 2. Proposed topology with four DC voltage levels considered, divided in six parts: input half-bridge and DC blocking capacitor (I), auto-transformer (II), voltage doubler (III), tap-selector (IV), output filter (V) and full-bridge unfolder (VI). All labeled potentials are referred to DC$_-$.

levels are generated in the DC-DC stage. A half-bridge circuit, operating with a $50\,\%$ duty cycle at a frequency $f_{\mathrm{sw,in}}$, together with a DC-blocking capacitor C_{p} (I), applies a zero-mean square-wave voltage v_{p} of amplitude $V_{\mathrm{Cdc}}/2$ to the input of a high-frequency multi-tapped auto-transformer (II). Depending on the turns ratio between the input tap and each output tap of the auto-transformer, scaled square-wave voltages $v_{\mathrm{tap,i}}$ appear at the input of the voltage doubler circuits (III), generating intermediate DC voltage levels $V_{\mathrm{Clevel,i}}$. A subsequent tap-selector (IV), operating at a PWM switching frequency $f_{\mathrm{sw,ts}}$, alternately connects to the individual $V_{\mathrm{Clevel,i}}$ such that the low-pass filtered voltage v_{out} resembles the voltage reference $v_{\mathrm{ref}} = |v_{\mathrm{mains}}|$ as shown in Fig.3 (c). Hence, a LC-filter (V) and a full-bridge unfolder (VI) are connected between the tap-selector and the mains to attenuate the high-frequency components of v_{ts} originate from the PWM operation of the tap-selector and to generate a low-frequency AC output voltage v_{mains}, respectively.

The unique feature of this novel topology is the resonant operation of the DC-DC auto-transformer based input stage. As mentioned in Section I, the DC-DC stage is dimensioned such that a series-resonance between C_{p}, $L_{\mathrm{s(i,j)}}$ and $C_{\mathrm{tap,i}}$ is excited. $L_{\mathrm{s(i,j)}}$ is the leakage inductance between the i^{th} and the j^{th} tap of the auto-transformer and it can be calculated from $L_{\sigma,\mathrm{i}}$ indicated in Fig.2. Consequently, the input current of the auto-transformer i_{Cp}, depicted in Fig.3 (d), is sinusoidal and, despite its time-varying envelope shown in Fig.3 (c), the resonant operation is maintained during the whole mains period.

The difficulty in maintaining the resonant operation is that, depending on the actual tap-selector position, the prevailing leakage inductance seen from the input tap of the auto-transformer changes. For example, when the tap-selector switches $\mathrm{S_{ts,2}}$ and $\mathrm{S_{ts,1}}$ are alternately operated, the leakage inductance results in a time-varying linear combination of $L_{\mathrm{s(1,2)}}$ and $L_{\mathrm{s(1,3)}}$. Therefore, the value of $C_{\mathrm{tap,i}}$ and C_{p} must be selected in order to match $L_{\sigma,\mathrm{i}}$, tuning the resonant frequency to $f_{\mathrm{sw,in}}$ in all the operating conditions. A closed-form expression defining this procedure will be provided in Section III, after a detailed modeling of the auto-trasformer. Consequently, near Zero Current Switching (ZCS) and ZVS, due to the magnetizing current of the employed auto-transformer [7], are achieved for $\mathrm{S_{in,1}}$ and $\mathrm{S_{in,2}}$.

The employed control scheme only operates simultaneously the two tap-selector switches which associated $V_{\mathrm{Clevel,i}}$ encloses v_{ref}. For example, if $V_{\mathrm{Clevel,2}} < v_{\mathrm{ref}} < V_{\mathrm{Cdc}}$, $\mathrm{S_{ts,2}}$ and $\mathrm{S_{ts,3}}$ are alternated as shown in Fig.3 (c). In the following, each operating pair of switches is addressed as tap-selector state: in the mentioned case, the associated state occurs for $t_1 < t < t_2$ in the first quarter of mains period, as shown in Fig.3 (c). This control strategy minimizes the voltage switched by the tap-selector switches and the current ripple of i_{Lfilter}, illustrated in Fig.3 (e), therefore reducing the occurring losses. Additionally, due to the bidirectional blocking capability of the tap-selector switches, a commutation strategy is required to continuously provide a path for the current i_{Lfilter} during the tap-selector dead-times [8].

In order to dimension the DC-DC stage components, the envelopes of i_{Cp} and of all the other currents flowing in the auto-transformer have to be calculated. As an example, a purely resistive load R_{out} is considered. Given a value for v_{ref}, assumed to be constant within the tap-selector switching period $T_{\mathrm{sw,ts}}$, the tap-selector state is determined and a duty-cycle d_{i} for each $\mathrm{S_{ts,i}}$ is computed in order to generate v_{out}. The average current in each tap-selector switch $I_{\mathrm{Sts,i}}$ results proportional to the output current i_{out}, constant within $T_{\mathrm{sw,ts}}$, as

$$I_{\mathrm{Sts,i}} = d_{\mathrm{i}} i_{\mathrm{out}} = d_{\mathrm{i}} \frac{v_{\mathrm{out}}}{R_{\mathrm{out}}}. \tag{1}$$

Furthermore, $I_{\mathrm{Sts,i}}$, assumed to be constant within an input switching period $T_{\mathrm{sw,in}}$, can be related to the peak of the high-frequency sinusoidal current $I_{\mathrm{Ctap,i,pk}}$ in the corresponding voltage doubler, imposing, on average, constant charge of $C_{\mathrm{level,i}}$

$$\begin{aligned} I_{\mathrm{Sts,i}} &= \frac{1}{T_{\mathrm{sw,in}}} \int_0^{T_{\mathrm{sw,in}}/2} I_{\mathrm{Ctap,i,pk}} \sin(2\pi f_{\mathrm{sw,in}} t)\, \mathrm{d}t \\ &= \frac{I_{\mathrm{Ctap,i,pk}}}{\pi}. \end{aligned} \tag{2}$$

Equating (2) and (1) through the common term $I_{\mathrm{Sts,i}}$, an expression relating the currents in the DC-DC stage to the currents in the output stage is obtained,

$$I_{\mathrm{Ctap,i,pk}} = d_{\mathrm{i}} \pi \frac{v_{\mathrm{out}}}{R_{\mathrm{out}}}. \tag{3}$$

According to (3), knowing d_{i} for each $\mathrm{S_{ts,i}}$, the corresponding $I_{\mathrm{Ctap,i,pk}}$ is determined directly from v_{out} for each $T_{\mathrm{sw,in}}$.

Because of the resonant operation of the input half-bridge, each current in the DC-DC stage can be characterized by a generic sinusoidal waveform

$$i_{\mathrm{x}} = I_{\mathrm{x,pk}} \sin\left(2\pi f_{\mathrm{sw,in}} t\right), \tag{4}$$

$$I_{\mathrm{x,pk}} = \widetilde{d}_{\mathrm{x}}(t) \pi \frac{v_{\mathrm{out}}}{R_{\mathrm{out}}}, \tag{5}$$

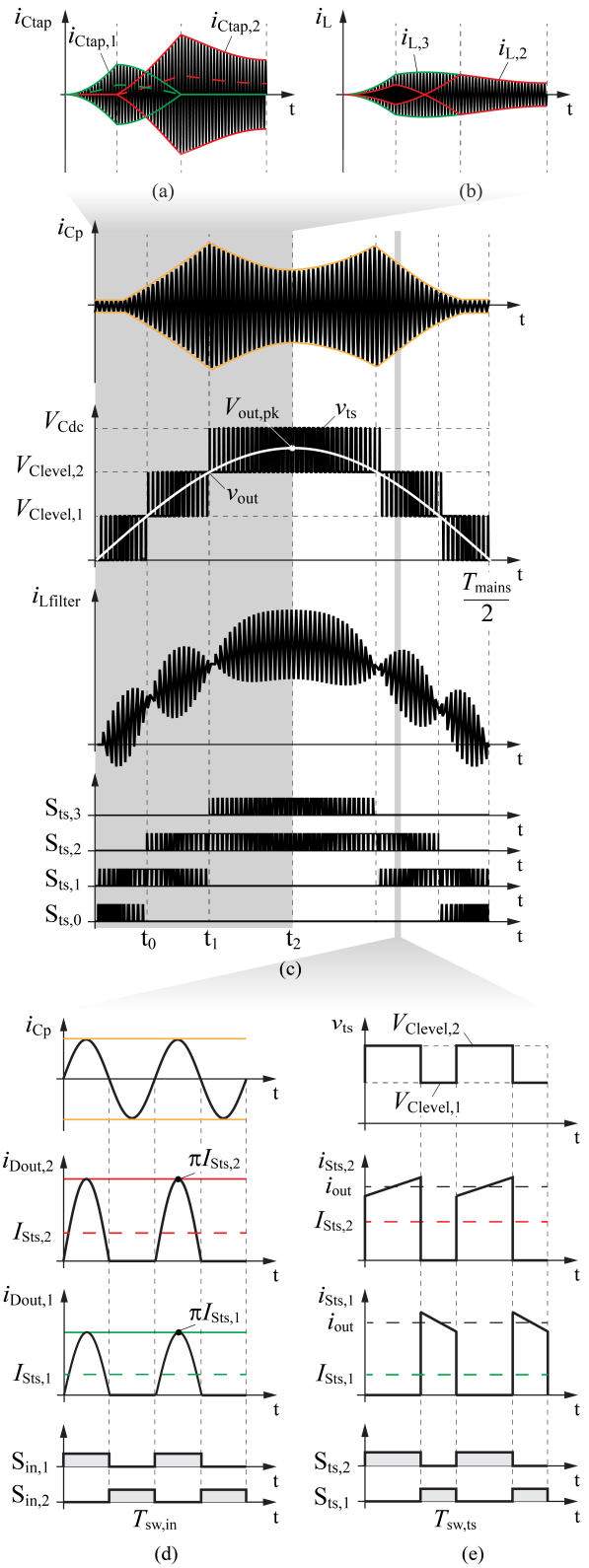

Fig. 3. Current and voltage waveforms in a mains half-period: (a) sinusoidal currents at the input of the voltage doubler circuits (b) sinusoidal currents in the auto-transformer winding (c) auto-transformer input current; PWM and filtered voltage at the output of the tap-selector; variable ripple current at the output of the tap-selector (d) zoom of the sinusoidal currents in the input half-bridge switches and in the voltage doubler circuits (e) zoom of the PWM voltage and of the triangular currents at the output of the tap-selector.

TABLE I

ENVELOPE OF THE CURRENTS IN THE AUTO-TRANSFORMER WINDING AND AT THE INPUT OF THE VOLTAGE DOUBLER CIRCUITS AS A FUNCTION OF THE OUTPUT VOLTAGE IN A QUARTER OF THE MAINS PERIOD. THE CORRESPONDENT TIMING IS INDICATED IN FIG.3 (C)

$\widetilde{d}_x$	$0 < t < t_0$	$t_0 < t < t_1$	$t_1 < t < t_2$
$\widetilde{d}_{Ctap,1}$	d^*	$2 - d^*$	0
$\widetilde{d}_{Ctap,2}$	0	$d^* - 1$	$3 - d^*$
$\widetilde{d}_{Cp} = \widetilde{d}_{L1}$	$d^*/3$	$d^*/3$	$2(3-d^*)/3$
$\widetilde{d}_{L2}$	$d^*/3$	$(3-2d^*)/3$	$(d^*-3)/3$
$\widetilde{d}_{L3}$	$-(2d^*)/3$	$(d^*-3)/3$	$(d^*-3)/3$

with different time-varying envelopes $\widetilde{d}_x(t)$. Subscript x denotes a component in the DC-DC stage and all the calculated $\widetilde{d}_x(t)$ are listed in Table I, when a uniform turns ratio in the auto-transformer winding is considered and the generic duty-cycle d^* is defined as

$$d^* \doteq \frac{v_{ref}}{V_{Cdc}/3}. \tag{6}$$

As example, particularizing (5) with $x = C_{tap,i}$ and comparing it with (3)

$$\widetilde{d}_{Ctap,i}(t) = d_i \tag{7}$$

results immediately. Considering, on first approximation, the auto-transformer as a loss-less network, knowing the voltage waveforms at its output taps and imposing power conservation at its ports, i_{Cp} can be calculated from $i_{Ctap,i}$, therefore determining $\widetilde{d}_{Cp}(t)$. Additionally, the current circulating in the winding i_{Li} can now be calculated directly from the Kirchoff's current law.

The so obtained close-form expressions for the current envelopes are highlighted in Fig.3 (a)-(b) in a quarter of mains period, perfectly matching the simulated results. In particular, the red and the green curves point out the correspondence between the high-frequency Fig.3 (d)-(e) and the mains frequency Fig.3 (a)-(b)-(c) currents in different plots. For example, when $S_{ts,3}$ is operating, part of the output current i_{out} flows directly from the DC-link, reducing the amplitude of i_{Cp} and the conduction losses in the DC-DC stage. Additionally, Fig.3 (a) shows that the current in the voltage doubler circuits $i_{Ctap,i}$ flows only when the relative tap selector is operated. Finally, Fig.3 (b) illustrates the current waveforms in the auto-transformer winding highlighting the reduction of copper losses with respect to the case of a conventional transformer. In fact, while in a step-down auto-transformer the whole primary current flows directly to the connected output tap, in a conventional transformer each output current would entirely flow in the corresponding secondary winding, having the envelope of $i_{Ctap,i}$ for the same load condition. A quantitative expression evaluating this advantage is provided in Section III.

III. MULTI-TAPPED HIGH-FREQUENCY AUTO-TRANSFORMER DESIGN AND MODELING

The auto-transformer is the key component of the presented converter and, as discussed in Section II, the high efficiency of the DC-DC stage results from its usage. In order to dimension the resonant circuit components, an equivalent circuital model of the auto-transformer, independent from the operating point of the converter and including the respective leakage inductances, is needed. A solution to this problem, based on the Short and Leakage Inductance Method (SLIM) [9], is explained in this section.

Initially, considering a particular auto-transformer design, a procedure to determine the values of $L_{s(i,j)}$ is presented. However, the leakage inductances seen from the primary side of the auto-transformer

$L_{s(1,j)}$ are not suitable for the model, since they depend on the actual tap-selector state. Therefore, a solution to estimate the leakage inductances $L_{\sigma,i}$ shown in Fig.2, is proposed later on. Hence, the values of C_p and $C_{tap,i}$ can be easily calculated in order to match the impedance of the associated $L_{\sigma,i}$, achieving a series-resonance at $f_{sw,in}$.

An E-type magnetic core with the winding configuration illustrated in Fig.4 (a), is considered as an example. The SLIM characterizes the non-ideality of a magnetic component by measuring or calculating each $L_{s(i,j)}$ through the magnetic energy of the system for a specific configuration of the winding taps. In particular, index i refers to a tap from which the inductance is measured and a current I is impressed, while index j refers to a tap which is shorted to the reference point. The impressed current generates a magnetic flux that is partially compensated by the current induced in the short circuit, while the remaining flux is related to the leakage inductances. To clarify the notation and to express the result only as a function of the position of the taps with respect to the total number of turns N_{tot}, the following three quantities are additionally defined. In particular, N_1 is the number of turns from the beginning of the winding q to the input tap a, N_2 between tap a and the output tap b and N_3 from tap b to the reference point r.

In the setup depicted in Fig.4, the magnetic energy $W_{M(a,b)}$ stored in the leakage inductance $L_{s(a,b)}$ can be expressed as

$$\begin{aligned} W_{M(a,b)} &= \frac{1}{2}\int_V B \cdot H \mathrm{d}V \\ &= \frac{1}{2} L_{s(a,b)} I^2 \end{aligned} \tag{8}$$

where the indicated integration volume V corresponds to the entire winding volume. Assuming that the magnetic field H is only oriented in y direction, constant in y and z directions, and directly proportional to the magnetic flux density B through μ_0, (8) can be simplified to

$$W_{M(a,b)} = \mu_0 \frac{l_w h}{2} \int_0^w H_y^2(x)\mathrm{d}x. \tag{9}$$

Considering piece-wise linear trends for H_y (10), reaching a maximum H_{pk} directly proportional to the ampere-turns and inversely proportional to h

$$H_y = \begin{cases} \frac{1}{h} N_3 \frac{N_2}{N_3} I \frac{x}{\frac{N_3}{N_{tot}} w} & 0 \le x < \frac{N_3}{N_{tot}} w \\ -\frac{1}{h} N_2 I \frac{x - \frac{N_2+N_3}{N_{tot}} w}{\frac{N_2}{N_{tot}} w} & \frac{N_3}{N_{tot}} w \le x \le \frac{N_2+N_3}{N_{tot}} w \\ 0 & \frac{N_2+N_3}{N_{tot}} w < x \le w \end{cases} \tag{10}$$

equation (9) can be solved

$$\begin{aligned} W_{M(a,b)} &= \frac{1}{2} \frac{\mu_0 l_w w}{h} \left(\frac{N_{tot}}{3}\right)^2 I^2 \frac{3(N_2+N_3)N_2^2}{N_{tot}^3} \\ &= \frac{1}{2} L_0 I^2 \frac{3(N_2+N_3)N_2^2}{N_{tot}^3} \end{aligned} \tag{11}$$

where for convenience

$$L_0 \doteq \frac{\mu_0 l_w w}{h} \left(\frac{N_{tot}}{3}\right)^2 \tag{12}$$

is defined. L_0 only depends on the geometrical characteristics w, h and l_w of the core, indicating the width and the height of the winding window and the average length of a turn, respectively. A general expression for $L_{s(a,b)}$ (13), only depending on the constructive parameters of the transformer, is obtained equating (8) and (11).

$$L_{s(a,b)} = L_0 \frac{3(N_2+N_3)N_2^2}{N_{tot}^3} \tag{13}$$

The general equation (13), valid for all the $L_{s(i,j)}$ of every auto-transformer design with the winding arrangement depicted in Fig.4, can now be applied to the specific case shown in Fig.2.

The auto-transformer employed in the DC-DC stage has one input and two output taps, therefore it can be characterized by means of three independent $L_{s(i,j)}$ which associated SLIM experiments are depicted in Fig.5. The current fractions derives directly from the adopted turns ratio. Considering the auto-transformer as an ideal voltage divider, the voltages at the output taps are fixed from the input voltage and the output current can be calculated imposing power conservation. Differently from a conventional transformer, a third current is flowing in the winding to compensate the difference between the input and the

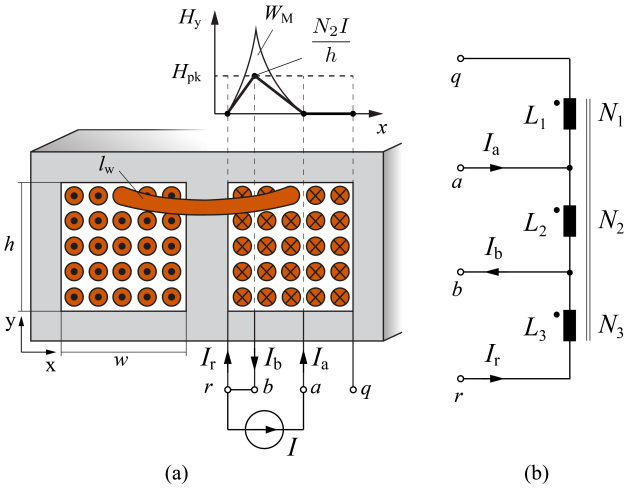

Fig. 4. Short and Leakage Inductance Method measurement circuit applied to a multi-tapped auto-transformer: (a) magnetic field H_y and magnetic energy $W_{M(a,b)}$ trends due to an impressed current I in a E-type magnetic core (b) equivalent circuital model.

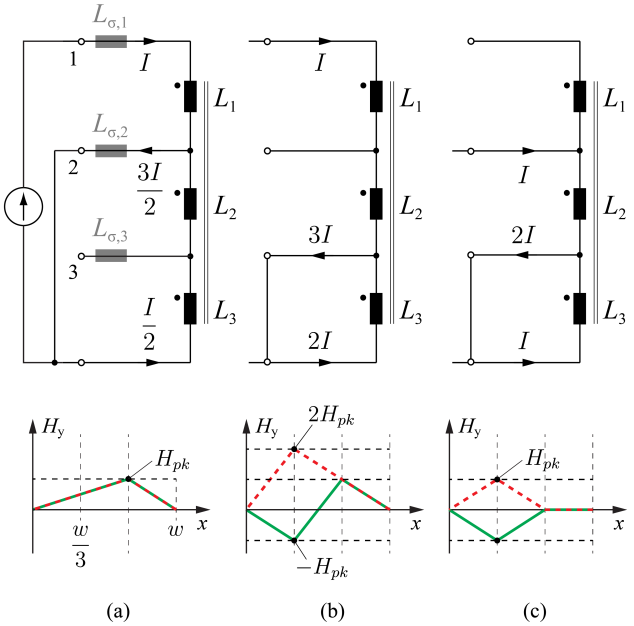

Fig. 5. Equivalent circuital models of the three Short and Leakage Inductance Method measurement circuits necessary to characterize the considered multi-tapped auto-transformer and magnetic field H_y trends due to an impressed current I for two different possible winding solutions: (a) $L_{s(1,2)}$ (b) $L_{s(1,3)}$ (c) $L_{s(2,3)}$.

TABLE II
EQUIVALENT NUMBER OF TURNS AS A FRACTION OF N_{tot} NEEDED TO APPLY (11) TO THE THREE EXPERIMENTS DEPICTED IN FIG.5 AND RESULTING VALUE FOR THE LEAKAGE INDUCTANCE $L_{\mathrm{s(i,j)}}$.

(i,j)	N_1/N_{tot}	N_2/N_{tot}	N_3/N_{tot}	$L_{\mathrm{s(i,j)}}$
$(1,2)$	0	$1/3$	$2/3$	$1/3 L_0$
$(1,3)$	0	$2/3$	$1/3$	$4/3 L_0$
$(2,3)$	$1/3$	$1/3$	$1/3$	$2/9 L_0$

output currents. If a uniform turn ratio is considered, each $L_{\mathrm{s(i,j)}}$ and each H_{y} can be calculated from equations (13) and (10) respectively, considering the values for the number of turns reported in Table II. For example, in the case of $L_{\mathrm{s}(1,2)}$, tap a coincides with tap q and represents tap 1 of the considered auto-transformer design ($N_1 = 0$), tap b represents tap 2 ($N_2 = 1/3 N_{\mathrm{tot}}$) and tap r is DC$-$ ($N_3 = 2/3 N_{\mathrm{tot}}$). Repeating the procedure for $L_{\mathrm{s}(1,3)}$ and $L_{\mathrm{s}(2,3)}$, the magnetic fields illustrated in red in Fig.5 and the value for $L_{\mathrm{s(i,j)}}$ summarized in Table II result.

If the winding arrangement is modified, for example interleaving the three winding segments, (10) is not valid anymore. However, this expedient can reduce the magnetic energy, often yielding to a preferable magnetic design. For example, swapping the turns associated to L_2 and L_3 and repeating the procedure, the magnetic fields illustrated in green in Fig.5 result. As can be seen in Fig.5 (b), the peak of the magnetic field is halved in the worst case, therefore only this second solution is examined further. In this case, $L_{\mathrm{s(i,j)}}$ can be expressed as

$$L_{\mathrm{s}} = \begin{bmatrix} L_{\mathrm{s}(1,2)} & L_{\mathrm{s}(1,3)} & L_{\mathrm{s}(2,3)} \end{bmatrix}^T \doteq \Lambda^T L_0 \qquad (14)$$
$$\Lambda = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{2}{9} \end{bmatrix}.$$

The inductances gathered in L_{s} do not have a direct correspondence in the considered auto-transformer equivalent circuit shown in Fig.2, therefore they must be translated to L_σ. A procedure aiming at this purpose have been developed and it is explained in the following. A compact notation is introduced to clarify the calculation; in particular, $W_{\mathrm{M(i,j)}}$ indicate the magnetic energy associated to the experiment considered for the calculation of $L_{\mathrm{s(i,j)}}$.

$$W_{\mathrm{M}} = \begin{bmatrix} W_{\mathrm{M}(1,2)} & W_{\mathrm{M}(1,3)} & W_{\mathrm{M}(2,3)} \end{bmatrix}^T$$
$$L_\sigma = \begin{bmatrix} L_{\sigma,1} & L_{\sigma,2} & L_{\sigma,3} \end{bmatrix}^T$$
$$C_\sigma^{-1} = \begin{bmatrix} \frac{1}{C_{\mathrm{p}}} & \frac{1}{C_{\mathrm{tap},2}} & \frac{1}{C_{\mathrm{tap},1}} \end{bmatrix}^T$$

Considering as example the case of $L_{\mathrm{s}(1,2)}$, the associated magnetic energy $W_{\mathrm{M}(1,2)}$ can be expressed as

$$W_{\mathrm{M}(1,2)} = \frac{1}{2} L_{\mathrm{s}(1,2)} I^2 = \frac{1}{2} I^2 \left[L_{\sigma,1} + \left(\frac{3}{2} \right)^2 L_{\sigma,2} + 0 L_{\sigma,3} \right]. \qquad (15)$$

Repeating the procedure for $L_{\mathrm{s}(1,3)}$ and $L_{\mathrm{s}(2,3)}$ and gathering the results,

$$W_{\mathrm{M}} = \frac{1}{2} L_{\mathrm{s}} I^2 = \frac{1}{2} M L_\sigma I^2 \qquad (16)$$

$$M = \begin{bmatrix} 1 & (3/2)^2 & 0 \\ 1 & 0 & 3^2 \\ 0 & 1 & 2^2 \end{bmatrix}$$

is obtained. Equation (16) provides the necessary transformation

$$L_\sigma = M^{-1} L_{\mathrm{s}} = M^{-1} \Lambda^T L_0 \qquad (17)$$

from L_{s} to L_σ. Consequently, the capacitors C_σ^{-1} can be calculated in order to tune the resonant frequency at $f_{\mathrm{sw,in}}$, as

$$C_\sigma^{-1} = (2\pi f_{\mathrm{sw,in}})^2 L_\sigma = (2\pi f_{\mathrm{sw,in}})^2 M^{-1} \Lambda^T L_0. \qquad (18)$$

As discussed in Section II and showed in Fig.3 (a)-(b) the utilization of an auto-transformer reduces the current flowing in the winding with respect to an equivalent transformer based solution. A simple analytical expression (21), comparing the copper losses in the two cases $P_{\mathrm{c,t}}$ and $P_{\mathrm{c,at}}$, can be obtained for single output designs. For the fairness of the comparison, two designs with the same input-to-output voltage ratio are considered. In the case of the auto-transformer, this assumption results in connecting the output tap after N_{s} turns out of the total N_{p} turns that form the winding.

Considering a conventional transformer, the copper losses $P_{\mathrm{c,t}}$ can be expressed as

$$\begin{aligned} P_{\mathrm{c,t}} &= R_{\mathrm{turn}} \left(N_{\mathrm{p}} I_{\mathrm{rms,p}}^2 + N_{\mathrm{s}} I_{\mathrm{rms,s}}^2 \right) \\ &= R_{\mathrm{turn}} N_{\mathrm{p}} I_{\mathrm{rms,p}}^2 \left(n + 1 \right) \end{aligned} \qquad (19)$$

assuming same $R_{\mathrm{turn}}\,(\Omega/\mathrm{turn})$ for the primary and the secondary windings. In the case of an auto-transformer, the equivalent primary current I_{p} flows in $N_{\mathrm{p}} - N_{\mathrm{s}}$ turns, while the difference between I_{p} and the equivalent secondary current I_{s} flows in N_{s} turns; therefore the copper losses $P_{\mathrm{c,at}}$ can be expressed as

$$\begin{aligned} P_{\mathrm{c,at}} &= R_{\mathrm{turn}} \left[\left(N_{\mathrm{p}} - N_{\mathrm{s}} \right) I_{\mathrm{rms,p}}^2 + N_{\mathrm{s}} \left(I_{\mathrm{rms,p}} - I_{\mathrm{rms,s}} \right)^2 \right] \\ &= R_{\mathrm{turn}} N_{\mathrm{p}} I_{\mathrm{rms,p}}^2 \left| n - 1 \right|. \end{aligned} \qquad (20)$$

Finally, the ratio $P_{\mathrm{c,ratio}}$ can be obtained as

$$P_{\mathrm{c,ratio}} = \frac{P_{\mathrm{c,t}}}{P_{\mathrm{c,at}}} = \frac{n+1}{|n-1|} \quad n = \frac{N_{\mathrm{p}}}{N_{\mathrm{s}}} \in \mathbb{Q} \setminus \{0, 1\}. \qquad (21)$$

As a general design rule, (21) shows that the auto-transformer is more and more beneficial when n approaches one. (21) can also be applied in the considered case of a multi-tapped auto-transformer, averaging the three different tap-selector states that occurs every quarter of mains period, according to the timing expressed in Fig.3 (c). In particular for $0 < t < t_0$, $n = 3$ and $P_{\mathrm{c,ratio}} = 2$ while for $t_1 < t < t_2$, $n = 3/2$ and $P_{\mathrm{c,ratio}} = 5$. For $t_0 < t < t_1$, $P_{\mathrm{c,ratio}}$ is depending on the output current but for continuity goes from 2 to 5. The duration of the three tap-selector states increases when the slope of v_{out} reduces, therefore it is necessary to weight and average the different values. The so obtained result is a good approximation of the simulated value $P_{c,ratio} = 4.2$.

IV. $\eta\rho$ PARETO OPTIMIZED DESIGN AND PERFORMANCE EVALUATION

The results of a $\eta\rho$ Pareto optimization, minimizing the total volume of the converter, are described in detail in this section.

In this optimization routine, the switching frequency of the DC-DC stage $f_{\mathrm{sw,in}}$ and of the tap-selector $f_{\mathrm{sw,ts}}$ are chosen independently in a range of 50 kHz-500 kHz. For each frequency pair within this design space, a subsequent routine optimizes the magnetic components, selecting the magnetic cores with the minimum volume and the most efficient winding solution [10]. Several constraints regarding, for instance, the saturation flux density and the maximum current density, address the choice among a wide range of cores available on the market. The optimized switching frequencies are $f_{\mathrm{sw,in}} = 105\,\mathrm{kHz}$ and $f_{\mathrm{sw,ts}} = 130\,\mathrm{kHz}$, while the optimal magnetic cores are indicated in Table III, among all other selected components listed.

In line with the aim of the LBC, modern wide band-gap semiconductors are employed in the converter. In particular, a 600 V n.OFF CoolGaN™ GaN Infineon Technologies power transistor is considered, providing both low switching and conduction losses. Solely the full-bridge unfolder, mainly because of its low-frequency operation, is realized with super-junction Si MOSFETs. Two anti-series connected devices, needed in order to prevent unwanted current flow through the body diode, are used as tap-selector switches, however, in the near

TABLE III
CHOICE OF COMPONENTS TO REALIZE THE PARETO OPTIMAL DESIGN.

Item	Quantity	Value	Code	Manufacturer	Description
$S_{in,i}$	2		n.a. - prototype	Infineon Technologies	600 V n.OFF CoolGaN™ Transistor
$D_{vd,i}$	2		n.a. - prototype	Infineon Technologies	600 V n.OFF CoolGaN™ Transistor
$D_{out,i}$	2		n.a. - prototype	Infineon Technologies	600 V n.OFF CoolGaN™ Transistor
$S_{ts,i}$	7		n.a. - prototype	Infineon Technologies	600 V n.OFF CoolGaN™ Transistor
$S_{out,i}$	4		IPW65R019C7	Infineon Technologies	650 V CoolMOS™ C7 Transistor
L_i	3	582 µH	E 40/16/12	TDK	N87 Ferrite
L_{filter}	1	20 µH	E 25/13/7	TDK	N87 Ferrite
C_{dc}	3	493 µF	B43991X0009A223	Panasonic	450 V Aluminium Electrolytic Capacitor
C_p	6	1 µF	C5750X7R2E105K230KA	TDK	250 V Multilayer Ceramic Capacitor
$C_{tap,2}$	4	1 µF	C5750X7R2E105K230KA	TDK	250 V Multilayer Ceramic Capacitor
$C_{tap,1}$	15	1 µF	C5750X7R2E105K230KA	TDK	250 V Multilayer Ceramic Capacitor
$C_{level,i}$	30	2.2 µF	C5750X6S2W225K250KA	TDK	450 V Multilayer Ceramic Capacitor
C_{filter}	3	2.2 µF	C5750X6S2W225K250KA	TDK	450 V Multilayer Ceramic Capacitor

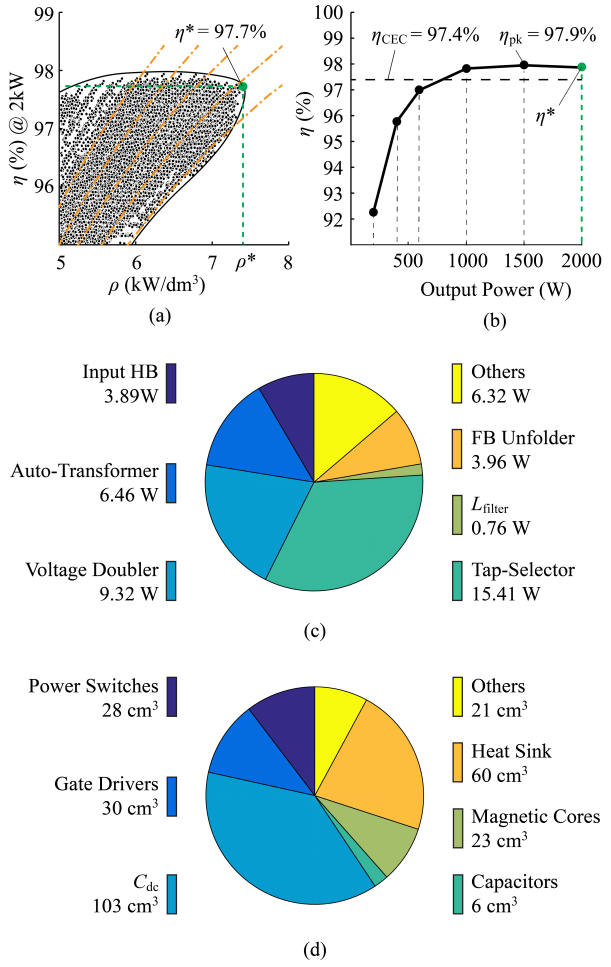

Fig. 6. Performance analysis in terms of efficiency and power density: (a) $\eta\rho$ Pareto optimization and power density optimized design (b) overall efficiency with respect to the output power (c) losses distribution in the different stages (d) contribution of the different component categories to the total volume.

future, single die four quadrants power semiconductors could replace them. Moreover, the rectifier diodes of the voltage doubler circuits are replaced with active switches for synchronous rectification, reducing the conduction losses.

Experimental measurements and numerical simulations have been conducted on the mentioned power switches in order to estimate the losses for different operating points, with the purpose of accurately evaluating the efficiency of the overall converter.

Multilayer ceramic capacitors, reaching a higher energy density than equivalent film capacitors, are employed in the different stages. In particular, X7R capacitors are preferred in the resonant circuits, guaranteeing a lower capacitance derating across the overall operating temperature range. Ripple specifications on V_{Cdc} directly provide an analytical expression for the dimensioning of C_{dc}. Due to its high value of $1.2\,\mathrm{mF}$, solely in this case electrolytic capacitors are preferred.

Fig.6 (a) shows the result of the optimization routine highlighting the selected solution among all the ones generated from the mentioned design space; in particular, an efficiency $\eta^* = 97.7\,\%$ at rated power and a power density $\rho^* = 7.4\,\mathrm{kW/dm^3}(121\,\mathrm{W/in^3})$ are reached. The $\eta\rho$ Pareto front and the analytical locus that limits ρ due to thermal constraints, as a function of η and for a given Cooling System Performance Index (CSPI), are also plotted in Fig.6 (a) to explain the peculiar alignment of the points. The obtained efficiency, with respect to the output power, is indicated in Fig.6 (b) together with the California Energy Commission (CEC) efficiency $\eta_{CEC} = 97.4\,\%$.

The contribution of the different component categories to the total volume of $271\,\mathrm{cm^3}$ $(16.54\,\mathrm{in^3})$ and the losses in the different stages of the converter are shown in the pie charts of Fig.6 (c)-(d). Analyzing Fig.6 (c), it becomes evident the highly efficient operation of the DC-DC stage ($>99\,\%$), and especially of the input half-bridge. Despite the employed modern wide band-gap semiconductors, the principal source of losses, is the tap-selector. The anti-series connection of the power-switches increases the conduction losses; furthermore, the hard-switching commutation of the tap-selector switches significantly contributes to the total switching losses. Although in the analyzed design only four DC voltage levels are used, already 17 switches are required to implement the described topology. However, their contribution to the total volume is comparably low, as shown in Fig.6 (d). The achievable power density is strongly affected by the DC-link capacitor C_{dc} and by the heat-sink volume. Since only a small fraction of the energy on average stored in C_{dc} is needed to

compensate the power pulsating at the double of the mains frequency, the electrolytic capacitor is poorly utilized. Instead of employing a purely passive capacitors bank, an active auxiliary converter called Power Pulsation Buffer can be installed to increase the power density [11]. In order to further decrease the volume needed to extract the heat, advanced cooling methods, such as heat-spreaders and extractors, are beneficial. In the described design, a cooling system with a $CSPI = 25.6\,\mathrm{W/dm^3/K}$ is considered, limiting, in only $60\,\mathrm{cm^3}$ ($3.66\,\mathrm{in^3}$), the temperature raise to $30\,^{\circ}\mathrm{C}$ at full load.

The performance of the described design, in terms of efficiency and power density, is comparable with many solutions presented at the LBC finals, confirming the potential of this novel inverter topology. However, the bright claims of above $99\,\%$ efficiency and $17.4\,\mathrm{kW/dm^3}$ ($285\,\mathrm{W/in^3}$) could not be proved with the approach presented herein.

Finally, with the purpose of verifying analytical waveforms and results presented in Section II, accurate circuit simulations have been carried out. The obtained waveforms are presented in Fig.7, showing stable intermediate DC voltage levels $V_{\mathrm{Clevel,i}}$ during the whole mains period and no visible distortion in the output voltage waveform when the tap-selector changes state. Considering i_{Lfilter} in Fig.7 (a), it is evident how the current ripple is drastically reduced in contrast to an equivalent conventional PWM converter design where only V_{Cdc} is available as DC voltage level. Similarly, considering v_{ts}, it is clear that for every tap selector transition, only $V_{\mathrm{Cdc}}/3$ is switched across the anti-series connected devices. Moreover, Fig.7 (b) illustrates the soft-switching condition and the resonant behavior of the input half-bridge when $\mathrm{S_{ts,1}}$ and $\mathrm{S_{ts,2}}$ are operated alternately and the load current is split between the two voltage doubler circuits.

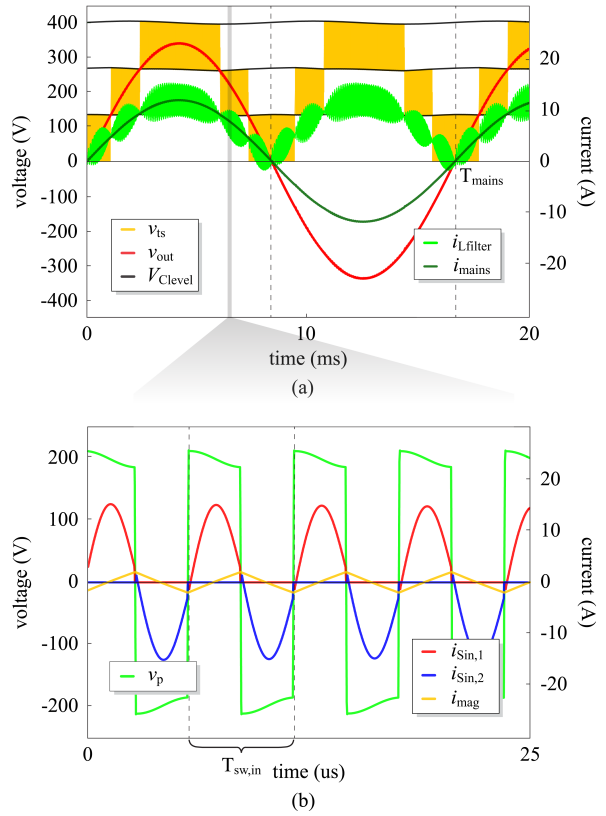

Fig. 7. Simulated current and voltage in a mains period at rated output power: (a) sinusoidal output voltage and current before and after the output filter (b) zoom of the sinusoidal currents in the input half-bridge switches highlighting the resonant operation and soft-switching conditions.

V. Conclusion

A novel, single-phase, PV inverter topology, based on a highly efficient resonant DC-DC converter stage, is presented in this paper. The advantages of generating intermediate voltage levels by means of a high-frequency multi-tapped auto-transformer are stated and confirmed with efficiency estimation and losses calculation, comparing the proposed solution with conventional PWM single-stage inverters and galvanic isolated topologies. The operating principle of the proposed inverter is outlined, providing close-form expressions for the analytical waveforms, validated with accurate simulations. The high-frequency resonant operation and the mains frequency current envelopes dependent on the tap-selector state are analyzed in detail to dimension the components in the DC-DC stage. Resonant operation and ZVS are maintained during the entire mains period and independently from the load, guaranteeing low switching losses in the DC-DC stage. The design of the auto-transformer is presented together with a procedure to calculate its leakage inductances, essential for the resonant operation. Hence, a circuit model for the auto-transformer, independent from the operating point, is derived and consequently, a procedure to dimension the resonant capacitors is obtained. A Pareto optimized design is finally presented and the resulting performance are discussed. High efficiency and high power density are reached, justifying the interest in a multi-tapped high-frequency auto-transformer based inverter system. However, even employing modern wide band-gap semiconductors and ensuring a very efficient operation, the bright claims of the LBC participant could not be confirmed in this work.

VI. Acknowledgment

The author thanks Infineon Technologies Austria AG for financially supporting this research.

References

[1] Google, "Detailed Inverter Specifications, Testing Procedure, and Technical Approach and Testing Application Requirements for the Little Box Challenge," Google Inc., Mountain View, California, USA, Tech. Rep., 2015.

[2] "Little Box Challenge," www.littleboxchallenge.com, accessed: 2016-03-01.

[3] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, "A New High-Efficiency Single-Phase Transformerless PV Inverter Topology," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[4] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$-Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the GOOGLE Little Box Challenge," in *Proc. IEEE Workshop on Control and Modeling for Power Electronics, COMPEL 2016*, Trondheim, Norway, June 2016.

[5] J. Wood and E. Shelton, "Interleaved, Folding, Interpolating dual-path Adiabatic Autotransformer based power converter," www.littleboxchallenge.com, accessed: 2016-03-01.

[6] D. A. Grant, Y. Darroman, and J. Suter, "Synthesis of Tapped-Inductor Switched-Mode Converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1964–1969, Sept. 2007.

[7] J.-H. Jung, H.-S. Kim, J.-H. Kim, M.-H. Ryu, and J.-W. Baek, "High Efficiency Bidirectional LLC Resonant Converter for 380V DC Power Distribution System Using Digital Control Scheme," in *Proc. IEEE Applied Power Electronic Conference and Exposition, APEC 2012*, Orlando, FL, USA, Feb. 2012, pp. 532–538.

[8] J. W. Kolar, M. Hartmann, and T. Friedli, "Three-Phase PFC Rectifier and AC-AC Converter Systems," in *Proc. IEEE Applied Power Electronic Conference and Exposition, APEC 2011*, Fort Worth, TX, USA, Mar. 2011, pp. 224–229.

[9] B. Hesterman, "Analysis and Modeling of Magnetic Coupling," Presentation at University Of Colorado, Apr. 2007.

[10] R. Burkart, H. Uemura, and J. W. Kolar, "Optimal Inductor Design for 3-phase Voltage-Source PWM Converters Considering Different Magnetic Materials and a Wide Switching Frequency Range," in *Proc. IEEE International Power Electronics Conference, IPEC 2014-ECCE Asia*, Hiroshima, Japan, May 2014, pp. 891–898.

[11] D. Neumayr, D. Bortis, and J. W. Kolar, "Ultra-Compact Power Pulsation Buffer for Single-Phase DC/AC Converter Systems," in *Proc. IEEE International Power Electronics and Motion Control Conference, IPEMC 2016-ECCE Asia*, Hefei, China, May 2016.