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Operating Behavior and Design of the Half-Cycle Discontinuous-Conduction-Mode Series-Resonant-Converter with Small DC Link Capacitors

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***Abstract*—The series-resonant-converter operated in half-cycle discontinuous-conduction-mode is a realization option for bidirectional isolated DC/DC converter modules, which are key components of modern solid state transformer (SST) concepts, among other applications. In SSTs the DC/DC converters are interfacing the input and output inverter stages via DC links. For reasons of costs as well as possible application-specific restrictions on weight and volume it is beneficial to use as small DC link capacitors as possible. However, when the resonant capacitance is higher than about 10% of the DC link capacitances, the deviation of the resonant current waveform from the sinusoidal shape becomes significant and the half-cycle duration is altered from values calculated using common approaches. Here, a comprehensive discussion of this case is given and design guidelines for the choice of the resonant capacitor are derived. The importance of the effect is illustrated by applying these to a complete design example.**

I. Introduction

In recent years, the concept of solid state transformers (SSTs), which has its origin back in the 1970ies [1] has regained much interest for high-power applications such as compact traction solutions [2]–[4], renewable energy generation [5], [6] and smart grid applications in general [7], [8]. As can be seen from the typical structure of an SST's single phase leg shown in Fig. 1, isolated DC/DC converters are a core component of such modular systems, providing potential separation and voltage scaling by means of medium-frequency (MF) transformers.

The series-resonant-converter operated in the half-cycle discontinuous-conduction-mode (HC-DCM-SRC) is an interesting option for realizing the isolated DC/DC converters since it provides isolation, fixed voltage transfer ratio and additionally enables zero-current-switching for all power semiconductors. The HC-DCM-SRC is thus a very promising variant of resonant converters, not only for high-power applications but also in other areas such as e. g. telecommunications power supplies [9]. The DCM mode of operation of SRCs has initially been described in the early 1970ies [10], where thyristor switches have been used. Further analysis and the derivation of a simple equivalent circuit representing the static and dynamic terminal behavior of the converter concept can be found in [11], [12].

If the DC link capacitors are sufficiently large, the input and output DC voltages of the converter can be considered constant and hence the transformer current is piecewise sinusoidal with the resonance frequency being fully determined by the transformer stray inductance, L_σ, and the resonant capacitor, C_r, connected in series (cf. topology shown in Fig. 2 and the ideal waveforms shown in Fig. 3).

In order to save costs, volume and weight it is in general desirable to design a DC/DC converter using as small DC link capacitors as possible considering DC voltage ripple specifications. Weight and volume restrictions are especially important for SST applications in future distributed railway traction drives or in aerospace applications as developed under the More Electric Aircraft paradigm and in emerging wind energy harnessing concepts like airborne wind turbines [13].

The well-known and direct relation $\omega_0 = 1/\sqrt{L_\sigma C_\mathrm{r}}$ between C_r, L_σ and the duration of a current half-cycle ($T_\mathrm{hc} = \pi/\omega_0$) is, however, not valid anymore if the ratio of the capacitances of the resonant capacitor and DC link capacitors increases, as will be discussed in this paper. First, the basic operating principle of the HC-DCM-SRC under ideal conditions is revised to give a starting point for a detailed analysis of the system behavior including the effects of the DC link capacitors, which is presented in Section III along with an experimental verification. From these considerations, design guidelines for the correct choice of the resonant capacitor are derived and applied to

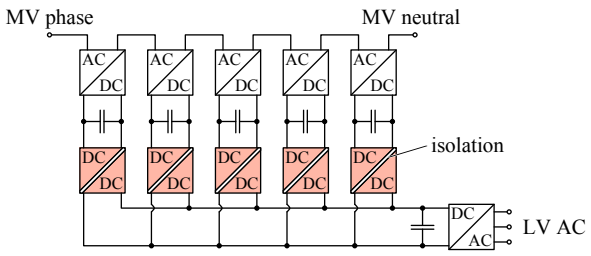

Fig. 1. Schematic overview of the tpyical structure of a single-phase traction SST or one phase leg of a three-phase SST system.

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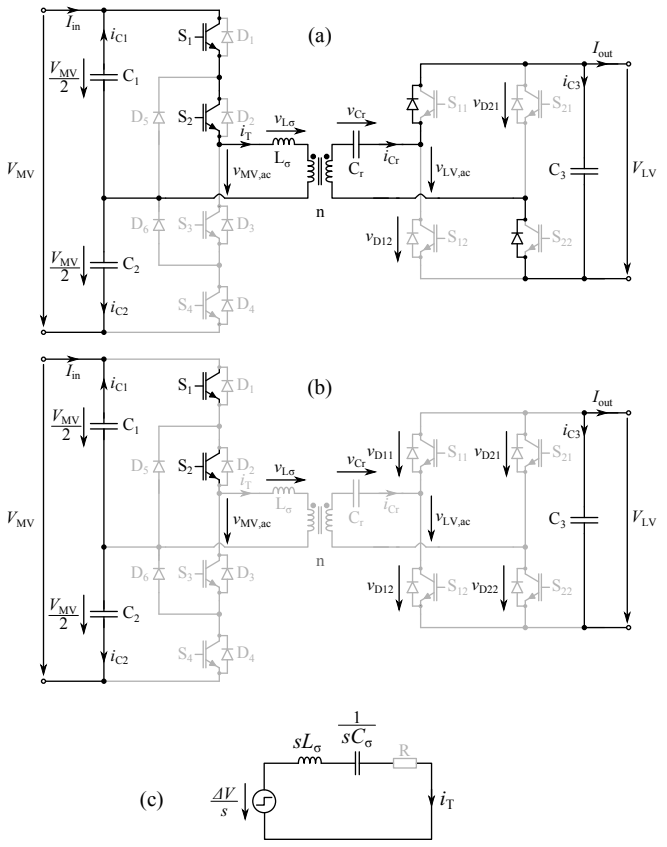

Fig. 2. Conduction states of the HC-DCM-SRC during the positive half cycle where (a) the resonant current, i_T, is flowing and (b) during the zero current interval; (c) simple equivalent circuit used to analyze the behavior under ideal conditions.

a design example in Section IV, which illustrates that for neglecting the described effects, the actual behavior of a system could deviate significantly from the results of a design.

II. Operating Principle

First, the basic operating principle of the HC-DCM-SRC is discussed, where infinite DC link capacitances, i. e. constant DC voltages, are assumed. The topology shown in Fig. 2(a, b) is considered, which features a neutral-point clamped (NPC) half bridge on the medium-voltage (MV) side in order to reduce the blocking voltage requirements for the MV side power semiconductors. For all considerations hereafter, power transfer from the MV to the low-voltage (LV) side is assumed, i. e. the LV bridge is operated completely passive as a diode rectifier while the MV bridge applies a 50 % duty cycle rectangular voltage. Considering power transfer in the other direction would yield equivalent results. In addition, all quantities marked with an apostrophe are referred to the MV side of the transformer.

A. Lossless Case

With the above assumptions, the analysis can be reduced to that of a simple series resonant circuit with a step voltage excitation as shown in Fig. 2(c). The series resistor, R, is grayed out since it will only be considered later. It is well known that in such a circuit a sinusoidal current, i_T, appears as a reaction to the said excitation,

$$i_\mathrm{T}(t) = \frac{\Delta V}{L_\sigma \omega_0} \sin(\omega_0 t), \tag{1}$$

where

$$\omega_0 = \frac{1}{\sqrt{C_\mathrm{r}' L_\sigma}}.$$

Fig. 3, interval A, shows the corresponding waveforms of i_T and v_Cr'. In contrast to what would happen in the simple equivalent model, i_T cannot reverse direction in the real circuit once it reaches zero, which means that it remains zero until the MV bridge applies negative output voltage; the transformer current is *discontinuous*, hence the name of the converter's operation mode. The duration, T_z, of the interval B, termed also as zero-current interval, can be used to optimize the converter efficiency as will be discussed later in section IV. The relationship between resonant frequency, f_0, and switching frequency, f_S, is then,

$$f_0 = \frac{f_\mathrm{S}}{1 - 2T_\mathrm{z} f_\mathrm{S}}. \tag{2}$$

The next step is to determine the excitation voltage, ΔV, which is done by analyzing the two main states, A and B, of the converter. During interval A the first half-period of the resonant oscillation between L_σ and C_r' takes place (cf. Fig. 2(b) and Fig. 3); the current flows through D_{11} and D_{22} on the LV side. Interval A ends when i_T reaches zero. Then, assuming identical diode properties, the voltages across the four rectifier diodes on the LV side are found by applying Kirchhoff's voltage law,

$$\begin{aligned} v_\mathrm{D11} = v_\mathrm{D22} &= \frac{1}{2} v_{\mathrm{Cr}'} \left(t = \frac{\pi}{\omega_0} \right) > 0, \\ v_\mathrm{D12} = v_\mathrm{D21} &= \frac{1}{2} \left(\frac{V_\mathrm{MV}}{2} + V_\mathrm{LV}' - v_{\mathrm{Cr}'} \left(t = \frac{\pi}{\omega_0} \right) \right) \\ &= \frac{V_\mathrm{MV}}{2} - \frac{1}{2} v_{\mathrm{Cr}'} \left(t = \frac{\pi}{\omega_0} \right) > 0. \end{aligned} \tag{3}$$

This clearly shows that all rectifier diodes are reverse biased and hence there is no possibility for the oscillation to continue by reversing the current direction; thus the resonant capacitor

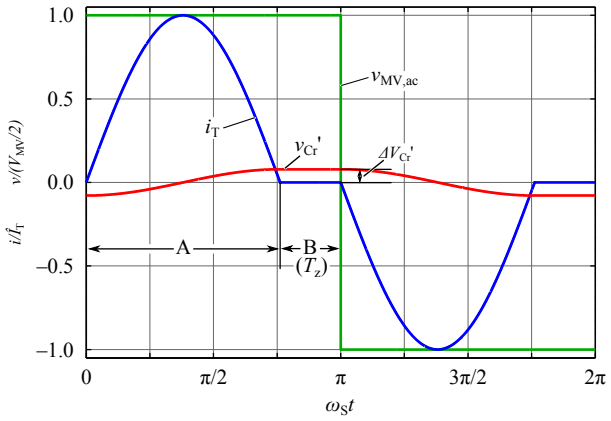

Fig. 3. Ideal waveforms of the HC-DCM-SRC.

voltage stays constant during T_z.

At the end of interval B the next switching half-cycle is initiated by changing the polarity of $v_{\mathrm{MV,ac}}$. Again by means of the KVL, it can be found that D_{12} and D_{21} become forward biased:

$$v_{\mathrm{D12}} = v_{21} = -\frac{1}{2} v'_{\mathrm{Cr}} \left(t = \frac{\pi}{\omega_0} \right) < 0 \tag{4}$$

Since ideal semiconductors are considered here, this equation is not valid as such—there must be another element that can take over the resonant capacitor's voltage: L_σ. Therefore, the step excitation voltage ΔV in the ideal case is given by the resonant capacitor's voltage at the beginning of the switching cycle,

$$\Delta V = v'_{\mathrm{Cr}} \left(t = \frac{\pi}{\omega_0} \right) =: V'_{\mathrm{Cr},0}. \tag{5}$$

The charge flowing into C'_r during one half cycle can be found from the power balance between DC and AC side,

$$\begin{aligned} P = V_{\mathrm{MV}} I_{\mathrm{in}} &= \frac{V_{\mathrm{MV}}}{2} \cdot \frac{2}{T_\mathrm{S}} \cdot \underbrace{\int_0^{T_\mathrm{S}} i_\mathrm{T}(t)\, dt}_{\Delta Q'_{\mathrm{Cr}}} \\ &= V_{\mathrm{MV}} f_\mathrm{S} \Delta Q'_{\mathrm{Cr}}. \end{aligned} \tag{6}$$

This leads directly to the initial condition

$$V'_{\mathrm{Cr},0} = \frac{P}{2 V_{\mathrm{MV}} f_\mathrm{S} C'_\mathrm{r}}, \tag{7}$$

which is independent of the shape of the current pulse. For the peak value of the resonant current, $\hat{I}_\mathrm{T}$, the following expression results:

$$\hat{I}_\mathrm{T} = \sqrt{\frac{C'_\mathrm{r}}{L_\sigma}} \Delta V = \sqrt{\frac{C'_\mathrm{r}}{L_\sigma}} \cdot \frac{P}{2 V_{\mathrm{MV}} f_\mathrm{S} C'_\mathrm{r}} = \frac{\pi P f_0}{V_{\mathrm{MV}} f_\mathrm{S}}. \tag{8}$$

B. Lossy Case

In a real converter, current-dependent losses are present. These result from the transformer winding resistances and the differential resistances of the power semiconductors and can be included into the simple model from Fig. 2(c) by means of a series resistance. Considering only the oscillatory case, i. e. the case where $R < \sqrt{4L_\sigma / C'_\mathrm{r}}$, the resonant current for the damped case can be found as

$$i_\mathrm{T}(s) = \frac{\Delta V}{L_\sigma \omega_\mathrm{d}} \sin(\omega_\mathrm{d} t) \mathrm{e}^{-\delta t} \tag{9}$$

where $\omega_\mathrm{d} = \sqrt{\omega_0^2 - \delta^2}$ and $\delta = \dfrac{R}{2L_\sigma}$.

Converter losses lead to an average voltage difference between the DC link voltages, i. e. $V_{\mathrm{MV}}/2 \neq V'_{\mathrm{LV}}$ in contrast to the loss-less case [11], [12]. This voltage difference also contributes to the initial condition ΔV. From the power balance, the converter efficiency, η, and the relation $I'_{\mathrm{out}} = 2 I_{\mathrm{in}}$, this voltage difference can be calculated as

$$\begin{aligned} P_{\mathrm{out}} = V'_{\mathrm{LV}} I'_{\mathrm{out}} = V'_{\mathrm{LV}} \cdot 2 I_{\mathrm{in}} &\overset{!}{=} \eta V_{\mathrm{MV}} I_{\mathrm{in}} = \eta P_{\mathrm{in}} \\ \Rightarrow \Delta V_{\mathrm{DC}} = \frac{V_{\mathrm{MV}}}{2} - V'_{\mathrm{LV}} &= \frac{V_{\mathrm{MV}}}{2} (1 - \eta). \end{aligned} \tag{10}$$

Therefore, the initial condition ΔV in the lossy case is given by

$$\begin{aligned} \Delta V &= \Delta V_{\mathrm{DC}} + V'_{\mathrm{Cr},0} \\ &= \frac{V_{\mathrm{MV}}}{2} (1 - \eta) + \frac{P}{2 V_{\mathrm{MV}} f_\mathrm{S} C'_\mathrm{r}}. \end{aligned} \tag{11}$$

In general it is desired to achieve high converter efficiencies, e. g. $\eta > 98\,\%$. Fig. 4 illustrates that for such cases the deviation from the ideal current waveform caused by the resistor is small. However, in addition to the converter efficiency also the choice of L_σ influences the damping, which is distorting the waveform. If the damping factor, $\zeta = \sqrt{C_\mathrm{r}/L_\sigma} \cdot R/2$, is low, e. g. $\zeta < 0.2$, the influence of the damping can be neglected during a design procedure since its effect on rms currents and T_z is only minor.

As a side note it is interesting to observe that (9) and (11) imply an important feature of the HC-DCM-SRC: it behaves like a "DC transformer". Any load change on the LV side terminals will, independent from the voltage difference resulting from converter losses, lead to a reduction of V'_{LV}, which corresponds to an increase of ΔV_{DC} and thus of the next current pulse's peak value. The power transfer from the MV side is automatically increased such that the DC voltage ratio is kept (almost) load-independent. When a combination of an NPC half-bridge on the MV side and a full bridge on the LV side is used, this implies also that the capacitor voltages of the MV side's split DC link stay balanced inherently.

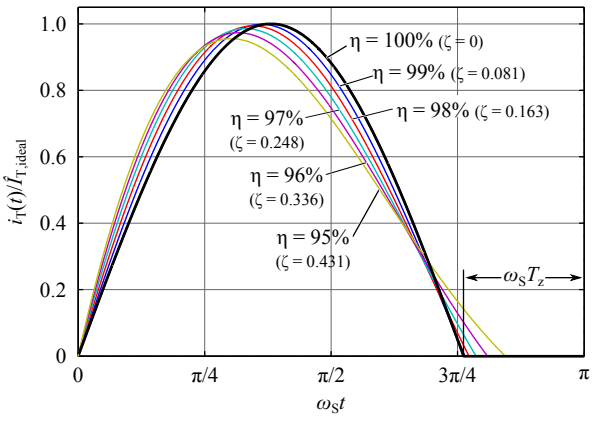

Fig. 4. Influence of the converter efficiency on the resonant current waveform. The damping factor, ζ, is defined as $\zeta = \sqrt{C_\mathrm{r}/L_\sigma} \cdot R/2$.

III. Operating Behavior with Small DC Capacitors

So far it has been assumed that the DC link capacitors are large enough to treat the DC voltages as constant, which implies also $C_1, C_2, C'_3 \gg C'_\mathrm{r}$; the behavior of the circuit resonance was thus fully determined by C'_r and L_σ. However, if the ratio between the resonant capacitor and the DC link capacitors becomes larger, the above assumptions are violated and thus a more detailed approach of analyzing the system has to be used. The loss-less case is considered again for reasons of clarity.

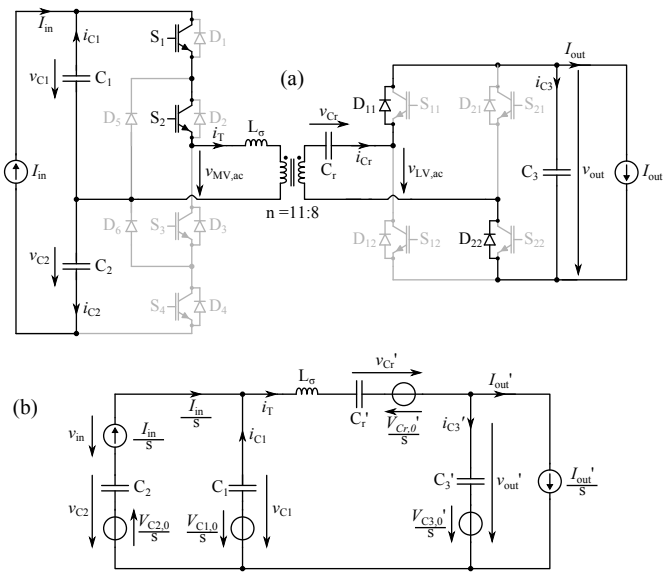

Fig. 5. (a) Circuit considered for the case with small DC link capacitors and (b) the Laplace equivalent circuit valid for the positive half-cycle.

A. Series Connection of Capacitors

Apparently, C_1 and C_3' take part in the resonance; the effective capacitance consists thus of the series connection of C_1, C_3' and C_r':

$$C_\mathrm{eq} := \left(\frac{1}{C_1} + \frac{1}{C_3'} + \frac{1}{C_\mathrm{r}'}\right)^{-1} < C_\mathrm{r}' \tag{12}$$

The resonance frequency, ω_0^*, is thus shifted to higher values when compared with the ideal case:

$$\omega_0^* = \sqrt{\frac{C_1C_3' + C_1C_\mathrm{r}' + C_3'C_\mathrm{r}'}{C_1C_\mathrm{r}'C_3'L_\sigma}} > \omega_0 \tag{13}$$

It can clearly be seen that for $C_1, C_3' \to \infty$ the expression reduces to ω_0 given in (1) because $C_\mathrm{eq} \to C_\mathrm{r}'$.

However, this is only part of the picture, as will become obvious considering the design example in Section IV: small DC link capacitors imply non-constant DC voltages, i. e containing a superimposed ripple at the switching frequency or its second harmonic. The voltage step applied to the resonant circuit, ΔV, depends on the momentary values of these DC voltages, and so does the current waveform itself. It is therefore necessary to analyze the system as a whole.

B. Complete System Modeling

Fig. 5(a) shows the circuit topology considered for the following derivations; the active parts and the current paths during the positive switching cycle, to which the considerations can be confined without loss of generality, are highlighted. To correspond to a realistic case, where sources and loads, which may be realized by other converter stages, are usually connected via inductors, input and output to the HC-DCM-SRC are modeled as DC current sources.

Transforming the highlighted part of the circuit to the Laplace domain and referring all quantities to the MV side leads to the equivalent circuit shown in Fig. 5(b). Applying standard circuit analysis techniques, the expression for the transformer current in the time domain becomes

$$i_\mathrm{T}(t) = \frac{\Delta V^*}{\omega_0^* L_\sigma}\sin(\omega_0^* t) + I_\mathrm{out}' \cdot F \cdot (1 - \cos(\omega_0^* t)),$$

where

$$F = \frac{1}{(\omega_0^*)^2 L_\sigma}\left(\frac{1}{C_3'} + \frac{1}{2C_1}\right), \tag{14}$$

$$I_\mathrm{out}' = \frac{2P}{V_\mathrm{MV}} \text{ and}$$

$$\Delta V^* = V_\mathrm{C1,0} + V_\mathrm{Cr,0}' - V_\mathrm{C3,0}'.$$

Note that ω_0^* has already been defined in (13) and I_out' follows from the power balance in the loss-less case. The transformer current, $i_\mathrm{T}(t)$, is thus a superposition of a sine and a $(1-\cos)$ function, as is illustrated by Fig. 6. If the DC link capacitors are much larger than the resonant capacitor, the $(1-\cos)$ part vanishes since $\lim_{C_1\to\infty, C_3'\to\infty} F = 0$. From the figure it can clearly be seen how the current shape is altered and the half cycle duration prolonged with respect to π/ω_0^* by the presence of a $(1-\cos)$ part. It is important to highlight that the current zero-crossing is no longer defined by a resonance frequency; instead the term *half-cycle duration*, T_hc, is used to describe the length of the current pulse.

The duration of a half cycle, T_hc, can formally be found by equating (14) to zero,

$$T_\mathrm{hc} = \frac{2\pi - 2\arctan\left(\omega_0^*\left(\frac{1}{C_3'} + \frac{1}{2C_1}\right)^{-1}\frac{V_\mathrm{MV}}{2P}\Delta V^*(T_\mathrm{hc})\right)}{\omega_0^*}. \tag{15}$$

Again, for $C_1, C_3' \to \infty$, the expression in the arctan goes towards infinity, resulting in $T_\mathrm{hc} = \pi/\omega_0$ as expected, since then also $\omega_0^* \to \omega_0$.

The reader may have noticed that ΔV^* in (15) is written as a function of T_hc. As indicated above, ΔV^* depends on the DC capacitor voltage ripples and they in turn depend on the current shape and T_hc. Therefore, the initial conditions of these capacitors are derived in the following.

It has already been discussed earlier that the initial voltage of the resonant capacitor, $V_\mathrm{Cr,0}'$, does not depend on the shape of

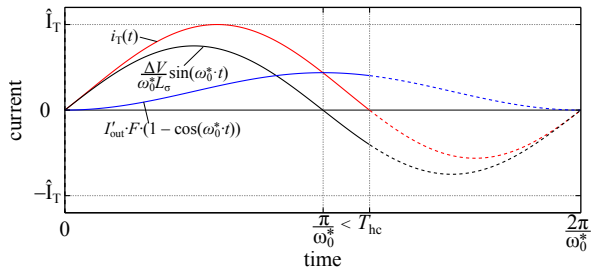

Fig. 6. Composition of the transformer current waveform of a sine and a $(1-\cos)$ part (qualitatively).

the current waveform. Hence, (7) remains valid in its structure, but f_s has to be expressed as $f_\mathrm{s} = 1/(2(T_\mathrm{hc} + T_\mathrm{z}))$, making $V'_{\mathrm{Cr},0}$ also a function of T_hc.

Fig. 7 qualitatively shows the currents of C_1 and C_3 and the resulting voltage ripples. The right half of the figure corresponds to the negative switching cycle, since the voltages at its end are the initial conditions for the positive half-cycle under consideration. Since the voltage ripples are symmetric with respect to the average DC voltages, the following relations for the initial capacitor voltages can be obtained,

$$\begin{aligned} V_{\mathrm{C}10} &= \frac{V_\mathrm{MV}}{2} + \frac{I_\mathrm{in}}{2C_1}(T_\mathrm{hc} + 2T_\mathrm{z}), \\ V'_{\mathrm{C}30} &= \frac{V_\mathrm{MV}}{2} - \frac{I'_\mathrm{out}}{2C'_3}T_\mathrm{z}. \end{aligned} \tag{16}$$

Substituting these initial conditions into ΔV^* yields an implicit equation for the half cycle duration, T_hc, which depends on component values and the zero current interval duration, T_z. It is not possible to solve this equation analytically; but standard numerical approaches are applicable to obtain T_hc.

C. Design Equation for C'_r

Now that the relationship between the half cycle duration and the component values has been established, it is possible to determine the required C'_r for a given specification of f_s and T_z, which might be the output of a loss-optimizing procedure (cf. Section IV). Using the relationship $T_\mathrm{hc} + T_\mathrm{Z} = T_\mathrm{S}/2$, the initial conditions can be reformulated,

$$\begin{aligned} V'_{\mathrm{Cr},0} &= \frac{P}{2f_\mathrm{S}C'_\mathrm{r}V_\mathrm{MV}}, \\ V_{\mathrm{C1},0} &= \frac{V_\mathrm{MV}}{2} + \frac{P}{2V_\mathrm{MV}C_1}\left(\frac{1}{2f_\mathrm{S}} + T_\mathrm{z}\right), \\ V'_{\mathrm{C3},0} &= \frac{V_\mathrm{MV}}{2} - \frac{P}{V_\mathrm{MV}C'_3}T_\mathrm{z}. \end{aligned} \tag{17}$$

Doing the same with (15), the defining relationship for C'_r is found,

$$\left(\frac{T_\mathrm{S}}{2} - T_\mathrm{z}\right) - \frac{2\pi - \arctan\left(\omega_0^*\left(\frac{1}{C'_3} + \frac{1}{2C_1}\right)^{-1}\frac{V_\mathrm{MV}}{2P}\Delta V^*\right)}{\omega_0^*} = 0. \tag{18}$$

Again, this equation can be solved numerically for those cases where a solution exists. The next subsection discusses this question among others and provides experimental verification for the above derivations.

D. Discussion

Fig. 8 shows the dependence of the the half-cycle duration, T_hc, on the ratio between C'_r and $C_\mathrm{DC,total}$, the latter being defined as $C_\mathrm{DC,total} = (1/C_1 + 1/C'_3)^{-1}$, and on the zero current interval duration, T_z. It can clearly be seen that the actual T_hc deviates significantly from both, values calculated assuming large DC links and values calculated using the equivalent capacitance, C_eq, as defined in (12), when $C'_\mathrm{r}/C_\mathrm{DC,total}$ becomes larger than about 0.2. Using the definition of $C_\mathrm{DC,total}$ and assuming similar DC link capacitors on the MV an LV side, i. e. $C_1 = C'_3$, it can be said that the effect becomes important when C'_r is larger than about 10 % of the individual DC link capacitances.

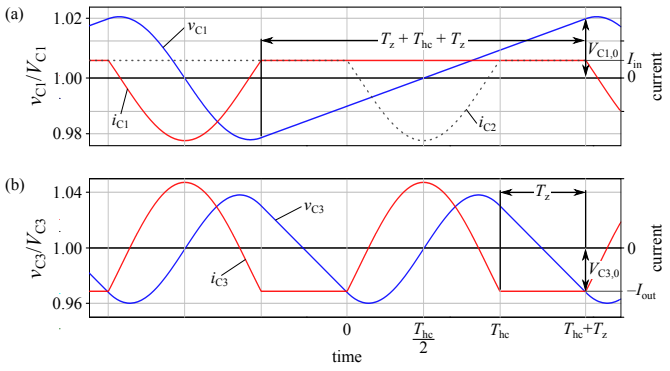

Fig. 7. Voltage and current waveforms (qualitative) of (a) C_1 and (b) C'_3.

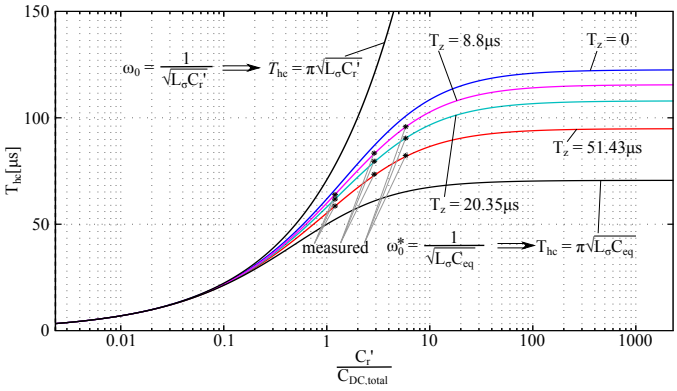

Fig. 8. Half-cycle duration, T_hc as a function of the ratio $C'_\mathrm{r}/C_\mathrm{DC,total}$ for different zero current interval durations, T_z

Ignoring the DC link capacitors results in an overestimation of the actual T_hc since $T_\mathrm{hc} < \pi/\omega_0$, or in an underestimation of the required C'_r for a specified T_hc. Including the DC link capacitors by means of C_eq only results in an underestimation of the actual T_hc since $T_\mathrm{hc} > \pi/\omega_0^*$, or in an overestimation of the required C'_r for a specified T_hc. The consequences that either error may introduce are illustrated by the design example presented in Section IV.

As another important result conveyed in Fig. 8 it should be noted that the influence of C'_r on T_hc is marginalized for large ratios $C'_\mathrm{r}/C_\mathrm{DC,total}$ and that the achievable T_hc is bounded for given DC link capacitors and given inductance L_σ. This is the reason that (15) and (18) may have no solution for certain combinations of the circuit parameters.

Ignoring the fact that L_σ often results from external considerations such as requirements on the dynamic response of the converter system or from mechanical constraints imposed on transformer construction, some general considerations can be made on the combination of L_σ and C'_r to achieve a desired T_hc. Using the design equation for C'_r given above in (18), C'_r

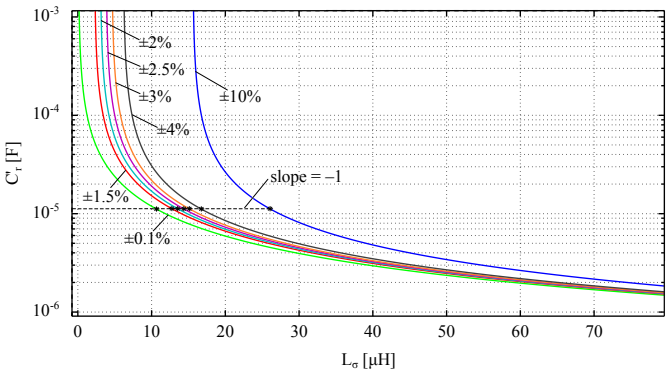

Fig. 9. Dependence of C'_r on L_σ for different allowed relative DC link voltage ripples, $\Delta V_\mathrm{DC,rel}$. The numerical values are based on the design example presented in Section IV. Note that the indicated slope is with respect to a plot using a non-logarithmic scale for C'_r.

can be calculated for any combination of C_1, C'_3 and L_σ for given f_s and T_z. Fig. 9 shows the resulting dependence of C'_r on the choice of L_σ for different allowed relative DC voltage ripples, $\Delta V_\mathrm{DC,rel}$.

If L_σ is chosen very small, the required resonant capacitor C'_r becomes very large. The smaller the DC link capacitors are (the higher the allowed $\Delta V_\mathrm{DC,rel}$), the larger L_σ has to be in order to be able to achieve the specified T_hc at all. It is interesting to note that this directly leads to the conclusion that improving converter dynamics requires to increase the DC link capacitors: fast dynamics imply a small L_σ [11], [12] and this again means large DC link capacitors for a given T_hc to be realizable. These considerations illustrate how the ratio $C'_\mathrm{r}/C_\mathrm{DC,total}$ and thus T_hc (cf. Fig. 8) is influenced by the choice of L_σ.

As discussed above, a small L_σ leads to very large resonant capacitors while choosing a very large L_σ is not desirable since converter dynamics are compromised and there is no significant reduction of C'_r (and hence of $C'_\mathrm{r}/C_\mathrm{DC,total}$) anymore. A good compromise between these two extreme cases could be to use the combination of C'_r and L_σ corresponding to a slope of -1. Then, the sensitivity of C'_r on variations of L_σ and vice-versa is similar. In a more general sense, the choice of the ratio C'_r/L_σ is a degree of freedom that can be included into a comprehensive efficiency and volume optimization of the HC-DCM-SRC.

E. Experimental Verification

Using a test setup corresponding to the circuit diagram shown in Fig 10, the above derivations have been experimentally confirmed. Table I gives an overview on the system specifications. Since the model to be verified assumes a loss-less system, the employed transformer and power semiconductors have been oversized such as to exclude deviations on T_hc that might have resulted from damping.

First, the ratio $C'_\mathrm{r}/C_\mathrm{DC,total}$ was adjusted by means of changing C_r within the range given in Table I. In addition, the switching frequency has been varied such that the desired T_z values were achieved. The measured values of the half

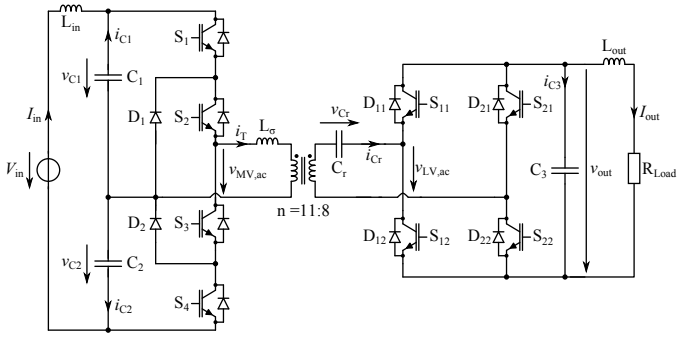

Fig. 10. Circuit diagram of the converter used for experimental verification.

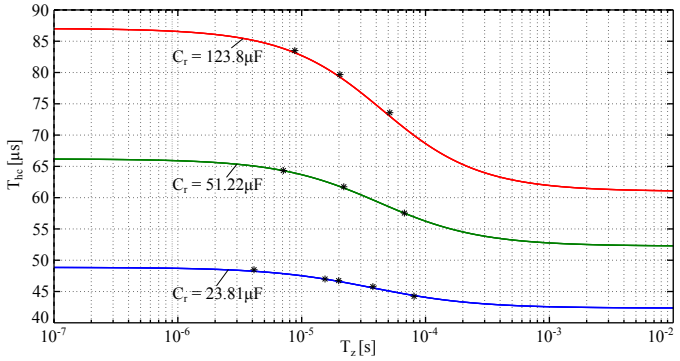

Fig. 11. Half cycle duration, T_hc, as a function of T_z for different resonant capacitor values.

cycle duration, T_hc, are plotted together with the calculated curves in Fig. 8. A very good agreement between calculation and measurement is evident. In addition, Fig. 11 shows the dependence of T_hc on T_z for three different C_r values, i. e. for different ratios $C'_\mathrm{r}/C_\mathrm{DC,total}$. Again, the measurements agree very well with the calculated curves.

It can thus be concluded that the presented system description and the derived expressions that allow calculation of T_hc or C'_r are correct.

IV. Design Example

In order to illustrate the consequences that could arise if the effect of small DC link capacitors is not considered

TABLE I
PARAMETERS OF THE CONVERTER USED FOR EXPERIMENTAL VERIFICATION.

Parameter	Value
V_MV	200 V
$n = N_1/N_2$	11/8
R_load	10 Ω
C_1, C_2	80 µF
C_3	60 µF
L_σ	22.5 µH
C_r	23.8 µF… 250.6 µF

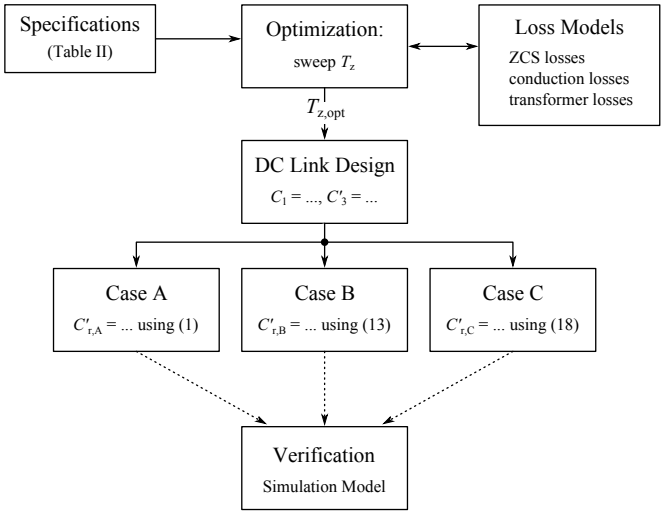

Fig. 12. Main steps of the design process described in the text.

properly, a design example for a HC-DCM-SRC with the specifications given in Table II is provided in the following. The topology from Fig. 10 and power flow from MV to LV side are considered. FF150R17KE4 IGBT modules are employed on the MV side and FF200R12KE4 modules on the LV side. From the transformer efficiency specified for purely sinusoidal current at f_s and the assumption $P_\mathrm{core} = P_\mathrm{cu}$, which corresponds to the well known optimum loss distribution and is also used by current MF transformer designs [14], the winding resistance $R_\mathrm{cu} = (1-\eta_\mathrm{transformer})V_\mathrm{MV}^2/(P\pi^2)$ is obtained, allowing for estimation of current-dependent losses.

Fig. 12 provides an overview on the main steps of the design process that will be discussed in the following paragraphs.

A. *Optimizing T_hc for Minimum Losses*

As can clearly be seen from the waveforms provided in Fig. 3, the HC-DCM-SRC provides zero-current switching (ZCS) for all switches. At higher power levels such as discussed here, IGBTs are usually employed. It has been discussed in [15]–[17] that the stored charge in IGBTs shows a delayed response with respect to the current flowing through the device. Thus, even tough ZCS is achieved there is still charge remaining in the devices, which has to be removed during commutation, causing switching losses. The behavior of the stored charge

TABLE II
DESIGN EXAMPLE SPECIFICATIONS.

Parameter	Value	Parameter	Value
P	80 kW	Transformer	
V_MV	2.2 kV	$n = N_1/N_2$	11/8
V_LV	800 V	$\eta_\mathrm{transformer}$	99.5 %
f_S	10 kHz	L_σ	9 µH
$\Delta V_\mathrm{DC,rel}$	3 %		

can be described by a simple analytic model [16] given as

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} + k_\mathrm{S}\cdot I_\mathrm{S}(t). \tag{19}$$

The validity of this model to estimate ZCS switching losses during the design phase of HC-DCM-SRCs has been shown in [17] and experimentally determined values for the parameters, i. e. $k_\mathrm{S} = 0.155$ and $\tau = 6.04\,\mu\mathrm{s}$ (at 125 °C junction temperature) for the FF150R17KE4 IGBT power module have been provided.

Since the charge carriers in the IGBTs recombine during the zero-current interval and therefore the amount of stored charge decays exponentially with time, an increase of T_z can be used to reduce switching losses [4], [17], [18]. However, since for a given f_s this means a reduction of T_hc, the peak and hence the rms value of the resonant current is increased, leading to higher conduction and transformer losses. Therefore, an optimum T_z resulting in minimum overall losses exists. In contrast to [17], where a comprehensive efficiency versus power density Pareto optimization has been carried out, here only T_z is varied to find the optimum value resulting in minimum losses for given f_s and transformer specifications.

To do so, the current waveform is approximated as being piecewise sinusoidal with a peak value given by (8) where f_0 for a given T_z and f_S is obtained using (2). In a second step, the stored charge model from (19) is used to determine the switching losses. This is done by calculating a magnetizing current that would be required to remove the remaining charge during the interlock time such as to enable ZVS for the turning-on switch. It has been shown in [3], [15], [17] that this results in minimum overall switching losses. Of course, the magnetizing current changes the shape of the current waveform and thus also the stored charge, making it necessary to find the optimum magnetizing current iteratively. The resulting current waveform is then considered during the calculation of transformer copper losses and semiconductor conduction losses. These are modeled following the procedure given in [19] and using datasheet forward characteristics.

A number of loss values is obtained by sweeping T_z over a certain range. The results shown in Fig. 13 clearly illustrate how

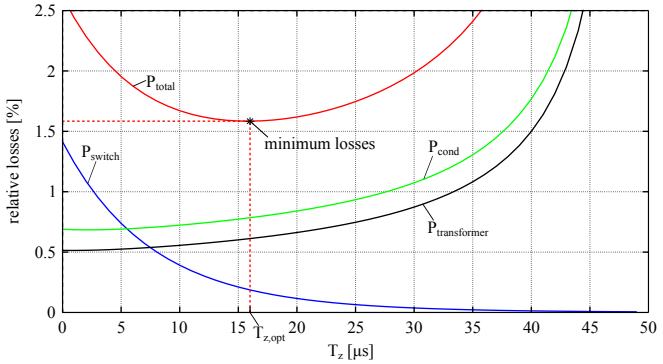

Fig. 13. Half cycle duration, T_hc, as a function of T_z for different resonant capacitor values.

the ZCS switching losses are reduced exponentially for higher values of T_z and how the rms-related losses are increased at the same time, resulting in an optimum at $T_{z,opt} = 16\,\mu s$. Together with the specified $f_S = 10\,kHz$ a required $T_{hc} = 34\,\mu s$ results; the expected efficiency with this T_z becomes 98.4 %.

B. DC Link Capacitances

Still assuming piecewise sinusoidal transformer current, it is meaningful to use f_0 and (2) to calculate the required capacitances on the MV side, C_1, and on the LV DC side, C_3, as a function of the maximum allowed relative voltage ripple, $\Delta V_{DC,rel}$, by means of integrating the capacitor currents (cf. Fig. 7) and solving for the capacitances. This yields

$$C_1 = \frac{P\left(2\sqrt{\pi^2 f_0^2 - f_s^2} + 2f_s \arcsin\left(\frac{f_s}{\pi f_0}\right) - \pi f_s\right)}{2V_{MV}^2 \Delta V_{DC,rel} \pi f_0 f_s} \quad (20)$$
$$= 37.7\,\mu F, \text{ and}$$

$$C_3 = \frac{P\left(\sqrt{\pi^2 f_0^2 - 4f_s^2} + 2f_s \arcsin\left(\frac{2f_s}{\pi f0}\right) - \pi f_s\right)}{4V_{LV}^2 \Delta V_{DC,rel} \pi f_0 f_s} \quad (21)$$
$$= 43.4\,\mu F,$$

where the given specifications and the $T_{z,opt}$ determined above have been used to obtain the numerical values.

C. Calculation of C_r' for given L_σ

There are three different equations to calculate the last free parameter, C_r', for given T_{hc}, L_σ and other parameters. A: using the assumption of large DC link capacitors and (1); B: using the equivalent capacitance and (13); C: using the correct model and the design equation (18) for C_r'. Table III gives numerical values for the three variants. It can be expected that the actual behavior of the converter system will vary strongly for each of the three cases. To analyze this quantitatively, simulations for all three cases have been carried out, the results of which will be discussed in the next subsection.

D. Simulation Results

Using the values for $C_{r,\{A,B,C\}}'$ given in Table III in a simulation model implemented in GeckoCIRCUITS [20], the resonant current waveforms shown in Fig. 14 are obtained. In addition, the T_{hc} values and the losses resulting from the simulation are also given in Table III.

These results clearly illustrate that large deviations from the desired T_{hc} value can result from not considering (cf. case A)

TABLE III
RESULTS FOR THE DIFFERENT APPROACHES TO CALCULATE C_r'.

Parameter	Case A	Case B	Case C
C_r'	13.0 µF	152.0 µF	26.5 µF
T_{hc}	27.1 µs	no	34.2 µs
$\Delta T_{hc,rel}$	−20.3 %	DCM	+0.6 %
η	98.27 %	97.66 %	98.4 %

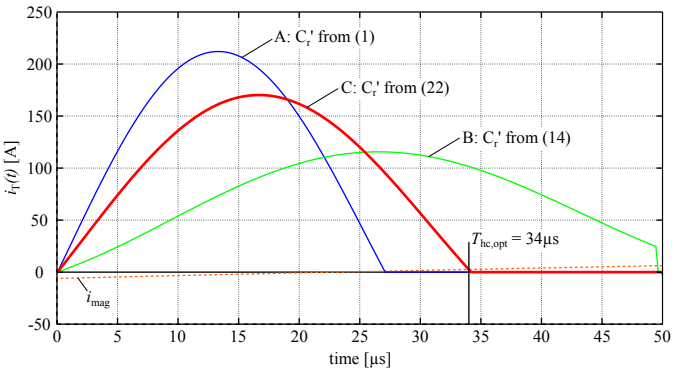

Fig. 14. Simulated resonant current waveforms for the different C_r' values given in Table III. Note that the magnetizing current shown in the figure has been substracted from the actual current waveforms for better visibility.

or not correctly considering (cf. case B) the small DC link capacitors in the calculations. Case B is worst, since then the resulting waveform is so slow that the current does not reach zero before the switching half-cycle is completed, i. e. DCM operation is lost, which results in significantly higher switching losses and correspondingly lower efficiency. Case A results in a current pulse which is shorter than expected, implying a shift towards higher T_z on the curve of overall losses in Fig. 13. Since the optimum is rather flat, the efficiency degradation in this case is not as bad as in case B.

However, the simulation results clearly illustrate the importance of correctly considering the effect of small DC link capacitors during converter optimization in order to ensure that the real converter is actually operated with the identified optimum T_z.

V. CONCLUSION

The half-cycle discontinuous-conduction-mode series-resonant-converter is a very interesting variant of isolated DC/DC converters, because it provides isolation, a simple control scheme and high efficiency due to ZCS for all switches. In this paper it has been shown that if the resonant capacitor is larger than about 10 % of the DC link capacitors, the deviation of the transformer current waveform from the sinusoidal shape becomes significant by altering the current pulse's half-cycle duration from values calculated with the commonly used approaches. If this effect is not considered appropriately, designs that are not operated in the expected optimum can result. Therefore, design guidelines to calculate resonant capacitor values to obtain the desired half-cycle duration also in the case of small DC link capacitors have been provided and applied to a design example, illustrating the importance of correctly considering the DC link capacitors during converter optimization.

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