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S. Coday,
D. Menzi,
J. Huber,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

A Novel Non-Mirrored Buck-Boost Flying Capacitor Multilevel DC-DC Converter Topology

Samantha Coday[1,2], David Menzi[1], Jonas Huber[1], Johann W. Kolar[1]
1. Power Electronic Systems Laboratory, ETH Zurich, Switzerland
2. Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, U.S.A
Email: scoday@berkeley.edu

***Abstract*– Enabling future electrification of air and ground transportation requires flexible, compact, and highly efficient power converters. Four-switch non-inverting bidirectional buck-boost dc-dc converters allow for wide and overlapping input and output voltage ranges, enabling integration of fuel cells and batteries whose voltages vary with state of charge and operating conditions. In this work, we propose a novel non-mirrored buck-boost (N-MBB) Flying Capacitor Multilevel (FCML) dc-dc converter. The proposed topology integrates the conventionally separated buck and boost bridge-legs, which is enabled by novel monolithic bidirectional GaN transistors featuring bipolar voltage blocking capability. Compared to the conventional mirrored buck-boost FCML converter, the proposed topology shows a higher inductor volume but advantageously a lower component count, better utilization of the installed chip area and flying capacitors, and lower conduction losses. Finally we introduce a topology variant with reduced inductor volume, the return-path-inductor (RPI) N-MBB FCML, and a direct non-isolated single-phase dc-ac N-MBB FCML inverter.**

I. Introduction

Future electric transportation requires flexible, dense and efficient power converters. Innovation within electric vehicle architectures for airborne [1] and ground applications [2] relies on dc-dc converters capable of both buck and boost mode operation to enable flexible integration of batteries and fuel cells with their wide and operating-point-dependent voltage ranges in the vehicles' on-board distribution busses [3], [4]. Recent work [5] has shown that multilevel topologies such as the Flying Capacitor Multilevel (FCML) converter [6], which utilizes energy-dense capacitors as the primary energy storage elements, facilitate very high power densities and high conversion efficiencies. Specifically, the four-switch non-inverting buck-boost converter with a buck and a boost FCML bridge-leg combined by a shared inductor is a symmetric structure and therefore in this work will be referred to as the mirrored buck-boost (MBB) FCML converter.

However, whereas the MBB FCML converter advantageously only operates either the buck or the boost bridge-leg with PWM while the other is clamped to the respective positive dc terminal, the transistors of the clamped bridge-leg are still in the current path and contribute to conduction losses. Therefore, this work proposes a new

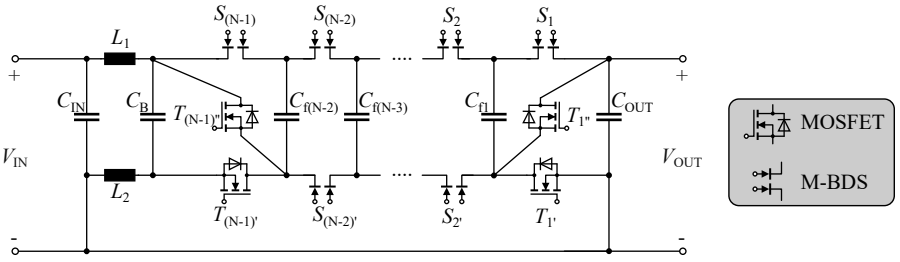

Fig. 1: Proposed non-mirrored buck-boost (N-MBB) N-level FCML topology employing dual-gate monolithic bidirectional bipolar blocking (GaN) switches (M-BDSs).

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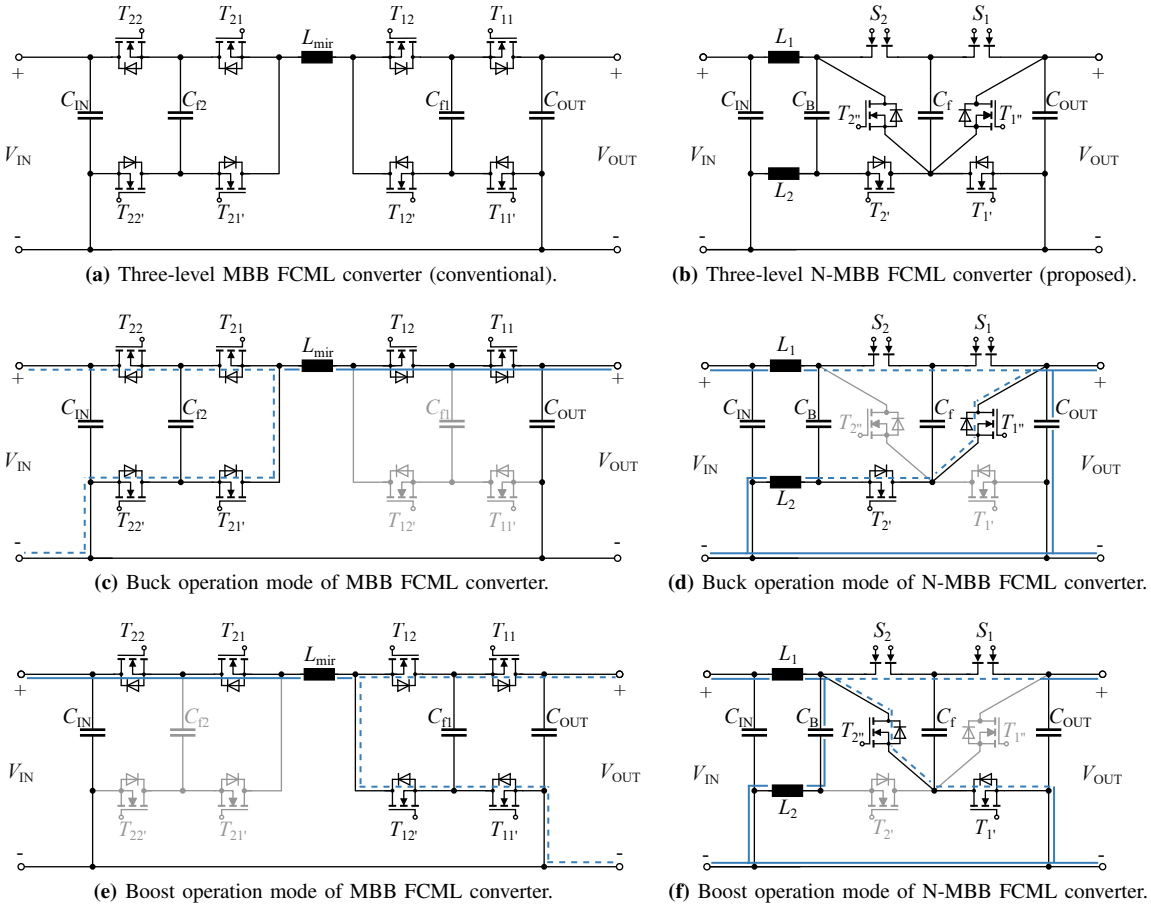


(a) Three-level MBB FCML converter (conventional).

(b) Three-level N-MBB FCML converter (proposed).

(c) Buck operation mode of MBB FCML converter.

(d) Buck operation mode of N-MBB FCML converter.

(e) Boost operation mode of MBB FCML converter.

(f) Boost operation mode of N-MBB FCML converter.

Fig. 2: Schematic of the conventional MBB FCML and the proposed N-MBB FCML converter topologies. Buck and boost operating modes are shown for the conventional and proposed converter topologies, whereby solid lines indicate continuous current flow and dashed lines indicate switched currents.

topology which merges the MBB FCML converter's two bridge-legs into a *non-mirrored* buck-boost (N-MBB) FCML topology shown in Fig. 1. As a consequence of the buck-boost functionality (i.e., operation with $V_{\mathrm{in}} > V_{\mathrm{out}}$ or $V_{\mathrm{in}} < V_{\mathrm{out}}$ is possible), the topology's main transistors ($\mathrm{S_x}$) must be able to block either voltage polarity. Novel monolithic bidirectional (GaN) switches (M-BDSs) [7]–[9] provide this functionality with only a minor increase of the chip area as compared to a unidirectional transistor, which is a key enabler for the proposed topology's advantages outlined in the following sections (i.e., lower switch count, lower switch conduction losses, a more favorable scaling with increased level-count, etc.).

II. Converter Operation

A. Topology Derivation

To best understand the proposed N-MBB FCML converter topology, it is helpful to first consider the conventional MBB FCML converter, the three-level version of which is shown in Fig. 2a. As shown in Fig. 2ce, the converter achieves buck and boost operating modes with a single inductor L_{mir} and by only high-frequency switching the input- *or* output-stage semiconductors, respectively, while the other stage clamps the inductor terminal to the positive dc-link rail. Therefore, during either operating mode the converter only operates half of the switches, and clamps one-fourth (two switches in the three-level case) in the on-state and one-fourth in the off-state. For example, as shown in Fig. 2b, during buck operation T_{12} and T_{11} are continuously conducting, while $T_{12'}$ and $T_{11'}$ are off. As a result, the converter suffers from undesired conduction losses from the clamped-on high-side switches, and essentially from a low utilization of the installed total chip area. Similarly, in each operating mode only half the flying capacitors are being used to transfer energy.

The goal of the topology presented in this work is to merge the two bridge-legs of the mirrored topology such that the number of switches in the current path is minimized and the utilization of the installed chip area and of the flying capacitors is improved. The proposed N-level N-MBB FCML converter topology is shown in Fig. 1, and the three-level version in Fig. 2b. This topology employs a split input inductor (see also [10]) to supply continuous current from the input for both buck

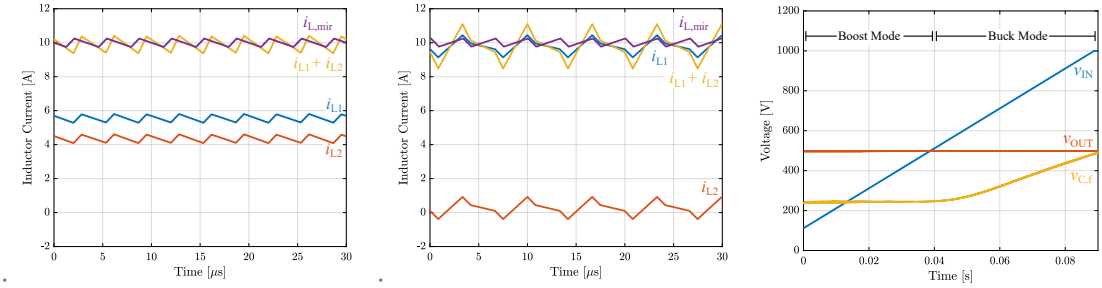


Fig. 3: Simulated waveforms for mirrored and non-mirrored three-level (see **Fig. 2**) topologies with equal inductance values (i.e., $L_1 = L_2 = L_{\text{mir}}$). The switching frequency, 150 kHz, and the output power, 5 kW, are equal in the simulations shown in **(a)** for buck mode [$V_{\text{IN}} = 800\,\text{V}$, $V_{\text{OUT}} = 500\,\text{V}$] and **(b)** for boost mode [$V_{\text{IN}} = 500\,\text{V}$, $V_{\text{OUT}} = 800\,\text{V}$] (note: the specific shape of the N-MBB FCML's triangular currents, i.e., i_{L1}, i_{L2}, and i_{L1}+i_{L2}, are dependent on the duty cycle). **(c)** Simulated flying capacitor voltage $v_{\text{C,f}}$ of the proposed N-MBB FCML converter, for the transition between buck and boost mode, where the output voltage is controlled to a fixed 500 V and the input voltage ramps from 100 V to 1 kV.

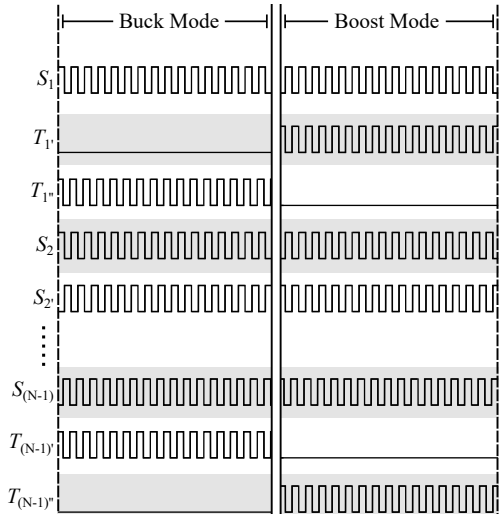


Fig. 4: Gate signals for an N-level N-MBB FCML converter, shown for both buck and boost mode operation.

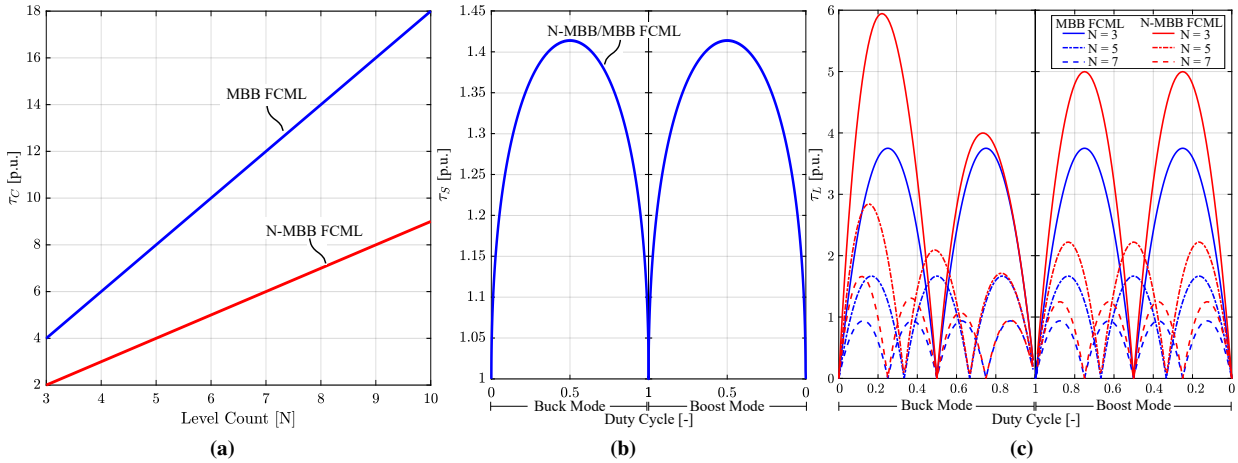
and boost operation. Note that these inductors can be placed on either the input or output side of the converter without changing the outcome of the analysis performed here.

As shown in Fig. 2b, the proposed N-MBB FCML converter also requires bipolar blocking switches as the voltage across the switches (S_x in Fig. 1 and Fig. 2) shows opposite polarity in boost and buck operating modes. If S_x would be realized as anti-series connections of normal transistors, no improvement regarding chip area and conduction losses over the conventional MBB FCML topology would be expected. However, novel dual-gate monolithic bidirectional (GaN) transistors [7]–[9] provide bipolar voltage blocking capability with only a minor chip area increase compared to a standard transistor. In the N-MBB FCML, these M-BDSs see a voltage stress of $V_{\text{ds}} = \frac{V_{\text{max}}}{N-1}$ (neglecting ripple and overshoot), where $V_{\text{max}} = \max(V_{\text{IN,max}}, V_{\text{OUT,max}})$.

Furthermore, the proposed topology requires four—independent of the NMBB FCML level count N—unipolar MOSFETs (T_x), implemented as diagonal switches to configure the converter operating state [11], [12]. Of these four devices, only two are switching during either operating mode and the other two are clamped in the off-state, i.e., do not contribute to conduction losses. The voltage rating of these unipolar switches T_x is higher than that of the bi-directional switches as they need to block the full input/output voltage. Note, however, that when the unipolar devices are operated with PWM, the voltage stress is $\frac{V_{\text{max}}}{N-1}$, which is the same as for the M-BDS devices.

B. Operating Modes

We describe the operating principle with the example of the three-level version of the proposed topology shown in Fig. 2b, with the buck and boost operating modes highlighted in Fig. 2d and Fig. 2f, respectively. Moreover, Fig. 4 shows the gate signals used to control the converter during buck and boost operating modes. In buck operating mode, the diagonal switch $T_{2''}$ and the low-side switch $T_{1'}$ are clamped in the off-state such that the configuration of the converter is similar to the split input inductor FCML proposed in [10]. Here, the current splits between the two inductors as a function of duty cycle. The inductor currents for buck operating mode are shown in Fig. 3a. In boost operating mode, the low-side switch $T_{2'}$ and the diagonal switch $T_{1''}$ are clamped off, such that the converter is configured as a typical boost FCML converter with an additional low-side inductor (L_2), whose average current is approximately zero, as shown in Fig. 3b. In both operating modes, the summed dc components of the N-MBB FCML converter's inductor currents is equal to the dc component of the inductor current in the conventional MBB FCML converter (i.e., $I_{\text{L1}} + I_{\text{L2}} = I_{\text{L,mir}}$). Moreover, considering equal inductances (i.e., $L_1 = L_2 = L_{\text{mir}}$), the sum of the inductor currents shows a peak-to-peak ripple which is double that for the conventional MBB FCML converter (i.e., $\Delta i_{\text{L1}} + \Delta i_{\text{L1}} = 2\Delta i_{\text{Lmir}}$). The flying capacitor's average



(a) (b) (c)

Fig. 5: **(a)** Switch conduction loss FOM τ_{C} over level count, showing favorable scaling for the proposed N-MBB topology. **(b)** Switching loss FOM τ_{S} over duty cycle, identical between the mirrored and non-mirrored topologies for any level count. **(c)** Inductor volume FOM τ_{L} shown as a function of duty cycle and level count, indicating larger inductor volume of the N-MBB topology.

TABLE I: Comparison of components for proposed MBB FCML converter and N-MBB FCML converter.

Parameter	Mirrored Topology	Non-mirrored Topology
Total Switches	$4(N-1)$	$2(N-1)+2$
Number of MOSFETs	$4(N-1)$	4
Number of M-BDSs	0	$2(N-2)$
Number of Inductors	1	2
Number of Flying Capacitors	$2(N-2)$	$N-2$
Effective Switching Frequency	$f_{\mathrm{sw}}(N-1)$	$f_{\mathrm{sw}}(N-1)$

voltage is equal to $\frac{\mathrm{i}\times V_{IN}}{N-1}$ in buck mode and $\frac{\mathrm{i}\times V_{OUT}}{N-1}$ in boost mode, where i is the index of the flying capacitor, identical to the standard MBB FCML converter. The transition between buck and boost mode is shown in Fig. 3c, which shows how the flying capacitor voltage remains balanced in either operating mode and during the transition between the two modes.

III. Comparative Evaluation of the Proposed N-MBB FCML Topology

Compared to the conventional MBB FCML topology, the proposed N-MBB FCML topology benefits from a reduced number of flying capacitors and a lower total number of switches (see Table I). However, the N-MBB FCML converter does require M-BDSs and two inductors as explained above. The remainder of this section provides a quantitative comparative evaluation of the two variants regarding relevant figures of merit (FOMs) as introduced in [13].

To quantify the expected conduction losses through the switches, the rms current through each switch was squared and summed as shown in (1), this value was then normalized to the maximum of the input and output current, $I_{\max}$.

$$\tau_{\mathrm{c}} = \frac{1}{I_{\max}^2} \sum_k \tilde{i}_k^2 \tag{1}$$

This switch conduction loss FOM, τ_{c}, does not depend on the duty cycle, but does increase with higher number of switches, as shown in Fig. 5a. Since the MBB FCML converter relies on half the high-side switches clamped in the on-state during either operating mode, higher conduction losses are expected. Therefore, this FOM shows the proposed N-MBB FCML converter scaling more advantageously with increased level count.

Since both the semiconductor voltage and current contributes to hard-switching losses, the switching loss FOM, τ_{S}, is a summation of the maximum voltage and rms current in each switch, which is then normalized to the product of the maximum of the input and output current and the maximum of the input and output voltage.

$$\tau_s = \frac{1}{I_{\max} V_{\max}} \sum_k \tilde{i}_k v_{\mathrm{ds},k} \tag{2}$$

This FOM, which does not depend on the level count N, is plotted over the duty cycle in Fig. 5b and is equivalent between the N-MBB FCML and conventional MBB FCML.

To compare the estimated inductor volume, the inductance, rms current and peak-to-peak current ripple were

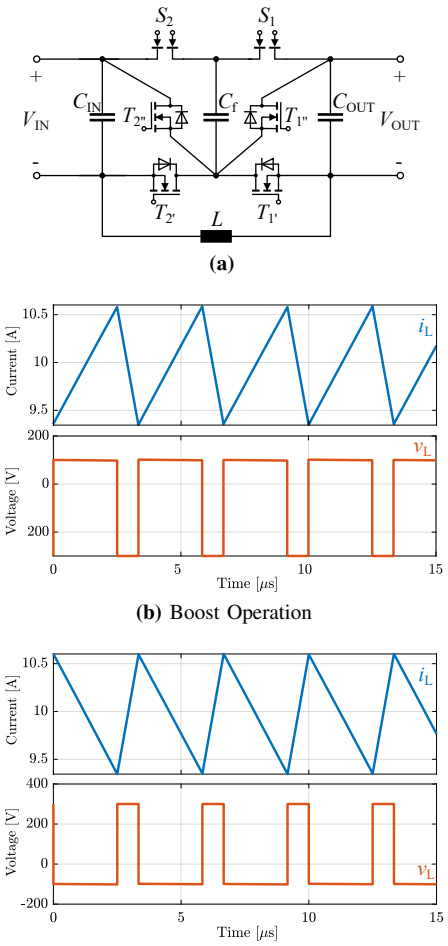


Fig. 6: **(a)** Schematic for a RPI N-MBB FCML converter. **b)** Inductor current and voltage, simulated with the same inductance and the same operating point shown in Fig. 3a [$V_{\mathrm{IN}} = 500\,\mathrm{V}$, $V_{\mathrm{OUT}} = 800\,\mathrm{V}$]. **c)** Inductor current and voltage, simulated with the same inductance and the same operating point shown in Fig. 3b [$V_{\mathrm{IN}} = 800\,\mathrm{V}$, $V_{\mathrm{OUT}} = 500\,\mathrm{V}$]. For both boost and buck operating modes the inductor voltage is seen as common-mode voltage on the input or output terminals.

computed for a given switching frequency and current ripple condition, chosen to be 100 kHz and 20% (peak) respectively. The inductor volume FOM τ_{L} is defined in (3), which is normalized to the maximum voltage, V_{max}, maximum current, I_{max}, and switching period, T_{s}.

$$\tau_L = \frac{1}{I_{\mathrm{max}} V_{\mathrm{max}} T_{\mathrm{s}}} \sum_m L_m \tilde{i}_m \hat{i}_m \tag{3}$$

Note that this FOM is summed over the total number, m, of inductors in each topology. Fig. 5c shows τ_{L} as a function of duty cycle and level count N. As the level count increases the N-MBB FCML converter's required FOM τ_{L} decreases by a factor of $(N-1)^2$, which is the same behavior as known from the conventional MBB FCML converter. However, the N-MBB FCML converter has a higher expected total inductor volume at each operating condition since two inductors are necessary for operation.

IV. Proposed Topology Variations

A. Return Path Inductor (RPI) N-MBB FCML Converter

As described in the previous section, the proposed N-MBB FCML converter topology has performance trade-offs when compared to the conventional MBB FCML converter, dependent on application and operating conditions. Therefore, this work also motivates the investigation of topology variants with possibly different trade-off characteristics. One such topology variant is shown in Fig. 6a and utilizes a return-path inductor (RPI) [14] instead of the split inductor of the original N-MBB FCML (see Fig. 1). The operation principle (e.g., gating of the switches) of the RPI N-MBB FCML topology remains the same as described above. The RPI variant reduces the required inductor volume; however, the RPI results in a high-frequency common-mode voltage on the input or output terminals. Fig. 6bc show the key waveforms for operation in boost and buck mode, highlighting also the inductor voltage, v_{L}, which results in a common-mode voltage, e.g., on the output terminals in the case of the input-side dc-terminal grounded / considered the reference potential.

Note that the RPI approach is especially beneficial in three-phase dc-ac converters that consist of three BB modules (Y-inverter), where the low-frequency current stress of the RPI inductor is massively reduced [14].

B. N-MBB FCML DC-AC Inverter

The N-MBB FCML can be operated as an inverter simply by adding an unfolder stage. However, with slight modification, the topology can also be configured to *directly* produce an ac output from a split dc bus. As shown in Fig. 7a by adding an additional diagonal switch, labelled $T_{2'''}$, the converter can be reconfigured to boost the negative input voltage. Moreover, for full ac operation all the switches are realized with M-BDSs as each switch must block both positive and negative voltage. The necessary gate signals to operate the converter are shown in Fig. 7b, and simulated key waveforms are shown in Fig. 7c. While the additional switch adds control complexity, the number of switches operating at any given time remains the same as in the dc-dc case, therefore no increase in switching losses should be observed.

V. Conclusion

Buck-boost dc-dc converters enable flexible power conversion in future electrified transportation applications. Novel monolithic bidirectional GaN switches (M-

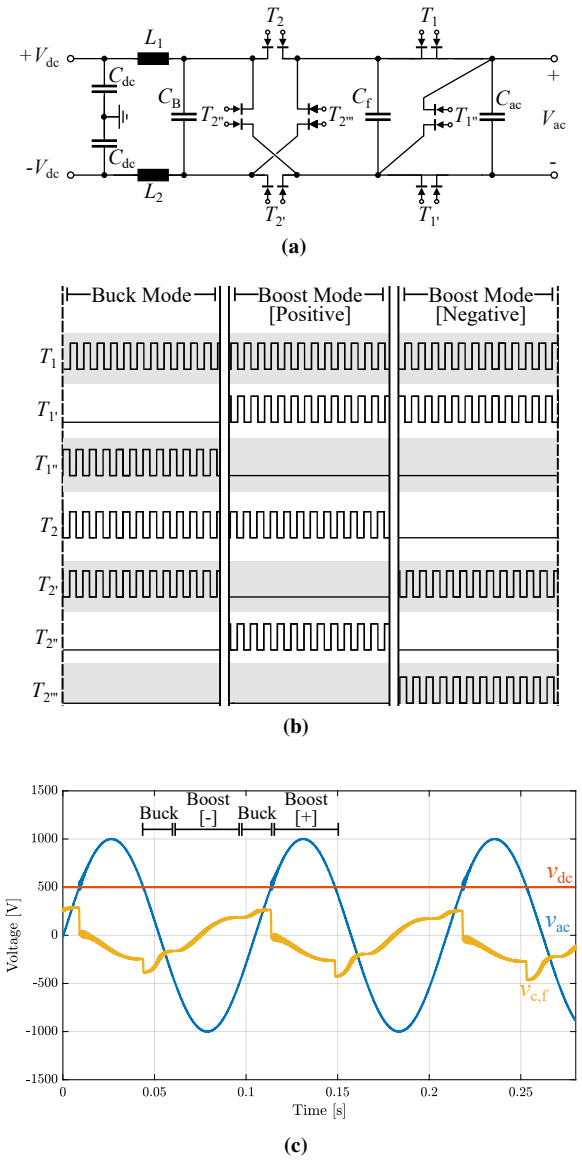


Fig. 7: **(a)** Three-level N-MBB FCML inverter topology. **(b)** Gate signals for controlling the N-MBB inverter. **(c)** Simulated waveforms showing the generated 60 Hz ac output with a peak of 1 kV and 10 kW, with a 500 V split bus input.

BDSs) motivate the derivation of the proposed non-mirrored buck-boost (N-MBB) flying-capacitor multi-level (FCML) converter. We explain the operating principle and characterize component stresses by figure of merits (FOMs), which also facilitate a comparative evaluation against the conventional (mirrored) FCML converter. Whereas the proposed N-MBB FCML converter results in a larger inductor volume, it advantageously features a reduced component count, lower conduction losses, and a better utilization of the installed chip area as we all as of the flying capacitors. The proposed return-path-inductor (RPI) N-MBB FCML reduces the number of inductors but results in a common-mode voltage on the output terminals. The RPI variant may be suitable for certain applications, especially for three-phase dc-ac Y-inverters. Finally, the introduced direct dc-ac inverter variant of the N-MBB FCML converter opens further directions for investigations utilizing this topology in a variety of applications.

REFERENCES

[1] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-board microgrids for the more electric aircraft—technology review," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5588–5599, 2019.

[2] Q. Xun, Y. Liu, and E. Holmberg, "A comparative study of fuel cell electric vehicles hybridization with battery or supercapacitor," in *Proc. Int. Symp. Power Elecon., Electrical Drives, Automation and Motion (SPEEDAM)*, Amalfi, Italy, Jun. 2018, pp. 389–394.

[3] J. A. Oliver, P. Zumel, M. Sanz, C. Raga, D. Izquierdo, O. Garcia, A. Barrado, R. Prieto, R. Azcona, B. Delicado, and J. A. Cobos, "High level decision methodology for the selection of a fuel cell based power distribution architecture for an aircraft application," in *Proc. IEEE Energy Conversion Congr. Expo. (ECCE USA)*, San Jose, CA, USA, Sep. 2009, pp. 459–464.

[4] E. Bataller-Planes, N. Lapena-Rey, J. Mosquera, F. Orti, J. A. Oliver, O. Garcia, F. Moreno, J. Portilla, Y. Torroja, M. Vasic, S. C. Huerta, M. Trocki, P. Zumel, and J. A. Cobos, "Power balance of a hybrid power source in a power plant for a small propulsion aircraft," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2856–2866, 2009.

[5] D. Menzi, Z. Yu, J. Huber, and J. W. Kolar, "Comparative evaluation of ultra-lightweight buck-boost DC-DC converter topologies for future eVTOL aircraft," in *Proc. 23rd IEEE Workshop Control Modeling Power Electron (COMPEL)*, Tel Aviv, Israel, Jun. 2022.

[6] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Conf. Rec. 23rd Annu. IEEE Power Electron. Specialists Conf. (PESC)*, Toledo, Spain, Jun 1992, pp. 397–403.

[7] T. Morita, M. Yanagihara, H. Ishida, M. Hikita, K. Kaibara, H. Matsuo, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "650 V 3.1 mΩcm2 GaN-based monolithic bidirectional switch using normally-off gate injection transistor," in *Proc. IEEE Int. Electron. Dev. Meet. (IEDM)*, Washington, DC, USA, Dec. 2007, pp. 865–868.

[8] B. Pandya, "600V GaN dual gate bidirectional switch," 2019. [Online]. Available: https://poweramericainstitute.org/wp-content/uploads/2020/01/Task-BP4-4.36-Q4-Infineon-Quad-chart.pdf

[9] F. Vollmaier, N. Nain, J. Huber, J. W. Kolar, K. K. Leong, and B. Pandya, "Performance evaluation of future T-Type PFC rectifier and inverter systems with monolithic bidirectional 600 V GaN switches," in *Proc. Energy Conversion Congr. Expo. (ECCE USA)*, Vancouver, Canada, Oct. 2021, pp. 5297–5304.

[10] A. Abdulslam and P. P. Mercier, "A battery-connected inductor-first flying capacitor multilevel converter achieving 0.77W/mm2 and 97.1% peak efficiency," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Austin, TX, USA, Apr. 2021.

[11] Y. Wang, J. Ye, R. Ku, and et al., "A modular switched-capacitor multilevel inverter featuring voltage gain ability," *Journal of Power Electronics*, 2022.

[12] C. Terbrack, J. Stöttner, and C. Endisch, "Design and validation of the parallel enhanced commutation integrated nested multilevel inverter topology," *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 15 163–15 174, 2022.

[13] D. Menzi, D. Bortis, and J. W. Kolar, "A new bidirectional three-phase phase-modular boost-buck AC/DC converter," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo. (PEAC)*, Shenzhen, China, Nov. 2018.

[14] D. Menzi, J. E. Huber, L. Kappeler, G. Zulauf, and J. W. Kolar, "New return path inductor buck–boost y-inverter motor drive with reduced current stresses," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 086–10 090, 2022.