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***Abstract*—On-chip switched capacitor (SC) converters for multicore microprocessor power delivery have the potential to reduce the overall energy consumption of future multicore microprocessor systems by independently regulating the voltage supply of each core. This paper describes an on-chip SC converter that can be reconfigured between a 2:1 and a 3:2 voltage conversion ratio to support a wide output voltage range from a single input supply. Regarding SC converter analysis and modeling, this paper extends an existing state space model framework to include the flying capacitors' parasitic bottom plate capacitors, which for on-chip SC converters significantly influence both the capacitor currents and the converter efficiency. A reconfigurable SC converter that supports an output voltage range of $700\,\mathrm{mV}$ to $1150\,\mathrm{mV}$ from a $1.8\,\mathrm{V}$ input supply is implemented in a $32\,\mathrm{nm}$ SOI CMOS technology that features the high-density deep trench capacitor. The converter achieves a maximum efficiency of 85.2% at $2.1\,\mathrm{W/mm^2}$ power density in the 2:1 configuration and a maximum efficiency of 84.1% at $3.2\,\mathrm{W/mm^2}$ in the 3:2 configuration.**

I. Introduction

High-performance microprocessor systems could benefit significantly on critical aspects such as total energy consumption by incorporating on-chip voltage regulators (OCVR). An OCVR is a fully integrated voltage regulator that generates the microprocessor's desired supply voltage (e.g. $0.9\,\mathrm{V}$ [1]) from a higher-than-nominal supply voltage (e.g. $1.8\,\mathrm{V}$). Furthermore, the OCVR is integrated on the same chip die as the microprocessor itself, thereby acting as a true point of load (POL) converter.

From a package point of view, an OCVR can reduce the number of power/ground pins that carry the high supply currents required by modern high-performance microprocessors [2–4]. Reducing the number of power/ground pins is extremely attractive because more than half the total number of package pins in today's microprocessors are reserved for power/ground [1], and trend analyses confirm these characteristics also for future microprocessor systems [4]. Furthermore, OCVRs enable per-core regulation in multicore microprocessor. Having one dedicated OCVR per microprocessor core facilitates new power management architectures in which the supply voltage of each core can be regulated according to its independent need. Applying ultra-fast dynamic voltage and frequency scaling (DVFS), which extends traditional DVFS by capturing within-workload supply voltage variations, has the potential to reduce the overall microprocessor system energy by up to 21% [5].

Traditionally, buck converters are used as POL converters for microprocessor power delivery. Research in microfabricated inductors have focused on achieving high inductor quality factors at small footprints. The current state of the art targets 3D chip integration, where the buck converter is implemented on an interposer in close proximity to the microprocessor chip die [6–9]. However, buck converters are typically not integrated on the same deep submicron chip die as the microprocessor. Inductors using only metals available in the chip metal stack (air core inductors) achieve poor quality factors because of the small metal thicknesses defined by the fabrication process [10]. Furthermore, magnetic materials that increase the quality factor and the inductance typically are not readily available in deep submicron processes.

In contrast, switched capacitor (SC) converters can be implemented using only switches and capacitors that are readily available in the deep submicron semiconductor technologies. For this reason, this paper focuses on on-chip SC converters.

A widely accepted model framework for SC converters was introduced in [11] and further developed in [12]. This model framework, which can be applied on any realizable SC converter topology, can be used to derive a switching frequency dependent equivalent output resistance R_{eq} that accounts for the converter's conduction losses. However, it has two disadvantages regarding OCVR applications: firstly, an approximation is used to calculate R_{eq}, and this approximation is least accurate when the SC converter is operated at its highest efficiency [13]. Secondly, it does not include switching losses, which are mainly associated with the parasitic bottom plate capacitors of the flying capacitors. Switching losses due to the parasitic bottom plate capacitor may not be of major concern for discrete SC converters since the parasitic bottom plate capacitors of discrete capacitors can often be neglected. However, they cannot be neglected for on-chip SC converters and may therefore have significant influence on the converter's output current and efficiency. In [13], a SC model framework based on conventional circuit analysis put into a state space model representation is used. Once all node equations have

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been put into matrix form, R_{eq} can be calculated accurately. However, also this model framework does not account for switching losses. This paper extends the state space modeling in [13] to take the effect of the parasitic bottom plate capacitor (i.e., switching losses) on capacitor currents and converter efficiency into account.

The voltage conversion ratio of a SC converter is determined by the topology, i.e. by the configuration of switches and capacitors. Prior SC converter art overcomes this limitation by using reconfigurable (gearbox) power stages, which can switch between voltage conversion ratios to increase the input/output voltage range [11, 12, 14–16]. However, the efficiency and power density performance of the these designs are limited by the MOS or MIM integrated capacitors available in the semiconductor processes used. Recent SC converter designs, which are implemented using integrated deep trench capacitors having high capacitance density and low parasitic bottom plate capacitance, have shown much improved efficiency and power density performance than SC converters using conventional MOS or MIM capacitors [2, 3]. However, these designs are single voltage conversion ratio only.

This paper presents an on-chip SC converter that can be reconfigured to having a 2:1 or a 3:2 step-down voltage conversion ratio. From a $1.8\,\mathrm{V}$ input supply, an output voltage range of $700\,\mathrm{mV}$ to $1150\,\mathrm{mV}$ is supported, thus making this design suited for ultra-fast DVFS in high-performance microprocessor applications. The SC converter is implemented in a 32 nm SOI CMOS technology with deep trench capacitors for high efficiency and high power density.

Section II treats the concept of the 2:1 and 3:2 reconfigurable SC converter. Section III introduces the improved model framework which includes switching losses. The model is verified against Matlab Simulink simulations. Section IV details the implementation of the reconfigurable SC converter in the $32\,\mathrm{nm}$ SOI CMOS semiconductor process. In Section V, measurement results of the prototype reconfigurable SC converter are presented and compared with prior art, revealing a more than twofold improvement in power density at an overall higher efficiency, as concluded in Section VI.

II. Reconfigurable Switched Capacitor Converters

A SC converter is often perceived as a converter with a fixed voltage conversion ratio. However, this is not the complete picture, as the output voltage of a SC converter can be operated below the voltage resulting from the conversion ratio. For instance, a 2:1 conversion ratio SC converter can support output voltages below half the input voltage. For a microprocessor application using DVFS, the output voltage range required can exceed the range covered by the 2:1 converter. Instead, a 3:2 conversion ratio SC converter may be more suitable, covering the output voltage below two-thirds of the input voltage. However, a characteristic of SC converters is that the efficiency drops linearly with the output voltage, as will be discussed in more detail in Section III. Hence it is undesirable to operate SC converters at an output voltage far

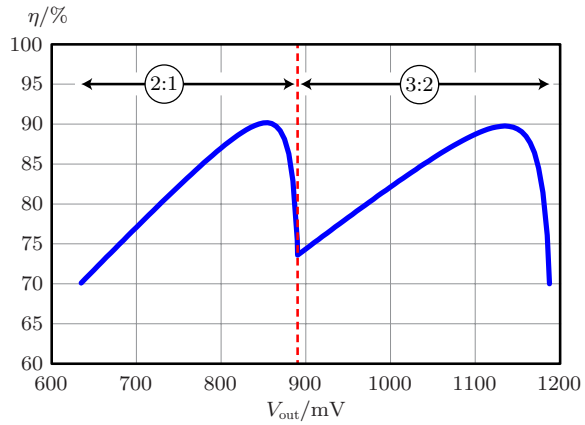

Fig. 1. Efficiency of a 2:1 and a 3:2 reconfigurable SC converter with $V_{\mathrm{in}} = 1.8\,\mathrm{V}$. Reconfigurable SC converters are a means to efficiently cover a wide output voltage range from a fixed input voltage.

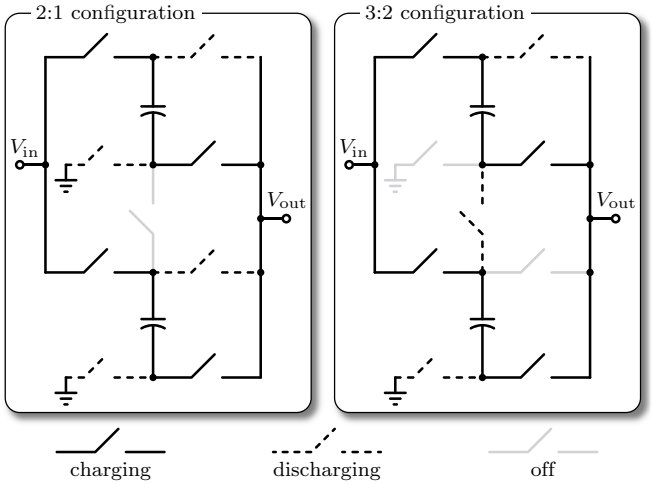

Fig. 2. The 2:1 and 3:2 reconfigurable SC converter power stage including the switch configuration in the charging and the discharging phase.

off the conversion ratio. A solution is a SC converter that can be reconfigured between the 2:1 and the 3:2 voltage conversion ratio to efficiently cover a wide output voltage range.

As an example: with $V_{\mathrm{in}} = 1.8\,\mathrm{V}$, the 2:1 converter covers the output voltage below $900\,\mathrm{mV}$, and the 3:2 converter covers an output voltage below $1.2\,\mathrm{V}$. By changing between the 2:1 and the 3:2 configuration, efficiency can be kept high over a wide output voltage range, as depicted in **Fig. 1**.

The output current (and thereby the output power) for a given output voltage depends on the dimensioning of capacitors and switches in the power stage. Output current regulation capability can be done by changing the switching frequency as in [2, 3, 14–17].

A. 2:1 and 3:2 reconfigurable power stage

The basic operating principle of the reconfigurable SC converter power stage is shown in **Fig. 2** [11, 12, 15, 16]. In each configuration, two flying capacitors are sequentially switched between a charging and a discharging phase at 50%

duty cycle. The rate at which the converter switches phase is denoted by the switching frequency f_{sw}. The implementation of this converter in a $32\,\mathrm{nm}$ SOI CMOS technology will be detailed further in Section IV.

III. State space model representation

Applying a model framework on a SC converter, as depicted in **Fig. 3**, translates the SC converter into an equivalent model that captures the steady state converter operation and power losses (efficiency) The transformer winding ratio $1{:}M$ models the voltage conversion ratio, R_{eq} models the equivalent output resistance that governs the conduction losses, and R_{bp} models the equivalent bottom plate resistance that governs the switching losses. Both R_{eq} and R_{bp} are functions of f_{sw}.

The model framework from [11, 12] can be used to estimate R_{eq}. However, as mentioned in the introduction, this model framework is not directly applicable for on-chip SC converters because of the presence of the flying capacitor's parasitic bottom plate capacitor C_{bp}, which significantly influences both steady state operation and efficiency. In other words, the influence of C_{bp} on R_{eq} and the inclusion of R_{bp} in Fig. 3 are not taken into account in [11, 12]. These effects have been indicated in e.g. [15, 17], but not in a comprehensive manner that considers steady state operation.

A. State space model framework including C_{bp}

The state space model from [13] is extended in the following to include C_{bp}, thereby being applicable in the design of on-chip SC converters. As opposed to [13], we have $2n$ capacitors (n flying capacitors and n appertaining bottom plate capacitors), which are put as diagonal elements into a $2n$ diagonal matrix $\mathbf{C}$. The input and the output voltage are composed into vector $\mathbf{u}$. Vectors $\mathbf{v}$ and $\mathbf{i}$ collect all capacitor voltages and currents, respectively, with $\mathbf{v}$ and $\mathbf{i}$ being related by

$$\mathbf{i} = \mathbf{C}\dot{\mathbf{v}}, \tag{1}$$

where $\dot{\mathbf{v}}$ is the time derivative of $\mathbf{v}$.

For the charging phase (phase 1), Kirchhoff's voltage and current laws (KVL and KCL, respectively) are applied to determine $2n$ independent equations of the form

$$\mathbf{E}_1\mathbf{i} + \mathbf{F}_1\mathbf{v} + \mathbf{G}_1\mathbf{u} = \mathbf{0}. \tag{2}$$

When KVL is applied, rows in $\mathbf{E}_1$ are resistances (transistor on-state resistances and / or flying capacitor equivalent series resistances), and rows in $\mathbf{F}_1$ and $\mathbf{G}_1$ are -1, 0, or 1. When KCL is applied, rows in $\mathbf{E}_1$ are -1, 0, or 1 and rows in $\mathbf{F}_1$ and $\mathbf{G}_1$ are all 0. Letting $\mathbf{v}$ represent the system states, (1) and (2) can be combined into

$$\begin{aligned} \dot{\mathbf{v}} &= \mathbf{A}_1\mathbf{v} + \mathbf{B}_1\mathbf{u} \\ \mathbf{A}_1 &= -\mathbf{C}^{-1}\mathbf{E}_1^{-1}\mathbf{F}_1 \\ \mathbf{B}_1 &= -\mathbf{C}^{-1}\mathbf{E}_1^{-1}\mathbf{G}_1, \end{aligned} \tag{3}$$

where $\mathbf{C}$ is always invertible because it is a diagonal matrix and $\mathbf{E}_1$ is invertible when KVL and KCL have been applied correctly [13]. The general solution to the system of differential equations in (3) is

$$\mathbf{v}(t) = \underbrace{e^{\mathbf{A}_1(t-t_0)}}_{\mathbf{\Phi}_1(t)}\mathbf{v}(t_0) + \underbrace{\left[\int_{t_0}^{t} e^{\mathbf{A}_1(t-\tau)}\mathbf{B}_1 \mathrm{d}\tau\right]}_{\mathbf{\Gamma}_1(t)}\mathbf{u}, \tag{4}$$

where we have utilized that $\mathbf{u}$ is independent of τ. $\mathbf{\Phi}_1(t)$ is known as the state transition matrix.

Using the same approach for the discharging phase (phase 2) results in $\mathbf{A}_2$ and $\mathbf{B}_2$, as well as $\mathbf{\Phi}_2(t)$ and $\mathbf{\Gamma}_2(t)$.

With 50% duty cycle, $t_1 = 1/(2f_{\mathrm{sw}})$ is the duration of the charging phase, and $t_2 = 1/(2f_{\mathrm{sw}})$ is the duration of the discharging phase. Hence, assuming the charging phase begins at $t_0 = 0$, the system states (capacitor voltages) at the end of each switching phase equals

$$\mathbf{v}(t_1) = \mathbf{\Phi}_1(t_1)\mathbf{v}(0) + \mathbf{\Gamma}_1(t_1)\mathbf{u} \tag{5}$$

$$\mathbf{v}(t_1 + t_2) = \mathbf{\Phi}_2(t_2)\mathbf{v}(t_1) + \mathbf{\Gamma}_2(t_2)\mathbf{u}. \tag{6}$$

In steady state, $\mathbf{v}(0) = \mathbf{v}(t_1 + t_2)$ applies, which, using (5) and (6), gives the initial condition

$$\mathbf{v}(0) = \big(\mathbf{I} - \mathbf{\Phi}_2(t_2)\mathbf{\Phi}_1(t_1)\big)^{-1}\big(\mathbf{\Phi}_2(t_2)\mathbf{\Gamma}_1(t_1) + \mathbf{\Gamma}_2(t_2)\big)\mathbf{u}, \tag{7}$$

where $\mathbf{I}$ is the $2n$ identity matrix. The charge delivered by each capacitor per switching phase is determined as

$$\mathbf{q}_1 = \mathbf{C}\left(\mathbf{v}(t_1) - \mathbf{v}(0)\right) \tag{8}$$

$$\mathbf{q}_2 = \mathbf{C}\left(\mathbf{v}(t_1 + t_2) - \mathbf{v}(t_1)\right) = -\mathbf{q}_1, \tag{9}$$

where the last equality holds because of charge conservation.

B. Example 2:1 SC converter analysis

In the following, the above state space model is applied on the 2:1 SC converter shown in **Fig. 4a**, where the equivalent circuit is shown in its charging and its discharging phase in Fig. 4b and Fig. 4c, respectively. In the equivalent circuit, each switch is replaced by an on-state resistance R_{on} when on and an open circuit when off, and the flying capacitor model includes its equivalent series resistance R_{esr} and the bottom plate capacitor C_{bp}.

The application of KVL and KCL put into the form of (2) yields the system matrices

$$\mathbf{C} = \begin{pmatrix} C & 0 \\ 0 & C_{\mathrm{bp}} \end{pmatrix},\ \mathbf{i} = \begin{pmatrix} i_C \\ i_{C\mathrm{bp}} \end{pmatrix},\ \mathbf{v} = \begin{pmatrix} v_C \\ v_{C\mathrm{bp}} \end{pmatrix},\ \mathbf{u} = \begin{pmatrix} V_{\mathrm{in}} \\ V_{\mathrm{out}} \end{pmatrix},$$

$$\mathbf{E}_1 = \begin{pmatrix} R_{\mathrm{on1}} + R_{\mathrm{esr}} & 0 \\ -R_{\mathrm{on3}} & R_{\mathrm{on3}} \end{pmatrix},\ \mathbf{E}_2 = \begin{pmatrix} R_{\mathrm{on2}} + R_{\mathrm{esr}} & 0 \\ R_{\mathrm{on4}} & -R_{\mathrm{on4}} \end{pmatrix},$$

$$\mathbf{F}_1 = \begin{pmatrix} 1 & 1 \\ 0 & 1 \end{pmatrix},\quad \mathbf{F}_2 = \begin{pmatrix} 1 & 1 \\ 0 & -1 \end{pmatrix},$$

$$\mathbf{G}_1 = \begin{pmatrix} -1 & 0 \\ 0 & -1 \end{pmatrix},\quad \mathbf{G}_2 = \begin{pmatrix} 0 & -1 \\ 0 & 0 \end{pmatrix}.$$

Now the procedure described above can be applied to calculate the capacitor charges in (8) and (9). From Fig. 4, the output charge in each phase can be found as

$$q_{\mathrm{out1}} = q_{C1} - q_{C\mathrm{bp1}}, \tag{10}$$

$$q_{\mathrm{out2}} = -q_{C2} = q_{C1}, \tag{11}$$

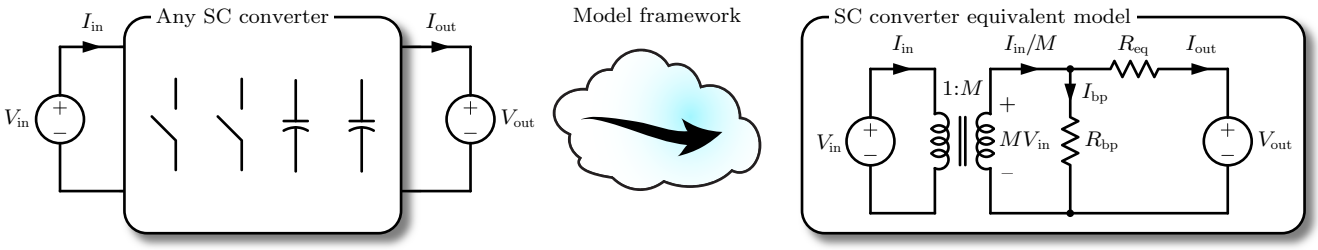

Fig. 3. Using a model framework to describe a SC converter by an equivalent model. The model framework presented in this paper takes into account the flying capacitors' parasitic bottom plate capacitors, whose effect significantly influence both steady state operation and efficiency.

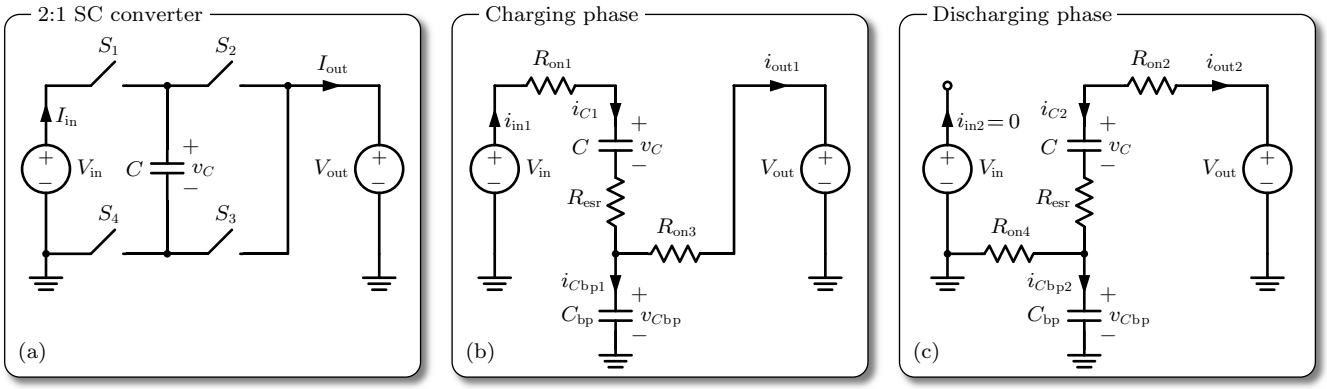

Fig. 4. Basic 2:1 SC converter consisting of 4 switches and 1 flying capacitor analyzed using the state space model framework presented in this paper. The converter is shown in both the charging and the discharging phase, including the transistor on-state resistances $R_{\mathrm{on}1-4}$, the equivalent series resistance R_{esr}, and the parasitic bottom plate capacitor C_{bp}.

and the total average output current over a full switching period becomes

$$I_{\mathrm{out}} = \frac{q_{\mathrm{out}1} + q_{\mathrm{out}2}}{t_1 + t_2} = \left(2q_{C1} - q_{C\mathrm{bp}1}\right) f_{\mathrm{sw}}. \tag{12}$$

Likewise, the total average input current is

$$I_{\mathrm{in}} = \frac{q_{\mathrm{in}1} + q_{\mathrm{in}2}}{t_1 + t_2} = q_{C1} f_{\mathrm{sw}}. \tag{13}$$

Using (12) and (13), the total efficiency of the 2:1 SC converter can be calculated as

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_{\mathrm{in}} I_{\mathrm{in}}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} \left(2 - \frac{q_{C\mathrm{bp}1}}{q_{C1}}\right). \tag{14}$$

To port this analysis to the equivalent model from Fig. 3, the resistances can be determined to be

$$R_{\mathrm{eq}} = \frac{MV_{\mathrm{in}} - V_{\mathrm{out}}}{I_{\mathrm{out}}} = \frac{\frac{1}{2}V_{\mathrm{in}} - V_{\mathrm{out}}}{\left(2q_{C1} - q_{C\mathrm{bp}1}\right) f_{\mathrm{sw}}} \tag{15}$$

$$R_{\mathrm{bp}} = \frac{MV_{\mathrm{in}}}{\frac{1}{M} I_{\mathrm{in}} - I_{\mathrm{out}}} = \frac{1}{2} \frac{V_{\mathrm{in}}}{q_{C\mathrm{bp}1} f_{\mathrm{sw}}} \tag{16}$$

where $M = 1/2$ is the voltage conversion ratio.

A similar analysis is carried out for the 3:2 SC converter, but the details have been omitted for space reasons.

C. Model verification

The state space model of the reconfigurable SC converter is verified against simulations using the Matlab Simulink environment. For the verification, $V_{\mathrm{in}} = 1.8\,\mathrm{V}$, $R_{\mathrm{on}1-9} = R_{\mathrm{esr}1,2} = 1\,\Omega$, and $C_{1,2} = 1\,\mathrm{nF}$. When sweeping the output voltage, the switching frequency is arbitrarily chosen to equal $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$, and when sweeping the switching frequency, the output voltage is arbitrarily chosen to equal $V_{\mathrm{out}} = 850\,\mathrm{mV}$. In the 2:1 configuration, I_{out} is doubled and R_{eq} and R_{bp} are halved since the power stage from Fig. 2 consists of two 2:1 SC converters in parallel.

Fig. 5 shows the model and simulation results for various ratios of bottom plate capacitor to flying capacitor

$$\alpha = C_{\mathrm{bp}}/C. \tag{17}$$

As can be seen, the state space model framework is able to accurately capture the influence of the bottom plate capacitors on the converter's steady state operation and efficiency. For $\alpha = 0\%$, which corresponds to omitting C_{bp}, the efficiency shown in Fig. 5a approaches 100% as I_{out} shown in Fig. 5b approaches 0 and V_{out} goes towards $\frac{1}{2}V_{\mathrm{in}}$ $\left(\frac{2}{3}V_{\mathrm{in}}\right)$ in the 2:1 (3:2) configuration. For $\alpha > 0\%$, the efficiency drops because of the switching losses. Moreover, the transition voltage between the 2:1 and 3:2 configurations is adjusted for each value of α to ensure a continuous efficiency over the entire voltage range. Regarding R_{eq} for $\alpha = 0\%$ shown in Fig. 5c, the well-known characteristics of a $1/f_{\mathrm{sw}}$ behavior at low switching

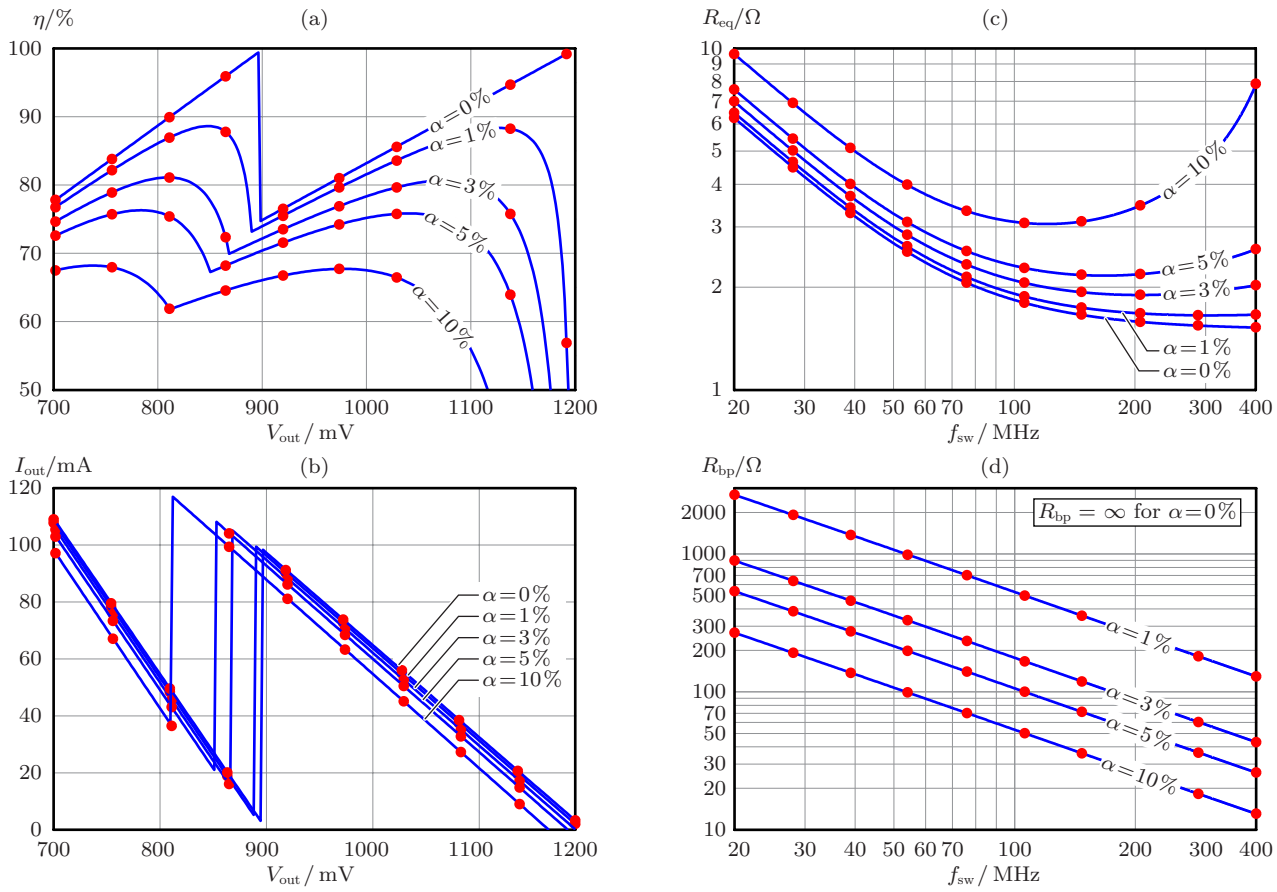

Fig. 5. Verification of (a) efficiency η, (b) output current I_{out}, (c) equivalent output resistance R_{eq}, and (d) equivalent bottom plate resistance R_{bp} resulting from the state space model framework. The simulated results (red dots) match the model results (blue lines) over both output voltage and switching frequency for various values of $\alpha = C_{\text{bp}}/C$.

frequencies and a constant behavior at high switching frequencies are observed [12]. For $\alpha > 0\%$, the decrease in I_{out} and the increase and upward bend at high switching frequencies in R_{eq} are associated with the presence of R_{bp} in Fig. 5d. From Fig. 3, R_{bp} sinks a current (I_{bp}) that would otherwise have been delivered to the output, thereby affecting both the efficiency and the output current. This behavior is not captured by the existing model frameworks [11–13].

D. Power loss distribution

The state space model facilitates an investigation of the distribution of conduction losses P_{eq} and switching losses P_{bp}, which are the power losses associated with R_{eq} and R_{bp}, respectively. Using the same model parameter values as above, the distribution of power losses for various values of α are shown in **Fig. 6**. For $\alpha = 0\%$, there are no switching losses ($P_{\text{bp}} = 0$) and conduction losses constitute all power losses in the converter ($P_{\text{loss}} = P_{\text{eq}}$). For $\alpha > 0\%$, the ratio between the losses is constant at low f_{sw}, since, from Fig. 5c and Fig. 5d, both R_{eq} and R_{bp} scale with $1/f_{\text{sw}}$. This leads to a constant ratio of $R_{\text{bp}}/R_{\text{eq}} \propto I_{\text{bp}}/I_{\text{out}} \propto P_{\text{bp}}/P_{\text{eq}}$. For higher f_{sw}, switching losses constitute an increasing fraction of the total power losses as R_{eq} ceases while R_{bp} continues to scale with $1/f_{\text{sw}}$. This leads to an increased ratio of $I_{\text{bp}}/I_{\text{out}}$ and thereby an increased ratio of $P_{\text{bp}}/P_{\text{eq}}$. For $\alpha > 3\%$, switching losses constitute more than two-thirds of the total power losses.

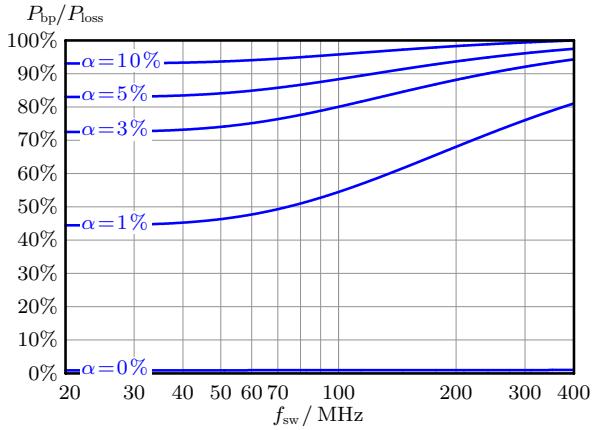

Fig. 6. Distribution of conduction losses P_{eq} and switching losses P_{bp} or various values of α. The total power loss is $P_{\text{loss}} = P_{\text{eq}} + P_{\text{bp}}$.

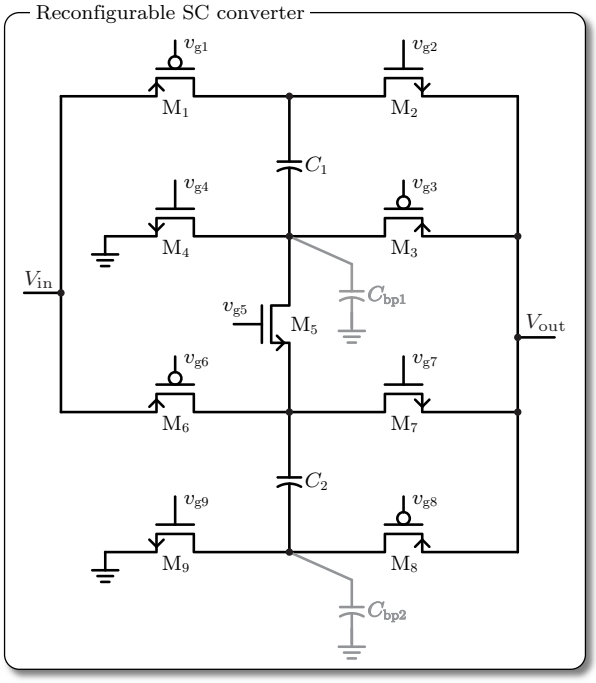

Fig. 7. Transistor level circuit diagram of the reconfigurable SC converter. The parasitic bottom plate capacitors are explicitly shown in gray.

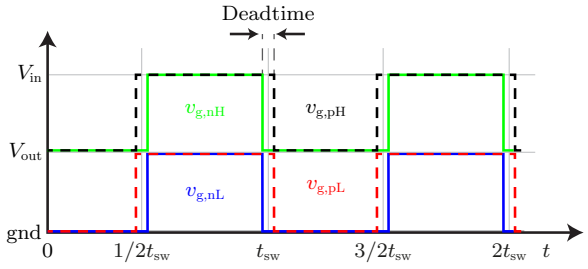

Fig. 8. Level-shifted and non-overlapping (deadtime) gate signals generated by the gate driver.

IV. Implementation in 32 nm SOI CMOS

The reconfigurable SC converter described in Section II and modeled in Section III is implemented in a 32 nm SOI CMOS process from IBM. This particular process features the deep trench capacitor, which, for OCVR applications, has shown superior efficiency and power density performance compared with other on-chip capacitor technologies [2, 3]. The performance benefits are a result of the deep trench capacitor's high capacitance density and low α.

The transistor level circuit diagram of the reconfigurable converter is shown in **Fig. 7**. For each transistor, its gate signal, which is derived from the level-shifted non-overlapping clock signals shown in **Fig. 8**, is listed in **Tab. I** for both the 2:1 and the 3:2 configuration. The change between clock feeds is implemented using multiplexers (not shown) set by a separate control signal. The gate driver used to generate the level-shifted non-overlapping clock signals in Fig. 8 is done as

TABLE I
Gate signals for all transistors in the 2:1 and the 3:2 configuration.

	2:1	3:2
v_{g1}	$v_{g,pH}$	
v_{g2}	$v_{g,nH}$	
v_{g3}	$v_{g,pL}$	
v_{g4}	$v_{g,pH}$	gnd
v_{g5}	gnd	V_{out}
v_{g6}	$v_{g,pH}$	
v_{g7}	$v_{g,nH}$	V_{out}
v_{g8}	$v_{g,pL}$	
v_{g9}	$v_{g,nL}$	

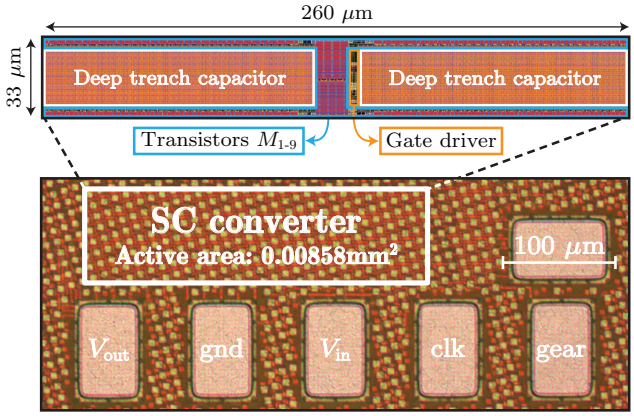

Fig. 9. Chip micrograph of the reconfigurable SC converter implemented in a 32 nm SOI CMOS technology, which features the high capacitance density and low α deep trench capacitor.

in [3]. In the literature, earlier implementations of this power stage use gate drivers that depend on either a) internal node voltages as in [15] or b) external voltage supplies as in [16]. In this implementation, all gate signals are based on V_{out}, V_{in}, and gnd only, see Fig. 8 and Tab. I. This greatly simplifies the gate driver design.

A chip photo with a layout view of the reconfigurable SC converter is shown in **Fig. 9**. The deep trench capacitors take up 72.1%, the transistors 27.3%, and the gate driver 0.6% of the total converter area. The pad labeled gear is used to externally configure between the 2:1 and the 3:2 configuration.

V. Experimental Results

Measurements are carried out on the unpackaged chip die mounted on a probe station. Keithley SourceMeters are used to measure the input and output currents by acting as both the input supply and the output sink. The input and output voltages are measured using Kelvin contacts to account for the voltage drops of cable and contact resistances. For each measurement point, the Keithley SourceMeters are configured such that the on-chip input and output voltages are at the desired levels.

An insufficient on-chip decoupling capacitance is implemented because of chip area limitations, so a discrete 33 nF capacitor is added externally to the chip to reduce the output voltage ripple. However, the extra decoupling capacitance is

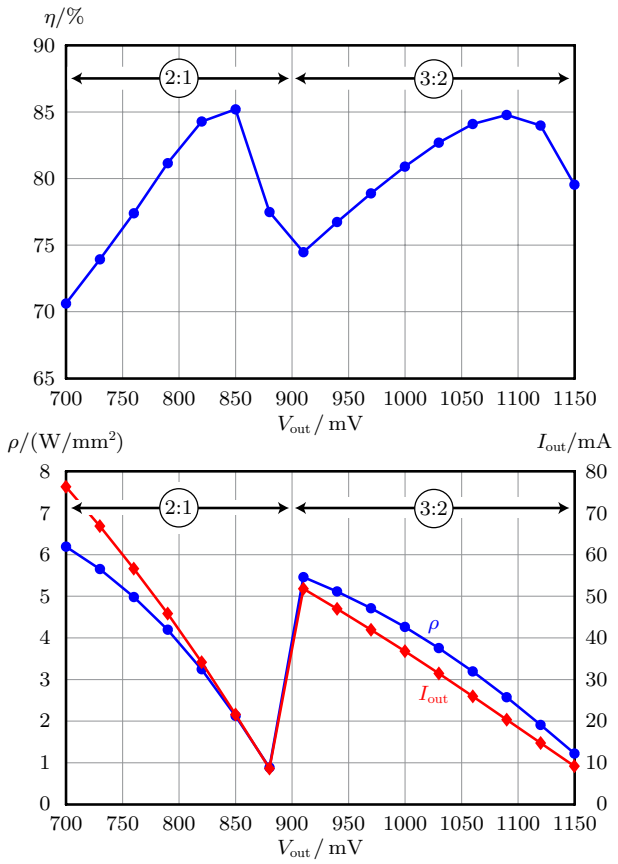

Fig. 10. Measured efficiency and power density results over the entire output voltage range for $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$.

not included in the power density measures as the converter presented here is intended to be used in interleaved on-chip SC converters, in which the need for output decoupling can be drastically reduced or even completely omitted [15–17].

The measurement results for $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$ are shown in **Fig. 10**. The converter achieves a maximum efficiency of 85.2% at $2.1\,\mathrm{W/mm^2}$ power density in the 2:1 configuration and a maximum efficiency of 84.1% at $3.2\,\mathrm{W/mm^2}$ in the 3:2 configuration. The efficiency across the entire voltage range of $700\,\mathrm{mV}$ to $1150\,\mathrm{mV}$ is above 70%. Moreover, the power density can be as high as $6\,\mathrm{W/mm^2}$, but at reduced efficiencies only.

A. Comparison of measurement and model framework results

The model presented in Section III is applied on the reconfigurable SC converter using model parameter values ($R_{\mathrm{on1-9}}$, C, α, and R_{esr}) that are extracted from the technology models provided by IBM. Thereafter, the model is sought fitted to the measurement results in order to investigate parameter variations between the expected and measured results.

The transistors' on-state resistance and the capacitance of the deep trench capacitor depend on the output voltage, thereby affecting the values of $R_{\mathrm{on1-9}}$ and C. However, both R_{on} and C are to a first order independent on switching frequency.

TABLE II
COMPARISON OF MODEL RESULTS USING PARAMETERS EXTRACTED FROM TECHNOLOGY MODELS AND PARAMETERS FITTED TO THE MEASUREMENT RESULTS WITH $V_{\mathrm{in}} = 1.8\,\mathrm{V}$ AND $f_{\mathrm{sw}} = 100\,\mathrm{MHz}$.

2:1	R_{on1}	R_{on2}	R_{on3}	R_{on4}	R_{on5}	R_{on6}
Model(extract)	$0.6\,\Omega$	$0.6\,\Omega$	$0.7\,\Omega$	$0.7\,\Omega$	–	$1.1\,\Omega$
Model(meas)	$1.1\,\Omega$	$1.1\,\Omega$	$1.2\,\Omega$	$1.2\,\Omega$	–	$1.9\,\Omega$
	R_{on7}	R_{on8}	R_{on9}	C	α	R_{esr}
Model(extract)	$1.3\,\Omega$	$0.7\,\Omega$	$0.7\,\Omega$	$1.0\,\mathrm{nF}$	1.8%	$0.7\,\Omega$
Model(meas)	$2.3\,\Omega$	$1.2\,\Omega$	$1.2\,\Omega$	$0.8\,\mathrm{nF}$	1.7%	$0.5\,\Omega$
	V_{out}	I_{out}	R_{eq}	R_{bp}	η	ρ
Model(extract)	$0.85\,\mathrm{V}$	$25\,\mathrm{mA}$	$1.7\,\Omega$	$286\,\Omega$	84.6%	$2.5\,\mathrm{W/mm^2}$
Model(meas)	$0.85\,\mathrm{V}$	$22\,\mathrm{mA}$	$2.3\,\Omega$	$369\,\Omega$	85.0%	$2.2\,\mathrm{W/mm^2}$

3:2	R_{on1}	R_{on2}	R_{on3}	R_{on4}	R_{on5}	R_{on6}
Model(extract)	$1.0\,\Omega$	$1.0\,\Omega$	$0.5\,\Omega$	–	$3.8\,\Omega$	$2.0\,\Omega$
Model(meas)	$1.4\,\Omega$	$1.4\,\Omega$	$0.7\,\Omega$	–	$5.2\,\Omega$	$2.7\,\Omega$
	R_{on7}	R_{on8}	R_{on9}	C	α	R_{esr}
Model(extract)	–	$0.5\,\Omega$	$0.5\,\Omega$	$1.0\,\mathrm{nF}$	1.8%	$0.7\,\Omega$
Model(meas)	–	$0.7\,\Omega$	$0.7\,\Omega$	$0.7\,\mathrm{nF}$	1.7%	$1.4\,\Omega$
	V_{out}	I_{out}	R_{eq}	R_{bp}	η	ρ
Model(extract)	$1.09\,\mathrm{V}$	$30\,\mathrm{mA}$	$3.5\,\Omega$	$501\,\Omega$	84.5%	$3.8\,\mathrm{W/mm^2}$
Model(meas)	$1.09\,\mathrm{V}$	$21\,\mathrm{mA}$	$5.3\,\Omega$	$791\,\Omega$	84.6%	$2.6\,\mathrm{W/mm^2}$

For these reasons, the model is fitted to the measurement results with $V_{\mathrm{out}} = 0.85\,\mathrm{V}$ for the 2:1 configuration and $V_{\mathrm{out}} = 1.09\,\mathrm{V}$ for the 3:2 configuration over the switching frequency range from $40\,\mathrm{MHz}$ to $200\,\mathrm{MHz}$. Furthermore, $V_{\mathrm{in}} = 1.8\,\mathrm{V}$ applies.

The fitting algorithm is designed for a best fit of the measured and modeled R_{eq} and R_{bp} over a switching frequency range. The error function S to be minimized is defined as the sum of the normalized root mean square error between measured and modeled values of R_{eq} and R_{bp}.

$$S = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(R_{\mathrm{eq,meas},f_{\mathrm{sw}i}} - R_{\mathrm{eq,model},f_{\mathrm{sw}i}}\right)^2}}{\frac{1}{N}\sum_{i=1}^{N} R_{\mathrm{eq,meas},f_{\mathrm{sw}i}}} + \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(R_{\mathrm{bp,meas},f_{\mathrm{sw}i}} - R_{\mathrm{bp,model},f_{\mathrm{sw}i}}\right)^2}}{\frac{1}{N}\sum_{i=1}^{N} R_{\mathrm{bp,meas},f_{\mathrm{sw}i}}}, \quad (18)$$

where N is the number of measurement points considered.

The extracted model parameter values are labeled 'Model(extract)' in **Tab II**, and the evaluation of the model using these parameters are listed. To reduce the number of model parameters to fit, the ratios between the extracted on-state resistance values in Tab. II are assumed to be valid when fitting to the measurement results. Using a Matlab script, the model framework is evaluated with different values for each model parameter. Thereafter, the best fit parameters are found by minimizing S from (18). The best fit results for both output voltages are listed as 'Model(meas)' in Tab. II, and the following observations are made from the comparison between extracted and fitted model parameter values:

- The increase in R_{on} is attributed to wire resistances that are not included in the schematic parameter extraction.

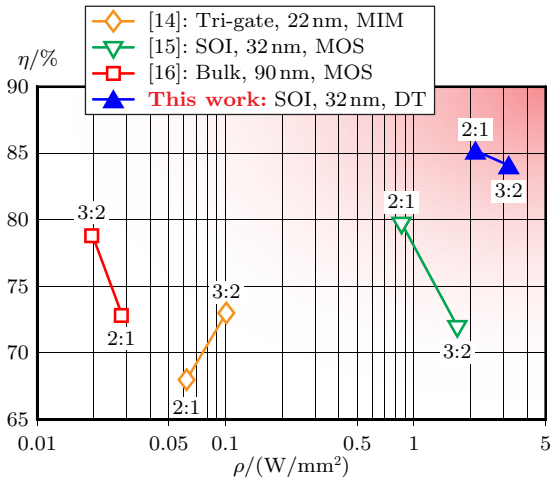

Fig. 11. Efficiency and power density performance comparison between the SC converter presented in this paper and prior art, showing the performance benefits facilitated by the deep trench (DT) capacitor.

- The lower C at higher V_{out} could indicate that the nonlinear voltage dependency on capacitance is more severe for the test chip than anticipated from the technology models.

B. Comparison with prior art

In **Fig. 11**, the performance of the converter presented is compared with that of other on-chip SC converters having (at least) the 2:1 and 3:2 configurations. The values compared are the maximum efficiency and appertaining power density in both configurations. The comparison in Fig. 11 clearly shows the deep trench capacitor's outstanding efficiency and power density performance compared with MOS or MIM capacitors. The power density is more than twice that of prior art at an overall higher efficiency.

VI. Conclusion

This paper extends an existing model framework for switched capacitor (SC) converters to include the parasitic bottom plate capacitor, which significantly influences both the operation and performance of on-chip SC converters. The model framework presented is verified using Matlab Simulink simulations. It is used to design a SC converter that can be configured to provide either a 2:1 or a 3:2 voltage conversion ratio, thereby efficiently extending the output voltage range supported from a fixed input supply. The reconfigurable SC converter is implemented in a $32\,\text{nm}$ SOI CMOS technology that features the deep trench capacitor, which has superior capacitance density and low parasitic bottom plate capacitance compared with MIM and MOS capacitors.

The measured efficiency across the entire voltage range of $700\,\text{mV}$ to $1150\,\text{mV}$ stays above 70%. The converter achieves a maximum efficiency of 85.2% at $2.1\,\text{W}/\text{mm}^2$ power density in the 2:1 configuration and a maximum efficiency of 84.1% at $3.2\,\text{W}/\text{mm}^2$ in the 3:2 configuration. The power density is more than twice that of prior art at an overall higher efficiency. With these efficiency and power density figures, on-chip SC converters using deep trench capacitors are viable as on-chip voltage regulators for multicore microprocessor power delivery applications.

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