# Synergetic Control of Three-Phase AC-AC Current-Source Converter Employing Monolithic Bidirectional 600 V GaN Transistors

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***Abstract*—AC-AC current-source converters (CSCs) are an interesting alternative to the widely-used voltage-source converters for next-generation motor drive applications, as they inherently feature continuous output voltages and minimum filter effort. This mitigates issues such as reflections on long motor cables, high-frequency motor losses, the need for expensive shielded motor cables, and common-mode currents that damage motor bearings. In this paper, we first propose a new synergetic control for an AC-AC CSC that always operates either the front-end rectifier or the output-side inverter stage with one phase clamped, reducing switching losses compared to conventional modulation that continuously operates all three phases. We then provide calorimetric switching loss measurements of a novel 600 V, 140 mΩ monolithic bidirectional GaN transistor, and model the impact of the third, passive switch present in CSC commutation cells on switching losses. This facilitates a subsequent quantitative performance evaluation of an exemplary AC-AC CSC motor drive that employs the GaN M-BDS and operates from a 200 V three-phase mains. For a nominal motor power of 1.5 kW and a required AC-AC semiconductor efficiency of 98 %, a conventionally controlled CSC can operate with a switching frequency of 48 kHz, whereas the proposed synergetic control enables twice the switching frequency, i.e., 96 kHz and accordingly facilitates a significant volume reduction of the DC-link inductor and the input and output side filter capacitors.**

## I. Introduction

About 45 % of the world's total electricity ultimately drives electric motors [1], which underlines the need for high efficiency variable speed drives (VSD) systems. Commonly, VSDs employ AC-AC voltage-source converters (VSCs), whose efficiency can be improved by replacing silicon IGBTs with wide-bandgap (WBG) power semiconductors. The associated steeper slopes of the switched inverter output voltages, however, exacerbate issues such as transient overvoltages at the motor terminals resulting from impedance mismatches in case of long motor cables, common-mode ground currents that can damage motor bearings, and radiated electromagnetic emissions which necessitate the use of expensive shielded motor cables [2]. On the other hand, the high switching-frequency capability of WBG devices facilitates integrating relatively compact LC output filters into VSCs, and, nevertheless, higher system-level efficiencies, also because sinusoidal output voltages result in a reduction of harmonic motor losses [3]–[5].

As an alternative, current-source AC-AC converters (CSCs, see **Fig. 1a**) inherently feature continuous output voltages. However, the DC link inductor has often been considered prohibitively bulky for low-power (kilowatts range) VSD applications. WBG devices facilitate higher switching frequencies that change this notion [6]–[8]. A further reduction of switching losses and hence increase of efficiency or switching frequency can be achieved with so-called two-third pulse-width modulation (PWM) that has been proposed for AC-DC or DC-AC current-source rectifiers (CSRs) and inverters (CSIs) [9]–[13]. Considering, e.g., a battery-supplied DC-AC CSI [8], [12], the necessarily present DC-side voltage-

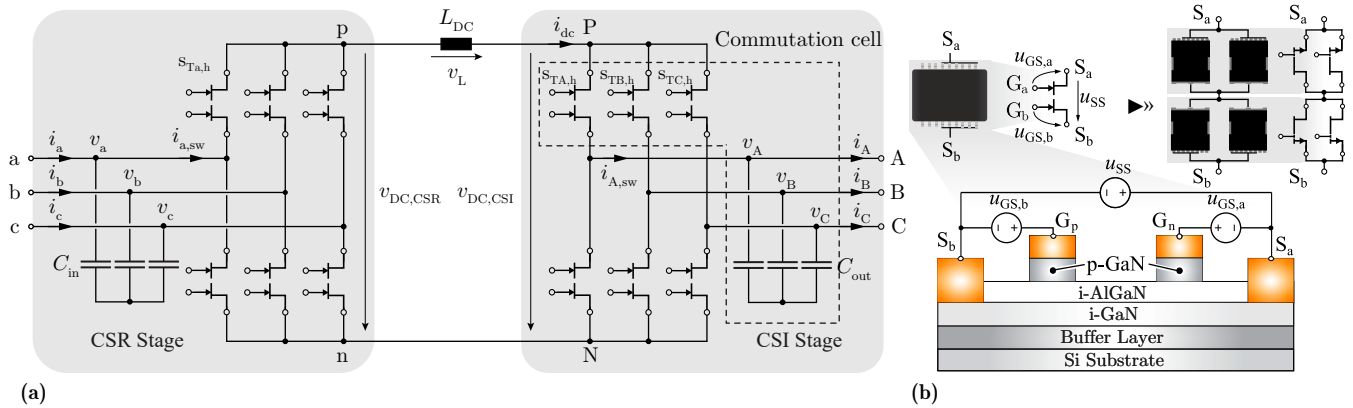


**Fig. 1. (a)** AC-AC CSC with AC-side filter capacitors (DM and CM EMI filter stages not shown). **(b)** Realization of a bidirectional switch (BDS) with four discrete unipolar GaN devices to achieve equal total on-state resistance as for a single unipolar device, and alternative realization as a dual-gate GaN monolithic BDS (M-BDS) with a shared drain-gate region for blocking either voltage polarity and accordingly substantially lower chip area.

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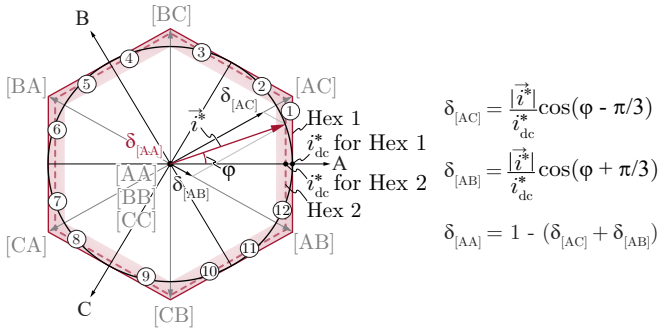


**Fig. 2.** Exemplary space vector diagram for a CSI stage with exemplary equations of the dwell times needed to synthesize the exemplary reference current vector $\vec{i}^*$. In case of 2/3-PWM, the shaping of the DC-link current $i_{dc}$ corresponds to a continuous scaling of the hexagon spanned by the space vectors such that its perimeter always coincides with the trajectory of the reference current vector $\vec{i}^*$.

to-current conversion stage (i.e., a buck converter) shapes the DC-link current such that the CSI can always clamp the phase with the highest current while only the two other phases need to operate with PWM ("2/3- PWM") in order to realize sinusoidal motor currents, resulting in a corresponding reduction of switching losses. Following this basic concept, we propose a synergetic control of an AC-AC CSC's CSR and CSI stages[1](cf. **Section II**) such that always one of the two stages operates with 2/3-PWM and the other stage is used for shaping the DC-link current.

Still, CSCs require switches with bipolar blocking voltage capability. If realized from available devices such as MOSFETs, this implies a factor of four penalty in terms of chip area required for comparable conduction and/or on-state voltage characteristics, see **Fig. 1b**. Research on *monolithic* bidirectional switches (M-BDSs), specifically on planar GaN M-BDSs, carried out over the past decade [14]–[17] has recently lead to industrial 1st generation samples of a 600 V, 140 mΩ GaN M-BDS [18], which almost completely eliminates this structural drawback of the CSC. The GaN M-BDS has already been applied in T-Type bridge-legs [19], but could also advantageously be employed in AC-AC CSC VSDs, for example in servo drive or HVAC applications, operating from a 200 V three-phase mains as used in Japan or in the U.S.A. Therefore, **Section III** provides calorimetric switching loss measurements of this M-BDS in a CSC commutation cell, and a model to account for the loss contributions caused by the third, passive, i.e., turned-off, switch present in a commutation cell of a CSC.

This lays the basis for **Section IV**, where we first quantify the performance improvement achieved by the proposed synergetic control of an AC-AC CSC compared to conventional operation with constant DC-link current. Second, we determine the achievable performance of an AC-AC CSC motor drive employing novel 600 V, 140 mΩ GaN M-BDSs in terms of AC-AC semiconductor efficiency and switching frequency. **Section V** concludes the paper with summarizing the main findings.

[1]Note that the denominations "CSR stage" and "CSI stage" are chosen for clarity and reflect the respective functions for power flow from the mains to the motor; however, the AC-AC CSC is a fully bidirectional system and thus the roles of the CSR and the CSI stages can change, e.g., for feeding power back to the grid during braking operation.

## II. Synergetic Control of AC-AC CSCs

**Fig. 1a** shows the analyzed three-phase AC-AC CSC, i.e., a back-to-back configuration of a grid-side CSR and a motor-side CSI that generates a three-phase output voltage system $v_{A,B,C}$ of variable amplitude and frequency, e.g., to drive a permanent-magnet synchronous motor (PMSM). The modulation index of the CSR and the CSI are defined as $m_r = \hat{I}_g/i_{dc}$ and $m_i = \hat{I}_m/i_{dc}$ respectively, where $i_{dc}$ is the DC-link current, and $\hat{I}_g$ and $\hat{I}_m$ are the amplitudes of the grid and motor phase currents. For the typical case of unity power factor at the grid and at the motor interface (typical for PMSMs), the relationship $V_m = m_r/m_i \cdot V_g$ follows from the input/output power balance, where $V_g$ and $V_m$ are the grid and motor line-to-line rms voltages. With $m_r, m_i \in [0, 1]$, the motor voltage can thus be smaller (buck operation) or larger (boost operation) than the grid voltage.

Conventionally, AC-AC CSCs operate with a constant DC-link current $i_{dc} = I_{dc}$, which, e.g., is maintained by the CSR stage while the CSI stage generates the required sinusoidal output currents $i_A$, $i_B$, and $i_C$ [6]. The minimum DC-link current is given by the highest peak value of the input and output phase currents. Considering, e.g., the CSI stage and **Fig. 2**, synthesizing a desired AC current vector $\vec{i}^*$ requires the use of the two neighboring space vectors ([AB] and [AC] for the example shown in the figure) but also of the freewheeling state ([AA]) within each switching period.[2] This implies that all three switches of a commutation cell must operate with PWM to achieve the desired sinusoidal output current. Therefore, this modulation method that is necessary in case of constant DC-link current is referred to as "3/3-PWM".

For AC-DC or DC-AC applications that feature a CSR or a CSI stage and a DC-DC converter stage to provide the necessary current-to-voltage conversion, synergetic control of the CSR or the CSI and the DC-DC stage has been described in literature as early as 2005 [9] and then later in [10]–[13]. Essentially, the DC-DC stage shapes (controls) the DC-link current such that it equals the maximum absolute value of the three-phase current references. Therefore, at any given instant the phase defining the DC current reference (i.e., the phase with the highest current) can be clamped to either the positive or the negative DC rail, directly impressing the correctly shaped DC-link current into that phase. The other commutation cell then switches only between the two remaining phases to shape the corresponding phase currents appropriately ("2/3-PWM"), instead of switching between all three phases as in 3/3-PWM. In terms of space-vector modulation, the shaping of the DC-link current can be understood as a continuous scaling of the hexagon spanned by the available space vectors such that its perimeter coincides with the circular trajectory of the reference phase current space vector $\vec{i}^*$ [12]. Hence, $\vec{i}^*$ can be generated without using freewheeling states, which avoids the corresponding switching transitions. Operating a CSR or a CSI with 2/3-PWM thus reduces its switching losses by at least 33 % (and considering the time-variation of the switched

[2]Applying only active vectors such as [AB] or [AC] facilitates reaching all points on the hexagon's perimeter; however, sinusoidal currents imply that $\vec{i}^*$ follows a circular trajectory and hence generally does not extend all the way to that perimeter. Thus, the freewheeling state is mandatory to adjust the length of $\vec{i}^*$ accordingly.

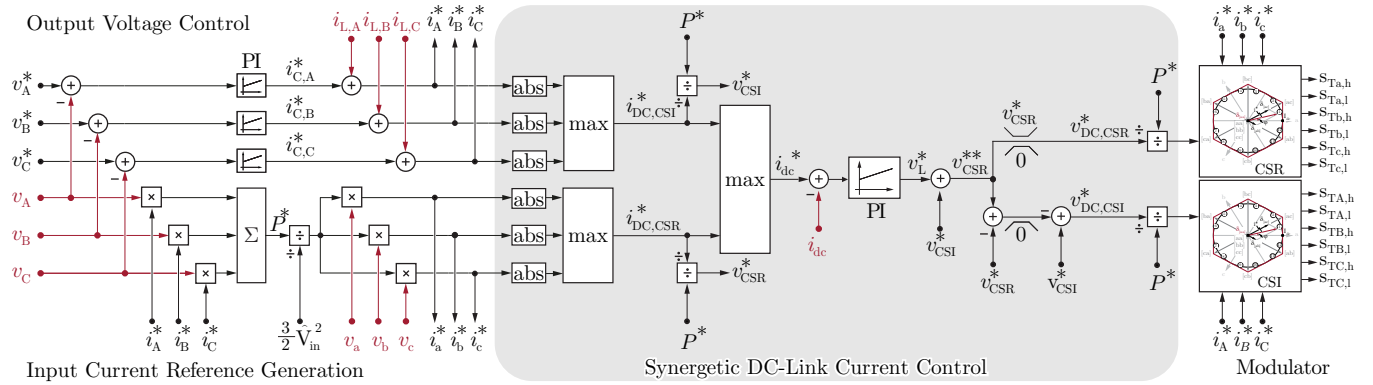


**Fig. 3.** Proposed synergetic DC-link current control of an AC-AC CSC as shown in **Fig. 1**. If the motor voltages are lower than the grid voltages (buck operation), the CSR stage operates with conventional 3/3-PWM and shapes the DC-link current to facilitate 2/3-PWM of the CSI stage, resulting in lower switching losses. Conversely, for boost operation, the CSI stage is employed for shaping the DC-link current and the CSR stage accordingly operates with 2/3-PWM. The depicted synergetic control structure furthermore achieves a seamless transition between these two cases, e.g., during acceleration of the motor from standstill and correspondingly increasing motor voltages. Note that all voltages and currents are local (over one switching period) average values. The shown generation of the six AC current references, which are inputs to the synergetic DC-link current controller, is an example only; additional outer control loops for motor speed and torque are not shown.

voltages for the typical case of near unity power factor by up to 83 % [12]). Since the shaped DC-current is always exactly as high as needed (and not higher), the conduction losses are furthermore reduced by about 8 % compared to operation with the minimum possible constant DC current.

### A. Proposed Synergetic Control of AC-AC CSCs

In the following, we propose a synergetic control method for AC-AC CSCs that facilitates 2/3-PWM for either the CSI or the CSR stage at all times. **Fig. 3** shows the control block diagram. As discussed above, the DC-link currents that would result in 2/3-PWM of the CSR or the CSI stage are

$$i^*_{\mathrm{DC,CSR}} = \max\left\{|i^*_{\mathrm{a}}|, |i^*_{\mathrm{b}}|, |i^*_{\mathrm{c}}|\right\}, \text{and} \tag{1}$$

$$i^*_{\mathrm{DC,CSI}} = \max\left\{|i^*_{\mathrm{A}}|, |i^*_{\mathrm{B}}|, |i^*_{\mathrm{C}}|\right\}, \tag{2}$$

where $i^*_{\mathrm{a,b,c}}$ and $i^*_{\mathrm{A,B,C}}$ are the grid-side and the motor-side phase current references, respectively. These phase current references are generated by application-specific outer control loops; **Fig. 3** shows a basic example featuring output voltage control and resistive mains behavior. As in general $i^*_{\mathrm{DC,CSR}} \neq i^*_{\mathrm{DC,CSI}}$, the common DC-link current reference must be selected as

$$i^*_{\mathrm{dc}} = \max\left\{i^*_{\mathrm{DC,CSR}}, i^*_{\mathrm{DC,CSI}}\right\}. \tag{3}$$

This forms the basis of the proposed synergetic control. Thus, in buck operation (motor voltage lower than grid voltage), we have $i^*_{\mathrm{DC,CSI}} > i^*_{\mathrm{DC,CSR}}$ and hence $i^*_{\mathrm{dc}} = i^*_{\mathrm{DC,CSI}}$; the CSI stage operates with 2/3-PWM whereas the CSR stage operates with 3/3-PWM and shapes the DC-link current. Similarly, in boost operation (motor voltage higher than grid voltage), the CSR stage operates with 2/3-PWM. The proposed synergetic control thus facilitates 2/3-PWM operation of always one of the CSC's two stages, and a seamless transition between buck and boost mode, i.e., a seamless exchange of the two stages' roles as facilitator or beneficiary of 2/3-PWM. With respect to **Fig. 3**, this is explained in detail in the following.

The DC-link current reference $i^*_{\mathrm{dc}}$ from (3) is compared against the measured DC-link current $i_{\mathrm{dc}}$ and the resulting error signal fed to a DC-link current controller to determine the inductor voltage reference $v^*_{\mathrm{L}}$ needed to adjust the current in the DC-link inductor. Further, the DC-side reference voltages $v^*_{\mathrm{CSR}}$ of the CSR and $v^*_{\mathrm{CSI}}$ of the CSI are obtained from the respective DC-link current references $i^*_{\mathrm{DC,CSR}}$ and $i^*_{\mathrm{DC,CSI}}$ and the output power reference $P^*$ as

$$v^*_{\mathrm{CSR}} = \frac{P^*}{i^*_{\mathrm{DC,CSR}}} \quad \text{and} \quad v^*_{\mathrm{CSI}} = \frac{P^*}{i^*_{\mathrm{DC,CSI}}}, \tag{4}$$

i.e., these are the DC-side voltages that would correspond to 2/3-PWM operation of the corresponding stage.

The core mechanism of the synergetic control then calculates the virtual reference voltage $v^{**}_{\mathrm{CSR}} = v^*_{\mathrm{CSI}} + v^*_{\mathrm{L}}$, i.e., the DC-side voltage that the CSR stage would need to generate such that the CSI stage could operate with 2/3-PWM (i.e., with $v^*_{\mathrm{CSI}}$ on its DC-side) *and* the required $v^*_L$ would be applied to the DC-link inductor. If $v^{**}_{\mathrm{CSR}} < v^*_{\mathrm{CSR}}$ (assuming $v^*_{\mathrm{L}}$ to be small, this corresponds to $v^*_{\mathrm{CSI}} < v^*_{\mathrm{CSR}}$ and, equivalently, $i^*_{\mathrm{DC,CSI}} > i^*_{\mathrm{DC,CSR}}$, i.e., buck operation), the limiter in the upper signal path is not clamping, the CSR stage receives $v^*_{\mathrm{DC,CSR}} = v^{**}_{\mathrm{CSR}}$ (and hence operates with 3/3-PWM, since the actual current reference to the CSR modulator is higher than $i^*_{\mathrm{DC,CSR}}$). The lower signal path ensures that $v^*_{\mathrm{DC,CSI}} = v^*_{\mathrm{CSI}}$, which implies that the DC-link current reference sent to the modulator of the CSI stage is $i^*_{\mathrm{DC,CSI}}$ and the CSI hence *automatically* operates with 2/3-PWM. Similarly, if $v^{**}_{\mathrm{CSR}} > v^*_{\mathrm{CSR}}$ (again assuming $v^*_{\mathrm{L}}$ to be small, this corresponds to $v^*_{\mathrm{CSI}} > v^*_{\mathrm{CSR}}$ and, equivalently, $i^*_{\mathrm{DC,CSI}} < i^*_{\mathrm{DC,CSR}}$, i.e., boost operation), the limiter in the upper signal path clamps $v^*_{\mathrm{DC,CSR}} = v^*_{\mathrm{CSR}}$ and consequently the CSR stage operates with 2/3-PWM. To still apply the required $v^*_{\mathrm{L}}$ to the DC-link inductor, the CSI stage's DC-side voltage must be adjusted according to $v^*_{\mathrm{DC,CSI}} = v^*_{\mathrm{CSR}} - v^*_{\mathrm{L}}$, which is ensured by the lower signal path,

$$v^*_{\mathrm{DC,CSI}} = v^*_{\mathrm{CSI}} - \left[v^*_{\mathrm{L}} + v^*_{\mathrm{CSI}} - v^*_{\mathrm{CSR}}\right] = v^*_{\mathrm{CSR}} - v^*_{\mathrm{L}}.$$

Consequently, the CSI stage operates with 3/3-PWM and shapes the DC-link current such that the CSR stage can operate with 2/3-PWM. Based on the DC-link current references generated by the synergetic control and the grid- and motor-side phase current references obtained by application-specific outer control loops, the dedicated CSR and CSI modulators calculate the respective duty-cycles of all the switches, as

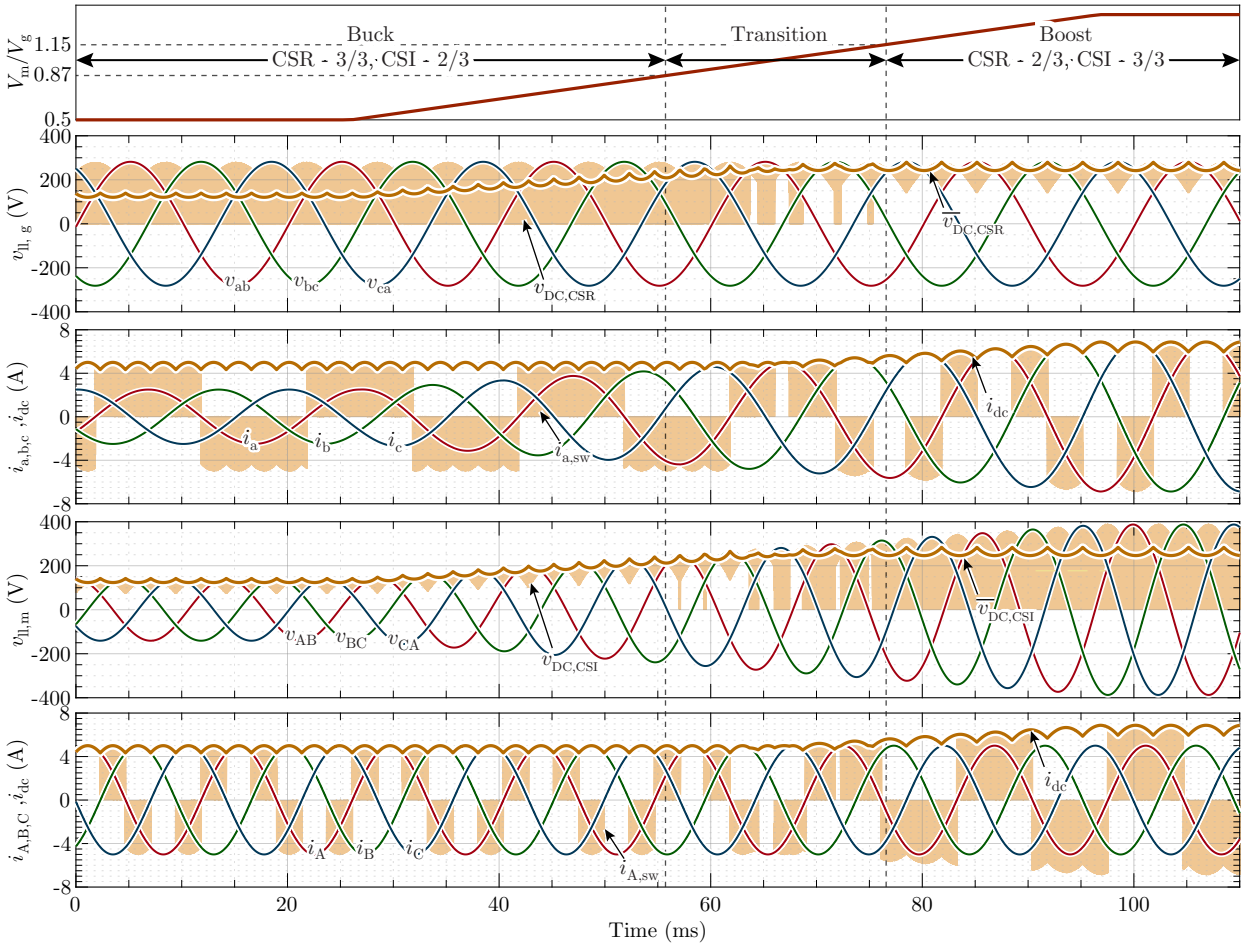


**Fig. 4.** Simulated waveforms of an AC-AC CSC (cf. **Fig. 1a**) employing the proposed synergetic control (cf. **Fig. 3**) and exemplary parameters $V_g = 200\,\text{V}$, $f_g = 50\,\text{Hz}$, $\hat{I}_m = 5\,\text{A}$, $f_m = 70\,\text{Hz}$. The output voltage $V_m$ varies between $100\,\text{V}$ and $400/\sqrt{2}\,\text{V}$. For $V_m \leq \sqrt{3}/2 \cdot V_g$, the CSI operates with 2/3-PWM and the CSR with 3/3-PWM, shaping the DC-link current. For $V_m \geq 2/\sqrt{3} \cdot V_g$, the CSR operates with 2/3-PWM and the CSI with 3/3-PWM, shaping the DC-link current. Note the absence of freewheeling states in either $v_{DC,CSI}$ or $v_{DC,CSR}$, i.e., in the switched DC-side voltages, and the continuous transition from buck to boost mode.

shown in **Fig. 2** for an example of sector 1 and 12. Thus, the obtained $i^*_{dc}$ for 2/3-PWM automatically results in the sum of the active vectors' duty cycles being equal to 1 and thus forcing the duty cycle of the zero vector to be 0, hence achieving the desired 2/3-PWM operation.

### *B. Simulation Results*

**Fig. 4** shows simulated waveforms of the proposed synergetic control of an exemplary AC-AC CSC with $V_g$ and output RMS current $I_m$ fixed at $200\,\text{V}$ and $3.5\,\text{A}$, respectively. The CSC operates in buck mode with $V_m = 100\,\text{V}$ until $t = 26\,\text{ms}$. Therefore, $i^*_{dc}$ is maintained equal to $i^*_{DC,CSI}$, resulting in 2/3-PWM of the CSI stage and 3/3-PWM of the CSR stage. This is reflected by the absence of freewheeling states in the simulated DC-link voltage waveform $v_{DC,CSI}$ of the CSI stage as well as by the switched current $i_{A,sw}$ of the CSI's phase A, respectively. As a result of the elimination of freewheeling states for 2/3-PWM of the CSI stage, $v_{DC,CSI}$ does never hit zero but attains only two of the three line-to-line voltages $|v_{xy}|$ and $|v_{yz}|$, where $y$ refers to the phase with the highest absolute value of phase current and $x, z$ to remaining two phases. Similarly, the switches $s_{TA,h}$ and $s_{TA,l}$ of the CSI's phase A are not switched when $|i_A| > \max\{|i_B|, |i_C|\}$, resulting in $|i_{A,sw}| = i_{dc}$ during this time interval.

To demonstrate the seamless transition from buck to boost mode, $V_m$ is ramped from $100\,\text{V}$ to $400/\sqrt{2}\,\text{V}$. The CSI stage operates with 2/3-PWM and the CSR with 3/3-PWM as long as $V_m \leq \sqrt{3}/2\ V_g$ applies. Once this threshold is crossed, the CSR and the CSI stage interchangeably operate with 2/3-PWM and 3/3-PWM, depending on the instantaneous value of $\max\{i_{a,b,c}(t), i_{A,B,C}(t)\}$. This demonstrates a seamless transition from buck to boost mode, which is ultimately entered once $V_m \geq 2/\sqrt{3}\ V_g$ is reached. Even though for the sake of clarity we only show the typical case of unity power factor operation of both, the CSR and the CSI stage, the proposed synergetic control also works in case of non-zero phase-shifts between currents and voltages at the input and/or at the output side.

## III. Characterization of Novel GaN M-BDS in a CSC Commutation Cell

To quantify the performance improvement of an AC-AC CSC obtainable with synergetic control, we consider a recently available 1st generation $600\,\text{V}, 140\,\text{m}\Omega$ GaN M-BDS [18], [19]. The switching losses of the novel M-BDS must be measured in a realistic CSC commutation cell configuration as highlighted in **Fig. 1a** and shown in detail in **Fig. 5a**. The commutation cell consists of *three* switches (instead of two

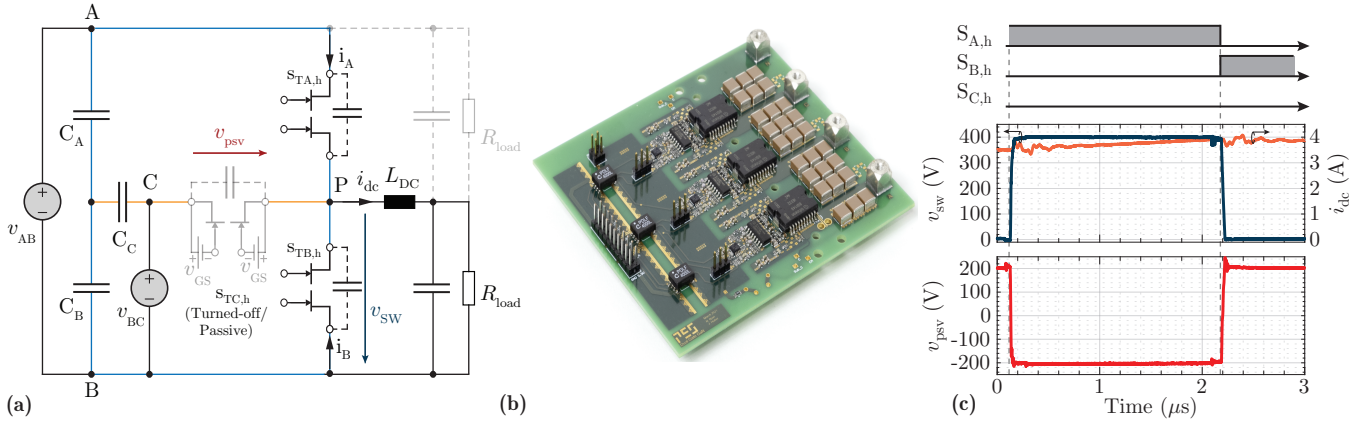


**Fig. 5.** **(a)** One commutation cell of the AC-AC CSC shown in **Fig. 1a** consisting of three M-BDSs, the AC-side filter capacitors and the (DC-link) inductor. The load connection and polarity of $v_{AB}$ is changed to characterize the M-BDS in all four quadrants. During a switching transition, two switches are actively switched ($S_{TA,h}$ and $S_{TB,h}$ in **(c)**) and the third switch ($S_{TC,h}$ in **(c)**) is inactive, i.e., passively "switched" as both gates are turned-off with a negative gate-source voltage. **(b)** Hardware implementation of the commutation cell used to evaluate the performance of the 600 V, 140 mΩ GaN M-BDS. **(c)** Measured switch-node voltage $v_{sw}$, inductor (DC-link) current $i_{dc}$, and voltage across the passive switch $v_{psv}$ for $v_{AB} = 400\,\text{V}$, $v_{BC} = 200\,\text{V}$ and $\bar{i}_{dc} = 4\,\text{A}$.

as in half-bridges of VSCs) that are connected to a common switched node, i.e., the DC-link terminal marked P in the commutation cell highlighted in **Fig. 1a**, and the respective output phases A, B and C. Owing to the symmetry of operation between the four commutation cells of the AC-AC CSC, it is sufficient to analyze one such commutation cell in detail.

### *A. Calorimetric Switching Loss Measurements*

As a first step, two of the commutation cell's three switches were mounted on a developed characterization PCB (see **Fig. 5b**). The circuit diagram with only two switches ($S_{TA,h}$ and $S_{TB,h}$) of the commutation cell is equivalent to a half-bridge circuit as shown in **Fig. 5a** (the components marked $C_C$, $v_{BC}$ and $S_{TC,h}$, are not placed on the PCB for the first characterization measurements). The half-bridge switching losses are measured with an accurate transient calorimetric method that furthermore allows the simultaneous measurement of the individual losses of $S_{TA,h}$ and $S_{TB,h}$, i.e., a separation of total switching losses into hard- and soft-switching losses. For the sake of brevity, we refer to [19] for a detailed description of the method.

**Fig. 6** shows the thus measured switching losses in dependence of switched current and voltage (including a linear fit) for operation of the M-BDS half-bridge with current-based 4-step commutation sequences, which are necessary to ensure that there is always a path for the (DC-link) inductor current without short-circuiting any of the capacitors. As the line-to-line voltage is switched by a CSC commutation cell, i.e., an AC voltage, the M-BDSs operate in all four quadrants of the voltage-current plane. For an exemplary operating point with a switched voltage of ±400 V and a switched current of ±4 A, **Fig. 6** indicates similar losses in all for quadrants.

### *B. Modeling of Loss Contribution of Passive Switch*

Since a CSC commutation cell consists of three switches, during a switching transition between the two switches actively performing the commutation, the blocking voltage across the output capacitance $C_{oss}$ of the third (turned-off) switch is forced to change as well. **Fig. 5a** shows the equivalent circuit of a commutation cell with all three switches. $S_{TA,h}$ and $S_{TB,h}$ are actively involved in the commutation, whereas $S_{TC,h}$ is

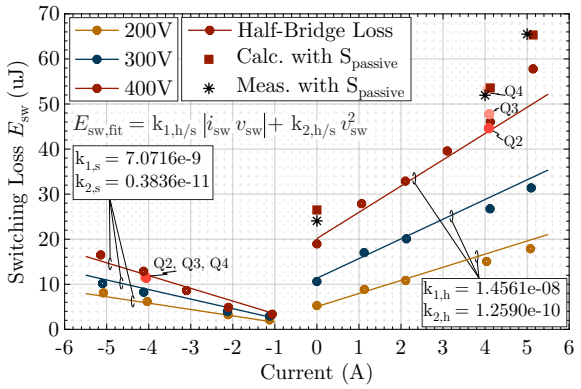


**Fig. 6.** Calorimetrically measured switching loss energies of a GaN M-BDS half-bridge in dependence of switched current and voltage. Note that due to the four-step commutation required for CSCs, switching energies are not directly comparable to those specified for unipolar devices in a half-bridge configuration. Furthermore, the fitted loss model used for semiconductor loss calculations is given. For an exemplary case of 400 V and 4 A, the measured losses for operating the M-BDS in all four quadrants of the voltage/current plane indicate similar behavior. Finally, the proposed modeling of the additional loss contribution caused by the presence of the commutation cell's third passive switch is verified by measurements.

passively "switched". **Fig. 5c** shows the measured switch-node voltage $v_{sw}$, (DC-link) current $i_{dc}$, and the voltage across the passive switch $v_{psv}$ during the commutations between $S_{TA,h}$ and $S_{TB,h}$ for $v_{AB} = 400\,\text{V}, v_{BC} = 200\,\text{V}$ and $i_{dc} = 4\,\text{A}$. For the given current direction, $S_{TA,h}$ and $S_{TB,h}$ experience hard- and soft-switching, respectively. With the given configuration, $v_{sw}$ toggles between 0 V and 400 V and $v_{psv}$ between −200 V and 200 V. The corresponding current flow through the passive switch's $C_{oss}$ causes losses that are mainly dissipated in the half-bridge switch that is hard turned-on (similar as in T-type bridge legs [20]). The additional losses due to the passive switch $E_{psv}$ can be estimated based on the energy balance between the beginning and the end of a switching transition [21] and using datasheet values of the charge $Q_{oss}(\text{V})$ and energy $E_{oss}(\text{V})$ stored in $C_{oss}$; for identical polarities of $v_{psv,0}$ and $v_{psv,1}$ with

$$E_{psv}(v_{psv,0}, v_{psv,1}) = \big(Q_{oss}(v_{psv,1}) - Q_{oss}(v_{psv,0})\big)\, v_{psv,1} - \big(E_{oss}(v_{psv,1}) - E_{oss}(v_{psv,0})\big) \quad (5)$$

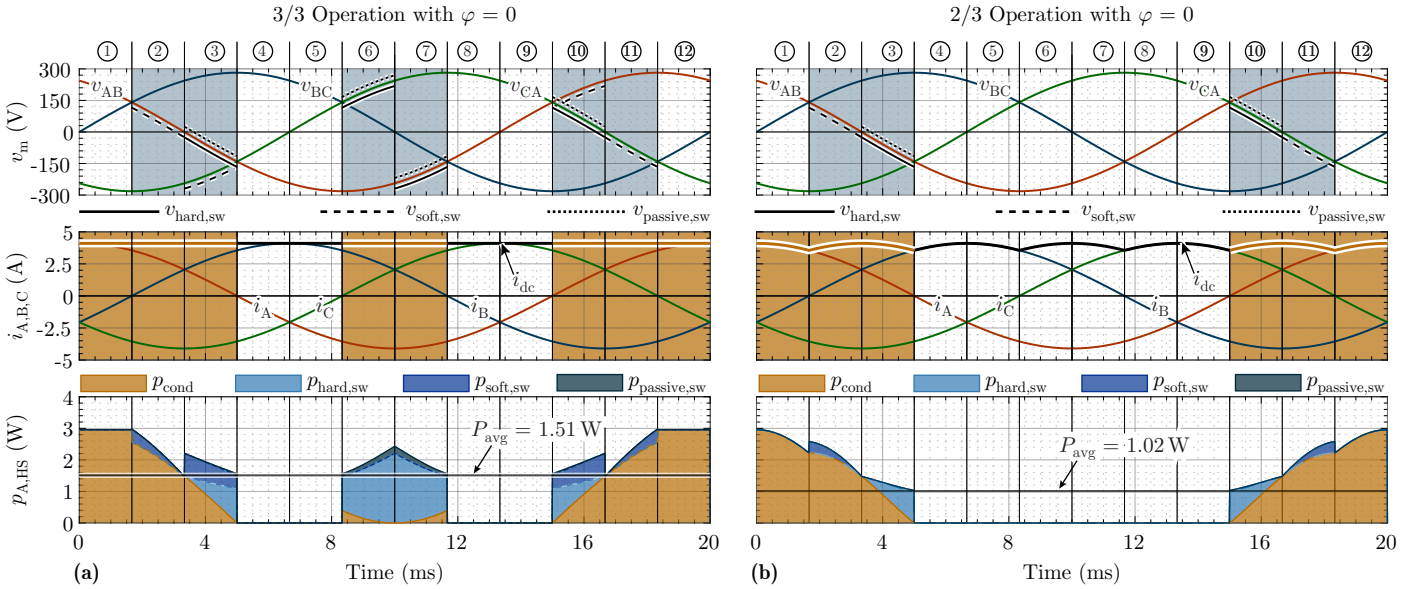


**Fig. 7.** Loss components of $S_{TA,h}$, i.e., the high-side transistor of the CSI's phase A, over a fundamental period for **(a)** 3/3-PWM and **(b)** 2/3-PWM for an exemplary operating point with $V_m = 200\,V$, $\hat{I}_m = 4\,A$, and a switching frequency of 100 kHz. Note especially the absence of switching losses in sectors 6 and 7 in case of 2/3-PWM, i.e., in the region with the highest phase current magnitude and also the highest switched line-to-line voltage in case of 3/3-PWM.

and for opposite polarities of $v_{psv,0}$ and $v_{psv,1}$ with

$$E_{psv}(v_{psv,0}, v_{psv,1}) = \big(Q_{oss}(v_{psv,1}) + Q_{oss}(v_{psv,0})\big)\, v_{psv,1} - \big(E_{oss}(v_{psv,1}) - E_{oss}(v_{psv,0})\big)\,. \quad (6)$$

$v_{psv,0}$ and $v_{psv,1}$ are the voltages across the passive switch before and after the switching transition, respectively.

The modeling of the additional loss contribution caused by the presence of the third, passive switch was experimentally verified by mounting the third switch on the characterization PCB and measuring the half-bridge switching loss with the same operating parameters as without the passive switch. The comparison of the additional losses estimated theoretically based on (5) and (6) with measured values is summarized in **Fig. 5c** and indicates an estimation error of less than 10 %.

## IV. Performance Evaluation

The detailed characterization of the novel M-BDSs in a CSC commutation cell enables a quantification of the achievable performance of an AC-AC CSC equipped with these novel devices and, in addition, of the improvements resulting from the proposed synergetic control. When the CSI stage in a motor drive operates with very low fundamental frequencies during startup, or even at standstill, the thermal inertia of the switches is not sufficient to average the time-varying losses over a fundamental period [22], i.e., the peak value of the losses defines the necessary cooling. It is therefore important to first analyze the time behavior of a transistor's loss components during a fundamental period. Considering a commutation cell with $i_{dc}$ flowing into the switch-node (cf. highlight in **Fig. 1a**), the switch $S_{Tx,h}$ or $S_{Tx,l}$ is soft-switched if the voltage of the phase connected to the switch-node prior to their respective turn-on is smaller than the corresponding phase voltage $v_x$, and hard-switched otherwise, where $x \in$ [a,A,b,B,c,C]. The hard- and soft-switching conditions reverse if $i_{dc}$ flows out of the switch-node. The loss contribution caused by the presence of the third, passive switch occurs in the switch that is hard turned-on. Based on these conditions, **Table I** lists the voltage and current values that give rise to the conduction and switching losses in $S_{TA,h}$ in the 12 sectors (see **Fig. 2**) of the fundamental period for 3/3-PWM and 2/3-PWM modulation, where

Table I
Loss components of switch $S_{TA,h}$ for $i_{dc}$ as defined in (7) for 3/3-PWM and 2/3-PWM, respectively, flowing into the switch-node.

| Sector | Conduction Loss 3/3 | Conduction Loss 2/3 | Switching Loss 3/3 | Switching Loss 2/3 |
|---|---|---|---|---|
| 1 | $i_{dc}$ | $i_{dc}$ | - | - |
| 2 | $\delta_{ac} \cdot i_{dc}$ | $\delta_{ac} \cdot i_{dc}$ | $E_s(i_{dc}, v_{BA})$ | $E_s(i_{dc}, v_{BA})$ |
| 3 | $\delta_{ac} \cdot i_{dc}$ | $\delta_{ac} \cdot i_{dc}$ | $E_h(i_{dc}, v_{BA})$, $E_s(i_{dc}, v_{CA})$, $E_{psv}(v_{CB}, v_{CA})$ | $E_h(i_{dc}, v_{BA})$ $E_{psv}(v_{CB}, v_{CA})$ |
| 4 | - | - | - | - |
| 5 | - | - | - | - |
| 6 | $\delta_{aa} \cdot i_{dc}$ | - | $E_h(i_{dc}, v_{CA})$ $E_{psv}(v_{BC}, v_{BA})$ | - |
| 7 | $\delta_{aa} \cdot i_{dc}$ | - | $E_h(i_{dc}, v_{BA})$ $E_{psv}(v_{CB}, v_{CA})$ | - |
| 8 | - | - | - | - |
| 9 | - | - | - | - |
| 10 | $\delta_{ab} \cdot i_{dc}$ | $\delta_{ab} \cdot i_{dc}$ | $E_h(i_{dc}, v_{CA})$ $E_s(i_{dc}, v_{BA})$ $E_{psv}(v_{BC}, v_{BA})$ | $E_h(i_{dc}, v_{CA})$ $E_{psv}(v_{BC}, v_{BA})$ |
| 11 | $\delta_{ab} \cdot i_{dc}$ | $\delta_{ab} \cdot i_{dc}$ | $E_s(i_{dc}, v_{CA})$ | $E_s(i_{dc}, v_{CA})$ |
| 12 | $i_{dc}$ | $i_{dc}$ | - | - |

$$i_{dc}(t) = \begin{cases} \max\left\{|i_A^*(t)|, |i_B^*(t)|, |i_C^*(t)|\right\} & \text{for 2/3-PWM} \\ \hat{i}_A^* = \hat{i}_B^* = \hat{i}_C^* = const. & \text{for 3/3-PWM} \end{cases}. \quad (7)$$

$E_h, E_s$ refer to hard- and soft-switching energies, respectively. **Fig. 6** gives the corresponding loss model for the considered M-BDSs. $E_{psv}$ is calculated with (5) and (6). $\delta_{xy}$ denotes the relative dwell time of the space vector (switching state) [xy].

**Fig. 7** visualizes these loss components of $S_{TA,h}$ for 3/3-PWM and 2/3-PWM and an exemplary operating point. The benefit of 2/3-PWM modulation is directly evident from the absent losses in sectors 6 and 7 (for 3/3-PWM, losses occur due to free-wheeling of $i_{dc}$ through $S_{TA,h}$ for $i_A < \{i_B, i_C\}$, while switching the highest line-line voltage $v_{ca}$ in sector 6

and $v_{ab}$ in sector 7) and slightly lower losses in the other sectors. For the selected operating point ($V_m = 200\,V$, $\hat{I}_m = 4\,A$) and a switching frequency of $f_{sw} = 100\,kHz$, the peak losses are roughly the same for 3/3-PWM and 2/3-PWM. This, however, would change for higher switching frequencies that would increase the switching losses in sectors 6 and 7 in case of 3/3-PWM.

In contrast, the average losses over the fundamental period with 3/3-PWM are $P_{avg,3/3} = 1.51\,W$ ($P_{sw,avg,3/3} = 0.53\,W$ and $P_{cond,avg,3/3} = 0.98\,W$), whereas with 2/3-PWM, the total average losses are only $P_{avg,2/3} = 1.02\,W$, i.e., only 67.5 % of $P_{avg,3/3}$. The switching losses reduce to $P_{sw,avg,2/3} = 0.12\,W$ (22 % of $P_{sw,avg,3/3}$) and the conduction loss to $P_{cond,avg,2/3} = 0.86\,W$ (91.4 % of $P_{cond,avg,3/3}$).

Considering the switching-loss-optimal space vector modulation that ensures that always only the lowest of the two line-to-line voltages is switched [6], both, the CSR and the CSI stage will each have two hard-switching and two soft-switching transitions within a switching period when operating with 3/3-PWM and only one hard-switching and one soft-switching transition when operating with 2/3-PWM. Owing to the symmetry within sectors, the average total switching losses of all six transistors of either the CSR or the CSI stage operating with 3/3-PWM can be calculated with

$$E_{sw,3/3} = \frac{12}{2\pi}\int_0^{\frac{\pi}{6}} \left[E_{sw}(i_{DC}, v_{AB}) + E_{sw}(i_{DC}, v_{BC})\right] d\phi = \frac{3\hat{V}_{LL}}{\pi}\cdot\left[k_{1x} I_{DC} + k_{2x}\hat{V}_{LL}\cdot\frac{4\pi - 3\sqrt{3}}{12}\right] \quad (8)$$

and for 2/3-PWM operation with

$$E_{sw,2/3} = \frac{12}{2\pi}\int_0^{\frac{\pi}{6}} E_{sw}(i_{DC}, v_{BC})\, d\phi = \frac{3\hat{V}_{LL}}{\pi}\cdot\left[\frac{k_{1x}\hat{i}}{4} + k_{2x}\hat{V}_{LL}\cdot\frac{2\pi - 3\sqrt{3}}{12}\right], \quad (9)$$

where $k_{nx} = (k_{n,h} + k_{n,s})$ with $n \in [1, 2]$.

As a first step towards the dimensioning of an AC-AC CSC system employing the novel GaN M-BDSs and the proposed synergetic control, we evaluate the maximum feasible DC-link current that is limited by the design junction temperature $T_j = 100\,°C$, which includes a certain margin for overload and standstill operation of the drive, where, instead of average losses, peak losses during a fundamental period will define the switch temperature rise [22] (see, e.g., $t = 0$ in **Fig. 7**). Furthermore, we consider a thermal resistance from the devices' junctions through the PCB (bottom-cooled packages) to the heatsink of $R_{j,hs} = 6.6\,K/W$ and a heatsink temperature of $T_{hs} = 80\,°C$. **Fig. 8** shows the individual maximum DC-link current limits $\hat{i}_{dc,lim}$ of the CSR and the CSI for $f_{sw}$ between 48 kHz and 288 kHz in dependence of $V_m$. During buck operation (i.e., $V_m \lessapprox 200\,V = V_g$), the CSR operates with 3/3-PWM and the CSI with 2/3-PWM. Because $P_{avg,3/3} > P_{avg,2/3}$, the $\hat{i}_{dc,lim}$ that ensures $T_j < 100\,°C$ for all switches is lower for the CSR. Similarly, for boost operation, $\hat{i}_{dc,lim}$ of the CSI is lower than that of the CSR. The decrease of the CSI's $\hat{i}_{dc,lim}$ with $V_m$ directly reflects the impact of the increasing line-to-line voltage on the switching losses.

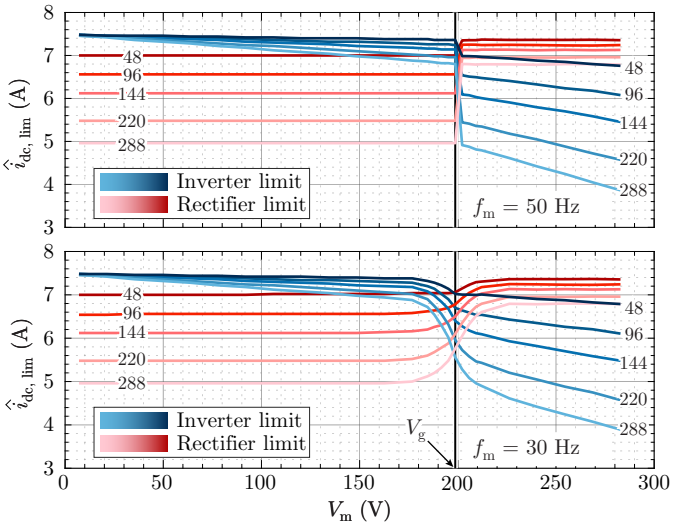


**Fig. 8.** Maximum DC-link current limited by $T_j \leq 100\,°C$ (heatsink temperature $T_{hs} = 80\,°C$) for the CSR and the CSI in dependence of $V_m$ and for different switching frequencies. For $V_m < V_g$ (buck operation), the CSI operates with 2/3-PWM whereas the CSR operates with 3/3-PWM and vice-versa for $V_m > V_g$ (boost operation). The CSR and the CSI operate partly with 2/3-PWM and 3/3-PWM in the transition region with $V_m \approx V_g$; the transition region becomes wider in case $f_m \neq f_g$.

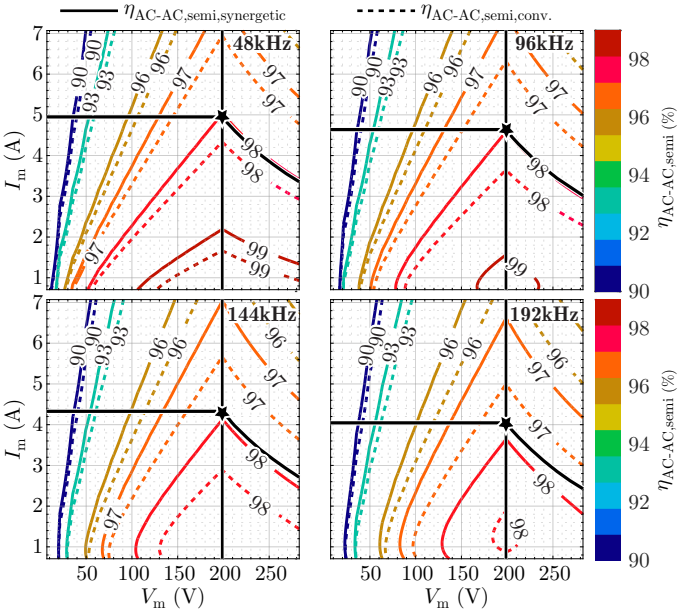


**Fig. 9.** Semiconductor AC-AC efficiency characteristics of a CSC motor drive employing the novel GaN M-BDSs and operating with or without the proposed synergetic control at different switching frequencies. The thick black lines indicate the output rms current limits that ensure $T_j = 100\,°C$ and which are very similar for both cases, i.e., conventional control and the proposed synergetic control, because always the stage operating with 3/3-PWM limits the allowable current (see **Fig. 8**).

Regarding a motor drive, ultimately the coverage of the output current vs. output voltage plane is of interest, which follows from $\hat{i}_{dc,lim}$ discussed above. Therefore, **Fig. 9** shows the resulting allowable output rms current limit $I_m$ vs. $V_m$. The nominal power $P_{nom}$ is defined at $V_m = 200\,V$. Whereas this limit is independent of whether synergetic modulation is used or not (as always the stage operating with 3/3-PWM limits the DC-link current, see above), **Fig. 9** also shows a clear improvement of the AC-AC semiconductor efficiency $\eta_{AC-AC,semi}$ for all attainable operating points when the proposed synergetic

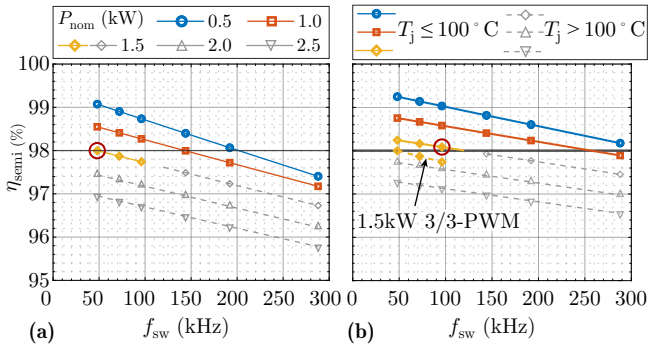


**Fig. 10.** AC-AC semiconductor efficiency of a CSC employing the novel GaN M-BDSs at different nominal power levels (nominal motor voltage $V_m$ = 200 V) in dependence of the switching frequency for **(a)** conventional and **(b)** the proposed synergetic control. Targeting an AC-AC semicondcutor efficiency at nominal power of $\eta_{AC-AC,semi} \approx 98\,\%$, the conventional control (const. DC-link current) facilitates $P_{nom} = 1.5\,kW$ at $f_{sw} = 48\,kHz$, whereas the proposed synergetic control enables twice the switching frequency, i.e., $f_{sw} = 96\,kHz$.

control is employed; this improvement becomes larger with increasing $f_{sw}$. This means that synergetic control enables either higher $\eta_{AC-AC,semi}$ for a given $P_{nom}$, or a higher $P_{nom}$ for a fixed target $\eta_{AC-AC,semi}$.

The latter is summarized in **Fig. 10**, which shows $\eta_{AC-AC,semi}$ at different $P_{nom}$ as a function of $f_{sw}$. The parts of the curves shown in gray indicate operating points that violate the thermal limit $T_j = 100\,°C$ discussed above. For a desired $\eta_{AC-AC,semi} \approx 98\,\%$, the conventional operation of an AC-AC CSC allows a maximum $P_{nom} = 1.5\,kW$ with $f_{sw} = 48\,kHz$. In contrast, the proposed synergetic control allows the same $P_{nom}$ but with $f_{sw} = 96\,kHz$, i.e., twice the $f_{sw}$, which translates into a smaller DC-link inductor and smaller EMI filter components.

## V. Conclusion

This paper proposes a synergetic control method for AC-AC current-source converters (CSCs), which considerably curtails switching losses by eliminating free-wheeling states of either the grid-side or the motor-side converter stage at all times. Further, novel monolithic bidirectional 600 V, 140 mΩ GaN transistors are characterized in a CSC commutation cell circuit configuration, and a model for the additional loss contributions occurring as a result of the presence of a third passive/inactive transistor connected to the commutation cell's switch-node is proposed and experimentally verified. The monolithic bidirectional switches (M-BDSs) and the proposed synergetic control enable an AC-AC CSC for 200 V motor drive applications with a nominal power of 1.5 kW and an AC-AC semiconductor efficiency of 98 % while operating with a switching frequency of 96 kHz. This is twice the switching frequency of 48 kHz that could be achieved without the proposed synergetic control under the same power and efficiency requirements.

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