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Abstract: **A wide output voltage range ($200-1000\,V_{DC}$) isolated two-stage three-phase EV charger is proposed. The system employs a boost-type two-level PFC rectifier front-end and the subsequent novel Hybrid Quantum Series Resonant DC/DC Converter (H-QSRC) output stage, which is left either unregulated with constant voltage transfer ratio or is used to emulate a buck or boost behavior. For reducing the H-QSRC voltage transfer ratio discretization, replacing one of the two-level primary side bridge-legs with a three-level T-type arrangement and a microscopic duty cycle operation are considered. The PFC rectifier stage is either operated in conventional boost-mode with two out of three phases switching ($^2/_3$-mode), or in $^1/_3$-mode. For $^1/_3$-mode, always the most positive and the most negative input phase are clamped to the positive and negative DC bus, and only the phase with the smallest voltage / current is switching, which minimizes switching losses. Different combinations of the operating modes of the PFC rectifier stage and the H-QSRC stage and the resulting current and voltage stresses on the main power components are analyzed. Furthermore, the best synergetic combination of the operating modes of both stages is identified for the different output voltage regions. Finally, a corresponding control structure, which achieves a smooth transition between all operating regimes is presented, and it is shown, that the extremely wide output voltage range can be covered without overdesign of any of the two converter stages.**

I. Introduction

The growing market of electric vehicles (EVs) calls for battery charging systems which are compatible with cars from different manufacturers, i.e. are able to cope with a wide output voltage range. **Fig. 1(a)** shows the operating range required for future high-power DC chargers which are typically realized following a modular approach, i.e. by combining sub-units of $10\,kW-20\,kW$ [1]. Each sub-unit should allow operation with battery voltages U_o between $200\,V$ and $1000\,V$, where for low voltage levels, the output current is limited to a certain maximum charging current, and for higher voltage levels, the battery is charged with constant output power, e.g. $10\,kW$. If the power is taken from the European three-phase LV grid with a line-to-line RMS voltage of $400\,V$, buck-boost capability of the charger is clearly required. Most state-of-the-art chargers consist of two stages [2,3], i.e. a boost-type two-level PFC rectifier is employed as grid interface in combination with a subsequent DC/DC converter to step down or further step up the constant DC link voltage. However, a constant DC link voltage limits the system efficiency for buck-mode operation (when U_o is lower than the maximum line-to-line voltage $u_{ll,max}$), because the PFC rectifier is boosting the voltage although step-down function of the overall system is required. If a small DC-link capacitor is employed, and the capacitor voltage is actively controlled by the DC/DC converter to follow the six-pulse shape of $u_{ll,max}$, $^1/_3$-modulation can be utilized, where only one instead of two bridge-legs ($^2/_3$-modulation) of the PFC rectifier stage is switched at a time [4], as shown in **Fig. 2(a.i) - (a.iii), (a.vii)**. Specifically, the upper switch of the bridge-leg with the most positive phase voltage and the lower switch of the bridge-leg with the most negative phase voltage are turned on continuously, while the sinusoidal shape of the input currents of the clamped phases is maintained by the pulsating DC link voltage, which in turn is controlled by the subsequent DC/DC converter. As a result, always only one PFC rectifier bridge-leg is operated with high-frequency PWM, whereby the switching losses can be reduced significantly, i.e. by more than 66% as the switched bridge-leg always carries the lowest phase current. A two-stage three-phase AC/DC converter system of this type is described in [4,5], but without considering galvanic insulation against the mains. Therefore, as isolation between the grid and the vehicle is mandatory for safety reasons, a bulky low-frequency (LF) transformer [6] would have to be employed. A more power-dense solution is to include isolation in the charger itself, i.e. to employ an isolated DC/DC converter stage. Resonant converters [7,8], as e.g., LLC converters, are typically used in such applications. However, with a wide output voltage range, the frequency variation required for resonant converters is significant, leading to limited conversion efficiency.

In this paper, a new type of series resonant DC/DC converter is used, which is referred to as the Hybrid Quantum Series Resonant Converter (H-QSRC), as shown in **Fig. 1(b)**. The resonant capacitor C_r is split among the primary and

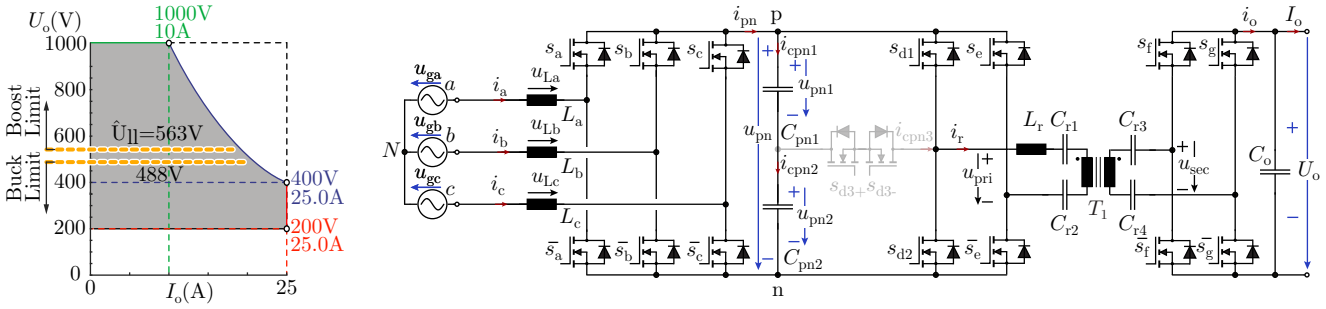

Fig. 1. (a) Battery voltage U_o and clamping current I_o range for a 10 kW module of a high-power DC electric vehicle (EV) charging system, **(b)** topology of the two-stage power circuit of the module comprising a PFC rectifier front-end and a full-bridge series resonant DC/DC converter (SRC) output stage. The SRC is always working at the resonant frequency and left uncontrolled or operating in buck or boost quantum (Q) mode. Furthermore, an extension of a primary side two-level bridge-leg into a three-level T-type bridge-leg is considered for improving the voltage control capability and lowering the stresses on the components. Accordingly, the DC/DC stage is denominated as H-QSRC. Finally considered component values and operating parameters according to **Fig. 2**.

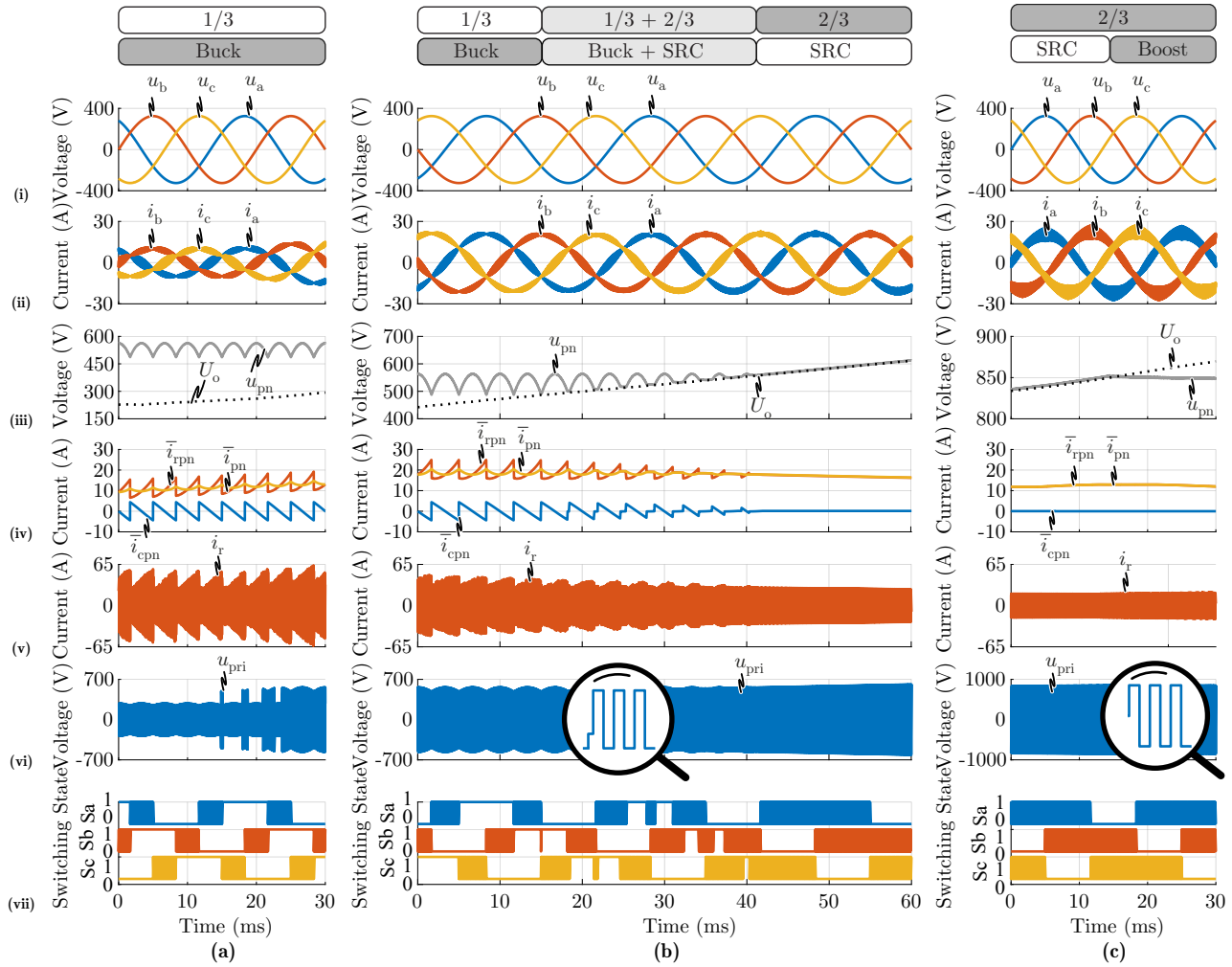

Fig. 2. Simulation waveforms of the two-stage EV charger power module (cf. **Fig. 1(b)**) employing Synergetic Operation 3 (cf. **Section III-E**) for **(a)** U_o = 210 V - 300 V, **(b)** U_o = 440 V - 610 V, **(c)** U_o = 830 V - 870 V: **(i)** grid voltages $u_{a,b,c}$, **(ii)** PFC rectifier inductor currents $i_{a,b,c}$, **(iii)** DC link voltage u_{pn}, output voltage U_o, **(iv)** average PFC rectifier stage output current $\bar{i}_{pn}$, average DC link current $\bar{i}_{cpn}$, and average input current $\bar{i}_{rpn}$ of the resonant converter over a switching period ($\bar{i}_{rpn} = \bar{i}_{pn} - \bar{i}_{cpn}$), **(v)** resonant current i_r, **(vi)** primary side switch-node voltage u_{pri}, **(vii)** gate signals of the three bridge-legs $S_{a,b,c}$ of the PFC rectifier stage. The main simulation parameters are: switching frequency of the PFC rectifier stage and the H-QSRC: 140 kHz, $L_{a,b,c}$ = 100 µH, $C_{pn1} = C_{pn2}$ = 100 µF = $2C_{pn}$, L_r = 50 µH, $C_{r1} = C_{r2} = C_{r3} = C_{r4} = 4C_r$ = 104 nF (with C_r representing the total capacitance) and C_o= 3 mF (to emulate the behaviour of batteries).

secondary sides of the transformer to prevent the magnetic core from saturation. It is also split among both terminals

of the windings in order to reduce the common-mode noise. Compared with a traditional QSRC [9,10], one bridge-leg of the primary side of the H-QSRC is replaced by a T-type bridge-leg, such that a hybrid (H) combination of a two-level and a three-level bridge-leg is employed, and the number of available voltage levels on the primary side is increased [11]. The detailed operating principle of the proposed H-QSRC is introduced in **Section II**, where different operating modes are explained. **Section III** investigates the suitability and performance of possible combinations of the different operating modes of the H-QSRC and the PFC rectifier stage. The resulting control options are then compared concerning component stresses. It is found that the best synergetic combination of operating modes and/or of the control of both stages depends on the output voltage region, and it is shown, that by using the identified optimal control scheme the extremely wide operating range of an EV charger can be covered without overdesign of any of the two stages. Finally, the complete control structure of the optimal scheme is presented in **Section III-E**, and the implementation of the synergetic control of the two stages is explained in detail. **Section IV** concludes the paper.

II. Operating Principle of the H-QSRC

Ideally, a series resonant converter (SRC) is operated at its resonant frequency, with an input to output voltage transfer ratio corresponding to the turns ratio of the transformer. However, due to the wide output voltage range required for EV chargers (cf. **Fig. 1(a)**), it is not always possible to keep its input voltage u_{pn} equal to the primary side referred output voltage $n \cdot U_{\mathrm{o}}$, which is why the H-QSRC considered in the case at hand needs to be operated in different modes for different output voltage levels. These modes will be introduced in the following, whereby for simplicity reasons, the turns ratio is assumed to be $n = 1:1$.

A. Buck-Mode

When U_{o} is lower than $u_{\mathrm{ll,max}}$, the PFC rectifier stage can be operated with $1/3$-modulation (cf. **Section I**), where u_{pn} needs to be controlled by the H-QSRC to follow the six-pulse course of $u_{\mathrm{ll,max}}$. Hence, the H-QSRC controls the net current i_{cpn} ($i_{\mathrm{cpn}} = \frac{1}{2}(i_{\mathrm{cpn1}} + i_{\mathrm{cpn2}} - |i_{\mathrm{cpn3}}|) = C_{\mathrm{pn}} \frac{du_{\mathrm{pn}}}{dt}$, $C_{\mathrm{pn}} = \frac{1}{2} C_{\mathrm{pn1}} = \frac{1}{2} C_{\mathrm{pn2}}$) in the DC-link capacitor in such a way, that the required six-pulse variation of the DC-link capacitor voltage is achieved (cf. **Fig. 2(a.iv)**). In addition to i_{cpn}, the H-QSRC ensures a six-pulse output current i_{pn} of the PFC rectifier stage, in order to extract a constant power from the three-phase grid. In this case, the H-QSRC is operated as controllable step down converter, which can either be achieved by adjusting the switching frequency, or by skipping power pulses, i.e. by introducing a freewheeling state on the primary side of the converter, as shown in **Fig. 3**. For the sake of simplicity, the high-frequency ripples in i_{pn} due to switching transitions of the PFC rectifier half-bridges are ignored and $i_{\mathrm{pn}} = \bar{i}_{\mathrm{pn}}$ is assumed throughout this section. Without the T-type extension of a bridge-leg (cf. **Fig. 1(b)**), three different voltage levels can be generated on the primary side: $\pm u_{\mathrm{pn}}$ (referred to as power period) and $0\,\mathrm{V}$ (referred to as free resonant period). The corresponding conduction states are shown in **Fig. 3(a)(b)** ($u_{\mathrm{pn}} = 490\,\mathrm{V}$, $U_{\mathrm{o}} = 400\,\mathrm{V}$) for a positive resonant current; **Fig. 3(d)** shows the key waveforms. It should be noticed that during power periods, since the primary side switch-node voltage u_{pri} is larger then the secondary side switch-node voltage u_{sec}, a positive net voltage is applied to the resonant tank, whereby i_{r} increases. On the contrary, in the free resonant periods, a negative net voltage is applied and i_{r} decreases. By controlling the resonant current, the charge taken out of C_{pn} can directly be controlled and u_{pn} can therefore be controlled accordingly, as shown in **Fig. 3(a.iii)**. As already mentioned, i_{pn} is the output current of the upstream PFC rectifier stage, and i_{cpn} is the share of the current flowing through the DC link capacitors C_{pn1} and C_{pn2}. With the T-type bridge-leg, two additional voltage levels can be generated: $\pm\frac{1}{2}u_{\mathrm{pn}}$ (referred to as half-free resonant periods). The extra conduction states are shown in **Fig. 3(c)**. Therefore, for the same output voltage ($U_{\mathrm{o}} = 400\,\mathrm{V}$), the zero-voltage state can be replaced by using half of the intermediate DC link voltage, whereby a more precise control of i_{r} and, therefore, u_{pn} can be achieved. **Fig. 3(d)(e)** shows the comparison between the operation without and with the T-type bridge-leg. It should be noted that the peak resonant current, as well as the amplitude of the voltage ripples of u_{pn}, are both decreased, while the latter also decreases the ripples of the PFC rectifier input inductor currents ($i_{\mathrm{a,b,c}}$) that are directly affected by the fluctuations of u_{pn}. Therefore, the T-type bridge-leg should be used whenever possible.

B. SRC-Mode

When the primary side referred output voltage $U_{\mathrm{o}}^{'} = n \cdot U_{\mathrm{o}}$ is higher than $u_{\mathrm{ll,max}}$, $1/3$-operation is not suitable anymore and the PFC rectifier starts operating with conventional $2/3$-modulation, i.e. as boost converter stepping up the voltage and controlling the three-phase inductor currents $i_{\mathrm{a,b,c}}$ at the same time. As a result, the H-QSRC can now be operated as ideal series resonant converter with $u_{\mathrm{pn}} = n \cdot U_{\mathrm{o}}$.

C. Boost-Mode

As for the specified output voltage range (cf. **Fig. 1(a)**), U_{o} can reach up to $1000\,\mathrm{V}$, it would be impossible to employ cost-effective and widely available $1200\,\mathrm{V}$ SiC devices in the H-QSRC and PFC rectifier stage for reliability reasons. In order to circumvent this issue, the H-QSRC can also be operated in boost-mode to reduce the voltage stresses of the PFC rectifier stage, such that only the secondary side switches of the H-QSRC need to have higher ($> 1200\,\mathrm{V}$) breakdown voltages. The characteristic waveforms and conduction states of boost-mode are shown in **Fig. 4** ($u_{\mathrm{pn}} = 850\,\mathrm{V}$, $U_{\mathrm{o}} = 1000\,\mathrm{V}$). When applying zero voltage on the secondary side, a positive net voltage is applied to the resonant tank, whereby i_{r} starts to increase. On the other hand, i_{r} decreases when power periods are used, since a negative net voltage is applied to the resonant tank. Hence, u_{pn} and/or U_{o} can be controlled by manipulating i_{r}. In this operating mode, the components suffer

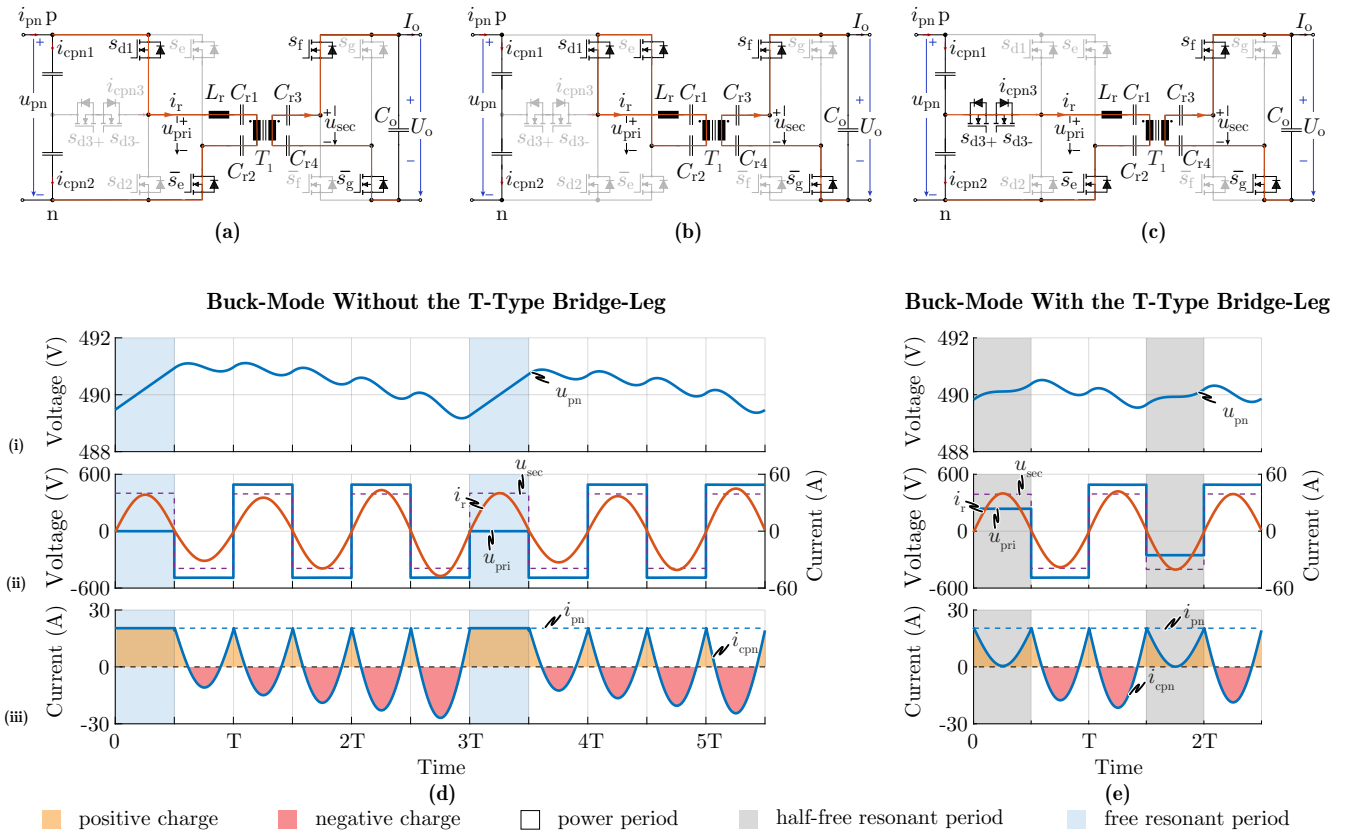

Fig. 3. Conduction states ($i_r > 0$) of the H-QSRC (DC/DC converter stage of the EV charger modulation, cf. **Fig. 1(b)**) in buck-mode for $u_{pn,ref} = 490\,V$ and $U_o = 400\,V$ for **(a)** power periods, **(b)** free resonant periods, **(c)** half-free resonant periods, and simulation waveforms for **(d)** without the T-type bridge-leg, and **(e)** with the T-type bridge-leg: **(i)** DC link voltage u_{pn}, **(ii)** primary side switch-node voltage u_{pri}, secondary side switch-node voltage u_{sec} and resonant current i_r, **(iii)** rectifier output current i_{pn} (assuming $i_{pn} = \bar{i}_{pn}$), net current flowing into the DC link capacitors i_{cpn} ($i_{cpn} = \frac{1}{2}(i_{cpn1} + i_{cpn2} - |i_{cpn3}|) = C_{pn}\frac{du_{pn}}{dt}$, $C_{pn} = \frac{1}{2}C_{pn1} = \frac{1}{2}C_{pn2}$), with orange marking of intervals charging C_{pn} and red marking of discharging C_{pn}. Different colors are used when different voltage levels are applied: light blue for free resonant periods, grey for half-free resonant periods and white marking of power periods.

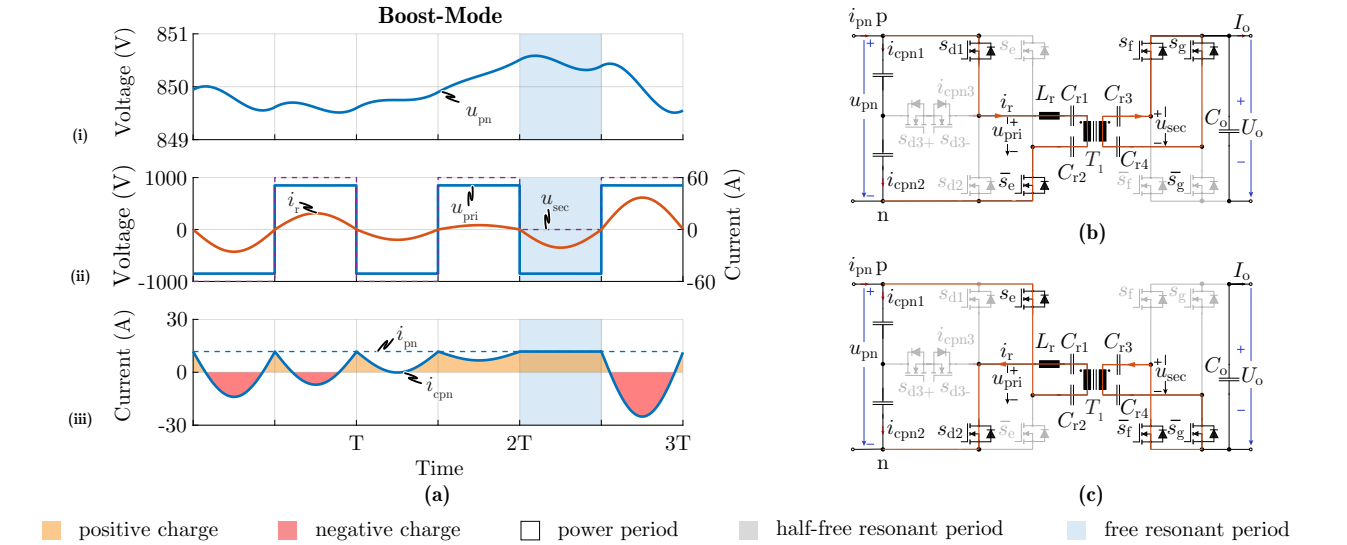

Fig. 4. **(a)** Simulation waveforms of the H-QSRC in boost-mode for $u_{pn,ref} = 850\,V$ and $U_o = 1000\,V$ **(i)** DC link voltage u_{pn}, **(ii)** primary side switch-node voltage u_{pri}, secondary side switch-node voltage u_{sec} and resonant current i_r, **(iii)** rectifier output current i_{pn}, net current flowing into the DC link i_{cpn}, and conduction states of half-free resonant periods for **(b)** $i_r > 0$, **(c)** $i_r < 0$.

from comparably high current stresses due to much higher net voltages applied to the resonant tank, which is why boost-mode is considered to be less efficient and its usage should be limited to the upper output voltage region. The optimal maximum output voltage of the PFC rectifier stage $u_{pn,max}$ is therefore subject to an optimization with regard to the overall

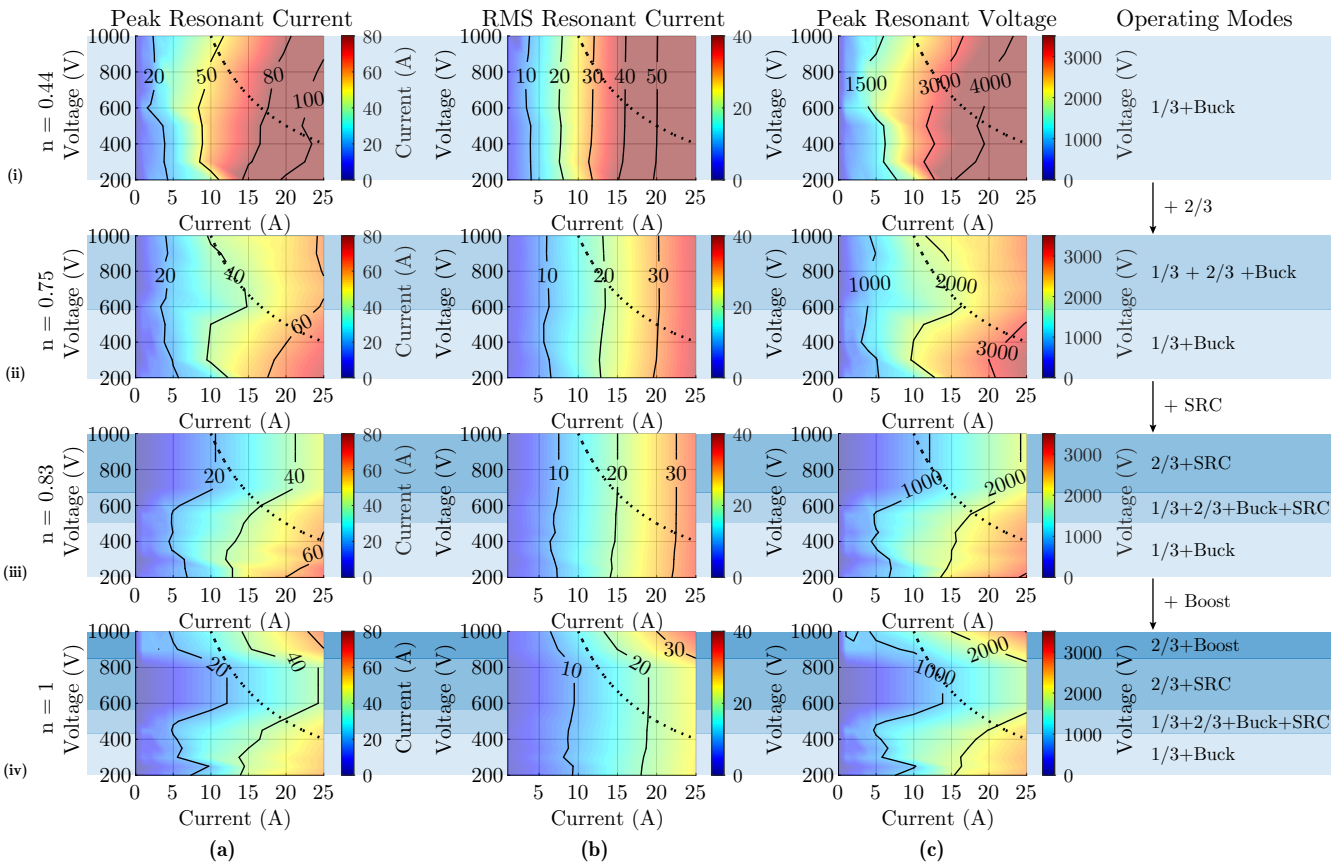

Fig. 5. Stresses of the H-QSRC for **(i)** Pure Buck Operation, **(ii)** Synergetic Operation 1, **(iii)** Synergetic Operation 2, **(iv)** finally selected Synergetic Operation 3: **(a)** peak resonant current, **(b)** RMS resonant current, **(c)** peak resonant voltage (total).

efficiency of the converter system. It needs to be noted that the half-free resonant periods are not utilized in boost-mode as this would result in higher RMS currents in the resonant tank. The reason is that when employing half-free resonant periods, less current is taken from C_{pn}, leading to increased i_{r} during power periods, such that the same average charge is extracted from the capacitor. Also the relatively large voltage applied to the resonant tank during free resonant periods results in higher peak currents, which, however, can be mitigated by duty cycle operation, as will be explained in **Section III-E**. Nevertheless, as the output currents for high output voltages (where boost-mode is mainly used) are comparably low, an increase of the peak currents does not affect the required core cross-section of the magnetic components or power density of the system.

As mentioned in the beginning of this paper, the three modes of operation (buck, SRC, boost) of the H-QSRC offer various possibilities for a synergetic control of the PFC rectifier stage and the subsequent H-QSRC. In the following section, different two-stage control strategies are investigated in detail and their benefits and drawbacks are discussed.

III. Control Schemes of the Two-Stage Boost-Buck Charging Module

By modifying the turns ratio n of the transformer, the maximum primary side referred output voltage $U_{\mathrm{o}}^{'}$ can be adjusted. Consequently, depending on n, the required operating modes are different. In this section, four possible synergetic control options are investigated and comprehensively evaluated, such that the most appropriate one can finally be selected for a certain application.

A. Pure Buck Operation

The most simple solution would be to operate the PFC rectifier stage with $1/3$-modulation only and the DC/DC stage in buck-mode across the whole operating range. This could be achieved by limiting the maximum $U_{\mathrm{o}}^{'}$ to be smaller than the minimum value of the instantaneous maximum line-to-line voltage $\min(u_{\mathrm{ll,max}})$. Hence, considering a certain margin, the turns ratio would have to be selected as $n = 4:9 = 0.44$, such that $U_{\mathrm{o,max}}^{'} = 440\,\mathrm{V}$. In this mode, the large voltage and current stresses are shifted to the components of the DC/DC stage while only one bridge-leg of the PFC rectifier stage is switching at a time, resulting in a very efficient operation of the rectifier front-end. The resulting main component stresses for the H-QSRC are plotted in **Fig. 5**, whereby the dashed line refers to a constant power of 10 kW. For output power values P_{out} lower than 3 kW, the rectifier stage is not anymore operated with $1/3$-modulation and u_{pn} is increased to 600 V, as a certain minimum reactive power is required to maintain the six-pulse course of u_{pn}, which is not available for $P_{\mathrm{out}} < 3\,\mathrm{kW}$. It should be noted that the component stresses are very high for this control strategy [$i_{\mathrm{r,peak,max}} = 110\,\mathrm{A}$, $i_{\mathrm{r,rms,max}} = 60\,\mathrm{A}$, $U_{\mathrm{Cr,peak}} = 4.9\,\mathrm{kV}$ (total voltage across all the resonant

capacitors $C_{r1,2,3,4}$)], especially for low $U_o^{'}$. Due to the small turns ratio, the transformer is stepping up the voltage for all operating points, which is why the step-down ratio of the system is further increased and the efficiency is therefore reduced.

B. Synergetic Operation 1

To decrease the current and voltage stresses of the resonant tank, the turns ratio can be increased whereby the $^2/_3$-operation of the PFC rectifier stage needs to be included, such that the DC link voltage can be boosted. If the breakdown voltage of the switches in the rectifier stage and the primary side of the H-QSRC is 1200 V, which is a standard voltage level for commercially available SiC power MOSFETs, the maximum allowed DC link voltage u_{pn} is limited to 850 V. Similarly, for the H-QSRC to work in buck-mode, a certain margin between u_{pn} and $U_o^{'}$ needs to be kept (for example $u_{diff} = 50$ V), such that the voltage applied to the resonant tank is large enough to regulate i_r with comparably high dynamics. Therefore, the maximum primary side referred output voltage $U_{o,max}^{'}$ is limited to around 800 V. Consequently, the turns ratio can be increased to $n = 0.75$. Thus, as long as $U_{o,max}^{'}$ is lower than $u_{ll,max} - u_{diff}$, the rectifier stage is again operated with $^1/_3$-modulation (cf. **Section III-A**). However, once $U_{o,max}^{'}$ exceeds $u_{ll,max} - u_{diff}$, the PFC rectifier has to start boost operation with $^2/_3$-modulation to keep u_{pn} above $U_{o,max}^{'}$. The H-QSRC still operates in buck-mode across the whole operating range and SRC-mode is not yet employed. Compared to pure buck operation, the peak value of the resonant current is decreased by 32% ($i_{r,peak,max} = 75$ A), the RMS current decreased by 38% ($i_{r,rms,max} = 37$ A), and the peak resonant capacitor voltage decreased by 33% ($U_{Cr,peak} = 3.3$ kV).

C. Synergetic Operation 2

An improvement of Synergetic Operation 1 can be achieved by adding SRC-mode of the H-QSRC. To use conventional 1200 V SiC devices in the PFC rectifier front-end, u_{pn} is again limited to 850 V. Since SRC-mode is added, $U_{o,max}^{'}$ can be increased to the same level as u_{pn}, and therefore the turns ratio can be chosen as 0.83. The transition between buck-mode and SRC-mode will be discussed in detail in **Section III-E**. Similarly, depending on $U_{o,max}^{'}$ and $u_{ll,max}$, the PFC rectifier changes between $^1/_3$- and $^2/_3$-operation, while the H-QSRC stage switches between buck-mode and SRC-mode in the same way, i.e., $^1/_3$-modulation of the rectifier stage is combined with buck-mode of the H-QSRC, and $^2/_3$-modulation of the PFC rectifier is used with SRC-mode of the H-QSRC. Compared to Synergetic Operation 1 (cf. **Section III-B**), the resonant inductor peak current is further decreased by 9% ($i_{r,peak,max} = 68$ A), the RMS current is decreased by 8% ($i_{r,rms,max} = 34$ A), and the peak resonant capacitor voltage is decreased by 9% ($U_{Cr,peak} = 3$ kV).

D. Synergetic Operation 3

Finally, by also utilizing boost-mode of the H-QSRC, the turns ratio can be set as 1 : 1. The upper limit of the PFC rectifier output voltage is again set to 850 V, which is why for output voltages above 850 V the H-QSRC stage switches from SRC-mode to boost-mode, and starts to step up the voltage. The choice of the optimal boundary between SRC-mode and boost-mode (850 V for now) may be changed in a practical application and is subject to a system optimization. Compared to Synergetic Operation 2 (cf. **Section III-C**), the resonant inductor peak current is decreased by 16% ($i_{r,peak,max} = 57$ A), the RMS current is decreased by 18% ($i_{r,rms,max} = 28$ A), and the peak resonant capacitor voltage is decreased by 17% ($U_{Cr,peak} = 2.5$ kV). It can be noted that the stresses in the boost-mode region are slightly higher than for Synergetic Operation 2 (for example, at $U_o = 1000$ V, $P_{out} = 10$ kW, $i_{r,rms}$ is increased from 13.3 A to 14.3 A). However, the stresses in the other regions are lower and the average efficiency over the whole operating range is still higher.

An output voltage sweep from 200 V to 1000 V was simulated for the above described control concept (Synergetic Operation 3) and the key transition waveforms are shown in **Fig. 2**. It should be noted that it is possible to design a suitable control structure which guarantees smooth transitions between the different modes of operation. Such control structure is introduced and discussed in detail in the next section.

E. Control Structure of Synergetic Operation 3

A multi-cascaded control structure implementing the aforementioned Synergetic Operation 3 is shown in **Fig. 6**. For the PFC rectifier stage, the output voltage U_o is measured and used to calculate the output power reference P_o^*, which is then translated to the references $i_{a,b,c}^*$ of the phase currents. The grid current controllers Ri_{grid} then set the reference values of the voltages across the inductors $L_{a,b,c}$, which are added to the measured mains phase voltages to create the references of the PFC rectifier switching stage input voltages (u_{Ba}^*, u_{Bb}^* and u_{Bc}^*). Based on these references, the gate signals of the half-bridges of the PFC rectifier are generated, and the required clamping of phases is performed [4,5].

For the H-QSRC stage, two controllers are working in parallel: the buck controller generating the gate signals for the primary side ($s_{d,e}$), and the boost controller which generates the gate signals for the secondary side ($s_{f,g}$). These two controllers have very similar structures, which is why in a first step only the buck controller is investigated in detail in the following sections.

*1) Hysteresis Controller (Block 1 in **Fig. 6**):* The DC-link voltage u_{pn} of the two-stage system is always controlled by the H-QSRC stage, whose reference $u_{pn,buck}^*$ is calculated using the output voltage U_o and $u_{ll,max}^*$, where the latter is the instantaneous maximum line-to-line input voltage reference, defined as $u_{ll,max}^* = u_{max}^* - u_{min}^*$. Furthermore, an additional term u_m is added to the output voltage reference U_o^*, whose purpose and magnitude will be discussed in **Section III-E3**. In a next step, $u_{pn,buck}^*$ is compared with the measured value u_{pn} to calculate the current reference i_{cpn}^*, which is then subtracted from i_{pn}^*, a feed-forward term representing the output current of the PFC rectifier, and can be calculated from the PFC rectifier inductor currents and the corresponding duty cycles

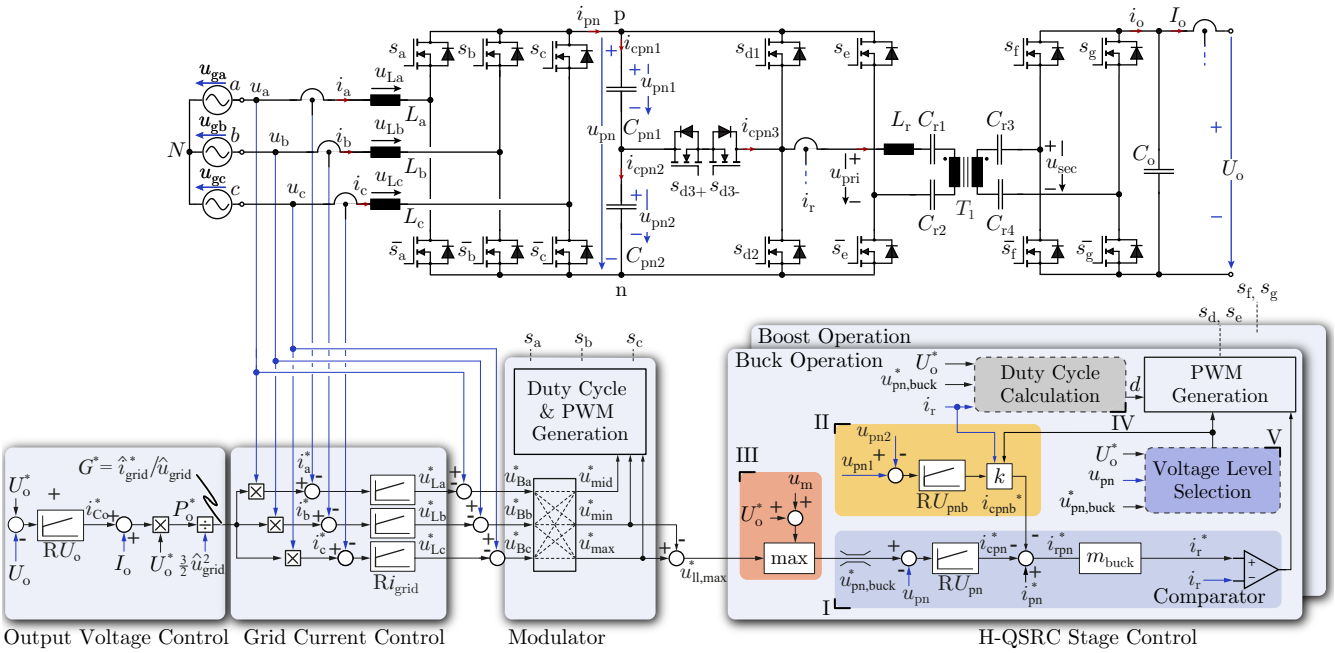

Fig. 6. Cascaded output voltage control structure of the two-stage EV charger power module comprising a three-phase PFC rectifier front-end and a DC/DC Hybrid Quantum Series Resonant Converter (H-QSRC) output stage, where measurement values are displayed in blue.

($i^*_{\mathrm{pn}} = i^*_{\mathrm{a}} d_{\mathrm{a}} + i^*_{\mathrm{b}} d_{\mathrm{b}} + i^*_{\mathrm{c}} d_{\mathrm{c}}$). Furthermore, a second term i^*_{cpnb} is subtracted from i^*_{pn}, which is used to ensure balanced voltages across the two DC link capacitors $C_{\mathrm{pn1}}, C_{\mathrm{pn2}}$, which will be explained in detail in **Section III-E2**. Finally, with $i^*_{\mathrm{rpn}} = i^*_{\mathrm{pn}} - i^*_{\mathrm{cpnb}} - i^*_{\mathrm{cpn}}$, the input current reference i^*_{rpn} of the H-QSRC stage is found. To calculate the resonant current reference i^*_{r} in buck-mode, i^*_{rpn} is multiplied by $m_{\mathrm{buck}} = u^*_{\mathrm{pn,buck}}/U^*_{\mathrm{o}}$, which is the same as the relationship between the input current and the inductor current in a conventional buck converter. Subsequently, i^*_{r} is compared to the measured resonant current $|i_{\mathrm{r}}|$ [12,13], which is sampled once every half period (peak current is sampled and divided by $2/\pi$ to calculate the average current). Based on this comparison, it can then be determined whether the resonant current should be decreased or increased, which, in combination with the results of the voltage level selection block and the duty cycle calculation block, is used to generate the PWM signals.

*2) Control of the Midpoint Voltage (Block II in **Fig. 6**):* As mentioned previously, the balance between the voltages across C_{pn1} and C_{pn2} needs to be maintained for proper operation of the converter. Therefore, a PI controller RU_{pnb} is added, where the difference of u_{pn1} and u_{pn2} is used as error signal. The output of this PI controller is then multiplied with an index k ($k = 1$ or -1) to obtain i^*_{cpnb}, whose sign depends on the selected voltage levels and the sign of the resonant current. For example, if $u_{\mathrm{pn1}} > u_{\mathrm{pn2}}$, the half-free resonant periods should be used more often for $i_{\mathrm{r}} < 0$ and less often for $i_{\mathrm{r}} > 0$ in order to discharge C_{pn1} (during half-resonant periods, C_{pn1} is only discharged for $i_{\mathrm{r}} < 0$, and C_{pn2} is only discharged for $i_{\mathrm{r}} > 0$). Therefore, if power periods and half-free resonant periods are used, i^*_{cpnb} should be positive ($k = 1$) for $i_{\mathrm{r}} < 0$ and negative ($k = -1$) for $i_{\mathrm{r}} > 0$, such that i^*_{r} is decreased for $i_{\mathrm{r}} < 0$ and increased for $i_{\mathrm{r}} > 0$, leading to more half-resonant periods used for $i_{\mathrm{r}} < 0$ and less used for $i_{\mathrm{r}} > 0$ to discharge C_{pn1}. The situation is exactly the opposite if half-free resonant periods and free resonant periods are used and is therefore not explained further.

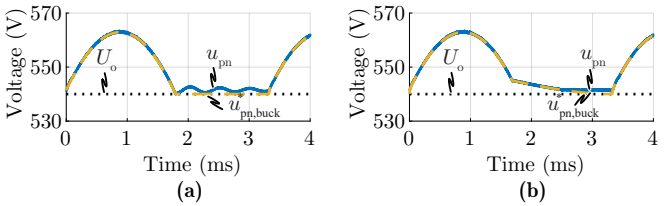

Fig. 7. Simulation waveforms of the DC link voltage u_{pn}, its reference $u^*_{\mathrm{pn,buck}}$ and the output voltage U_{o} when the H-QSRC transitions between buck-mode and SRC-mode for $U_{\mathrm{o}} = 540\,\mathrm{V}$ **(a)** without the transition voltage u_{m} and **(b)** with the transition voltage u_{m}.

*3) Intermediate DC-Link Voltage Reference (Block III in **Fig. 6**):* Ideally, the voltage reference $u^*_{\mathrm{pn,buck}}$ should be selected from the maximum of two values, the output voltage U_{o} and $u^*_{\mathrm{ll,max}}$, as it is done in [4,5]. However, due to the limited dynamic response of the resonant converter, the transition from buck-mode to SRC-mode cannot be achieved instantaneously. When the rectifier is operated with $1/3$-modulation, the average input current $\bar{i}_{\mathrm{rpn}}$ of the H-QSRC is different from the average rectifier output current $\bar{i}_{\mathrm{pn}}$, due to the average capacitor current $\bar{i}_{\mathrm{cpn}}$. However, as soon as the H-QSRC enters SRC-mode, its input current $\bar{i}_{\mathrm{rpn}}$ should be adapted to the rectifier output current $\bar{i}_{\mathrm{pn}}$, as in SRC-mode the H-QSRC is operated in open-loop and does not control $\bar{i}_{\mathrm{pn}}$ anymore. However, in H-QSRCs, it is difficult to adjust the resonant current fast and accurately during a short time interval, especially if a relatively large resonant inductor is employed. This is relevant, as even a small deviation

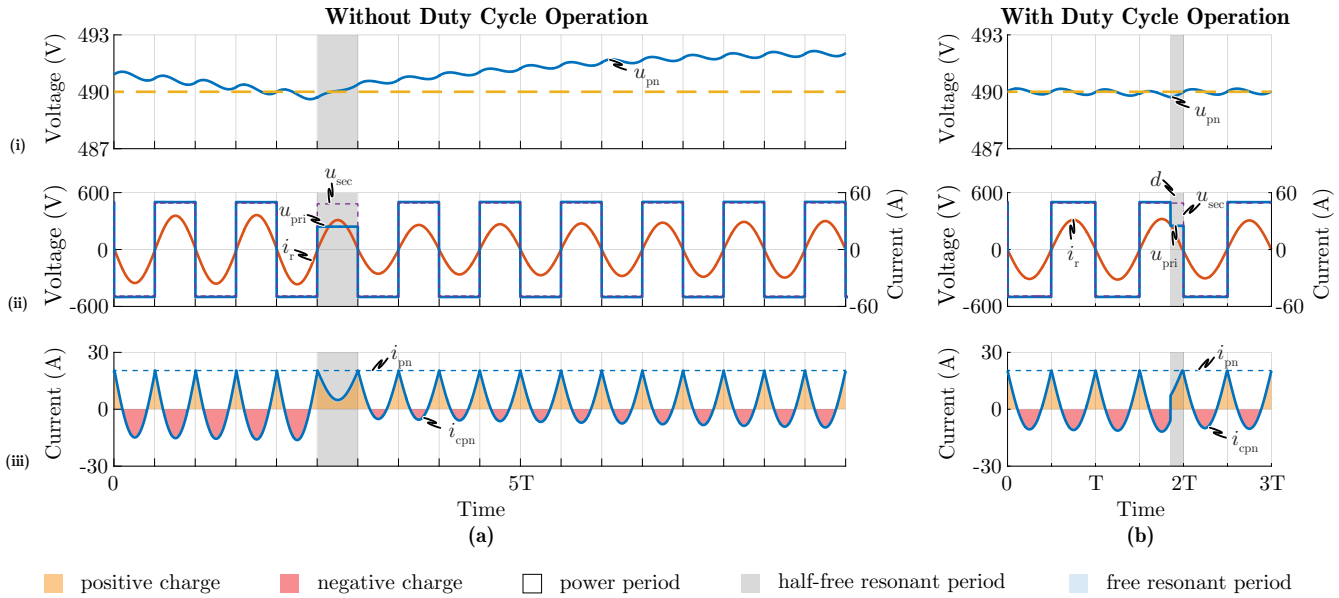

Fig. 8. Simulation waveforms of the H-QSRC in buck-mode for $u^*_{\mathrm{pn,buck}} = 490\,\mathrm{V}$ and $U_\mathrm{o} = 480\,\mathrm{V}$ **(a)** without duty cycle operation and **(b)** with duty cycle operation: **(i)** DC link voltage u_pn, its reference $u^*_{\mathrm{pn,buck}}$, **(ii)** primary side switch-node voltage u_pri, secondary side switch-node voltage u_sec, resonant current i_r, **(iii)** rectifier output current i_pn, net current following into the DC link i_cpn.

from the steady-state can cause oscillations as shown in **Fig. 7(a)**. Therefore, to achieve a smooth transition as shown in **Fig. 7(b)**, a voltage u_m is added to U^*_o, which gradually decreases to zero with a much lower rate, e.g., a quarter of a sinusoidal wave, with a small amplitude, e.g., 5 V, and a low frequency, e.g., 150 Hz, such that the resonant current is adjusted step by step until $\bar{i}_\mathrm{rpn} = \bar{i}_\mathrm{pn}$.

*4) Duty Cycle Operation (Block IV in **Fig. 6**):* For a conventional QSRC, large voltage ripples would appear in u_pn, especially when the input and output voltages are close, as the differences between the absolute voltage-time areas applied to the resonant tank during half-free resonant periods and power periods are very large. In this condition, the 'net' voltage applied to the resonant tank during power periods is nearly zero, while in half-free resonant periods, it is close to half of the DC link voltage, as shown in **Fig. 8(a)**. Consequently, the decrease rate of i_r during the free-half resonant periods is much larger than the increase rate during the following power periods. As a result, it takes a comparably long time (tens of half periods) to bring the current back to its reference value. Consequently, a low-frequency ripple appears across u_pn with a large amplitude, leading to distortions in the three-phase PFC rectifier input currents. This problem can be mitigated by introducing duty cycle operation, as shown in **Fig. 8(b)**, where only a fraction of a full half-free resonant period is used. By introducing duty cycle operation, the effective voltage-time area applied to the resonant tank during one half-free resonant period is much smaller, enabling a much smoother regulation of u_pn.

To ensure soft-switching for every switching transition in duty cycle operation, the appropriate voltage level sequence has to be selected. For example, if power and half-free resonant periods are used, the higher voltage level always needs to be applied first, such that the direction of i_r during the intermediate transition from u_pn to $\frac{1}{2}u_\mathrm{pn}$ inherently results in soft switching (cf. **Fig. 8(b)**). Nevertheless, for a certain duty cycle, i_r is not anymore precisely in phase with u_pri, which means it may reach zero before the end of the half period, leading to hard-switching transitions. There are two solutions to achieve soft switching under this circumstance: 1. increasing the switching frequency (slightly increasing the switching frequency does not affect the output voltage), 2. using the magnetizing current of the transformer, which is the subject of current research. Having ensured soft switching in duty cycle operation, the calculation of the appropriate duty cycle needs to be investigated. Ideally, it can be derived considering the voltage-time-area balance, i.e., zero net voltage applied to the resonant tank during a control period. A control period is defined as the time interval where the average of u_pn is equal to the reference. Considering again the case depicted in **Fig. 8(a)** with the same u_pn and U_o, and assuming a control period containing n half periods, the duration d of the half-free resonant period can be derived as

$$d = d_\mathrm{vb} = 2(n+1)\cdot\frac{u_\mathrm{pn} - U_\mathrm{o}}{u_\mathrm{pn}}. \tag{1}$$

However, as the current is not in phase with the voltage due to the applied duty cycle, the secondary side applied voltage u_sec is not anymore in phase with u_pri, leading to different voltage-time areas which are applied to the resonant tank. For the considered component values of the resonant tank, the H-QSRC operates in continuous conduction mode, as the voltage across the resonant capacitor C_r is larger than U_o when i_r reaches zero. Thus, even if all four switches of the secondary side full-bridge are turned off, the large capacitor voltage forces a continuation of i_r through the anti-parallel diodes of the switches. To compensate for this voltage-time-area discrepancy, another term is added to d_vb, where d_off

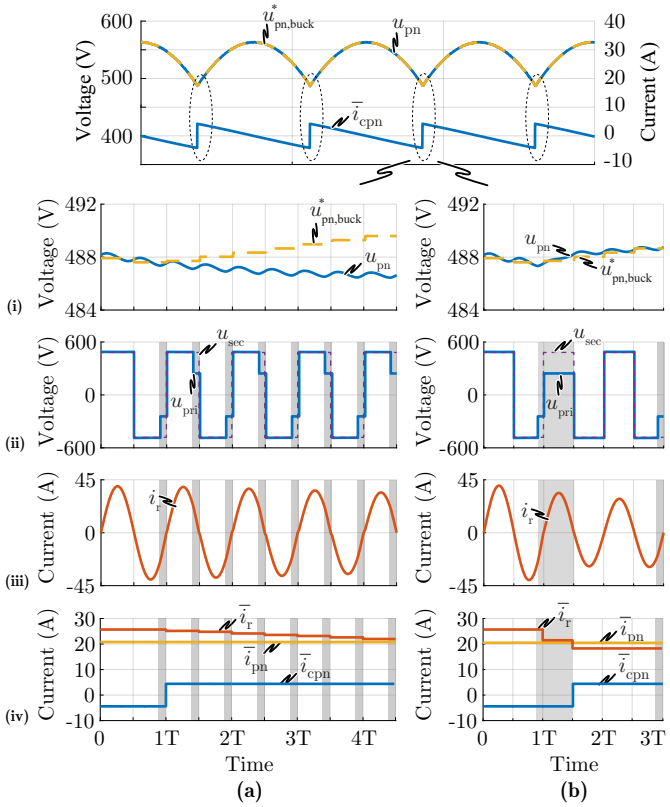

Fig. 9. Simulation waveforms of the H-QSRC in buck-mode when $u^*_{\mathrm{pn,buck}}$ reaches the lowest point of its six-pulse course ($u_{\mathrm{pn}} \approx u_{\mathrm{ll,max}}$) and $U_{\mathrm{o}} = 480\,\mathrm{V}$ **(a)** without d_{ic} and **(b)** with d_{ic}: **(i)** DC link voltage u_{pn}, its reference $u^*_{\mathrm{pn,buck}}$, **(ii)** primary side switch-node voltage u_{pri}, secondary side switch-node voltage u_{sec}, **(iii)** resonant current i_{r}, **(iv)** average rectifier output current $\bar{i}_{\mathrm{pn}}$, average DC link current $\bar{i}_{\mathrm{cpn}}$, and average resonant current $\bar{i}_{\mathrm{r}}$ over a switching period ($\bar{i}_{\mathrm{r}} = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}}\bar{i}_{\mathrm{rpn}} = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}}(\bar{i}_{\mathrm{pn}} - \bar{i}_{\mathrm{cpn}})$).

represents the time interval where the current is flowing into the opposite direction:

$$d = d'_{\mathrm{vb}} = d_{\mathrm{vb}} + 4 \cdot \frac{d_{\mathrm{off}} U_{\mathrm{o}}}{u_{\mathrm{pn}}}; \tag{2}$$

d_{off} is a function of d_{vb} and can be calculated with the differential equations of the inductor current and the capacitor voltage. As (2) does not have an explicit solution, the duty cycle d'_{vb} needs to be calculated numerically. Furthermore, it should be noted that (2) needs to be modified accordingly if the impedance of the resonant tank is decreased to a certain extent, when the system enters discontinuous conduction mode.

It can be noted from (1) that, the closer u_{pn} and U_{o} get, the smaller the duty cycle is, which however, leads to limited dynamic performance of the system. In buck-mode, u_{pn} follows the six-pulse course, where between each pulse, the capacitor current needs to be changed instantaneously (cf. **Fig. 2(a.iv),(b.iv)**), requiring the H-QSRC to react accordingly. Therefore, another term d_{ic} is added to the duty cycle calculation, which varies depending on the required capacitor current:

$$d = d'_{\mathrm{vb}} + d_{\mathrm{ic}}. \tag{3}$$

Fig. 9 shows the comparison of different duty cycles applied, without and with d_{ic} in the calculations respectively, when $U_{\mathrm{o}} = 480\,\mathrm{V}$ ($u^*_{\mathrm{pn,buck,min}} = 488\,\mathrm{V}$). It can be noted that when U_{o} is close to u_{pn}, d'_{vb} is comparably small (grey areas in **Fig. 9(a)**), and the system is not capable of decreasing the resonant current i_{r} fast enough, leading to insufficient current feeding into C_{pn}, whereby the capacitor voltage u_{pn} cannot be increased as required. Hence, the duty cycle d has to be adjusted if a certain dynamic response is required, as in **Fig. 9(b)**, which is realized by means of d_{ic}. To calculate d_{ic}, first of all, the required change of the resonant current has to be identified. According to the power balance, the output current i_{o} can be calculated as

$$i_{\mathrm{o}} = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}} \cdot i_{\mathrm{rpn}}. \tag{4}$$

With $i_{\mathrm{rpn}} = i_{\mathrm{pn}} - i_{\mathrm{cpn}}$ and $i_{\mathrm{o}} = |i_{\mathrm{r}}|$, (4) can be re-written as

$$|i_{\mathrm{r}}| = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}} \cdot (i_{\mathrm{pn}} - i_{\mathrm{cpn}}). \tag{5}$$

The same applies to the average values:

$$|\bar{i}_{\mathrm{r}}| = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}} \cdot (\bar{i}_{\mathrm{pn}} - \bar{i}_{\mathrm{cpn}}). \tag{6}$$

Thus the change of the resonant current due to the required change of the capacitor current is

$$\Delta|\bar{i}_{\mathrm{r}}|_{\mathrm{max}} = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}} \cdot \Delta\bar{i}_{\mathrm{cpn,max}} = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}} \cdot 2\bar{i}_{\mathrm{cpn,max}}, \tag{7}$$

where $i_{\mathrm{cpn}} = C_{\mathrm{pn}} \frac{du_{\mathrm{pn}}}{dt}$ and its average value over one switching period $\bar{i}_{\mathrm{cpn}}$ is shown in **Fig. 2(a.iv),(b.iv)**.

Similarly, the relationship between d_{ic} and the required change of the resonant current $\Delta|\bar{i}_{\mathrm{r}}|$ needs to be determined numerically. For the sake of simplicity, it can be assumed that before each half period with a certain duty cycle, the steady-state is reached, i.e., $\bar{i}_{\mathrm{r}} = I_{\mathrm{o}}$ and i_{r} reaches zero at the end of the half period, whereby the resonant current can be calculated and the change of its average value with respect to the previous period can be derived. One solution to avoid complicated calculations of d_{ic} is to keep always a certain margin ($u_{\mathrm{diff}} = 50\,\mathrm{V}$) between u_{pn} and U'_{o}, as long as U'_{o} is smaller than the absolute maximum line-to-line voltage (around 563 V), and only changing to SRC-mode when no additional i_{cpn} is present ($\bar{i}_{\mathrm{rpn}} \approx \bar{i}_{\mathrm{pn}}$).

Ideally, the sharp reduction of $\bar{i}_{\mathrm{r}}$ should be accomplished within a short time interval, e.g., in 1 or 2 resonant half cycles as shown in **Fig. 9(b)**, which however, cannot be achieved for all operating points. It can be noted from (7) that the lower the U_{o}, the higher the $\Delta|\bar{i}_{\mathrm{r}}|_{\mathrm{max}}$. Therefore, for a small U_{o} the required change of the resonant current may not be achieved even by applying a complete free-resonant period ($d = 1$), especially for resonant tanks with comparably large inductors, as shown in **Fig. 10(a)** with $U_{\mathrm{o}} = 240\,\mathrm{V}$. After one cycle where $d = 1$, i_{r} has not yet been reduced to the desired value

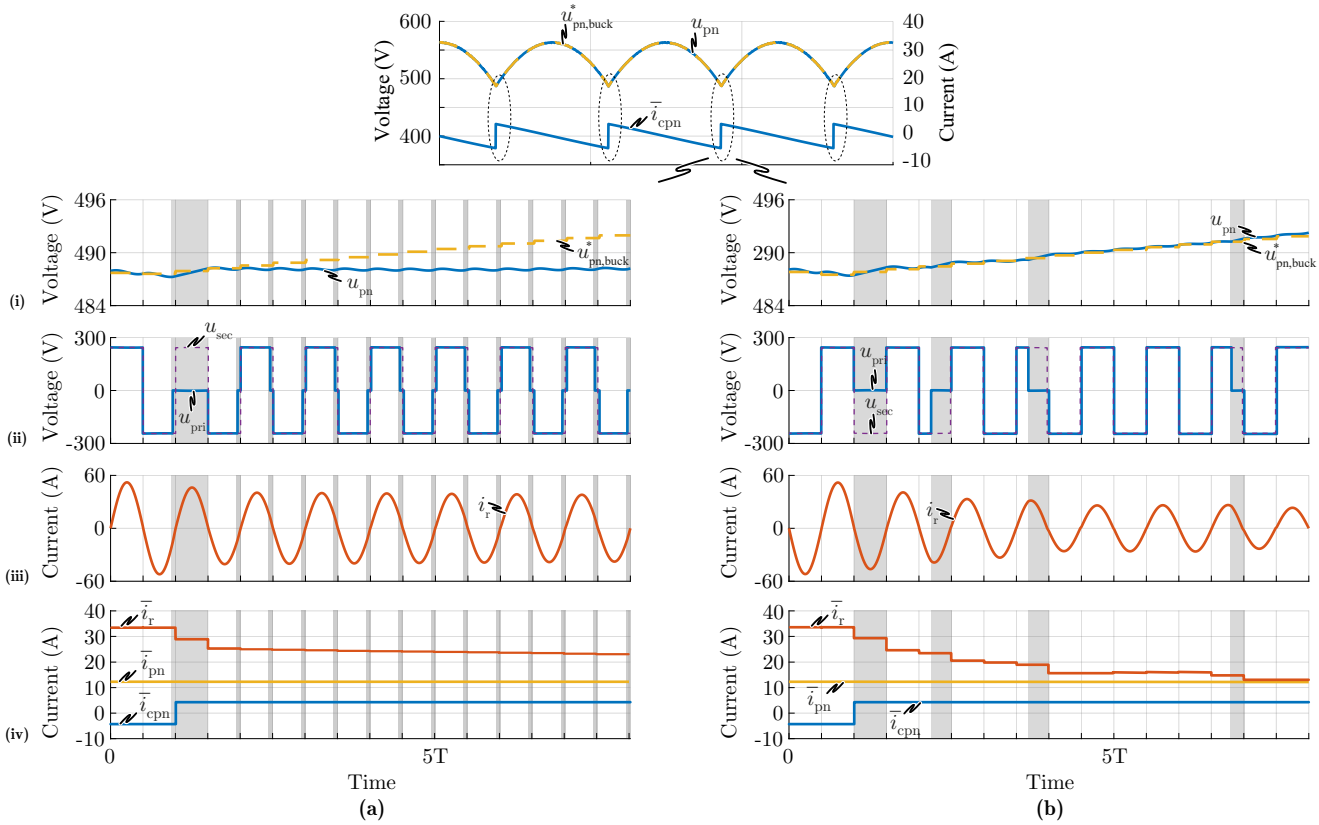

Fig. 10. Simulation waveforms of the H-QSRC in buck-mode when $u^*_{\mathrm{pn,buck}}$ reaches the lowest point of its six-pulse course ($u_{\mathrm{pn}} \approx u_{\mathrm{ll,max}}$) and $U_{\mathrm{o}} = 240\,\mathrm{V}$, with larger requirement of $\Delta|\bar{i}_{\mathrm{r}}|_{\mathrm{max}}$ **(a)** without adjusted d_{ic} and **(b)** with adjusted d_{ic}: **(i)** DC link voltage u_{pn}, and its reference $u^*_{\mathrm{pn,buck}}$; **(ii)** primary side switch-node voltage u_{pri}, secondary side switch-node voltage u_{sec}, **(iii)** resonant current i_{r}, **(iv)** average rectifier output current $\bar{i}_{\mathrm{pn}}$, average DC link current $\bar{i}_{\mathrm{cpn}}$, and average resonant current $\bar{i}_{\mathrm{r}}$ over a switching period ($\bar{i}_{\mathrm{r}} = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}}\bar{i}_{\mathrm{rpn}} = \frac{u_{\mathrm{pn}}}{U_{\mathrm{o}}}(\bar{i}_{\mathrm{pn}} - \bar{i}_{\mathrm{cpn}})$.

and the d'_{vb} in the next few periods is not sufficient to decrease i_{r} fast enough (due to a small difference between u_{pn} and U_{o}), resulting in low-frequency ripples across u_{pn}. Thus, once $\Delta|\bar{i}_{\mathrm{r}}|_{\mathrm{max}}$ is above $\Delta|\bar{i}_{\mathrm{r}}|_{\mathrm{d=1}}$, d_{ic} needs to be adjusted according to i_{r} as well until it reaches the required value. Another solution would be to use a resonant tank with smaller impedance, e.g., reducing L_{r} to 25 µH or to decrease the value of C_{pn}, e.g., to 25 µF. However, this would lead to larger RMS currents or larger fluctuations across u_{pn}, which would deteriorate the performance of the system.

*5) Voltage Level Selection (Block V in **Fig. 6**):* Depending on the output voltage, different voltage levels on the primary side are applied to the resonant tank. In general, if U_{o} is lower than $\frac{1}{2}u^*_{\mathrm{pn,buck}}$, free-resonant periods (0) and half-free resonant periods ($\pm\frac{1}{2}u_{\mathrm{pn}}$) should be used, whereas power periods ($\pm u_{\mathrm{pn}}$) and half-free resonant periods ($\pm\frac{1}{2}u_{\mathrm{pn}}$) should be used when $U_{\mathrm{o}} > \frac{1}{2}u^*_{\mathrm{pn,buck}}$. However, when U_{o} is in the near vicinity of $\frac{1}{2}u_{\mathrm{pn}}$, due to the voltage drop across all the components, the voltages applied to the resonant tank (u_{pri} and u_{sec}) may be slightly different from u_{pn} and U_{o}. As a result, if the measured U_{o} is smaller than $\frac{1}{2}u_{\mathrm{pn}}$ and the T-type bridge-leg is used to increase i_{r}, u_{pri} may be smaller than u_{sec}, leading to a decreased i_{r} instead. Such inappropriate selections of voltage levels are causing distortions across u_{pn}, as shown in **Fig. 12(a)**, which will affect the inductor currents $i_{\mathrm{a,b,c}}$ of the PFC rectifier stage. Hence, in order to facilitate a smooth transition from one pair of voltage levels to another, the system is allowed to switch back and forth between the voltage pairs. A flowchart is shown in **Fig. 11**, exhibiting the procedure of the voltage level selection. First of all, u_{pn} is compared to $u^*_{\mathrm{pn,buck}}$ to check if the system is in the transient state due to disturbances or due to a load step, etc. If u_{pn} deviates from $u^*_{\mathrm{pn,buck}}$ by more than u_{n2} (in the range of 5...10V), then only power periods and free resonant periods are used, such that the system is brought back to the steady state fast enough. In this situation, the use of duty cycle operation is disabled. Next, if U_{o} falls in the range of $\frac{1}{2}u_{\mathrm{pn}} \pm u_{\mathrm{n}}$ (u_{n} is again around 3 V...5 V), all voltage levels are used. When u_{pn} is lower than its reference $u^*_{\mathrm{pn,buck}}$, free-resonant periods (0) and half-free resonant periods ($\pm\frac{1}{2}u_{\mathrm{pn}}$) are employed, while power periods ($\pm u_{\mathrm{pn}}$) and half-free resonant periods ($\pm\frac{1}{2}u_{\mathrm{pn}}$) are utilized if u_{pn} is larger than its reference $u^*_{\mathrm{pn,buck}}$, whereby the controllability of i_{r} is guaranteed. **Fig. 12** shows the comparison between using the aforementioned selection strategy (**Fig. 12(b)**) and simply selecting the voltage level according to the relationship between U_{o} and $u^*_{\mathrm{pn,buck}}$ (**Fig. 12(a)**). It can be noted that the transitions become much smoother with the proposed strategy.

It needs to be mentioned that due to the requirement of $\Delta|\bar{i}_{\mathrm{r}}|$ in the valley of the six-pulse course of u_{pn}, as discussed in the last section, for a U_{o} which is only slightly above $\frac{1}{2}u^*_{\mathrm{pn,buck}} +$

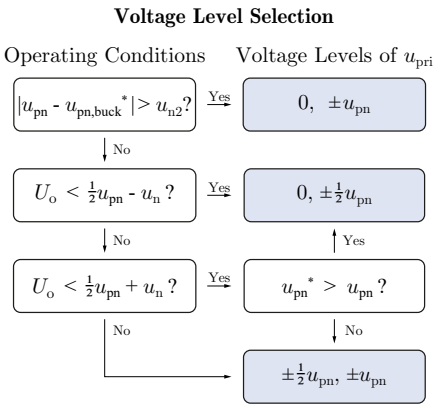

Fig. 11. Flowchart for selecting the appropriate voltage levels of the primary side switch-node voltage u_{pri} used for the generation of PWM signals.

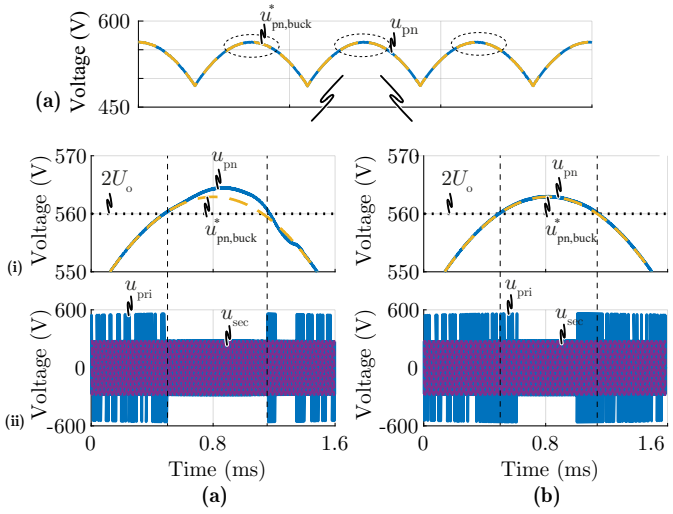

Fig. 12. Simulation waveforms of the H-QSRC in buck-mode for $U_o = 280\,V$ **(a)** selecting the voltage levels simply based on the relationship between U_o and $u_{pn,buck}^*$ and **(b)** with the modified strategy depicted in **Fig. 11**: **(i)** DC link voltage u_{pn} and its reference $u_{pn,buck}^*$, **(ii)** primary side applied voltage u_{pri}, and secondary side applied voltage u_{sec}.

u_n, applying half-free resonant periods cannot reduce i_r fast enough as well, and free resonant periods need to be used. Again similar strategies are implemented here, i.e., as long as the resonant current is not decreased to the required value, switching back and forth between voltage levels is allowed.

6) Boost-Mode: In boost-mode, the control of the H-QSRC is much simpler than in buck-mode, as $u_{pn,boost}^*$ is fixed at 850 V, which is the highest voltage level the primary side switches can withstand safely. Furthermore, i_{cpnb}^* is set to zero as the T-type bridge-leg is not used. The voltage selection block is also disabled since there is no T-type bridge-leg on the secondary side. Moreover, $m_{boost} = 1$, which is the same as in a conventional boost converter, where the inductor current is equal to the input current. Moreover, the calculation of the duty cycle is easier as $d_{ic} = 0$ and $d = d_{vb}'$. The PWM signals are therefore calculated based on i_r, i_r^* and the calculated duty cycle.

To sum up, with the all aforementioned control blocks, Synergetic Operation 3 can be implemented successfully; the resulting simulation waveforms are shown in **Fig. 2**.

IV. Conclusions

In this paper, a two-stage module of a high-power electric vehicle DC charger employing a three-phase boost-type PFC rectifier front-end and a novel Hybrid Quantum Series Resonant DC/DC Converter (H-QSRC) output stage is proposed, with a special focus on how to cope with the three-phase PFC rectifier stage to cover an extremely wide output voltage range. Different operating modes are demonstrated and analyzed for both stages. Subsequently, four different synergetic combinations of the PFC rectifier and the DC/DC converter control were developed. All combinations are evaluated considering the stresses on the main power components, whereby it could be concluded that by utilizing all degrees of freedom of the control of the individual stages and a synergetic partitioning of the overall control tasks between the stages, the required wide operating range could be covered without overdesign of any of the stages. Finally, a detailed explanation of the optimal control scheme is provided, which ensures smooth transitions between the different operating modes. Furthermore, the necessary analytical solutions, which are required for the control implementation are provided, in order to support hardware implementation of the system, which is in the scope of future research.

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