Power Electronic Systems
Laboratory

Proceedings of the 14th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2013), Salt Lake City, USA, June 23-26, 2013

Mixed MOSFET-IGBT Bridge for High-Efficient Medium-Frequency Dual-Active-Bridge Converter in Solid State Transformers

G. Ortiz,
C. Gammeter,
J. W. Kolar,
O. Apeldoorn

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Mixed MOSFET-IGBT Bridge for High-Efficient Medium-Frequency Dual-Active-Bridge Converter in Solid State Transformers

G. Ortiz, Ch. Gammeter, J. W. Kolar and O. Apeldoorn*
Power Electronic Systems Laboratory, ETH Zurich
*Power Electronics and Medium Voltage Drives, ABB Switzerland AG
Email: ortiz@lem.ee.ethz.ch

***Abstract*—High power DC-DC conversion is a key element within the Solid-State-Transformer concept. In order to reduce the switching losses of the Medium-Voltage side semiconductors, a Triangular-Current-Mode modulation scheme presents an attractive option. This modulation scheme, however introduces considerable challenges in the design of the low-voltage side power electronic bridges, which need to deal with high conducted and high switched currents.**

In order to increase the converter's efficiency, a combination of IGBTs and MOSFETs in a full-bridge configuration is considered. Practical hardware realizations are utilized in order to quantify the improvements introduced by the combination of these switches. Furthermore, the MOSFET's current conduction phase is supported by parallel connected IGBTs, which are used in order to further increase the full-bridge's efficiency, as shown by the provided experimental verification.

I. Introduction

High flexibility in energy delivery is a key required feature in the Smart Grid concept [1–3], whereby the electrical energy must be dynamically and efficiently exchanged between distributed sources and loads. In this context, the Solid-State-Transformer (SST) concept represents a powerful enabling technology, given its mains and load side active power circuits which can be actively and dynamically controlled in order to meet with the requirements of the grid operations. Moreover, enabled by the development of semiconductors devices operated with appropriate soft-switching modulation techniques, the SST is able to reach switching frequencies in the Medium-Frequency (MF) range, resulting in compact, light-weight systems, thus complying with the requirements of modern traction solutions [4–6].

Different structures for the construction of the SST have been analysed, including: 1) single-stage; 2) two-stage and 3) three-stage approaches [7]. Given its inherent modularity and

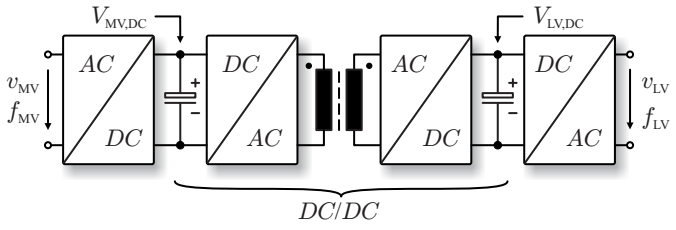

Figure 1: Three-stage Solid-State-Transformer concept comprising high power DC-DC conversion stage operated at Medium-Frequency.

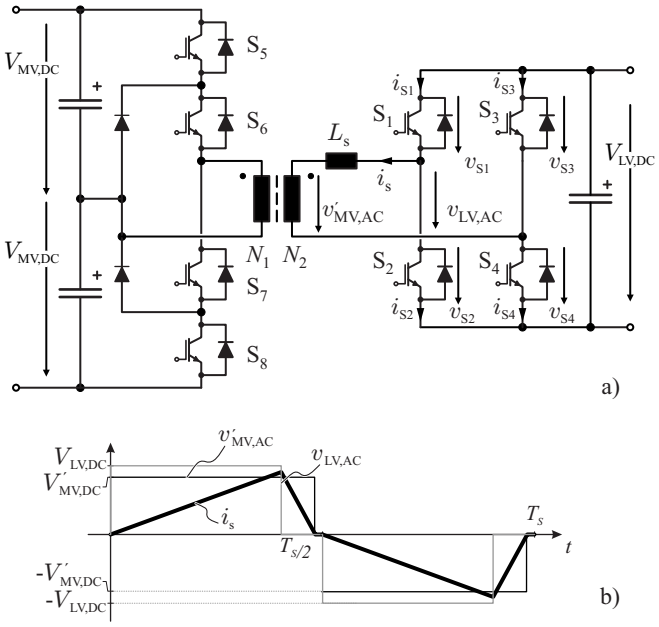

Figure 2: a) DAB comprising neutral-point-clamped-based bridge on the MV side and a full-bridge on the LV side linked by a MF transformer; b) Voltage and current in the transformer for TCM modulation scheme achieving ZCS on the MV side switches.

available Medium-Voltage (MV) and Low-Voltage (LV) DC-links, the three-stage approach has been widely considered [7–9]. This arrangement comprises a MV side rectifier and a LV side inverter linked through a high power DC-DC conversion stage, as shown in Fig. 1. This high power DC-DC converter presents the main challenges in the construction of the SST due to the combination of MF and MV and the required galvanic isolation [10]. In order to reach the desired efficiency goals while still operating at MF, it is often mandatory to operate the MV side semiconductor devices under Zero-Current-Switching (ZCS) conditions.

A commonly considered DC-DC converter topology which fulfils the aforementioned requirements of MF and ZCS operation is the Half-Cycle Discontinuous-Conduction-Mode Series-Resonant-Converter [11, 12]. This converter, however, is characterized by a tight link between MV and LV DC-link voltages, whereby power transfer control is not supported. In cases where power transfer control is required, the

978-1-4673-4916-1/13/$31.00 ©2013 IEEE

Dual-Active-Bridge operated under Triangular-Current-Mode (TCM-DAB) represents an attractive solution. A schematic representation of this converter is shown in Fig. 2-a) whereby the MV side active bridge is built with a Neutral-Point-Clamped (NPC) structure while the LV side converter comprises a full-bridge arrangement. As mentioned earlier, both bridges are linked through a MF transformer in series with inductance L_s. The voltages $v'_{\text{MV,AC}}$ and $v_{\text{LV,AC}}$ on the transformer terminals and the current through the transformer i_s for TCM modulation are shown in Fig. 2-b). By adjusting the phase-shift between the MV and LV side converters and their respective duty cycles together with proper selection of the transformer's turns ratio $n = N_1/N_2$, ZCS of the MV side semiconductors can be ensured for all operating conditions [13]. On the LV side converter however, the peak current must be switched off, leading to considerable switching losses. Moreover, due to the triangular-shaped current, the conduction losses on these semiconductors can also reach high values due to the comparatively high RMS currents.

For these reasons, a full-bridge structure able to efficiently operate under TCM modulation scheme is required. In order to decide on a suitable topology for this bridge, the current and voltage waveforms in each of the LV side switches for the TCM modulation strategy are studied in **Section II**, leading to the proposed bridge structures presented and evaluated in **Section III**. Further improvements to these proposed systems are presented in **Section IV** whereby a summary of the achieved improvements is presented in **Section V**.

II. Triangular-Current-Mode Modulation Scheme

A detailed description of the modulation scheme presented in Fig. 2-b) (power transferred from the LV to the MV side) is described in the following:

- At the beginning of the switching cycle, S_1, S_4, S_5 and S_6 are turned-on, thus the voltage applied to the series inductor is $v_{\text{LV}}(t)$ - $v'_{\text{MV}}(t)$. If the transformer turns ratio $n = N_1/N_2$ is higher than the ratio $V_{\text{MV}}/V_{\text{LV}}$, the current through the inductor L_s increases linearly until the LV side duty cycle is over.
- At this point, S_4 is switched-off and the current freewheels in the LV side through switches S_1 and the antiparallel diode of S_3. The voltage applied to inductor L_s is now -$v'_{\text{MV}}(t)/n$, thus the current is decreasing until it reaches zero at the time the MV side is switched-off with ZCS.
- The operation during the second half-cycle ($t > T_s/2$) is analogous, where, in the LV side, S_2 is used to switch the current off while the freewheeling path is formed by S_3 and the antiparallel diode of S_1.

The currents and voltages in the LV side switches during one switching period are presented in Fig. 3. During the first half cycle, the peak current is switched-off with whereby S_3 is turned on with Zero-Voltage-Switching (ZVS) conditions while S_1 is switched off with zero current. During the second half cycle, switch S_2 is required to turn-off the peak current (ZVS in S_1) while S_3 is switched off with zero current.

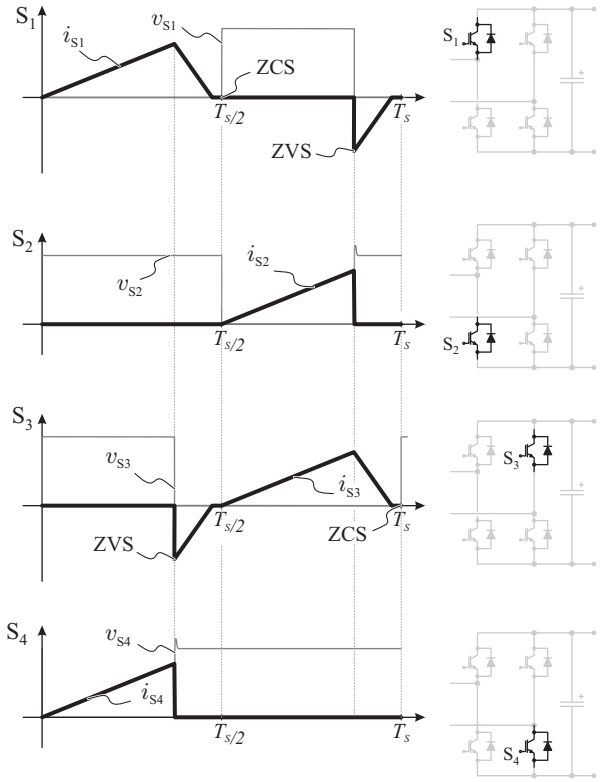

Figure 3: Current waveforms through all LV-side full-bridge switches. The high-side switches S_1 and S_3 are operated in ZCS while the low side switches S_2 and S_4 are operated with ZVS.

Additionally, it can be observed that S_1 and S_3 conduct current during a comparatively longer portion of the switching cycle, in relation to switches S_2 and S_4.

The aforementioned behaviour can be summarized as follows:

- Devices S_1 and S_3, the high-side switches, are operated under ZCS and conduct during a comparatively longer portion of the switching cycle.
- Devices S_2 and S_4, the low side switches, are always operated under soft switching conditions and conduct current during a comparatively shorter period of the switching cycle.

When aiming for a high efficient system, these switching transitions and current waveforms suggest the use of semiconductor devices with good switching performance, e.g. MOSFETs, for the low-side switches S_2 and S_4 and semiconductor devices with good conduction performance, e.g. IGBTs, for the high-side (ZCS operated) switches, i.e. a mixed bridge. The different options for combining these semiconductor devices into a full-bridge together with the hardware realizations and experimental results will be discussed in the next section.

III. Mixed MOSFET/IGBT Bridges

As previously mentioned, a convenient combination of MOSFETs and IGBTs in a full-bridge configuration operated under TCM modulation scheme is as shown in Fig. 4-a) whereby IGBTs are utilized for the high-side switches and MOSFETs for the low-side switches. The modulation scheme

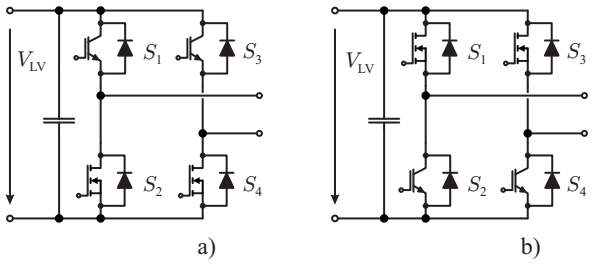

Figure 4: Options for combination of MOSFET and IGBT in a TCM operated full-bridge for reduction of overall losses: a) MOSFETs on the low-side; b) MOSFETs on the high-side.

described in **Section II** can be modified in order to invert the operation of the high-side and low-side switches, i.e. in order to operate the low-side switches S_2 and S_4 with ZCS while allowing the high-side switches S_1 and S_3 to perform the current turn-off. In this case, the arrangement shown in Fig. 4-b) would enable a reduction of the overall bridge losses. This mixed bridge structure and other variations have been previously reported in literature [14–16] mainly for inverter (hard switched) applications. However, the combination of the TCM modulation scheme together with the presented mixed bridge, which enables ZCS operation of IGBTs while the current turn-off is performed only by MOSFETS, has not been previously reported.

In order to quantify the improvement achieved by the combination of MOSFETs and IGBTs in a mixed full-bridge configuration, the arrangement shown in Fig. 4-a) was built considering a $V_{LV} = 400\,\mathrm{V}$ LV side DC-link operated at $f_s = 20\,\mathrm{kHz}$ with a duty cycle duration of $20\,\mu\mathrm{s}$. The peak current to be switched is $1000\,\mathrm{A}$. It should be noted that this voltage level is very favourable for the implementation of the mixed bridge since suitable IGBTs and MOSFETs would be of the $600\,\mathrm{V}$ class, which constitute a very mature semiconductor technology.

Two concepts were considered for the bridge construction: 1) A single device arrangement with discrete MOSFETs and IGBTs and 2) a modular construction whereby the MOSFETs are arranged around an IGBT module.

The single device bridge hardware realization is shown in Fig. 5-a). In this case, the utilized MOSFET is a IPW60R041C6 $650\,\mathrm{V}/77\,\mathrm{A}$ CoolMOS from Infineon while the IGBT is a IKW75N60T $600\,\mathrm{V}/75\,\mathrm{A}$ device from Infineon. These current ratings make it possible to build a mixed full-bridge able to switch $80\,\mathrm{A}$ current peak. Fig. 5-b) shows the full-bridge built based on these devices. As can be seen, in parallel to the low-side MOSFETs, there are parallel-connected IGBTs which are used to further reduce the losses of this bridge, as will be shown in **Section IV**. The layout of the components in the printed circuit board displayed in Fig. 5-a) is presented in Fig. 5-c). The goal of this discrete component construction is the reduction of parasitic effects related to interconnection inductances. In order to switch the $1000\,\mathrm{A}$ peak current however, several of these bridges would be necessary, increasing the complexity of the system. For this reason, a second mixed bridge modular construction is

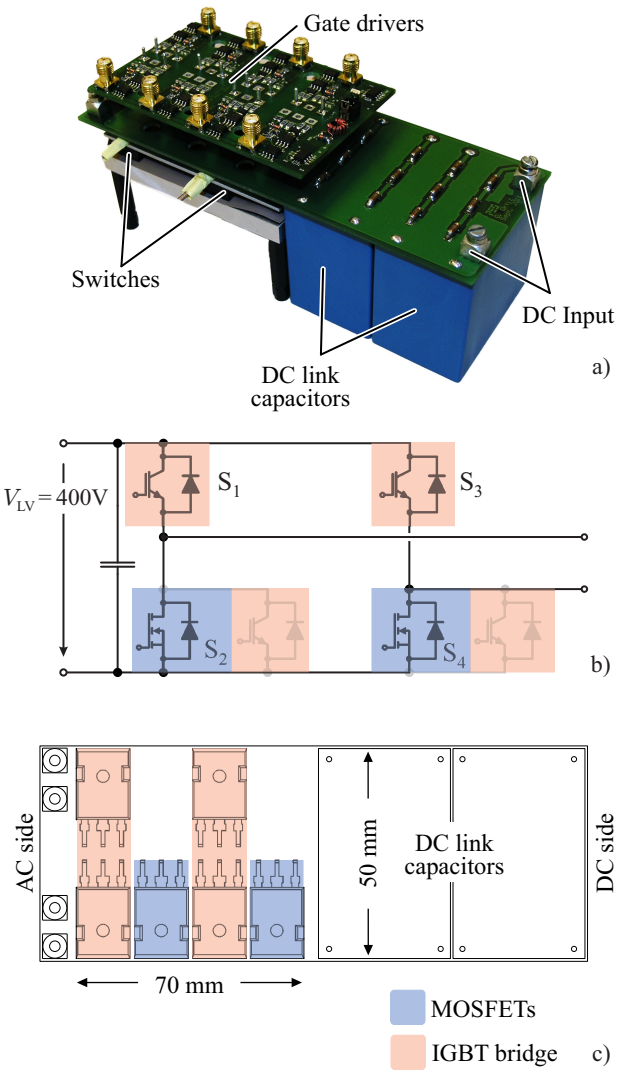

Figure 5: Laboratory prototype arrangement for a single component (discrete MOSFETs and IGBTs) full-bridge: a) Picture of the hardware realization; b) Circuit view of the bridge shown in a); c) Components' layout for the realized hardware shown in a). The MOSFETs and IGBTs are placed in close vicinity in order to reduce the value of the interconnecting parasitic inductance.

also considered.

The hardware realization of the modular mixed bridge configuration is depicted in Fig. 6-a). The utilized IGBT the Infineon FF600R06ME3 $600\,\mathrm{V}/600\,\mathrm{A}$ half-bridge module. In order to match the IGBT module's current driving capability, 8 IPW60R041C6 CoolMos MOSFETS where connected in parallel in order to build S_2 (cf. Fig. 6-b)). As with the single-based mixed bridge, the low-side switch of the IGBT module is only utilized in **Section IV** for further loss reduction. In this case only a bridge leg was built, which was used to realize all experimental tests. Two of these half-bridge legs would be then required to build the complete mixed bridge. The mechanical layout of the module and the MOSFETs is shown in Fig. 6-c) (DC-link capacitors not shown). In addition to the IGBT module and MOSFETs, snubber diodes where placed in order to deal with the fast transients generated by the MOSFETs'

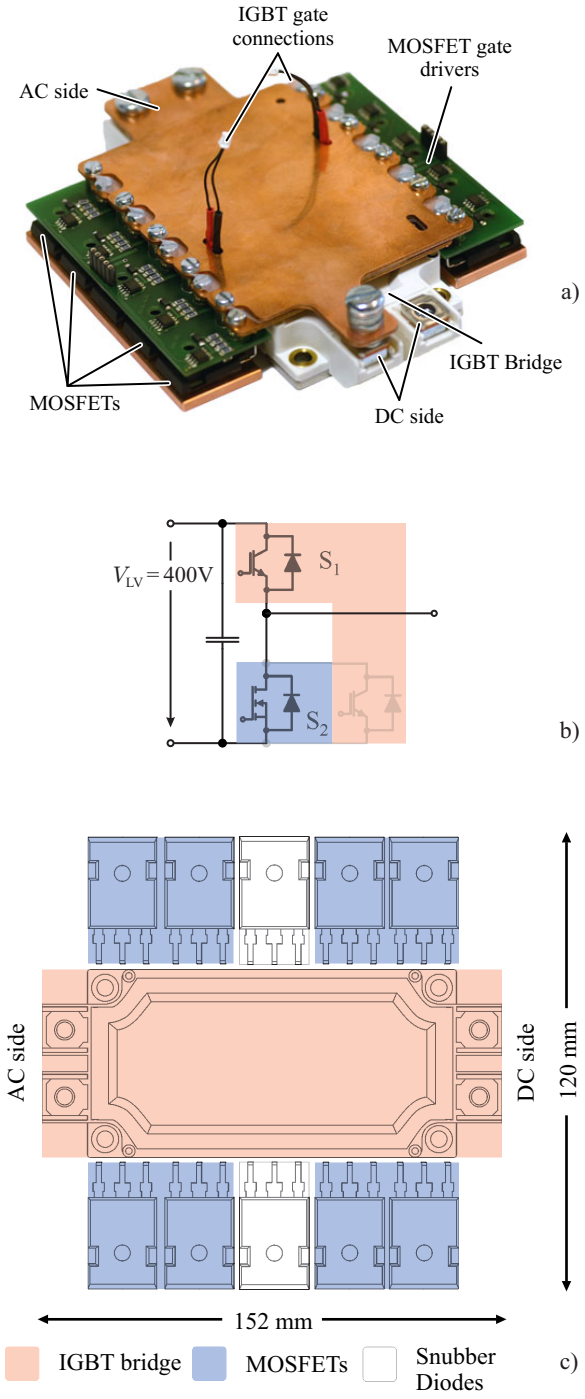

Figure 6: Laboratory prototype arrangement for a module component (discrete MOSFETs arranged around an IGBT module) full-bridge: a) Picture of the hardware realization; b) Circuit view of the bridge shown in a); c) Components' layout for the realized hardware shown in a). Eight MOSFETs are placed around the IGBT module whereby snubber diodes are also introduced in order to reduce the effects of fast transients caused by the MOSFETs' switching.

switching. The modular bridge arrangement has the advantage that only 4 of these mixed half-bridge configurations as shown in Fig. 6-a) would be necessary in order to reach the required current driving capability.

Switching loss measurements at 120 °C junction temperature were performed on the IGBTs and MOSFETs for both constructions. These measurements combined with the datasheet values for output characteristics of the devices were utilized in order to compare the performance of the bridges with respect to full MOSFET and full IGBT realizations (considering the same devices as with the respective mixed bridges). The results are summarized as follows:

Single-based bridge (Fig. 5-a)):

- Full MOSFET: 512 W
- Full IGBT: 320.53 W
- Mixed bridge: 250.1 W

Module-based bridge (Fig. 6-a)):

- Full MOSFET: 2500 W
- Full IGBT: 1802 W
- Mixed bridge: 1220 W

As can be seen, a reduction of ca. two times in the losses compared to the full MOSFET construction is achieved for both single and modular based constructions when considering the proposed mixed bridge arrangement, rendering this concept suitable for high-power DC-DC converters operated with TCM modulation schemes. These results will be summarized in **Section V** together with the outcome of further loss reduction strategy introduced in the next section.

IV. Conduction Enhancement through MOSFET/IGBT Parallel Connection

In order to further improve the performance of the presented mixed-bridge under TCM modulation scheme, the MOSFETs of this bridge can be assisted by parallel connected IGBTs which support the conduction phase of the MOSFET, providing an additional low resistive path for the current, thus reducing the overall conduction losses. This solution is often called hybrid-switch and has been previously proposed in [17–20] for inverter solutions, whereby all switches in the bridge are composed of parallel connected IGBTs and MOSFETs. The resulting bridge with the IGBT assisted conduction is shown in Fig. 7-a).

The experimental prototype bridges presented in **Section III** already include the additional parallel connected IGBT introduced in Fig. 7-a), hence the experimental testing of this concept at 120 °C junction temperature was also verified. The operation of the mixed bridge with hybrid switch is explained with Fig. 7-b), where the experimental waveform for one operating point of the single-based bridge is presented. This figure shows the current waveform of the hybrid switches in Fig. 7-a), corresponding to devices S_2 and S_4 in Fig. 3.

In the following, switches $S_{2,1}$ and $S_{2,2}$ will be used to explain the bridge's operation. The behaviour of $S_{4,1}$ and $S_{4,2}$ is analogous. At the beginning of the switching cycle ($t = 5\,\mu s$ in Fig. 7-b)), both the MOSFET $S_{2,1}$ and the IGBT $S_{2,2}$ are

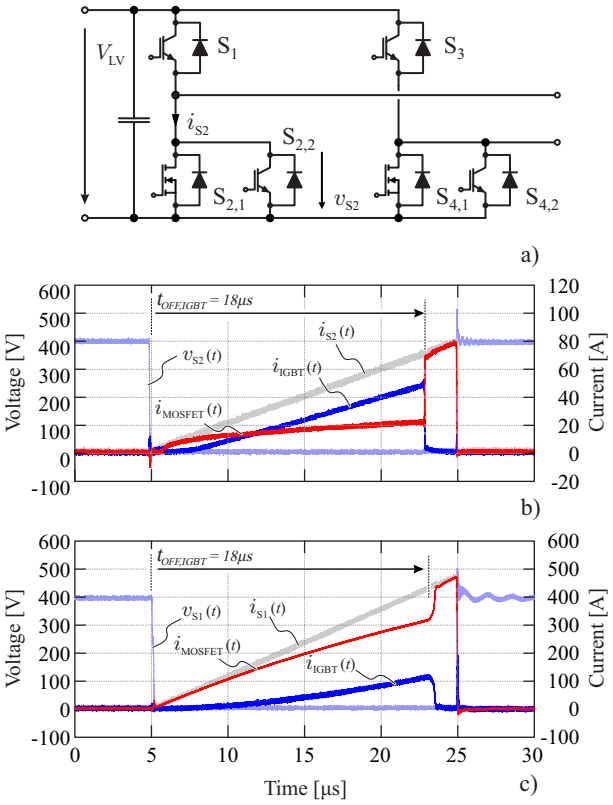

Figure 7: a) Mixed full-bridge comprising IGBTs in parallel with the low-side MOSFETs in order to reduce the conduction losses of the bridge; b) Experimental waveform of the hybrid switch in the single-based prototype with an IGBT turn-off time of $t_{\text{OFF,IGBT}} = 18\,\mu\text{s}$; c) Experimental waveform of the hybrid switch in the module-based prototype with an IGBT turn-off time of $t_{\text{OFF,IGBT}} = 18\,\mu\text{s}$;

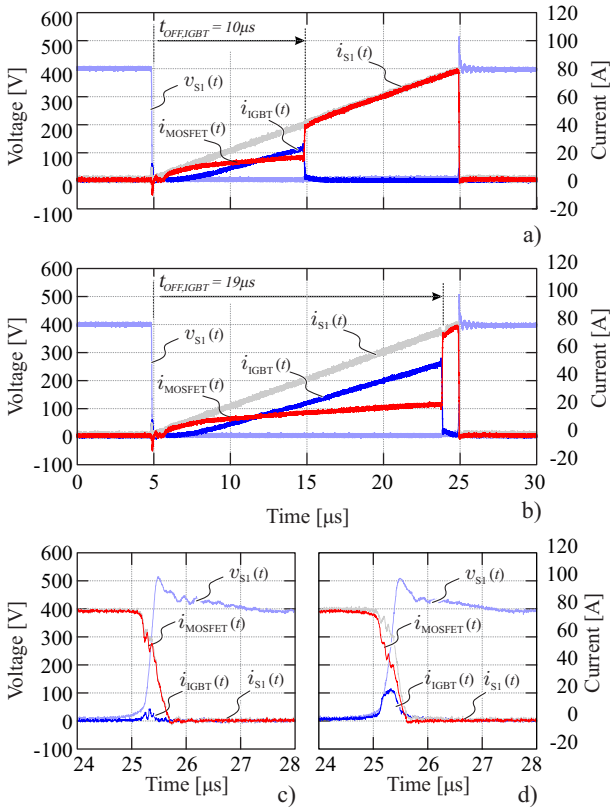

Figure 8: Trade-off encountered with the selection of $t_{\text{OFF,IGBT}}$. When selected short as in a), the MOSFET conduction losses are increased while the IGBT's switching losses are reduced, as seen in c) where a detailed view of the switching process of a) is shown. In the other hand, if $t_{\text{OFF,IGBT}}$ is chosen large as in b), the conduction losses of the MOSFET become considerably and switching losses are encountered in the IGBT, as shown by the current spike in the IGBT's current in d).

turned on. Assuming S_3 was previously in on state from the freewheeling interval, the output current flows through both the IGBT and the MOSFET, providing two parallel paths for the current, leading to reduced conduction losses. Before the end of the respective duty cycle (20 µs in Fig. 7-b)), the IGBT is turned off, thus the load current is entirely commutated to the MOSFET. Virtually no losses are generated during this commutation since the MOSFET is on state, keeping the IGBT's blocking voltage close to zero. At the end of the duty cycle, the MOSFET performs the turn-off of the current, thus generating comparatively low switching losses.

The result of the aforementioned switching strategy for the hybrid switch is the optimal utilization of the available semiconductor devices, whereby mainly the IGBT is utilized for the conduction of current and the MOSFET is in charge of the current switch-off.

The module-based mixed-bridge comprising the introduced hybrid-switch was also tested under these conditions, the results of this test are displayed in Fig. 7-c). In this case, the parasitic components present in the IGBT-MOSFET connection result in an unfavourable current sharing, as will be explained later in this section.

The selection of the time $t = t_{\text{OFF,IGBT}}$ at which the IGBT turns off affects the sharing of losses in the parallel connected MOSFET and IGBT. This phenomenon is explained through Fig. 8. If $t_{\text{OFF,IGBT}}$ is selected short, as presented Fig. 8-a) for $t_{\text{OFF,IGBT}} = 10\,\mu\text{s}$, the MOSFET would conduct for a comparatively long portion of the switching cycle, leading to higher conduction losses due to the higher on state resistance in comparison to the IGBT. On the other hand, if $t_{\text{OFF,IGBT}}$ is made long, as shown in Fig. 8-b) for $t_{\text{OFF,IGBT}} = 19\,\mu\text{s}$, the best utilization of the switches' conduction potential is achieved, whereby the MOSFET only conducts the full load current during a small portion of the duty cycle.

In this last case however, switching losses are encountered in the IGBT due to the limited time available for recombination of its internal charge carriers [21]. This effect is seen in Fig. 8-d) where a detailed view of the MOSFET turn-off process for the case presented in Fig. 8-a) is depicted. As can be seen, a visible current spike through the IGBT is present during the turn-off process of the MOSFET, leading to switching losses in the IGBT. It should be noted that this current spike in the IGBT's current is not present when observing Fig. 8-d), corresponding to the detailed MOSFET's switching process for the conditions presented in Fig. 8-b).

As a consequence, the selection of the time $t = t_{\text{OFF,IGBT}}$ at which the IGBT turns off is a trafe-off between MOSFET conduction losses and IGBT switching losses and its optimized

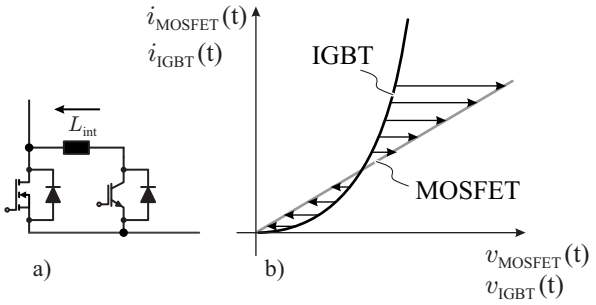

Figure 9: Effect of parasitic inductance in interconnection of the IGBT and MOSFET shown in a). The output characteristics of the MOSFET and IGBT shown in b) deteriorates the performance of the hybrid-switch as a result of the uneven current sharing between the two devices.

value results from the minimization of the overall losses of the mixed bridge.

Since the modelling of the IGBT's internal charge dynamic requires semiconductor parameters not available in the device's datasheet, this optimization was experimentally performed for the single and module-based bridges by measuring the total conduction and switching losses of both MOSFET and IGBT while increasing stepwise the value of $t_{\text{OFF,IGBT}}$ starting from $t_{\text{OFF,IGBT}} = 0$. In case of the single based bridge, this optimal timing is $t_{\text{OFF,IGBT}} = 19\,\mu\text{s}$ leading to total losses of $170.9\,\text{W}$. In case of the module-based bridge, the optimal timing is $t_{\text{OFF,IGBT}} = 17\,\mu\text{s}$ resulting in $1173\,\text{W}$ of losses.

As shown in Fig. 7-c), the current sharing between the MOSFET and the IGBT presents slow dynamics. This phenomenon is related to parasitic inductances in the interconnection between the MOSFET and the IGBT, as analyzed in [17]. Fig. 9 can be used to explain this effect. The output characteristics of the MOSFET and IGBT show that as long as the current is low, it is conducted by the MOSFET, since it offers lower impedance for the current (cf. Fig. 9-b)). As the current increases, the voltage drop in the MOSFET becomes higher than in the IGBT, thus the current starts to commutate to the IGBT as seen at the beginning of the conduction phase of the single-based bridge (cf. Fig. 7-b)). However, the parasitic inductance L_{int} in the interconnection of the MOSFET and IGBT increases the time required to commutate the current from the MOSFET to the IGBT, given the relatively small voltage applied to it, which is only the difference between the IGBT and MOSFET forward voltage drops.

In order to overcome this problem, a delay $t_{\text{ON,MOSFET}}$ in the turn-on signal of the MOSFET is introduced, leaving only the IGBT conducting for a portion of the duty cycle. This way, the MOSFET is only turned on when the IGBT offers a lower impedance path for the current, improving the current sharing between these two devices.

The delay $t_{\text{ON,MOSFET}}$ introduces a new degree of freedom in the operation of the hybrid switch, whereby a two-dimensional optimization ($t_{\text{OFF,IGBT}}$ and $t_{\text{ON,MOSFET}}$) is required in order to find the values of these two variables which minimize the total losses of the bridge. This optimization was performed for both single and module-based mixed bridges by stepwise modifying

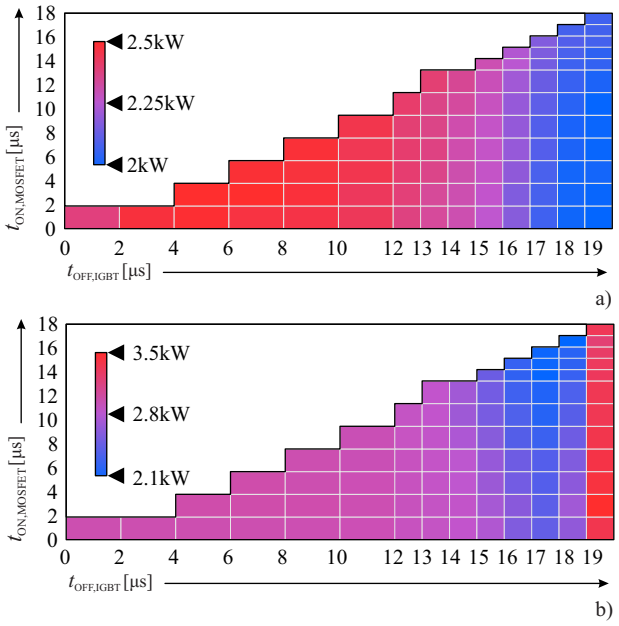

Figure 10: Two dimensional optimization for the switching times $t_{\text{OFF,IGBT}}$ and $t_{\text{ON,MOSFET}}$, aiming for minimization of overall bridge losses: a) Single-based bridge; b) Module-based bridge.

the values of $t_{\text{OFF,IGBT}}$ and $t_{\text{ON,MOSFET}}$ while measuring all switching and conduction losses. The results of this sweep are found in Fig. 10-a) and b) for the single and modular-based bridges respectively. Here, the values for losses are scaled in order to reach the desired $1000\,\text{A}$ peak current with both bridges.

For the single-based bridge, the optimized timings correspond to $(t_{\text{OFF,IGBT}}, t_{\text{ON,MOSFET}}) = (19\,\mu\text{s}, 4\,\mu\text{s})$. The good current sharing already available in this bridge due to the comparatively small achieved parasitic components leads to a small value $t_{\text{ON,MOSFET}}$ in this case. On the other hand, the high value of $t_{\text{OFF,IGBT}}$ is related to a fast recombination process in the IGBT.

For the module based bridge this optimal switching times correspond to $(t_{\text{OFF,IGBT}}, t_{\text{ON,MOSFET}}) = (18\,\mu\text{s}, 14\,\mu\text{s})$. The value of $t_{\text{ON,MOSFET}}$ is comparatively large due to the larger parasitics encountered in this construction, given the larger dimensions of the bridge (cf. Fig. 6). As a consequence, in order to achieve a current sharing that ensures minimal losses, the conducted current of the IGBT is increased by increasing the value of $t_{\text{ON,MOSFET}}$. It should also be noted that the value of $t_{\text{OFF,IGBT}}$ is smaller in comparison to the single-based construction, phenomena possibly related to the longer recombination time constant of the module's semiconductor in comparison to the discrete IGBTs of the single-based arrangement.

The final waveforms for the aforementioned optimized values of $t_{\text{OFF,IGBT}}$ and $t_{\text{ON,MOSFET}}$ are shown in Figs. 11-a) and b) for the single and module based bridges respectively. The final results of this optimization compared to the other presented realizations are discussed in the next section.

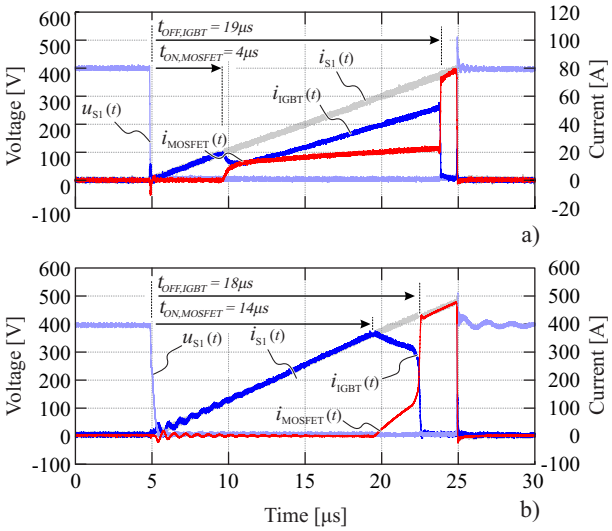

Figure 11: Waveforms for the a) single-based and b) modular-based bridges with their respective optimized switching times $t_{\text{OFF,IGBT}}$ and $t_{\text{ON,MOSFET}}$.

V. Summary and Comparative Evaluation

The analysed mixed MOSFET/IGBT full-bridges posses different current ratings due to utilized components in each realization. In order to compare the modular and single based constructions with respect to losses, the obtained results are scaled in order to reach the desired current driving capability of 1000 A with both modular and single based constructions.

Fig. 12 shows a summary of these scaled loss values for the different bridge realizations and switching time optimizations discussed in the previous sections. Taking a full MOSFET realization (all four switches of the full-bridge implemented with MOSFETS) as reference system, a loss reduction higher than 50 % is obtained in both module and single based constructions by implementing the mixed bridge presented in Fig. 4-a). In the single-based realization (cf. Fig. 5), the adjustment of the switching times ($t_{\text{OFF,IGBT}}$ and $t_{\text{ON,MOSFET}}$) leads to a total reduction of 68 % with respect to the full MOSFET realization.

In the module based mixed bridge (cf. Fig. 6) the additional loss reduction achieved with the introduction of the hybrid switch is comparatively low with respect to the mixed bridge arrangement. This is due to the large value of the interconnecting inductance L_{int} in this construction, which does not allow the parallel utilization of the MOSFET and IGBT capabilities during the conduction phase.

VI. Conclusion

SSTs are envisioned as the key enabling technology for modern traction solutions and the Smart Grid. In these SSTs, often an isolated DC-DC converter is utilized to transfer power from the MV to LV side converters. Due to the combination of MF and MV, it is often mandatory to operate these DC-DC converters with ZCS modulation schemes. The TCM modulation strategy provides this functionality while also enabling the active control of the transferred power between the MV and LV sides.

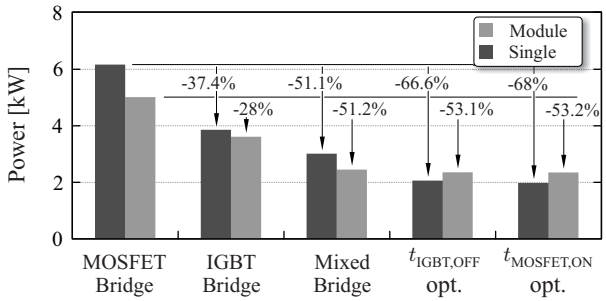

Figure 12: Summary of the obtained losses for the different considered full-bridges and the reduction reached with the introduced combination of IGBT and MOSFET.

When closely observing the current waveforms through the LV side converter switches, it is found that full-bridge built with a combination of MOSFETs and IGBTs exploits the best characteristics of these devices by utilizing the good conduction behaviour of the IGBT with the outstanding switching performance of MOSFETs. Two prototypes, a discrete component and a module-based approach, considering this mixed bridge concept were constructed in order to quantify the potential benefit of this mixed MOSFET/IGBT bridge, resulting in ca. 50 % less losses when compared to a pure MOSFET realization.

Further loss reduction is achievable by assisting the MOSFETs'conduction phase with a parallel connected IGBT, building a hybrid-switch. In this case, two degrees of freedom, the IGBT's turn off and the MOSFET's turn on time, are available for minimizing the bridge's losses. This optimization leads to a 68 % loss reduction in case of the single-based bridge with respect to a pure MOSFET realization. In case of the modular arrangement, the parasitic inductance present in the IGBT/MOSFET connection given by the larger dimensions of the prototype, result in poor current sharing between the IGBT and the MOSFET during the conduction phase, rendering the hybrid-switch approach less attractive for a modular construction.

References

[1] A. Huang, M. Crow, G. Heydt, J. Zheng, and S. Dale, "The Future Renewable Electric Energy Delivery and Management (FREEDM) System: The Energy Internet," in , *Proc. of the IEEE*, 2011, pp. 133–148.

[2] D. Borojevic, I. Cvetkovic, D. Dong, R. Burgos, F. Wang, and L. F., "Future Electronic Power Distribution Systems - A Contemplative View," in *Proc. of the Intern. Conf. on Optimization of Electr. and Electronic Equipment (OPTIM)*, 2010, pp. 1369–1380.

[3] J. Wang, A. Huang, W. Sung, Y. Liu, and B. Baliga, "Smart grid technologies," *IEEE Industrial Electronics Magazine*, vol. 3, pp. 16–23, 2009.

[4] B. Engel, M. Victor, G. Bachmann, and A. Falk, "Power Electronics Technologies for Railway Vehicles," in *Proc. of the Power Conversion Conference*, 2007, pp. 1388–1393.

[5] M. Pitterman, P. Drabek, M. Cedl, and J. Fort, "The Study of Using the Traction Drive Topology with the Middle-Frequency Transformer," in *Proc. of the International Power Electronics and Motion Control Conference*, 2008, pp. 1593–1597.

[6] D. Dujic, F. Kieferndorf, and F. Canales, "Power Electronics Transformer Technology for Traction Applications - An Overview," in *Proc. of the International Conference on Power Electronics and Motion Control Conference*, 2012, pp. 636–642.

[7] L. Heinemann and G. Mauthe, "The universal power electronics based distribution transformer, an unified approach," in *Annual Power Electronics Specialists Conference*, 2001, pp. 504–509.
[8] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Power and Energy Society General Meeting*, 2010, pp. 1–8.
[9] J. Clare, "Advanced power converters for universal and flexible power management in future electricity networks," in *European Conference on Power Electronics and Applications*, 2009, pp. 1–29.
[10] S. Inoue and H. Akagi, "A bi-directional isolated dc/dc converter as a core circuit of the next-generation medium-voltage power conversion system," in *Power Electronics Specialists Conference*, 2006, pp. 1–7.
[11] C. Zhao, S. Lewdeni-Schmid, J. Steinke, M. Weiss, T. Chaudhuri, M. Pellerin, J. Duron, and P. Stefanutti, "Design, implementation and performance of a modular power electronic transformer (pet) for railway application," in *Power Electronics and Applications*, 2011, pp. 1–10.
[12] J. Huber, G. Ortiz, F. Krismer, N. Widmer, and J. W. Kolar, "Etha-rho pareto optimization of bidirectional half-cycle discontinuous-conduction-mode series-resonant dc/dc converter with fixed voltage transfer ratio," in *Applied Power Electronics Conference and Exposition*, 2013, pp. 1413–1420.
[13] N. Schibli, "Symmetrical multilevel converters with two quadrant DC-DC feeding," Ph.D. dissertation, EPFL, 2000.
[14] Y. Jiang, G. Hua, E. Yang, and F. Lee, "Soft-switching of igbts with the help of mosfets in bridge-type converters," in *Power Electronics Specialists Conference*, 1993, pp. 151–157.
[15] J. Qian, A. Khan, and I. Batarseh, "Turn-off switching loss model and analysis of igbt under different switching operation modes," in *Industrial Electronics, Control, and Instrumentation*, vol. 1, 1995, pp. 240–245.
[16] M. Frisch and T. Ernö. (2010) Innovative topologies for high efficient solar applications. [Online]. Available: http://www.vincotech.com/news/articles.html
[17] K. Hoffmann and J. Karst, "High frequency power switch - improved performance by mosfets and igbts connected in parallel," in *Power Electronics and Applications*, 2005, p. 11.
[18] J. Kaerst and K. Hoffmann, "High speed complementary drive of a hybrid mosfet and igbt power switch," in *Power Electronics and Applications*, 2005, p. 9.
[19] S. Woothipatanapan, A. Jangwanitlert, and P. Chancharoensook, "Efficiency improvement of converter for switched reluctance motor drives by mixed parallel operation of igbt and mosfet," in *TENCON 2010*, 2010, pp. 1841–1846.
[20] D. Chen and S. A. Chin, "Bipolar-fet combinational power transistors for power conversion applications," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 20, no. 5, pp. 659–664, 1984.
[21] G. Ortiz, H. Uemura, D. Bortis, J. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of igbts in high-power high-efficiency dual-active-bridge dc/dc converters," *IEEE Transactions on Electron Devices*, vol. 60, no. 2, pp. 587–597, 2012.