On-State Voltage Measurement of Fast Switching Power Semiconductors

Mattia Guacci, Dominik Bortis, and Johann W. Kolar

***Abstract*—The on-state resistance $R_{ds,on}$ is a key characteristic of unipolar power semiconductors and its value depends on the operating conditions, e.g. junction temperature, conducted current and applied gate voltage. Hence, the exact determination of the $R_{ds,on}$ value cannot rely on datasheet information and requires the measurement of current and on-state voltage during operation. Besides the determination of the conduction losses, the on-state voltage measurement enables dynamic $R_{ds,on}$ analysis, device temperature estimation, condition monitoring and consequently time-to-failure prediction. However, in contrast to a switch current measurement, several challenges arise in the design of an on-state voltage measurement circuit (OVMC), i.e. high measurement accuracy (mV-range) during on-state, high blocking voltage capability (kV-range) during off-state and fast dynamic response (ns-range) during switching transitions are demanded. Different OVMC concepts are known from IGBT applications, however, the more severe requirements introduced from the high switching frequency and low OV characterizing the operation of fast switching power semiconductors, prevent their usage. Off-the-shelf products hardly satisfy the mentioned specifications, whereas the performance of state-of-the-art OVM research prototypes require further investigations and/or improvements. With this aim, an innovative OVMC concept is designed, analyzed, calibrated and tested in this paper. Furthermore, the conduction losses of different power semiconductors are measured as function of their operating conditions to validate the performance and highlight the potential of the proposed OVMC.**

***Index Terms*—Conduction loss measurement, on-state resistance, on-state voltage measurement circuit.**

I. Introduction

TODAY, the detailed experimental analysis of a power converter circuit is typically focused on the switching behavior of the power semiconductors, e.g. switching overvoltages and voltage oscillations occurring in hard-switching [1] and/or switching voltage and current time displacement relative to zero-voltage switching (ZVS) [2]. However, with the increasing switching speed enabled by wide bandgap devices and/or with employing ZVS concepts, the loss contribution of the semiconductors is more and more dominated by the conduction losses.

Manuscript received February 1, 2018. This work was supported by the Swiss State Secretariat for Education, Research and Innovation (SERI) under contract number 15.0161. The opinions expressed and arguments employed herein do not necessarily reflect the official views of the Swiss Government. (*Corresponding author: Mattia Guacci.*)

The authors are with Power Electronic Systems Laboratory, ETH Zurich, Switzerland (e-mail: guacci@lem.ee.ethz.ch).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00016

The power converter operating conditions are significantly influencing the occurring conduction losses. Junction temperature, conducted current, applied gate voltage, switching frequency, manufacturing variability and aging take, in fact, a combined impact on the instantaneous value of the semiconductors on-state resistance $R_{ds,on}$. Despite this premise and contrary to switching loss analysis, no on-state behavior analysis and/or no experimental verification of the calculated $R_{ds;on}$ value is typically carried. Hence, worst-case approximations, based on datasheet information, are inferred to estimate the conduction losses. Performing online $R_{ds,on}$ measurements would allow to accurately verify conduction loss calculations and hence to improve optimization procedures for the design of power converters [3], [4]. In order to achieve this, the voltage across and the current through the device-under-test (DUT) have to be measured accurately and simultaneously. Several solutions are suitable to obtain the DUT current, i.e. it can be directly measured (e.g. with a series connected current shunt) or indirectly derived from the load current and the gate signals, both available for control purposes. In contrast, the usage of conventional voltage probes to accurately measure the DUT on-state voltage (OV) is prevented from the resulting dynamic range, i.e. the ratio between the maximum voltage (during off-state) and the minimum voltage (during on-state) applied at the input of the measurement circuit. The extreme required dynamic range limits the measurement resolution. This can be understood considering an example. If a conventional 12-bit oscilloscope is set to capture the voltage blocked (e.g. 1000 V) from a specimen power MOSFET (e.g. $R_{ds,on}$= 25 mΩ), the least significant bit, i.e. the measurement resolution, corresponds to $1000\ V/2^{12} \approx 250$ mV. This voltage is already half the OV of the mentioned MOSFET conducting 20 A (25 mΩ · 20 A = 500 mV) and the resulting accuracy is definitely insufficient. Ideally, in order to perform this measurement with an accuracy of 1%, the least significant bit should correspond to 5 mV (0.01 · 500 mV); in other words, an 18-bit oscilloscope ($1000\ V/2^{18} \approx 4$ mV) would be required [5]. Alternatively, the conventional oscilloscope full-scale voltage would have to be limited to 20 V ($20\ V/2^{12} \approx 5$ mV). The full-scale voltage reduces to 1 V if the same accuracy is desired while measuring only 1 A (25 mΩ · 1 A = 25 mV, 0.01 · 25 mV = 0.25 mV and 0.25 mV · 2^{12} = 1 V). However, if the oscilloscope range is limited to measure the sole OV (e.g. 1 V), the overdrive of the oscilloscope amplifiers caused by the voltage blocked in off-state significantly distorts the measurements and could damage the instrument.

It results clear that the achievable accuracy is insufficient because of the trade-off with the excessive dynamic range. Therefore, only dedicated on-state voltage measurement cir-

cuits (OVMCs), limiting the voltage during off-state to values within the oscilloscope input voltage range, allow accurate measurements during on-state. For example, a full-scale voltage of 10 V guarantees a measurement resolution of 10 V/$2^{12} \approx 2.5$ mV, sufficient in most cases.

Beside accuracy and resolution, also the bandwidth of OVMCs is of importance, since modern Gallium-Nitride (GaN) semiconductors often present dynamic $R_{ds,on}$ effects [6], [7], i.e. a high initial (i.e. immediately after a turn-on switching transition) $R_{ds,on}$ value which slowly (i.e. with time constants varying in the µs-range) settles to a constant value. In order to characterize this phenomenon, OVMCs should measure the correct OV immediately after the turn-on transition of the DUT. The dynamic $R_{ds,on}$ is a fundamental figure-of-merit in the evaluation of GaN semiconductors and it depends on the voltage blocked during off-state, as well as on the switching frequency [7]-[9]. Being this information not specified in the datasheet, the importance of the experimental on-state behavior analysis is remarked.

In addition to dynamic and stationary OV analysis, other application areas are envisaged in literature, resulting in requirements of an ideal OVMC. The OV is a promising temperature sensitive electrical parameter, i.e. a circuit parameter ensuring high sensitivity and good linearity with respect to temperature variations [10]. Measuring the OV offers the potential for replacing conventional temperature measurements in application with severe volume constraints. Furthermore, the OV is identified as a favorable aging indicator. E.g. in power modules, a crack in the metallization layer and/or the lift-off of a bond-wire cause an increase of the $R_{ds,on}$ value, i.e. of the OV [11], [12]. This establishes a positive feedback mechanism accelerating the aging process. Monitoring the OV allows a detection of the failure and potentially time-to-failure predictions, advantageous e.g. in reliability critical or remote applications. Accordingly, a trend towards intelligent gate drivers integrating OVMCs is traced [13] and, to facilitate this, compactness is generally demanded. As well the mentioned bandwidth requirement, associated to a fast dynamic response of the OVMC after a switching transition, is of importance in all the foreseen application areas, if fast switching semiconductors are considered.

Finally, the online measurement of conduction losses enabled by OVMCs can significantly improve the measurement accuracy of calorimetric switching loss measurement methods [14]-[16]. This application is commented in detail in Section IV-C, since it constitutes a main reason for this research work. Summarizing, high accuracy, fast dynamic response, low complexity, and high compactness are the desirable characteristics of OVMCs.

The nowadays most common OVM approaches can be traced back more than thirty years [17], [18]. Recently, the increased interest of the power electronic community in wide bandgap semiconductors, combining reduced $R_{ds,on}$ values with increased switching speeds, motivated the interest to derive solutions offering better accuracy and higher bandwidth, e.g. [19] and [20], where also a comprehensive

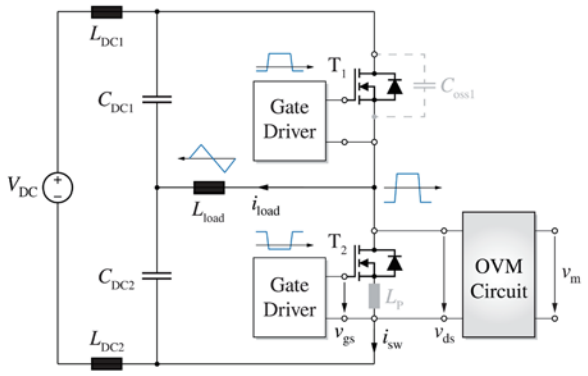


Fig. 1. Power converter setup considered as reference for the overall analysis. The two power semiconductors in half-bridge configuration T_1 and T_2 are operated with complementary 50% duty cycles. The output inductor L_{load} tapped to the split DC link capacitors C_{DC1} and C_{DC2} ensures symmetric triangular current mode (TCM) operation (blue waveforms). The parasitic inductance L_P and parasitic output capacitance of T_1 (i.e. C_{oss1}) are as well shown. An OVMC (gray) is connected in parallel to the low-side semiconductor T_2, enabling online $R_{ds,on}$ measurements.

overview of the state-of-the-art is discussed. However, these concepts still reveal limited performance: [20] suffers significantly from noise and common-mode disturbances, and is tested only at high OV values, while [18] and [19] have an intrinsic accuracy limitation, i.e. an unknown diode forward voltage drop in the OVM path, as discussed in Section II. A solution to the latter issue is proposed in [12], where a novel OVMC is presented to monitor the wear-out of high power IGBT in power modules. Unfortunately, the performance of this OVMC highlighted in [12], [21], [22] and the provided guidelines are insufficient and inadequate for fast switching power semiconductors, especially in terms of bandwidth and dynamic response. Significant distortions are introduced from this OVMC at its output for tens of µs and also the settling time of the designed analog circuitry itself is already in the range of 1 µs, i.e. comparable to a conduction period of a device operating with a switching frequency in the hundreds of kHz-range. Moreover, with respect to IGBTs, where the OV is rarely below 500 mV, when considering fast switching semiconductors with $R_{ds,on}$ values in the mΩ -range, it results significantly more challenging to guarantee the same OVM accuracy. Only limited information on the accuracy are provided in [12] and the performed OVMs are not completely validated with an alternative setup. Nevertheless, this OVMC is considered as a promising solution for the foreseen achievable accuracy enabled by the correction of the unknown diode forward voltage drop in the OVM path. Lately, also OVM probes became commercially available [23], [24], aiming to replace OVM integrated circuits [25]. A commercial solution is tested, but poor dynamic performance is experienced, as commented in Section III-D. Consequently, it results necessary to develop an OVMC able to satisfy all above-mentioned requirements in order to cover all applications.

The reference setup, supporting the analysis presented in this paper, is shown in Fig. 1. It highlights an OVMC (gray)

connected to the low-side power semiconductor (i.e. T_2, the DUT) of an half-bridge configuration. The same circuit could be connected to the high-side T_1, however, for simplicity, only the depicted solution is analyzed in the following. Different power semiconductors are then selected for T_2, enabling their comparison.

The proposed OVMC is presented in Section III, where the achieved accuracy and bandwidth are verified through measurements on a calibrated test-bench. Afterwards, the turnon behavior of different Silicon (Si), Silicon-Carbide (SiC) and Gallium-Nitride (GaN) power semiconductors is experimentally analyzed, validating the dynamic performance of this OVMC. The main challenges faced during the online measurement of conduction losses are commented in Section IV-A, anticipating the measurement results discussed in Section IV-B (conduction losses) and Section IV-C (switching losses). Conclusions are presented in Section V.

II. Conventonal On-State Voltage Measurement Circuits

The schematics depicted in Fig. 2 show the two most common implementations of OVMCs. They ideally perform as a shortcircuit (i.e. $v_{ds} \approx v_{1,a}$ and $v_{1,b}$) when the power transistor T_2 (i.e. DUT, see Fig. 1) is conducting (on-state) and as an open-circuit when it is blocking the DC-link voltage V_{DC} (offstate). As explained in the introduction, the accuracy of v_1 during on-state and the dynamic performance of the transition between the two states are the most important figures-of-merit of an OVMC. These two approaches are compared according to these criteria in the rest of this section. The final aim is to highlight their respective advantages in order to facilitate the design of a better performing solution.

The OVMC illustrated in Fig. 2(a) [18] is based on the MOSFET T_p. The gate of T_p is connected to a voltage source V_p and when T_p is in on-state, i.e. $V_p > v_{1,a} + V_{th,Tp}$, the measured voltage

$$v_{1,a} = \frac{R_1}{R_1 + R_{T_p}} v_{ds}. \tag{1}$$

$V_{th,Tp}$ and R_{Tp} are the threshold voltage and the on-state resistance of T_p, respectively. Typically $R_{Tp} \ll R_1$, therefore $v_{1,a} \approx v_{ds}$. Regarding the transition between the two states, two control strategies are possible:

- *active*: V_p is switched to 0V before T_2 is turned off and back to V_p after T_2 is completely turned on;
- *passive*: V_p is kept constant and T_p operates in its linear region during the off-state of T_2.

The active solution is intuitively effective but increases the complexity of this OVMC, e.g. logic and delay circuitry between the gate drivers of T_2 and T_p results necessary and introduces a blanking time. Therefore, the less intuitive passive solution is preferred and herein considered, however additional challenges need to be faced [20].

The OVMC of Fig. 2 (b) [17] is realized with the diode D_1 instead of the MOSFET T_p. When $v_{ds} < V_p - V_{fv,D1}$, D_1 conducts and

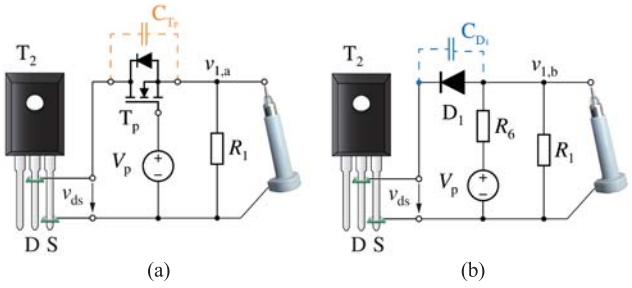


Fig. 2. Schematic representation of the two most common implementations of OVMCs. The input voltage v_{ds} is sensed at the DUT leads (see Fig. 1); by means of the MOSFET T_p (a) or of the diode D_1 (b), the output is decoupled during the DUT off-state and connected during its on-state. While the dynamic performance of (a) are affected from C_{T_p}, the accuracy of (b) is compromised by v_{D1}.

$$v_{1,b} = v_{ds} + v_{D_1}(T_{D_1}, i_{D_1}). \tag{2}$$

$V_{fv,D1}$, T_{D1} and i_{D1} are the forward voltage, the junction temperature and the current of D_1 respectively. During off-state, $v_{1,b}$ is fixed from V_p and D_1 naturally blocks V_{DC}. Differently from (1), a significant error term (i.e. v_{D1} in the range of hundreds of mV) appears in (2), causing an offset on $v_{1,b}$. As specified in (2), v_{D1} is function of T_{D1} and i_{D1} , however, an approximate value is commonly subtracted from $v_{1,b}$ to obtain v_{ds} [18], [19]. This only partially compensates it and compromises the accuracy of the measurement. Nevertheless, this OVMC is often preferred (e.g. in desaturation circuits) to the one previously described, giving lower importance to the achievable accuracy than to hardware complexity and dynamic performance. The latter aspect is the focus of the following paragraph.

The transition between the two DUT states, i.e. the commutation of the half-bridge (Fig. 1), implies charge and discharge of the parasitic output capacitances of T_1 and T_2 (i.e. C_{oss1} and C_{oss2} in Fig. 1) as well as of the input capacitance of the OVMCs. In fact, C_{T_p} (orange in Fig. 2(a)) and C_{D_1} (blue in Fig. 2(b)) are charged to V_{DC} when T_2 is in off-state while are discharged when T_2 is conducting. The charging/discharging network includes the resistor R_1 or R_6, whose range of suitable values is limited from the operation of the OVMCs (e.g. R_1 defines the off-state current in the MOSFET-based solution). Consequently, C_{T_p} and C_{D_1} should be minimized:

- compared to C_{oss} in order not to affect the switching transition of the half-bridge, i.e. slowing down the voltage slope of the switching node dv_{ds}/dt in soft-switching transitions or significantly increasing the capacitive energy dissipated in hard-switching transitions;
- accordingly minimizing the magnitude of the charging/discharging current spikes, potentially damaging measurement and/or supply circuitry;
- minimizing the time constant of the *RC*-network formed with R_1 or R_6, improving the dynamic performance of the OVMCs (cf. Section III-D).

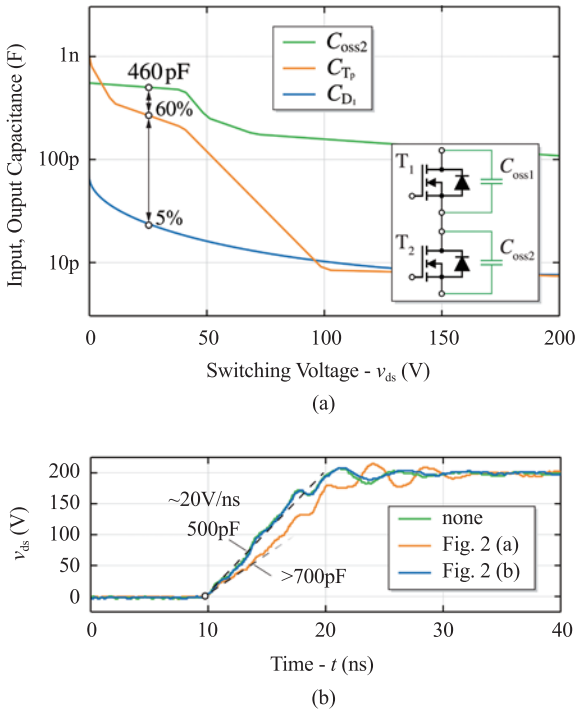


Fig. 3. (a) Comparison of the parasitic capacitances of the devices selected to realize the OVMCs of Fig. 2. For $v_{ds} < 100$ V, C_{D_1} is considerably smaller than C_{T_p} and, more important, negligible compared to C_{oss2}. This reflects on the switching behavior of the half-bridge (b): the presence of T_p, i.e. C_{T_p} (orange), significantly reduces dv_{ds}/dt during a soft-switching turn-off transition of T_2, whereas C_{D_1} (blue) does not have any influence.

These considerations clearly address the selection of T_p and D_1 towards devices featuring a small parasitic capacitance. Additionally, a low-inductance package and a short connection from the OVMC to the DUT are preferred in order to limit the voltage oscillations of v_1 inevitably excited from the switching transitions. According to these criteria, in the considered setups, a 800 V N-channel Si MOSFET [26] is selected for T_p as in [10] and a 600 V SiC Schottky diode [27] for D_1.

In order to prove the first statement, the parasitic capacitances of the selected devices are compared with the parasitic output capacitance C_{oss2} of a commercial 650 V E-mode GaN HEMT (Specimen C in TABLE II) as function of v_{ds} in Fig. 3(a). At $v_{ds} = 25$ V, C_{D_1} is a negligible fraction (i.e. 5%) of C_{oss2}, while C_{T_p} contributes to the overall capacitance (i.e. C_{oss2}+C_{T_p}) for more than 30%. As mentioned, this influences the switching behavior of the half-bridge where Specimen C is selected for T_2, e.g. in soft-switching operation. In Fig. 3 (b), measured waveforms of v_{ds} and dv_{ds}/dt for three different conditions are shown: without any OVMC (green), with the MOSFET-based approach (orange) and with the diode-based approach (blue) connected to T_2. While the presence of D_1 does not affect $dv_{ds}/dt \approx 20\ \frac{V}{ns}$, T_p slows it down especially in the first phase where C_{T_p} is comparable with C_{oss2}. This effect is clearly undesired and can be attributed to the selected T_p. However, depending on T_2, the range of suitable T_p (in terms of C_{T_p}) narrows, reaching a bottleneck in the case of interest of fast switching power semiconductors. Differently, parasitic capacitance of 600 V commercially available diodes can be in the range of few pF, enabling a more general OVM solution. Consequently, the approach presented in the next section is derived from the diode-based circuit. It aims to improve its accuracy, while benefiting from the reduced parasitic capacitance.

III. Proposed On-State Voltage Measurement Circuit

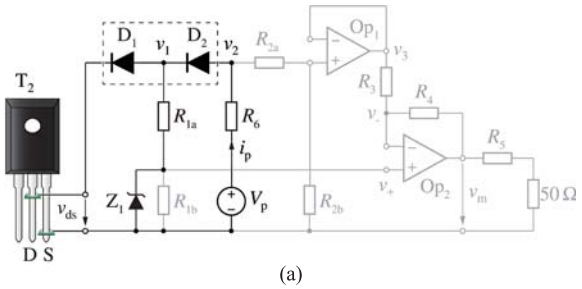
In Section II, strengths and weaknesses of the two most common OVM approaches are highlighted. In this section, a promising solution derived from the diode-based circuit and originally presented in [12], is analyzed in detail. As discussed in the introduction, it results significantly more challenging to perform OVMs in the case of fast-switching semiconductors compared to IGBTs, e.g. due to the higher switching frequency and lower OV. Considering the design guidelines proposed herein, relative in particular to the small input parasitic capacitance, the usage of a 50 Ω output stage, the high-bandwidth conditioning circuitry, the integrated generation of the supply voltages and the thoughtful design and calibration process, this OVMC is improved to combine high accuracy, outstanding dynamic performance and reduced circuit complexity. This ultimately enables its usage in the mentioned application areas of interest, as verified with the described measurement results. Initially, the operating principle of this OVMC is presented to better comprehend its possible limitations, providing the basis for its improvement.

A. Operating Principle

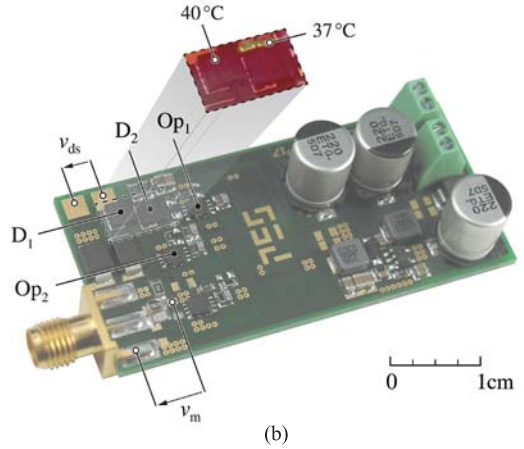
The schematic of the proposed OVMC for fast switching power semiconductors is depicted in Fig. 4(a) (a simplified version is in Fig. 4(c)) together with its hardware realization (Fig. 4(b)). The concept is derived from the approach shown in Fig. 2(b), but now two identical diodes (i.e. D_1 and D_2) are connected in series at the input. During the on-state of T_2 (see Fig. 2(c)), the same current i_D is assumed to flow through D_1 and D_2 ($i_{D_1} = i_{D_2}$), therefore, given the same operating point for the two diodes, the respective voltage drops v_D are assumed to be identical ($v_{D_1} = v_{D_2}$). Since thanks to the zener diode Z_1, only D_1 blocks V_{DC}, v_{D_2} can be measured and subtracted (with the operational amplifier Op_2) from v_1. Consequently, the offset v_{D_1} present in (2) can be, with this OVMC, exactly corrected rather than roughly compensated. During off-state, the operation is similar to the one of the OVMC in Fig. 2(b).

The transfer function of the complete OVMC (Fig. 4(a)) is herein derived. In the case of $v_{ds} < V_p - v_{D_2} - v_{D_1}$ and with Op_1 and Op_2 operating linearly (always assumed from here on),

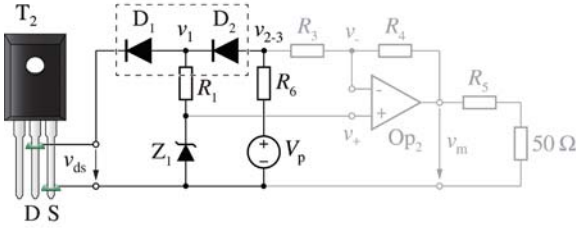
$$\begin{cases} v_+ = \dfrac{R_{1b}}{R_{1a}+R_{1b}} v_1 \\ v_3 = \dfrac{R_{2b}}{R_{2a}+R_{2b}} v_2 \\ v_m = v_- - \dfrac{R_4}{R_3}(v_3 - v_-) \end{cases} \tag{3}$$



(a)



(b)



(c)

Fig. 4. Schematic representation of the realized (a) and simplified (c) versions of the proposed OVMC. (b) depicts the hardware realization of (a). D_1 and D_2 are thermally well coupled (dashed box) and electrically connected in series at the input of the OVMC in order to improve the measurement accuracy.

holds. The system of equations given in (3) can be solved for the output voltage v_m if $v_+ = v_-$ is assumed, obtaining

$$v_{\rm m} \overset{(3)}{=} \frac{R_{1\rm b}}{R_{1\rm a}+R_{1\rm b}}\left(1+\frac{R_4}{R_3}\right)v_1 - \frac{R_{2\rm b}}{R_{2\rm a}+R_{2\rm b}}\frac{R_4}{R_3}v_2. \quad (4)$$

Defining $R_{1,\rm b} = R_{2,\rm b} \doteq R_\beta$ and $R_{1,\rm a} = R_{2,\rm a} \doteq \beta R_\beta$ so that

$$\frac{R_{1\rm b}}{R_{1\rm a}+R_{1\rm b}} = \frac{R_{2\rm b}}{R_{2\rm a}+R_{2\rm b}} = \frac{1}{1+\beta}$$

and selecting $R_3 = R_4$, (4) can be simplified to

$$v_{\rm m} \overset{(4)}{=} \frac{1}{1+\beta}(2v_1 - v_2). \quad (5)$$

Finally, it must be noticed that the term

$$2v_1 - v_2 = v_1 - (v_2 - v_1) = v_1 - v_{\rm D_2}, \quad (6)$$

under the assumption that $v_{D_2} = v_{D_1}$, can be used in (5) to obtain

$$v_{\rm m} \overset{(6)}{=} \frac{1}{1+\beta}(v_1 - v_{\rm D_1}) = \frac{1}{1+\beta}v_{\rm ds}. \quad (7)$$

Hence, the proposed OVMC corrects the offset on v_1, i.e. v_{D1}, producing an output voltage v_m referred to the source potential of the DUT, exactly proportional to v_{ds} during its on-state.

In case the scaling of v_{ds} obtained by means of the voltage dividers formed by R_{1a}–R_{2a} and R_{1b}–R_{2b} is not needed, they can be bypassed (i.e. $R_{2,a}$= 0 Ω, $R_{1,b}$ and $R_{2,b}$ removed). Consequently Op_1 results unnecessary as well (Fig. 4(c)) and the system of equations given in (3) reduces to

$$v_{\rm m} = v_1 - \frac{R_4}{R_3}(v_2 - v_1) \overset{(6)}{=} v_{\rm ds}. \quad (8)$$

The degree of freedom given by β is lost, i.e. the input voltage range of the circuit is reduced, but the number of required components is halved.

To provide a better understanding of the proposed OVMC, additional considerations are herein reported to conclude the section. As in the diode-based circuit presented in Fig. 2(b), the values of V_p and R_6 fix the current in D_1 and D_2 during on-state. V_p = 10 V (Section III-B) and R_6 = 750 Ω (Section II) are selected. If the currents flowing in the voltage dividers formed by R_{1a}–R_{2a} and R_{1b}–R_{2b} are negligible (see Fig. 4(a)), the operating point of the OVMC when T_2 is in on-state is defined by

$$i_{\rm p} = \frac{V_{\rm p} - v_{\rm D_2} - v_{\rm D_1} - v_{\rm ds}}{R_6}. \quad (9)$$

If v_{ds} = 0 V and $v_{D_1} = v_{D_2}$ = 1 V are assumed, $i_p \approx 10$ mA $\doteq I_{p,nom}$. Consequently, $P_{p,nom} = V_p I_{p,nom} \approx 100$ mW defines the power consumption of the OVMC from the main power source. It is important to limit i_p to a negligible fraction, e.g. 1%, of the current flowing through T_2 to avoid an increase and/or distortion of the OV (and to limit $P_{p,nom}$). This limit is strictly application dependent and, if exceeded, the additional OV should at least be considered in the calculation of $R_{ds,on}$. Moreover, a lower boundary of i_p is also set from the parasitic currents circulating in the OVMC, e.g. in the voltage divider formed by R_{1a}–R_{2a} and in the input of Op_2. If i_p is reduced below a certain threshold, it would result impossible to neglect them and the fundamental assumption $i_{D_1} = i_{D_2}$ would be violated, compromising the accuracy of the measurement. V_p defines as well, together with Z_1, the value of v_{ds} at which the circuit snaps. The blocking voltage of Z_1 is selected to be bigger than V_p to avoid its conduction during on-state of T_2, but on the other hand low enough to limit v_1 during off-state. Consequently the sole D_1 blocks the off-state voltage V_{DC}, protecting the measurement circuitry.

Finally, in order to facilitate the modular integration of the

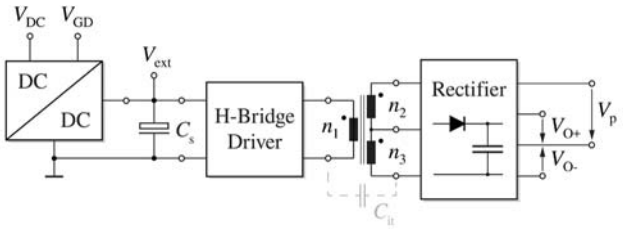


Fig. 5. Schematic representation of the OVMC supply circuitry. V_p, V_{O+} and V_{O-} can be generated from one of the supply voltages available in the power converter, e.g. V_{DC} and V_{GD}, facilitating the integration of the OVMC. Galvanic isolation is guaranteed and a small value of parasitic capacitance C_{it} ensures high common-mode rejection ratio.

OVMC in a power converter (e.g. towards intelligent gate drivers), Fig. 5 illustrates different options for the generation of the required supply voltages. In the proposed solution, V_p and the supply voltages of the operational amplifiers V_{O+} and $V_{O-} = -V_{O+}$ are galvanic isolated and generated from the gate driver supply voltage V_{GD}. A small value of parasitic capacitance C_{it} ensures high common-mode rejection ratio. Thanks to the isolated supplies, the proposed OVMC can be connected, without any additional precaution, as well to the high-side power semiconductor T_1 (Fig. 1). Hence, the OV of T_1 can be measured with respect to its source potential, i.e. v_{ds}. To avoid a differential measurement and common mode disturbances, it can be convenient to refer the OVM to a constant voltage, e.g. V_{DC}. To do so, the schematic of the proposed OVMC should be mirrored and referred to the drain potential of T_1. Afterwards, all the calculations performed for the low-side case remain valid.

B. Accuracy Measurement and DC Calibration

The accuracy of the proposed OVMC with respect to the assumptions made in Section III-A is herein verified and calibration measurements support the analysis.

The first requirement for a correct operation of this OVMC is based on the identity $v_{D_2} = v_{D_1}$. First, in order to guarantee $i_{D_1} = i_{D_2}$, the current flowing in the voltage divider formed by $R_{1,a}$–$R_{1,b}$ (if present) must be negligible. If this cannot be achieved by increasing the value of $R_{1,a}$+$R_{1,b}$, an operational amplifier Op_3 can be added between v_1 and R_{1a}.

However, even if $i_{D_1} = i_{D_2}$, the eventually different junction temperatures of the diodes (i.e. T_{D_1} and T_{D_2} respectively) and their manufacturing variability can cause a mismatch of v_D.

T_{D_1} can generally be higher than T_{D_2} because D_1 is exposed to a wide input voltage excitation and is also physically closer to T_2, where the major losses, i.e. heat, are dissipated. In order to minimize the problem, the nominal operating point of the circuit can be tuned at a temperature-independent point of the *V-I* characteristic of the diodes (if existing and coinciding between them). Alternatively, two diodes in the same package can be chosen in order to maximize their thermal coupling. Unfortunately, as explained in Section II, several constraints already drive the selection of the diodes (e.g. small parasitic output capacitances) if good dynamic performance are required and it results difficult to find devices combining all these characteristics. More realistically, as shown in Fig. 4(b) (dashed box), a sufficient and good practice is to thermally well couple D_2 with D_1 on the OVMC PCB (and if necessary provide separation between the OVMC and T_2 without excessively increasing the parasitic inductance of the connection). Hence, a $\Delta T_D = T_{D_1} - T_{D_2}$ of only 3 °C (Fig. 2(b)) is measured in the worst-case operating conditions of interest (i.e. maximum losses of 8 W in T_2 at the highest switching frequency of 1 MHz and off-state voltage of 400 V). In particular, depending on the operating conditions of T_2, T_{D_1} varies between $T_{D_1,min} = 30$ °C and $T_{D_1,max} = 40$ °C.

Concerning the device variability, before assembling the circuit, two diodes featuring the same v_D in the operating conditions of interest must be selected (a variability in the range of 10 mV is experienced in worst case among the available ones). To minimize this issue, it is convenient to reduce the variation of i_p from $i_{p,min} < I_{p,nom} < i_{p,max}$, caused by a variation of v_{ds} (according to (9)). For this reason, in [12], the voltage source V_p–R_6 is replaced with a current source I_p. However, considering the experiment presented in the introduction (i.e. a specimen power MOSFET with $R_{ds,on} = 25$ mΩ conducting ±20 A), the excursion of v_{ds} is in the range of ±500 mV and the current variation results

$$\Delta i_p = \frac{i_{p,max}}{i_{p,min}} \overset{(9)}{=} \frac{V_p - v_{D_2} - v_{D_1} - v_{ds,min}}{V_p - v_{D_2} - v_{D_1} - v_{ds,max}} \approx 1.1. \quad (10)$$

Even a worst-case ±15% variation, i.e. ±1.5 mA, is assumed not to have any influence on the OVMC accuracy. To quantitative support this statement, v_{D_1} and v_{D_2} are reported in TABLE I as a function of i_p and T_{D_1} . A worst-case mismatch in the diode voltage drops $v_{\Delta D} = v_{D_1} - v_{D_2} = 2$ mV and a temperature coefficient of 1 $\frac{mV}{°C}$ are observed. $v_{\Delta D}$ must be negligible compared to the measured vds not to affect the OVM accuracy. This becomes more and more difficult to achieve at low OV levels, e.g. with $v_{ds} < 40$ mV, and if desired an even more sophisticated diode matching and/or calibration procedure can be adopted. However, other problems arise when v_{ds}, i.e. the DUT current, approaches 0 V and are discussed in Section IV-A. Finally, it can be noticed that, due to the small value of i_p, the diode model provided in [27] is not valid. The proposed calibration procedure is required to enable the performance of the OVMC described in this section. Other interesting considerations regarding the precise tuning of the proposed OVMC are reported in Appendix A as guideline for its design.

To conclude, once the crucial aspects related to the design of the proposed OVM hardware are clarified and taken into account, the achieved accuracy is measured. Fig. 6 illustrates the relative error ε_r (right y-axis) from a DC input v_{ds} (*x*-axis) to a DC output v_m (left *y*-axis) in a range from −2 V to 2 V. ε_r is confined between ±2% with an absolute maximum error $\varepsilon_{max} = 5$ mV. Here, and in the rest of the analysis, the gain of the proposed OVMC is normalized to 1 for the sake of clarity.

TABLE I
MISMATCH IN THE DIODE VOLTAGE DROPS AS FUNCTION OF THEIR TEMPERATURE AND CURRENT

i_p	T_{D_1}	v_{D_1} (mV)	v_{D_2} (mV)	$v_{\Delta D}$ (mV)
$i_{p,min}$	$T_{D_1,min}$	831	832	-1
	$T_{D_1,max}$	820	818	2
$i_{p,max}$	$T_{D_1,min}$	838	839	-1
	$T_{D_1,max}$	828	826	2

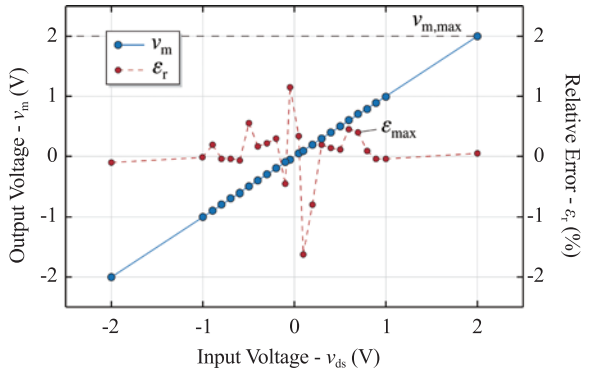


Fig. 6. Results of the DC calibration of the proposed OVMC. When a DC voltage -2 V < v_{ds} < 2 V is applied at the input (x-axis), the output v_m (left y-axis) deviates less than 5 mV, corresponding to ε_r < 2% (right y-axis) in worst-case.

C. Bandwidth Measurement and AC Calibration

A severe bandwidth requirement is mandatory in all the application areas of OVMCs mentioned in the introduction when fast switching semiconductors are considered. The bandwidth and the accuracy in AC operation of the proposed OVMC are verified in this section to evaluate its applicability in the conditions of interest. Measurements are preceded from a brief discussion pointing out the most significant aspects enabling its performance.

Accurately sensing a high-frequency signal with a conventional oscilloscope probe (as in Fig. 2(a)-(b)) results in a challenge. In fact, when the high-impedance input (i.e. 1 MΩ) of the oscilloscope is used, precise tuning of the probe internal capacitance is required to have a flat gain for all the frequency range of interest. Hence, the 50 Ω input of the oscilloscope is preferred. $R_5 \approx 50$ Ω is added at the output of the proposed OVMC (cf. Fig. 4(a)-(c)) to match the output impedance of Op_2 with the characteristic impedance of the used cable (i.e. 50 Ω). This is possible only given the presence of Op_2, driving the necessary output current in the oscilloscope without affecting the circuit performance. Therefore, the selection range of operational amplifiers is limited from their output current and voltage capabilities. Among the available devices, a low-noise 1 GHz 10 V 40 mA operational amplifier [28] is selected to maximize the achievable bandwidth of the OVMC.

The results of the high-frequency calibration are described in Fig. 7. Three different triangular waveforms at 700 kHz

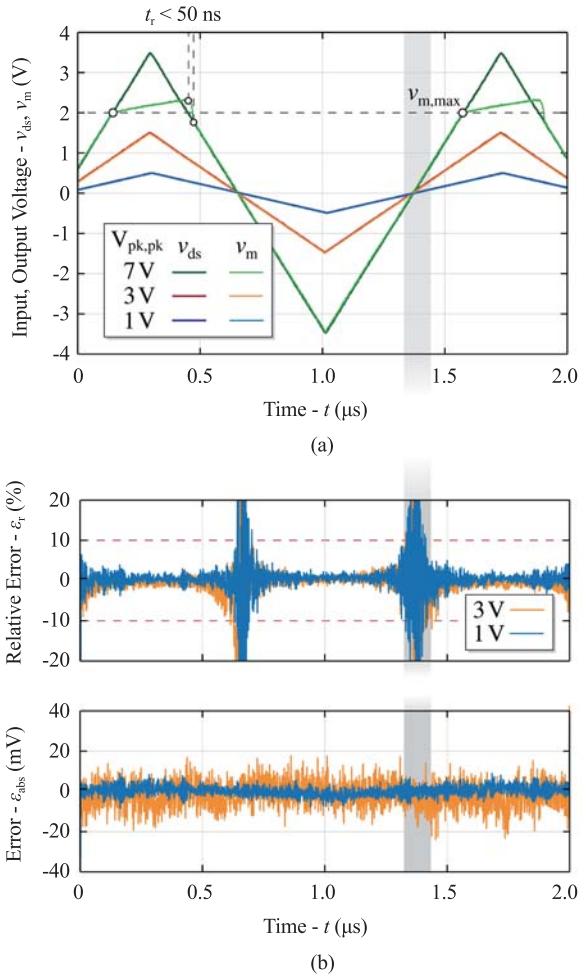


Fig. 7. Results of the AC calibration of the proposed OVMC. When AC voltage waveforms of different amplitudes are applied at the input v_{ds}, the output waveforms v_m are practically indistinguishable from them: ε_{abs} is limited by the oscilloscope resolution.

with peak-to-peak voltage amplitudes $V_{pk,pk}$ increasing from 1 V to 7 V are generated at the input v_{ds} and plotted (blue, red and dark green) on top of the measured output v_m (sky blue, orange and light green) in Fig. 7(a). When v_{ds} < 2 V the input and output waveforms are indistinguishable. At v_{ds} = $v_{m,max}$ = 2 V, Op_1 saturates and v_m (light green) is distorted. In Fig. 7(b), the relative ε_r and absolute ε_{abs} errors are reported. ε_{abs} is limited between $\varepsilon_{abs;max}$ = ±10 mV in the worst-case of $3V_{pk;pk}$ and has a zero mean. It must be mentioned that with a 10 bits oscilloscope on a 8 V vertical window, $\varepsilon_{abs;max}$ is in the range of the oscilloscope resolution (8 V/2^{10} ≈ 8 mV). ε_r is, for the same reason, mainly in a ±5% range; however, when v_{ds} approaches zero (gray shaded area), the division between two small numbers causes a numerical issue and ε_r diverges.

Finally, with a vector network analyzer, the bandwidth of the proposed OVMC is measured exciting it at the input v_{ds} with sinusoidal waveforms up to $2V_{pk,pk}$. The −3 dB bandwidth is outside the measurable frequency range of the instrument (i.e. 50 MHz) while the more intuitive normalized linear gain g_{lin} is 1.0 until 1 MHz and still 0.97 at 10 MHz,

TABLE II
SPECIFICATIONS OF THE POWER SEMICONDUCTORS CONSIDERED AS DUT FOR THE PROPOSED OVMC

Specimen	Type	$V_{dc,max}$ (V)	$I_{ds,max}$ (A)	$R_{ds,on}$ (mΩ)	Package	Figures
A	SiC Power MOSFET	1200	98	25	TO-247-3	14 (a), 13, 11 and 9
B	Si Super-Junction MOSFET	700	46	40	TO-247	14 (b) and 10 (b)
C	E-mode GaN HEMT	650	30	50	GaN*PX*™	14 (c), 10 (a) and 3

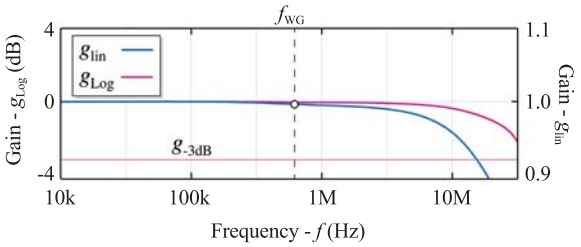


Fig. 8. Measured bandwidth of the proposed OVMC. The –3 dB bandwidth is above 50 MHz (magenta) while g_{lin} = 1.0 until 1 MHz and 0.97 at 10 MHz (blue).

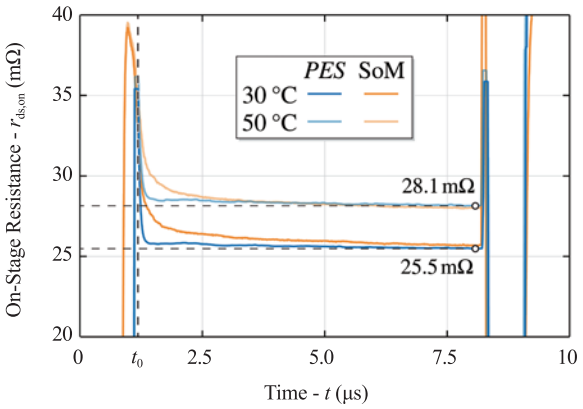


Fig. 9. Comparison in terms of dynamic response between the proposed OVMC (*PES*) and a state-of-the-market (SoM) commercial OVM probe. When the DUT turns on at t_0, the output of the proposed OVMC immediately measures the correct OV, i.e. the nominal $r_{ds,on}$ value, whereas the commercial device features a time constant in the µs-range. E.g. a fast dynamic response increases the maximum switching frequency at which an OVMC can perform useful measurements, since the dynamic transient must be negligible compared to the duration of the DUT on-state.

independently of the input signal amplitude (Fig. 8). In order to guarantee the linearity in these measurements, the input signal never exceeds $v_{m,max}$. The real bandwidth of the circuit is, instead, strongly influenced from its dynamic response after the DUT turn-on switching transition, which is the topic of the next section.

D. Dynamic Response

To conclude the characterization of the proposed OVMC, its outstanding dynamic response is analyzed in this section, accompanied by a discussion on the main features enabling this achievement.

As mentioned, it is important to perform accurate OVMs immediately after the turn-on transition of the DUT. This allows to capture eventual dynamic $R_{ds,on}$ effects, the diode conduction phase during dead-times and enables high-frequency measurements necessary in all the mentioned application areas. In fact, the time constant of the dynamic response must be negligible compared to the duration of the DUT on-state to obtain meaningful OVMs.

In Fig. 9, the dynamic response of the proposed OVMC is compared with the one of a state-of-the-market (SoM) commercial OVM probe. The two measured waveforms highlight the faster response of the proposed approach (blue). The measured signal is the on-state resistance $r_{ds,on}(t)$ (time dependency is omitted from now on) of a commercial 1200 V SiC Power MOSFET (Specimen A in TABLE II) for two different case temperatures. The value of $r_{ds,on}$ is obtained dividing the output of the OVMCs v_m by the DUT current i_{sw} (see Fig. 1) and must be limited to the time window where the DUT is in on-state (i.e. after t_0). The key design guidelines at the basis of the achieved performance rely on the selection of high bandwidth operational amplifiers and diodes with small parasitic capacitance, and on a low inductive PCB design (especially concerning the commutation loop of D_1). In order to quantify the dynamic response time of the proposed OVMC, two more measurements, showing the turn-on transition of different DUTs, are performed (Fig. 10). In Fig. 10(a), a commercial 650V E-mode GaN HEMT (Specimen C in TABLE II) is tested. The three voltage measurements are v_{ds} (yellow), v_{gs} (green) and v_m (blue). When the high-side transistor T_1 is turned off, v_{ds} drops from V_{DC} to 0 V because of a positive load current i_{load} (not shown, see Fig. 1). The anti-parallel body diode of T_2 (i.e. D_{T_2}) immediately conducts and $v_m = -V_{fv,BD} = -7$ V is clamped to the bottom of the oscilloscope screen. When v_{gs} reaches V_{th,T_2} (green dot), T_2 turns on and i_{sw} commutates from D_{T_2} to the channel of T_2. Consequently v_m changes from the forward voltage of D_{T2} (i.e. $-V_{fv,BD}$) to $r_{ds,on}i_{sw}$. As the white cursors highlight, the response time of the proposed OVMC is less than 50 ns if the real transition is assumed instantaneous.

The same situation is reproduced in Fig. 10(b) with a commercial Si Super-Junction MOSFET (Specimen B in TABLE II). In this condition, $V_{fv,BD} \approx 0.8$ V can be accurately measured during all the conduction time of D_{T_2}. In transparency a second measurement with a shorter dead-time is overlapped.

IV. ONLINE CONDUCTION LOSS MEASUREMENT

In this section, the integration of the proposed OVMC in a power converter (Fig. 1) is commented and the OV, i.e. $R_{ds,on}$,

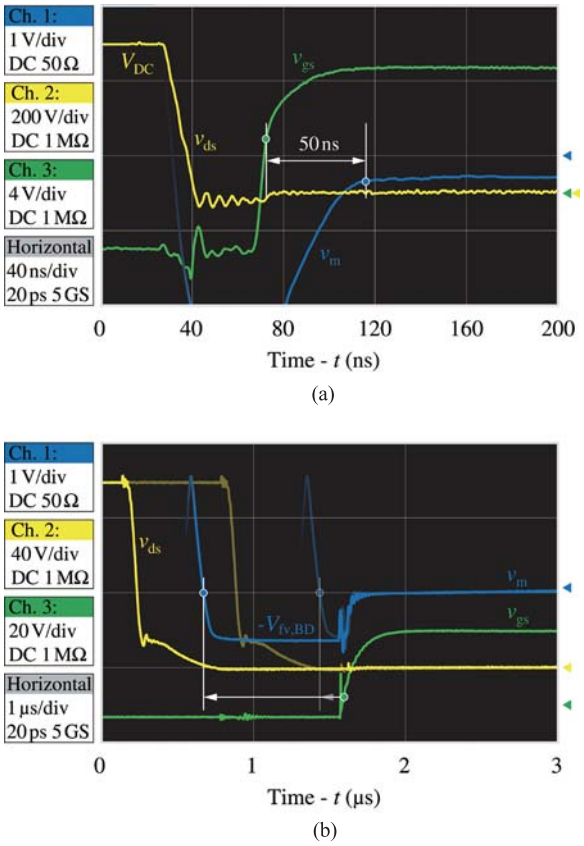


Fig. 10. Analysis of the dynamic response of the proposed OVMC. (a) less than 50 ns after v_{gs} has reached V_{th,T_2} (green dot), v_m (blue) is settled to the correct value, even in the case of significant $V_{fv,BD}$, e.g. > 2 V. (b) when $V_{fv,BD}$ is in the measurable range, the proposed OVMC allows to monitor the conduction time of D_{T_2} , evaluating the dead-time conduction losses and its effective duration.

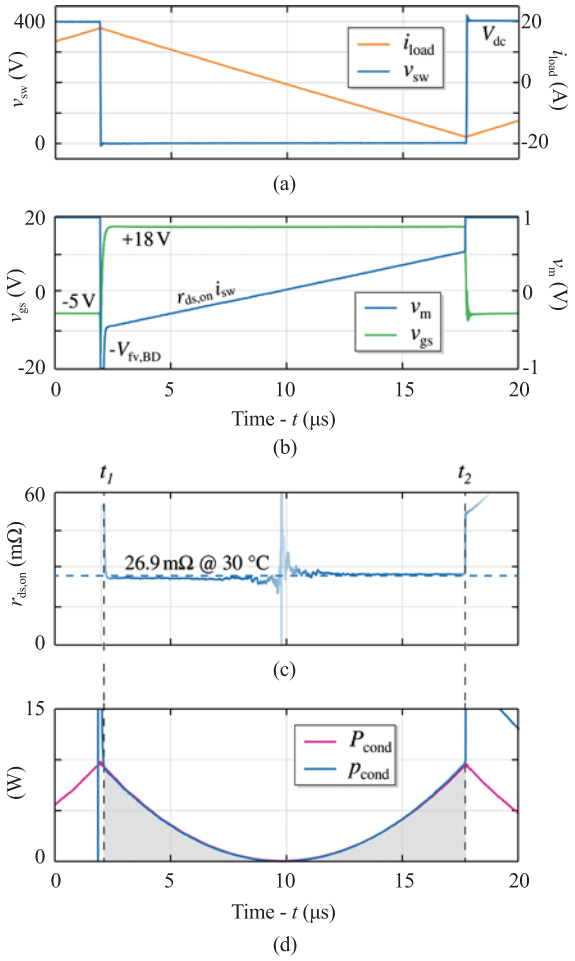


Fig. 11. Typical waveforms (a)-(b) measured on the half-bridge (Fig. 1) operating in triangular current mode (TCM). When $v_{gs} = V_{gs,ON}$ (green), T_2 conducts and v_m (blue) is proportional to i_{sw} (orange). In (c) $r_{ds,on}$ is calculated between t_1 and t_2 dividing v_m by i_{sw}, while in (d) p_{cond} is obtained multiplying v_m and i_{sw} .

of different power semiconductors is measured as function of their operating conditions. The measurement setup is initially described. The associated challenges are then addressed and the proposed solutions are ultimately commented. Finally, since the original reason motivating the development of this OVMC is the improvement of the measurement accuracy of calorimetric switching loss measurement methods, the presented results are discussed accordingly.

A. Conduction Loss Measurement Setup

The setup is equivalent to the schematic shown in Fig. 1. Assuming symmetrical triangular current mode (TCM) operation of the half-bridge (i.e. T_1 and T_2 are operated with complementary 50% duty cycles and no load is connected), the analysis can be limited to the conduction time of T_2. All the relevant measured waveforms are shown in Fig. 11 (a)-Fig. 11(b). In particular, the switch node voltage v_{ds} (blue in Fig. 11 (a)), the load current i_{load} (orange), the gate voltage v_{gs} (green, $V_{gs,ON}$ = 18 V and $V_{gs,OFF}$ = –5 V) and the output of the proposed OVMC v_m (blue in Fig. 11(b)). Inside the time window t_1–t_2, the on-state resistance $r_{ds,on}$ of T_2 can be determined dividing v_m by $-i_{load} = i_{sw}$ (Fig. 11(c)). The instantaneous conduction losses pcond can be calculated as $r_{ds,on}i^2_{sw}$ or equivalently $v_m i_{sw}$ (blue in Fig. 11(d)). Finally, the average conduction losses can be obtained as average of p_{cond} during on-state of T_2 (gray shaded area).

Similarly, an average $R_{ds,on}$ value can be obtained as average of $r_{ds,on}$. In this case, $R_{ds,on}$ = 26.9 mΩ (Fig. 11(c)) results for Specimen A in TABLE II. Consequently, the approximated conduction losses P_{cond} can be directly calculated as $R_{ds,on}i^2_{sw}$ (magenta in Fig. 11(d)). Given the almost perfect overlap between the blue and magenta curves in Fig. 11(d), when p_{cond} and P_{cond} are averaged, 3.6 W results in both cases. However, in general, the first approach is preferred, since it takes into account dynamic $R_{ds,on}$ effects and the eventual current dependency of $R_{ds,on}$.

In order to perform accurate measurements in this setup and operating conditions, two challenges, associated in particular with the reduced OV and high current slopes that needs to be measured, are faced. The first challenge to overcome is represented by the parasitic inductance L_P (Fig. 1) in series with T_2. Fig. 12(a) highlights the load current slope $di_{load}/dt = -di_{sw}/dt$ (up to tens of A/µs) that in combination with L_P causes a voltage offset (red in Fig. 12(b)) on v_m according to

$$v_{\mathrm{m}} = R_{\mathrm{ds,on}} i_{\mathrm{sw}} + L_{\mathrm{P}} \frac{\mathrm{d}i_{\mathrm{sw}}}{\mathrm{d}t} \tag{11}$$

(blue in Fig. 12(b)). Hence, calculating $r_{\mathrm{ds,on}}$ as

$$r_{\mathrm{ds,on}} = \frac{v_{\mathrm{m}}}{i_{\mathrm{sw}}} \overset{(11)}{=} R_{\mathrm{ds,on}} + \frac{L_{\mathrm{P}}}{t} = R_{\mathrm{ds,on}} \left(1 + \frac{\tau_{\mathrm{RL}}}{t}\right), \tag{12}$$

the term $\frac{\tau_{\mathrm{RL}}}{t}$ $\left(\tau_{\mathrm{RL}} \doteq \frac{L_{\mathrm{P}}}{R_{\mathrm{ds,on}}}\right)$ distorts the result. Therefore, in contrast to a constant $R_{\mathrm{ds,on}}$ (dashed in Fig. 12(c)), the waveform of $r_{\mathrm{ds,on}}$, solid in Fig. 12(c), is obtained. E.g. if L_{P} = 8 nH and $R_{\mathrm{ds,on}}$ = 50 mΩ then $\tau_{\mathrm{RL}} \approx$ 150 ns. Hence, after $t = 5\tau_{\mathrm{RL}}$ = 800 ns, $r_{\mathrm{ds,on}}$ = 1.2 $R_{\mathrm{ds,on}}$ = 60 mΩ. From (12) it can be concluded that L_{P} should be minimized, i.e. the connection from the DUT to the OVMC should start as close as possible from the drain and source terminals of T_2, excluding any additional path where i_{sw} flows. Unfortunately, part of L_{P} is located internally in the package of the DUT and no design expedient results helpful. A compensation network could be inserted and tuned, however it would negatively affect the dynamic performance of the proposed OVMC. Alternatively, the inductive voltage drop $v_{\mathrm{m,o}}$ can be isolated from the resistive one taking advantage of the zero crossing of i_{sw}.

I.e., measuring v_{m} and $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$ when i_{sw} = 0 A, (11) can be solved for L_{P}. Formally

$$v_{\mathrm{m,o}} \doteq v_{\mathrm{m}}|_{i_{\mathrm{sw}}=0} \overset{(11)}{=} L_{\mathrm{P}} \frac{\mathrm{d}i_{\mathrm{sw}}}{\mathrm{d}t}. \tag{13}$$

Repeating this measurement for different $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$, L_{P} can be calculated as average of several

$$L_{\mathrm{P_i}} = \frac{v_{\mathrm{m,o_i}}}{\mathrm{d}i_{\mathrm{sw_i}}/\mathrm{d}t} \tag{14}$$

and its value can be used to adjust $v_{\mathrm{m_i}}$. From the practical point of view, this results in subtracting $v_{\mathrm{m,o_i}}$ from $v_{\mathrm{m_i}}$ in each measurement, ensuring $v_{\mathrm{m_i}}$ = 0 V when $i_{\mathrm{sw_i}}$ = 0 A. Whereas this assumption sounds legit and sufficient by itself, calculating L_{P} as in (14) provides a physical motivation to this adjustment. Moreover, obtaining constant $L_{\mathrm{P_i}}$ across different measurements guarantees their correctness. This becomes more and more important when the zero crossing of i_{sw} is not present and/or measurable and the knowledge of L_{P} is the only option to correct the measurement result. Alternatively, $r_{\mathrm{ds,on}}$ can be calculated as the ratio between $\mathrm{d}v_{\mathrm{m}}/\mathrm{d}t$ and $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$. Even if not affected from $v_{\mathrm{m,o}}$, this approach loses accuracy when the voltage and current slopes become flatter.

The second challenge is easily highlighted applying the propagation of uncertainty rule on $r_{\mathrm{ds,on}} = v_{\mathrm{m}}/i_{\mathrm{sw}}$:

$$\begin{aligned} \sigma_{r_{\mathrm{ds,on}}} &= \sqrt{\left(\frac{\partial r_{\mathrm{ds,on}}}{\partial v_{\mathrm{m}}} \sigma_{v_{\mathrm{m}}}\right)^2 + \left(\frac{\partial r_{\mathrm{ds,on}}}{\partial i_{\mathrm{sw}}} \sigma_{i_{\mathrm{sw}}}\right)^2} \\ &= \frac{1}{i_{\mathrm{sw}}} \sqrt{\sigma_{v_{\mathrm{m}}}^2 + (r_{\mathrm{ds,on}} \sigma_{i_{\mathrm{sw}}})^2} \end{aligned} \tag{15}$$

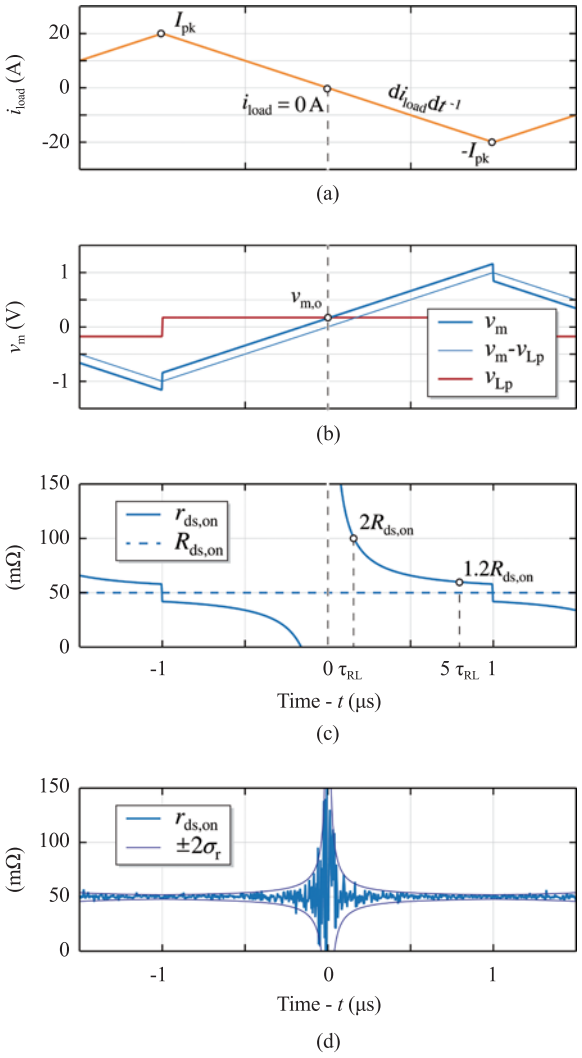


Fig. 12. Comparison of real and ideal waveforms simulated on the half-bridge (Fig. 1) operating in TCM. The combination of L_{P} and $\mathrm{d}i_{\mathrm{sw}}/\mathrm{d}t$ causes a distortion on v_{m} (b) and consequently on $r_{\mathrm{ds,on}}$ (c). Moreover, a measurement error on v_{m} translates into an error on $r_{\mathrm{ds,on}}$ (d) according to (16), particularly amplified for small i_{sw} as in (15).

and

$$\sigma\%_{r_{\mathrm{ds,on}}} = \frac{\sigma_{r_{\mathrm{ds,on}}}}{r_{\mathrm{ds,on}}} \overset{(15)}{=} \frac{\sigma_{v_{\mathrm{m}}}}{r_{\mathrm{ds,on}} i_{\mathrm{sw}}} = \sigma\%_{v_{\mathrm{m}}}. \tag{16}$$

σx and $\sigma\%x$ indicate the absolute and relative error on the measured quantity x, respectively. (15) proves why $\sigma_{r_{\mathrm{ds,on}}}$ and therefore $r_{\mathrm{ds,on}}$ diverges when i_{sw} approaches zero (see Fig. 11(c) and Fig. 12(c)-(d)). (16), instead, expresses how $\sigma\%_{r_{\mathrm{ds,on}}}$ coincides with $\sigma\%_{v_{\mathrm{m}}}$ when $\sigma_{i_{\mathrm{sw}}} = 0$. In other words, any error on v_{m} reflects one-to-one (relatively) on $r_{\mathrm{ds,on}}$ (i.e. on p_{cond}). An example of $r_{\mathrm{ds,on}}$, corrected from $v_{\mathrm{m,o}}$, but resulting from v_{m} with $\sigma_{v_{\mathrm{m}}}$ = 5 mV to highlight the effect, is shown in Fig. 12(d). Since the only expedient to minimize both phenomena described from (15) and (16) is to reduce $\sigma_{v_{\mathrm{m}}}$, this section clearly justifies the effort placed on the accuracy analysis of the proposed OVMC addressed in Section III. Moreover, it highlights how measurements of low $r_{\mathrm{ds,on}}$ and/or high $\mathrm{d}i_{\mathrm{load}}/\mathrm{d}t$ (e.g. wide bandgap semiconductors) introduce new

challenges in the OVMs.

B. Conduction Loss Measurement Results

Several measurements are performed with the proposed OVMC analyzing different DUTs in different operating conditions. The results are commented in this section.

Fig. 13 compares the nominal value of $R_{ds,on}$ reported in the datasheet of Specimen A in TABLE II with the values of $R_{ds,on}$ measured with the proposed OVMC during double pulse test (DPT) operation (in the same conditions described in the datasheet). The black dashed line R_{data} is plotted as function of the junction temperature $T_{j,data}$ (i.e. bottom x-axis) while the blue measurement points R_{DPT} are plotted as function of the measured case temperature $T_{c,DPT}$ (i.e. top x-axis). Since the DPT has electric dynamics which are assumed to be faster than the thermal dynamics of the DUT, $T_{c,DPT} \approx T_{j,DPT}$ is considered and the two x-axis coincide (i.e. $T_{j,DPT} \approx T_{j,data}$). R_{DPT}, measured with the proposed OVMC as described in Fig. 9, match R_{data} with an approximation of ±3% (blue confidence bar is ±5%). The discrepancy can be attributed mainly to the device manufacturing variability. However, the results are satisfactory and confirm the performance of the proposed OVMC.

Fig. 14(a), (b) and (c), instead, summarize the values of $R_{ds,on}$ measured in two different continuous operating conditions for all the Specimens of TABLE II. In particular, the orange points R_{TCM} are measured (with the proposed OVMC) in the conditions described in Section IV-A (i.e. TCM operation with V_{DC} = 400 V, I_{pk} = 20 A and f_{sw} = 30 kHz) while the green points R_{DC} are measured (with the proposed OVMC and a multimeter to monitor its accuracy) in DC operation. The DC current $I_{DC} = I_{pk}/(\sqrt{3}\sqrt{2}) = 8$ A is selected to ensure that approximately the same losses occur in the DUT in DC operation as in TCM operation (legitimately neglecting the soft-switching losses [15]), such that $T_{j,DC} \approx T_{j,TCM}$ when $T_{c,DC} = T_{c,TCM}$ is measured. All the circuit parameters are maintained the same in both the experiments, in particular matching the value recommended in the datasheet. For Specimen A, R_{TCM} (cf. also Fig. 11(c)) and R_{DC} (Fig. 14(a)) are slightly higher than R_{data} and R_{DPT} (cf. Fig. 13). The reason behind it is the difference in T_j between the two sets of measurements ($T_{j,DC} \approx T_{j,TCM} > T_{j,data} \approx T_{j,DPT}$) due to the losses continuously occurring in the DUT. As a consequence, the positive temperature coefficient of $R_{ds,on}$ affects the result. More interesting to notice is that R_{DC} is very close, i.e. within ±4% (orange confidence bar is ±5%), to R_{TCM} as expected, since $T_{j,DC} \approx T_{j,TCM}$ and the current dependency of $R_{ds,on}$ is practically negligible in this range. The discrepancy can be attributed to the accuracy of the current measurement and of the OVMC, and to slightly different operating conditions. An equivalent set of measurements is performed on Specimen B in Fig. 14(b) and identical conclusions can be drawn. Hence, the accuracy and the performance of the proposed OVMC are once more validated. Fig. 14(c) summarizes R_{TCM} and R_{DC} for Specimen C in TABLE II. In this case a significant discrepancy (i.e. ≈ 50%) between the two series is observed. $T_{j,DC} \approx T_{j,TCM}$ is not a true assumption anymore, since more losses are now unexpectedly occurring in the DUT in TCM operation. The discrepancy is attributed in this case to the DUT, i.e. to dynamic $R_{ds,on}$ effects, which are confirmed in [7].

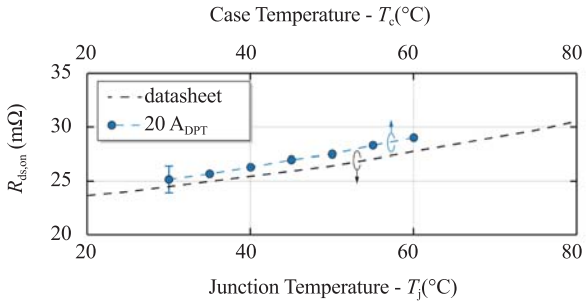


Fig. 13. Average value of $r_{ds,on}$ (i.e. R_{DPT}) measured with the proposed OVMC in double pulse test (DPT) operation for Specimen A in TABLE II compared with the nominal $R_{ds,on}$ values reported in its datasheet (i.e. R_{data}). The measured points match the nominal values within ±3%.

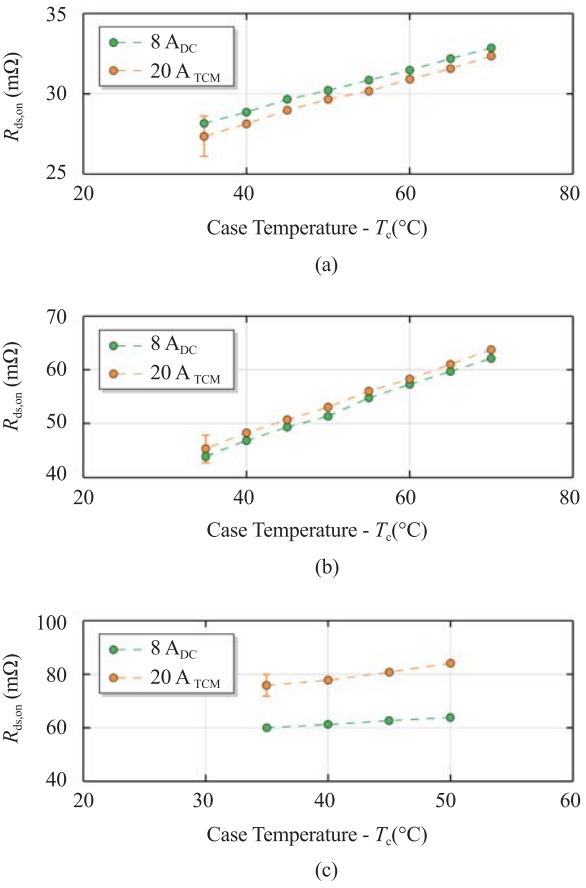


Fig. 14. Average value of $r_{ds,on}$ measured with the proposed OVMC for different operating conditions of the half-bridge, for different DUTs (TABLE II) and as a function of T_c. R_{TCM} (orange) and R_{DC} (green) are similar (within ±5%) for Specimen A (a) and B (b) when the power loss conditions are matched. In the case of Specimen C, a significant discrepancy (i.e. ≈ 50%) between the two measurement sets is observed (c).

C. Influence on Calorimetric Switching Loss Measurement

The results illustrated in the last section can be applied to improve the accuracy of the calorimetric switching loss measurements presented in [15]. Calorimetric switching loss measurement methods, in contrast to electric switching loss measurement methods, e.g. the DPT, determine the switching losses from the measurement of thermal quantities [14], [16]. The power semiconductor under test is installed in a calorimetric test-bench, whose thermal parameters (e.g. thermal resistance and thermal capacitance) are known. While the device operates, the occurring losses generate heat and cause a variation of temperature in the test-bench. The exact amount of losses can be derived from the temperature increase.

Both conduction losses and switching losses occur simultaneously in the DUT, hence only their sum can be thermally measured. However, initially operating the DUT in the test-bench at a switching frequency at which the switching losses (P_{sw}) can be neglected compared to the total losses (P_{th}), the conduction losses (P_{cond}) can be accurately measured. A set of measurements performed on Specimen C show an agreement between the two methods (i.e. calorimetric and OVMC) with an uncertainty in the range of 5%, mostly attribute to the calorimetric test-bench itself [15].

The measurement method proposed in [15] to perform calorimetric switching loss measurement consists of two phases. First, accurate calorimetric measurement of the total semiconductor losses are performed (P_{th}). Afterwards, P_{cond} are estimated and subtracted to isolate

$$P_{\mathrm{sw}} = P_{\mathrm{th}} - P_{\mathrm{cond}}. \tag{17}$$

It results immediately clear that the accuracy of the measured P_{sw} (σP_{sw}) is influenced both from the accuracy of the calorimetric measurement itself (σP_{th}) and of the P_{cond} estimation (σP_{cond}). If $\sigma P_{th} = 0$ is assumed for the purpose of this analysis, σP_{sw} can be expressed, applying the propagation of uncertainty rule, as

$$\sigma_{\%P_{\mathrm{sw}}} = -\frac{P_{\mathrm{cond}}}{P_{\mathrm{sw}}}\sigma_{\%P_{\mathrm{cond}}}. \tag{18}$$

The integration of the proposed OVMC in this measurement setup aims to improve σP_{cond}.

In [15], $R_{ds,on}$ is measured in DC operation as a function of P_{th}, similarly to R_{DC} in Fig. 14(a)-(c). Afterwards an opportune (i.e. for the same P_{th} conditions) value of $R_{ds,on}$ is considered to calculate and subtract P_{cond} from P_{th} in TCM operation. The proposed OVMC, enabling online measurement of R_{TCM}, has the potential to minimize σP_{cond} , but confirmed as well the validity of the approach developed in [15] against, for example, the usage of R_{data}. At least for Specimen A and B, in fact, R_{TCM} and R_{DC} (orange and green points in Fig. 14(a)-(b)) coincide with good approximation (within ±5%). Hence, the results shown in [15] are correct under this aspect. Differently, the discrepancy observed for Specimen C (cf. Fig. 14(c)) would introduce a significant error if the [15]-approach would be blindly adopted. Fig. 15(a) compares the results of the two conduction loss measurement methods (i.e. R_{TCM} and R_{DC}) for one of the DUTs analyzed in [15], similar to Specimen C. In this case, the two approaches give significantly different results and the importance of OVMCs for fast switching power semiconductors is again remarked. The accurate measurement of R_{TCM} at 1 MHz is the final achievement of this work, only enabled from the sophisticated design and calibration procedures described along this paper. R_{TCM} is up to 50% higher than R_{DC}, i.e. P_{cond} is 50% higher than previously estimated. According to (18), P_{sw} results up to 28% lower (see Fig. 15(b)). The physical cause behind the underlying loss mechanism is still under investigation [29].

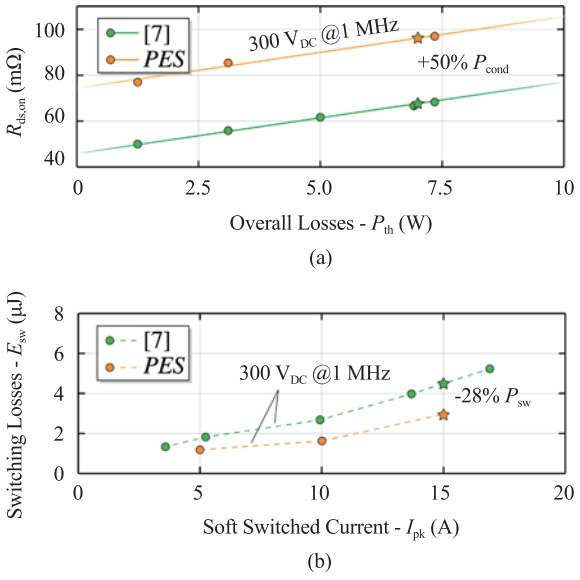


Fig. 15. Comparison between R_{TCM} (orange) and R_{DC} (green) as function of P_{th} (a). The online measurement of conduction losses enabled by the proposed OVMC, more representative of the real operating conditions, results in higher (i.e. ≈ 50%) P_{cond}. The mismatch results in lower estimated P_{sw} (i.e. ≈ –28%) according to the calculation reported in TABLE III (b).

TABLE III
DERIVATION OF THE ERROR ON THE SWITCHING LOSSES CAUSED BY THE INACCURACY ON THE CONDUCTION LOSS ESTIMATION

Parameter	[15]	proposed OVMC	Note
I_{pk} (A)	15		Fig. 15(b)
P_{th} (W)	6.90	6.90	Fig. 15(a)
$R_{ds,on}$ (mΩ)	65	95	Fig. 15(a)
P_{cond} (W)	2.40	3.60	$P_{\mathrm{sw}} = R_{\mathrm{ds,on}} I_{\mathrm{rms}}^2$, $I_{\mathrm{rms}} = I_{\mathrm{pk}}/(\sqrt{3}\sqrt{2})$
P_{sw} (W)	4.50	3.30	$P_{\mathrm{sw}} = f_{\mathrm{sw}} E_{\mathrm{sw}}$, (17) and Fig. 15(b)
$\sigma\%P_{cond}$	50%		$\left\lvert \frac{P_{\mathrm{cond},[7]} - P_{\mathrm{cond,OVMC}}}{P_{\mathrm{cond},[7]}} \right\rvert$ and Fig. 15(a)
$\sigma\%P_{sw}$	-28%		(18) and Fig. 15(b)

The calculations for the case of I_{pk}= 15 A are reported in TABLE III as an example.

V. Conclusion

An on-state voltage measurement circuit (OVMC) for fast switching power semiconductors is presented and fully characterized in this paper. The correction of the offset voltage present in typical OVMCs, the small input parasitic capacitance, the usage of a 50 Ω output stage, the high-bandwidth conditioning circuitry, the integrated generation of the supply voltages and the thoughtful design and calibration process are key features and/or main improvements of the proposed approach when compared with state-of-the-art solutions.

The operating principle of this OVMC is described and detailed design guidelines are given. Furthermore, accurate DC and high-frequency calibration measurements are performed. Several challenges, e.g. measurement distortion due to the DUT parasitic inductance and noise amplification at low DUT current values, arise when the proposed OVMC is integrated in the measurement setup of interest considering fast switching power semiconductors. However, implementing the addressed precautions, the achieved accuracy (< ±2%), bandwidth (> 50 MHz) and dynamic response (< 50 ns) finally enable precise OVMs in the case of both low $R_{ds,on}$ values and at high switching frequencies, e.g. in applications featuring wide bandgap semiconductors. Ultimately, OVMs are performed on several power semiconductors for different operating conditions, and the results in terms of $R_{ds,on}$ are presented, underlying the advantageous practical applicability of the circuit.

In summary, the proposed OVMC generally enables on-state behavior analysis of power semiconductors (e.g. dynamic $R_{ds,on}$ effect investigation) and improves the accuracy of power converters loss breakdown models and of calorimetric switching loss measurement methods. Moreover, the OVM is envisaged as fundamental feature of next generation intelligent gate drivers, including temperature and condition monitoring, as well as time-to-failure prediction circuits.

Appendix

Considerations for the Accurate Tuning of the Proposed On-State Voltage Measurement Circuit

The influence of a mismatch in the diode (i.e. D_1 and D_2) voltage drops $v_{\Delta D}$ can be accurately characterized. In particular, if

$$v_{\mathrm{D_1}} \neq v_{\mathrm{D_2}} = v_{\mathrm{D_1}} \pm v_{\Delta \mathrm{D}},$$

then

$$v_{\mathrm{m}} \overset{(7)}{=} \frac{1}{1+\beta}(v_{\mathrm{ds}} \mp v_{\Delta \mathrm{D}}). \tag{19}$$

As in the diode-based approach of Fig. 2 (b), a mismatch in the correction of v_{D_1} translates in an offset of $v_{\Delta D}$ on v_m. However, Section III-B proved how, with the necessary precautions, a good accuracy can be reached. An offset on v_m can results also from resistive mismatches. First, if

$$R_3 \neq R_4 \quad \longrightarrow \quad \frac{R_3}{R_4} = 1 \pm \delta_{\mathrm{R}}$$

then

$$\begin{aligned} v_{\mathrm{m}} &\overset{(4)}{=} \frac{1}{1+\beta}\left((2 \pm \delta_{\mathrm{R}})v_1 - (1 \pm \delta_{\mathrm{R}})v_2\right) \\ &\overset{(6)}{=} \frac{1}{1+\beta}(v_{\mathrm{ds}} \mp \delta_{\mathrm{R}} v_{\mathrm{D_2}}). \end{aligned} \tag{20}$$

Second, if

$$\frac{R_{1\mathrm{b}}}{R_{1\mathrm{a}}+R_{1\mathrm{b}}} \neq \frac{R_{2\mathrm{b}}}{R_{2\mathrm{a}}+R_{2\mathrm{b}}} = (1 \pm \rho_{\mathrm{R}})\frac{R_{1\mathrm{b}}}{R_{1\mathrm{a}}+R_{1\mathrm{b}}}$$

then

$$\begin{aligned} v_{\mathrm{m}} &\overset{(4)}{=} \frac{1}{1+\beta}\left(2v_1 - (1 \pm \rho_{\mathrm{R}})v_2\right) \\ &\overset{(6)}{=} \frac{1}{1+\beta}(v_{\mathrm{ds}} \mp \rho_{\mathrm{R}} v_2). \end{aligned} \tag{21}$$

These information are relevant for the calibration of the proposed OVMC, e.g. understanding the causes of inaccuracy from the error trends. In particular, while $v_{\Delta D}$ in (19) and $\delta_R v_{D_2}$ in (20) are practically constant error terms, $\rho_R v_2$ in (21) is proportional to the variable measured voltage. Moreover, it results clear that precise resistors should be used for R_1–R_4.

Acknowledgment

The author would like to thank Dominik Neumayr for his precious advices and Jon Azurza Anderson for the support provided during the experiments.

References

[1] M. Guacci, D. Bortis, I. F. Kovačević-Badstübner, U. Grossner, and J. W. Kolar, "Analysis and design of a 1200 V all-SiC planar interconnection power module for next generation more electrical aircraft power electronic building blocks," *CPSS Transactions on Power Electronics and Applications,* vol. 2, no. 4, pp. 320-330, 2017.

[2] D. Bortis, O. Knecht, D. Neumayr, and J. W. Kolar, "Comprehensive evaluation of GaN GIT in low- and high-frequency bridge leg applications," in *Proc. of the IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia 2016),* Hefei, China, 2016, pp. 21-30.

[3] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$-pareto optimization and comparative evaluation of inverter concepts considered for the GOOGLE little box challenge," in *Proc. of the IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL 2016)*, Trondheim, Norway, 2016, pp.1-5.

[4] T. Foulkes, T. Modeer, and R. C. N. Pilawa-Podgurski, "Developing a standardized method for measuring and quantifying dynamic on-state resistance via a survey of low voltage GaN HEMTs," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC 2018),* San Antonio, TX, USA, 2018.

[5] "Measuring RDS(on) with high-definition oscilloscopes," *Rhode & Schwarz,* 2018.

[6] N. Badawi, O. Hilt, E. Bahat-Treidel, J. Böcker, J. Würfl, and S. Dieckerhoff, "Investigation of the dynamic on-state resistance of 600 V normally-off and normally-on GaN HEMTs," *IEEE Transaction on Industry Application,* vol. 52, no. 6, pp. 4955-4964, 2016.
[7] R. Li, X. Wu, G. Xie, and K. Sheng, "Dynamic on-state resistance evaluation of GaN Devices under hard and soft switching conditions," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC 2018)*, San Antonio, TX, USA, 2018, pp. 898-903.
[8] E. F. de Oliveira, C. Noeding, and P. Zacharias, "Impact of dynamic on-resistance of high voltage GaN switches on the overall conduction losses," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe 2017),* Nuremberg, Germany, 2017.
[9] Y. Cai, A. J. Forsyth, and R. Todd, "Impact of GaN HEMT dynamic on-state resistance on converter performance," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC 2017),* Tampa, FL, USA, 2017, pp. 1689-1694.
[10] A. Griffo, J. Wang, K. Colombage, and T. Kamel, "Real-time measurement of temperature sensitive electrical parameters in SiC power MOSFETs," *IEEE Transaction on Industrial Electronics*, vol. 65, no. 3, pp. 2663-2671, 2017.
[11] M. A. Eleffendi and C. M. Johnson, "In-service diagnostics for wire-bond lift-off and solder fatigue of power semiconductor packages," *IEEE Transaction on Power Electronics,* vol. 32, no. 9, pp. 7187-7198, 2017.
[12] S. Beczkowski, P. Ghimire, A. Ruiz de Vega, S. Munk-Nielsen, B. Rannestad, and P. Thøgersen, "Online vce measurement method for wear-out monitoring of high power IGBT modules," in *Proc. of the 15th European Conference on Power Electronics and Applications (EPE 2013),* Lille, France, 2013, pp. 1-7.
[13] M. Denk and M. -M. Bakran, "IGBT gate driver with accurate measurement of junction temperature and inverter output current," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe 2017),* Nuremberg, Germany, 2017.
[14] D. Rothmund, D. Bortis, and J. W. Kolar, "Accurate transient calorimetric measurement of soft-switching losses of 10 kV SiC MOSFETs and diodes," *IEEE Transaction on Power Electronics*, vol. 33, no. 6, pp. 5240-5250, 2016.
[15] D. Neumayr, M. Guacci, D. Bortis, and J. W. Kolar, "New calorimetric power transistor soft-switching loss measurement based on accurate temperature rise monitoring," in *Proc. of the IEEE 29th International Symposium on Power Semiconductor Devices and ICs (ISPSD 2017),* Sapporo, Japan, 2017, pp. 447-450.
[16] J. Azurza A, C. Gammeter, L. Schrittwieser, and J. W. Kolar, "Accurate calorimetric switching loss measurement for 900 V 10 m SiC MOSFETs," *IEEE Transaction on Power Electronics,* vol. 32, no. 12, pp. 8963-8968, 2017.
[17] B. Carsten, "Clipping pre-amplifier for accurate scope measurement of high voltage switching transistor and diode conduction voltages," in *Proc. of the 31st International Power Conversion Electronics Conference and Exhibit,* 1995.
[18] K. Kaiser, "Untersuchung der verluste von pulswechselrichterstrukturen mit spannungszwischenkreis und phasenstromregelung," Ph.D. dissertation, Technische Universität Wien, 1987.
[19] N. Badawi and S. Dieckerhoff, "A new method for dynamic ron extraction of GaN Power HEMTs," in *Proc. of the International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM Europe 2015),* Nuremberg, Germany, 2015, pp.1-6.
[20] R. Gelagaev, P. Jacqmaer, and J. Driesen, "A fast voltage clamp circuit for the accurate measurement of the dynamic on-resistance of power transistors," *IEEE Transaction on Industrial Electronics*, vol. 62, no. 2, pp. 1241-1250, 2015.
[21] S. Dusmez and B. Akin, "An accelerated thermal aging platform to monitor fault precursor on-state resistance," in *Proc. of the IEEE International Electric Machines and Drives Conference (IEMDC 2015)*, Lille, France, 2015, pp. 1352-1358.
[22] P. Ghimire, A. Ruiz de Vega, S. Beczkowski, B. Rannestad, S. Munk-Nielsen, and P. Thøgersen, "Improving power converter reliability: online monitoring of high-power IGBT modules," *IEEE Industrial Electronics Magazine,* vol. 8, no. 3, pp. 40-50, 2014.
[23] The Clipper - Springburo GmbH. (2017, November). [Online]. Available: www.springburo.weebly.com.
[24] CS1110 - Cleverscope Ltd. (2017, November). [Online]. Available: www.cleverscope.com/products/CS1110.
[25] *IR25750LPBF, International Rectifier,* 2015.
[26] *STL2N80K5, STMicroelectronics NV,* 09 2015, Rev. 3.
[27] *C3D1P7060Q, Cree Inc.,* 10 2015, Rev. F.
[28] *ADA4817-1 ADA4817-2, Analog Devices Inc.*, 2017, Rev. D.
[29] G. Deboy, O. Haeberlen, and M. Treu, "Perspective of loss mechanisms for silicon and wide band-gap power devices," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 89-100, 2017.

Mattia Guacci studied Electronic Engineering at the University of Udine, Italy where in July 2013 and in October 2015 he received his B.Sc. summa cum laude and his M.Sc. summa cum laude, respectively. In 2014 he was with Metasystems SpA in Reggio nell'Emilia, Italy working on EV onboard battery chargers. In November 2015 he joined the Power Electronic Systems Laboratory (PES) at ETH Zurich as a scientific assistant investigating innovative inverter topologies. In September 2016 he started his Ph.D. at PES focusing on integrated modular high efficiency and weight optimized power electronic converters for aircraft application.

Dominik Bortis received the M.Sc. degree in electrical engineering and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects. Since January 2016 Dr. Bortis is heading the newly established research group Advanced Mechatronic Systems at PES.

Johann W. Kolar received his M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria. Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 60 Ph.D. students. He has published over 650 scientific papers in international journals and conference proceedings, 3 book chapters, and has filed more than 140 patents. The focus of his current research is on ultra-compact and ultraefficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors. Dr. Kolar has received 23 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, and two ETH Zurich Golden Owl Awards for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the steering committees of several leading international conferences in the field and has served from 2001 through 2013 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.