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Wide-Input-Voltage-Range 3 kW DC-DC Converter with Hybrid LLC & Boundary / Discontinuous Mode Control

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***Abstract*—Growing applications such as electric vehicles, data centers, and industrial robotics require power-dense and efficient converters systems to provide high output currents at low output voltages of generally 12 V. Today's converters achieve high efficiencies at a specific input voltage, but drastically lose efficiency once the input voltage deviates from its nominal value. A large voltage swing, however, is a common situation in the aforementioned applications, as the respective input voltages, in worst-case, can easily drop by 50 %, whereby full functionality still needs to be maintained. In this work, we demonstrate a wide-input-voltage-range 400 V to 12 V, 3 kW dc-dc converter with a novel control method and transformer design. The employed boundary/discontinuous mode control scheme reduces circulating currents over conventional LLC techniques, and the "snake-core" matrix transformer achieves ideal parallel-connected secondary voltage balance. The converter achieves 350 $\mathrm{W/in^3}$ power density while operating from 300 V to 430 V input voltage and from 10 % to full load. An advanced design for a data center power supply application additionally utilizes the magnetizing inductance for boost operation in order to optimize the operating conditions of the converter system and to increase the overall efficiency. A performance comparison is finally explored for comparing the advanced design with the current hardware demonstrator and with conventional LLC converters.**

***Index Terms*—Resonant Converter, LLC, Soft Switching, Boundary/Discontinuous Mode Control, Wide-Input-Voltage Range.**

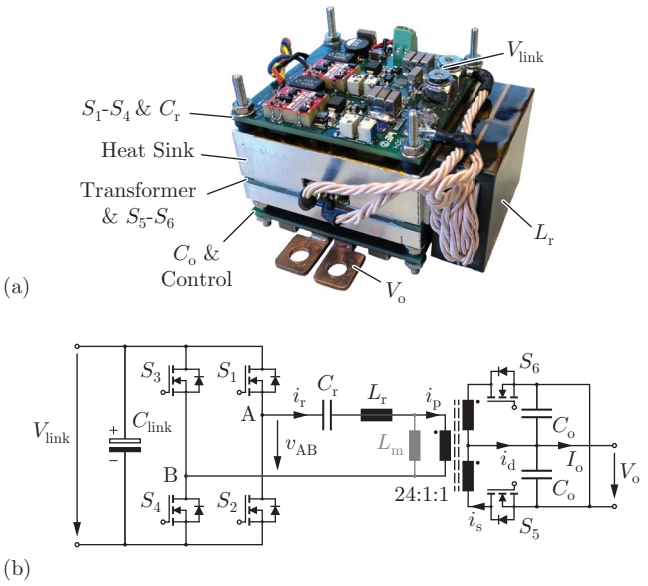

Fig. 1. (a) Implemented 3 kW hardware prototype of the B/DCM converter, measuring 2.0 in x 2.7 in x 1.6 in (350 $\mathrm{W/in^3}$). **(b)** Simplified power circuit topology of the current prototype, with the transformer implemented as the snake-core matrix transformer from [1] with 4 parallel-connected synchronous rectifier stages.

I. Introduction

A key power conversion stage in a broad range of emerging applications is a kW-scale, high-step-down-ratio dc-dc converter with a 12 V output. In electric vehicles, for example, this stage converts the high-voltage battery output, which typically varies between 250 V and 450 V, to 12 V for chassis electronics [2]. In data centers, the output of a mains-connected PFC rectifier is converted to supply the 12 V distribution bus, with nominal input voltage near 400 V and fault operation required down to 300 V [3]. Similar specifications are also required in automated industrial robotics [4]. These diverse applications feature common demands for this 12 V dc-dc converter: exceptional power density, high efficiency, and a wide input voltage range (cf. **Table I**).

Previous approaches to meet the given requirements are limited by the tradeoff between zero-voltage-switching (ZVS) and wide-input-voltage range; LLC-based, soft-switched designs achieve high efficiency within a narrow V_{link} range [5]–[7] while hard-switched topologies are lossy but can achieve the required range [8,9]. A design that combines the best features of both approaches is, however, mandatory in order to comply with the design specifications of **Table I**, where we require relatively high efficiency despite the large full-power output current and a tightly-regulated output voltage throughout the wide-input-voltage range.

In this paper, we introduce and validate novel control, magnetics, and topological schema for a converter to support

TABLE I
DC-DC CONVERTER DESIGN SPECIFICATIONS AND EXPECTED PERFORMANCE

Output voltage (V_o)	12 V
Full-load output power (P_o)	3 kW
Full-load output current (I_o)	250 A
Nominal input voltage range ($V_{link,nom}$)	300 V-430 V
Targeted power density	350 W/in^3
Targeted efficiency	95 %

both wide input voltage and high output current requirements. Specifically, the converter operates from 300 V-430 V and from 0 to 250 A output current (I_o). Our hardware prototype (see **Fig. 1(a)**) achieves a high power density of 350 W/in^3 and an efficiency of 94 %, near the targeted efficiency of 95 %. For a data center power supply with an efficiency target of 97.5 % or greater, however, we explore a circuit-level improvement for an advanced prototype that is described in detail. In **Section II**, the current hardware prototype is introduced and insights on the proposed control technique are given. **Section III** presents the main contribution of this paper, where we propose a topological redesign to support loss reduction across all operating modes. The 3D-model of the data center power supply prototype is included and discussed in **Section IV**. **Section V** summarizes the main takeaways from this paper.

II. HARDWARE PROTOTYPE CONVERTER

A. Overview

+ The current hardware prototype of **Fig. 1(b)** comprises a full-bridge, series resonant converter with a matrix transformer, and is operated with the boundary/discontinuous conduction mode control technique ("B/DCM") [1]. At most load levels, the converter is operated in boundary conduction mode (BCM), where the switching frequency (f_s) is modulated based on required output power and the duty cycle is varied to operate exactly at the discontinuous (DCM) and continuous conduction mode (CCM) boundary, as shown in **Fig. 2(a)**. In BCM, the transformer current is nearly sinusoidal, which reduces ac-related winding losses and peak currents, and the full-bridge and synchronous rectifier (SR) power switches operate under ZVS. At low output power, very high f_s would be required to maintain BCM, leading to high frequency-related losses in the magnetic components and gate-drives, whereby the converter is instead operated in DCM at a fixed, maximum f_s under duty cycle control (cf. **Fig. 2(b)**). In DCM, one half-bridge leg switches with ZVS while the other operates under zero-current-switching (ZCS) conditions. Relative to conventional CCM control technique of LLC converters, the additional degree of freedom due to the variable duty cycle of B/DCM extends the allowable input voltage range, achieves ZVS over a wide load range, and decreases the harmonic content of the currents in the circuit.

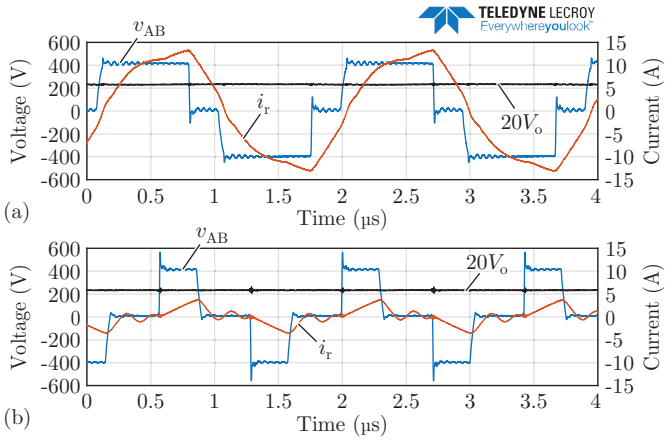

Fig. 2. (a) Key measured waveforms under BCM operation at 70 % load and 400 V_{link} (notation from **Fig. 1(b)**). **(b)** Key measured waveforms under DCM operation at 10 % load and 400 V_{link}.

The large output current (250 A) is split between four center-tapped, parallel-connected secondary windings, as introduced in [1], where we demonstrated a "snake-core" transformer (SNT) that overcomes the problem of flux imbalance in paralleled secondary windings. Information on the SNT design and circulating currents issue is given in [1], and is therefore not further discussed in this paper.

Unlike conventional LLC converters, the hardware prototype is operated as a step-down converter only, which is why the magnetizing current, and therefore the magnetizing inductance L_m of the SNT, is not used for the converter operation at all. Consequently, L_m is chosen to be large in order to minimize the circulating magnetizing current, as it would mainly introduce additional conduction losses. Even though this design constraint is relaxed in **Section III** to explore possible design improvements, the large magnetizing inductance is neglected in the following considerations, in order to simplify the analysis and comparison between BCM and CCM operations.

B. BCM versus CCM

The boundary and continuous conduction modes differ essentially on the shape of the tank excitation voltage v_{AB}. BCM controls the full-bridge such that v_{AB} assumes 0 V for a certain time before i_r crosses zero, allowing the combination of frequency and duty cycle modulations. CCM, however, generates only positive and negative V_{link}, limiting the output regulation to frequency control. The additional 0 V interval allows BCM to have a larger conversion-ratio range for the same switching frequency relative to CCM, as now the resonant gain

$$\mathrm{G}\left(f_s, d, Q\right) = \frac{nV_o}{V_{link}} = \mathrm{H}\left(f_s, Q\right)\sin\left(\pi d\right) \tag{1}$$

$$\mathrm{H}\left(f_s, Q\right) = \frac{\frac{f_s}{f_r}}{\sqrt{\left(\frac{f_s}{f_r}\right)^2 + Q^2\left[\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2}} \tag{2}$$

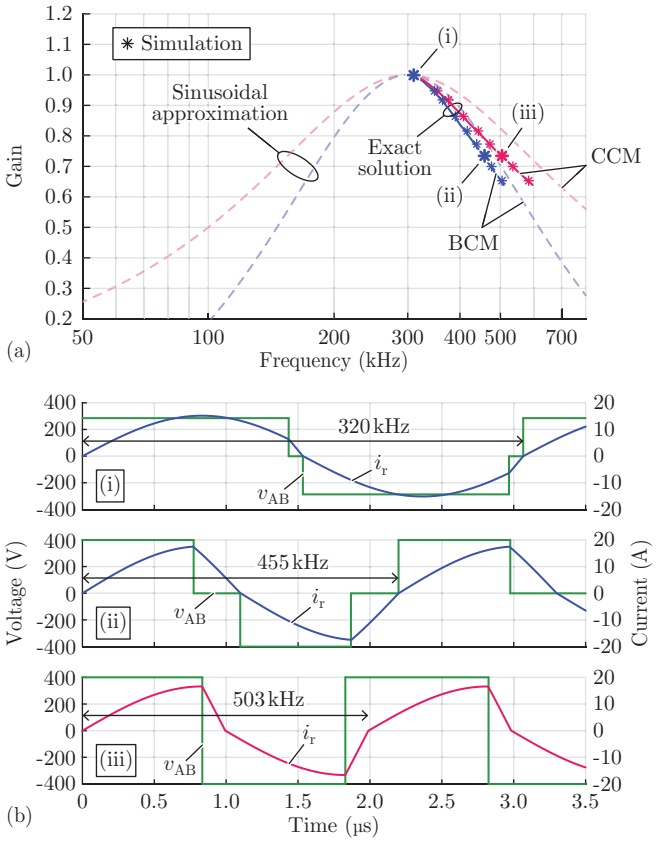

Fig. 3. (a) Resonant-tank gain-*versus*-frequency plots using the sinusoidal-approximation [10] solution of (1) and (2), and the exact solution of (3) and (4) at full-power. **(b)** Particular time-domain waveforms are shown to highlight the frequency deviation between BCM and CCM: (i) At $G = 1$, both BCM and CCM switch with $f_s \approx 320\,\text{kHz}$; while at $G = 0.735$, (ii) BCM switches with $f_s = 455\,\text{kHz}$ and (iii) CCM with $f_s = 503\,\text{kHz}$.

depends also on the duty cycle d of v_{AB}. If d equals 0.5, v_{AB} assumes a square shape and CCM operation takes place. In this particular case, $\sin(\pi d)$ equals 1 and we simplify G to the gain-*versus*-frequency characteristic of (2), i.e., the well-known dependency of G on f_s and Q. The quality factor (Q) is load-dependent and can be written as $Q = Z_r/R_{o,p}$, where $Z_r = \sqrt{L_r/C_r}$ is the tank characteristic impedance and $R_{o,p} = \frac{8n^2}{\pi^2}R_o$ is the equivalent load resistance seen from the primary side, which depends on both output resistance R_o and transformer turns-ratio n. **Fig. 3(a)** plots the gain-*versus*-frequency characteristic of the current prototype for both BCM and CCM at full-power (dashed lines). Both modes have, by definition, the same gain near the resonant frequency ($f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = 300\,\text{kHz}$). In this situation, $\frac{nV_o}{V_{link}}$ equals 1 and the turns ratio is set according to the lowest input voltage required: $V_{link,fault} = 300\,\text{V}$, $V_o = 12\,\text{V} \rightarrow n = 25$. At any higher input voltage, both BCM and CCM have to increase the switching frequency in order to keep the output at 12 V. In BCM, however, the same gain can be achieved by switching at a lower frequency (see dashed lines in **Fig. 3(a)**). BCM control therefore extends the allowable input voltage range relative to

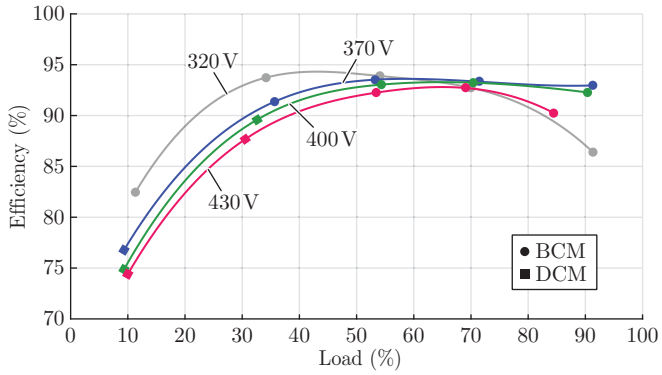

Fig. 4. Measured dc-dc efficiency across input voltage and load variation (prototype of **Fig. 1(a)**).

CCM and benefits from lower switching losses and conduction losses in frequency-related resistances.

As i_r is far from having a sinusoidal shape for frequencies higher than f_r (see waveforms in **Fig. 3(b)**), the sinusoidal approximation [10] used to derive expressions (1) and (2) is not accurate enough for comparing gain plots with circuit-simulation results. The exact solution is found solving the 2nd-order, resonant-tank equations,

$$v_C(t) = -(v_{AB}(t) - nV_o - V_{C,0})\cos(2\pi f_r t) + \\ + I_{L,0}\sin(2\pi f_r t)Z_r + v_{AB}(t) - nV_o \quad (3)$$

$$i_L(t) = \frac{v_{AB}(t) - nV_o - V_{C,0}}{Z_r}\sin(2\pi f_r t) + I_{L,0}\cos(2\pi f_r t), \quad (4)$$

for each different v_{AB} excitation over one switching period. **Fig. 3(a)** shows, in solid lines, the exact solution of the gain-*versus*-frequency plot for both BCM and CCM. The accuracy is compared and validated by circuit-simulation data displayed on the top of these lines and three different operating points are chosen for comparison purposes. Near the resonant frequency of the tank ($V_{link} = 300\,\text{V}$, $f_s = 320\,\text{kHz}$), both BCM and CCM achieve the same gain by switching at the same frequency. That does not hold true for lower gain values though, as the curves of BCM and CCM start to move away from each other. If we analyse v_{AB} and i_r at $G = 0.735$ (waveforms (ii) and (iii) in **Fig. 3(b)**), BCM achieves the same gain switching 50 kHz slower than CCM due to the lower $\frac{di_r}{dt}$ of BCM during the zero-volt interval of v_{AB}. This puts CCM at a disadvantage, setting the preference for BCM as the converter's ideal modulation scheme.

C. Experimental Performance

The preferred BCM control is implemented in the hardware prototype of **Fig. 1(a)**, which was characterized across the wide-V_{link} range from 10 % load to the full 3 kW output power. Measured efficiencies for the implemented converter are reported in **Fig. 4** (key components specified in **Table II**), with a maximum of 94 % near 50 % load and the minimum V_{link}. The converter power density is $350\,\text{W/in}^3$, with 16 % of

TABLE II
KEY COMPONENTS OF THE CURRENT HARDWARE PROTOTYPE.

S_1-S_4	CoolGaN (GaN) 600 V IGLD60R070D1 70 mΩ ($R_{ds(on)}$) 41 nC @ 400 V (Q_{oss})
S_5-S_6	OptiMOS (Si) 40 V BSC007N04LS6 0.7 mΩ ($R_{ds(on)}$) 103 nC @ 20 V (Q_{oss})
Transformer	Snake-Core Transformer [1] PCB windings, 4-layers N49 core, no airgap
Res. Inductor	8 µH, 16 A peak current Litz wire, 6 turns N49 core, 2 mm airgap
Res. Capacitor	13x 2.7 nF, 450 V, C0G CGA4J4C0G2W272J125AA

the volume dedicated to the resonant inductor (L_r) and 41 % consumed by the snake-core matrix transformer.

This converter achieves high power density and validates the control technique and transformer design with reasonably efficient operation across wide V_{link} and load ranges. In the hardware converter, there is significant self-heating in the GaN HEMTs at high output power, degrading efficiency due to increased $R_{ds,on}$ at high junction temperatures. Additionally, the SR body diodes conduct for a significant portion of the on-time (approximately one-sixth of the switching period), increasing losses in these MOSFETs by a factor of 3. In a first approximation, diode losses increase linearly with output power ($P_{diode} \approx V_F I_{avg}$), reducing efficiency across all load levels.

III. DESIGN IMPROVEMENTS

A. Data Center Power Supply Application

One increasingly important application that demands high efficiency ($> 97.5\,\%$), high power-density, and a wide input-voltage range is data center dc-dc power supplies. This application usually specifies a certain hold-up time (t_{hold}), during which the converter needs to maintain full functionality in case of mains failure. This hold-up time criterion directly determines the ratio between the required dc-link capacitance and the dc-dc converter input voltage range, as will be shown in the following. During the aforementioned mains failure, the 12 V output must maintain the regulated voltage for a couple of milliseconds (t_{hold}) while supplying the load with worst-case, full-power energy $\Delta E_o = P_o t_{hold}$. This energy is typically stored in dc-link capacitors, with the downstream dc-dc converter guaranteeing output voltage regulation during discharging. The dc-link discharges with $\Delta E_{link} = \frac{1}{2} C_{link} \left(V_{link,nom}^2 - V_{link,fault}^2\right)$ and the minimum capacitance that fulfills the hold-up time criterion is calculated as

$$C_{link} \geq \frac{2 P_o t_{hold}}{\eta_{dc\text{-}dc} \left(V_{link,nom}^2 - V_{link,fault}^2\right)}, \tag{5}$$

where $\eta_{dc\text{-}dc}$ corresponds to the dc-dc converter efficiency at full-power P_o. From (5), we see that the dc-link capacitance – and hence dc-link volume and cost – is minimized if the spread between the nominal voltage, $V_{link,nom}$, and the lowest operational voltage, $V_{link,fault}$, is maximized, demanding a dc-dc converter with wide-input-voltage-range capability.

This application requires a minor reconsideration of the specifications of **Table I** and the converter demonstrated in **Section II**. Most stringently, efficiently must be increased to a minimum of 97.5 %. In order to support this improvement, the power density requirement can be relaxed to $300\,\mathrm{W/in^3}$, which still allows to achieve the required overall power density of $80\,\mathrm{W/in^3}$ [11] considering also the PFC rectifier stage and dc-link capacitor. In this case, the efficiency should be optimized in the nominal operating range of $V_{link,nom} = 370\,\mathrm{V}$-$430\,\mathrm{V}$ but must operate continuously down to $V_{link,fault} = 300\,\mathrm{V}$. First, we consider the achievable efficiency improvements from a circuit and control scheme reconsideration with fixed power density, and subsequently relax the size constraints to meet the 97.5 % efficiency benchmark.

B. Additional Degree of Freedom

A reconsideration of the circuit design and control scheme are needed to increase the converter efficiency. By setting the lowest input voltage at the resonant frequency (gain of 1 in **Fig. 3(a)**), the converter can only operate in a "buck" mode. As resonant converters are most efficient switching at the resonant frequency, the buck-only operation of the current hardware prototype maximizes efficiency at the minimum V_{link} (as seen experimentally in **Fig. 4** for $320\,\mathrm{V}_{link}$), which occurs only during the infrequent fault operation. In the nominal operating range for this application ($V_{link} = 370\,\mathrm{V}$-$430\,\mathrm{V}$), the switching frequency is relatively high and DCM – where one of the half-bridges is hard-switched – is used extensively, resulting in the steep degradation of efficiency at light load seen in **Fig. 4.**

Intuitively, a design would have higher efficiency if f_s was closer to the L_r-C_r resonant frequency (f_r) in the nominal V_{link} range; that is, if the gain of 1 operating point ($\frac{nV_o}{V_{link}} = 1$) was selected nearer the 370–430 V_{link} range. Fault operation would then operate in a "boost" mode, which requires a finite magnetizing inductance (L_m) and LLC-style operation in this boost regime [12]. Considering L_m as an additional design parameter, the gain transfer function of (2) is expanded into a new form:

$$\mathrm{H}(f_s,Q) = \frac{(m-1)\left(\frac{f_s}{f_r}\right)^2}{\sqrt{\left[m\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2 + Q^2(m-1)^2\left(\frac{f_s}{f_r}\right)^2\left[\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2}} \tag{6}$$

where $m = 1 + \frac{L_m}{L_r}$ represents the ratio between L_r and L_m. As the magnetizing inductance becomes much larger than L_r ($L_m \to \infty$), (6) collapses to (2).

Fig. 5(a) plots the gain function (1) in combination with (6) for three different selections of L_m. The reduction of the magnetizing inductance L_m allows for an operation in "boost"-mode, with gains above unity. Here, in addition to the aforementioned BCM and DCM control schemes used to operate the current hardware prototype (cf. **Fig. 2**), we introduce the "LLC-mode" for switching frequencies below the resonant frequency of 300 kHz. Typical waveforms of the three operating modes are shown in **Fig. 5(b,c,d)**. If the converter requires "boost"-mode operation, the control imposes a square-wave v_{AB} voltage with $f_s < f_r$, as shown in **Fig. 5(b)**, and gains above 1 can be achieved. On the other hand, BCM control is used in "buck"-mode operation for $f_r < f_s < f_{s,max}$ up to a maximum switching frequency ($f_{s,max}$) defined by design (waveforms shown in **Fig. 5(c)**). For $f_s = f_{s,max}$, DCM is used and the switching frequency is fixed while the duty cycle of v_{AB} is changed to control the power flow (cf. **Fig. 5(d)**).

DCM should only be used at light load conditions, as i_r is no longer sinusoidal and high losses result for high output-power values (P_o). For this reason, it would be reasonable to select the design with $L_m = 53\,\mu H$ instead of $89\,\mu H$ in **Fig. 5(a)**, as a lower step-down gain at the transition between BCM and DCM is achieved, extending BCM operation to lower P_o values. However, the design with $L_m = 53\,\mu H$ requires twice as much resonance inductance L_r for keeping the maximum boost gain at 1.2, increasing the volume of this component accordingly. Furthermore, a smaller L_m yields larger magnetizing currents (i_m), which, on the one hand, increase conduction losses, but, on the other hand, support ZVS at light loads. The magnetizing inductance as a free design parameter therefore introduces a tradeoff in the converter design, but nevertheless we expect efficiency improvements, as the new degree of freedom of L_m allows to shift the converter's nominal operating region closer to the most-efficient gain-of-1 operating point. The extent of these improvements will be assessed in the following subsections.

C. Design Considerations

In order to confirm the benefits of the proposed enhanced control scheme, a performance comparison between the current hardware prototype, the next-iteration design and common LLC designs must be conducted. To accomplish this comparison, we evaluate performance across the V_{link} and load ranges for all these three designs: (i) the buck-only prototype of **Section II** ("B/DCM"), (ii) a design with B/DCM control in the nominal range and LLC-mode control during fault conditions ("Hybrid"), and (iii) an LLC-only design without B/DCM control ("LLC"). The B/DCM design operates only with the waveforms that are shown in **Fig. 5(c,d)**, while the LLC design is mostly characterized by the waveforms of **Fig. 5(b)**. The Hybrid control, however, benefits from all three operating modes in **Fig. 5(b,c,d)**. These designs must operate

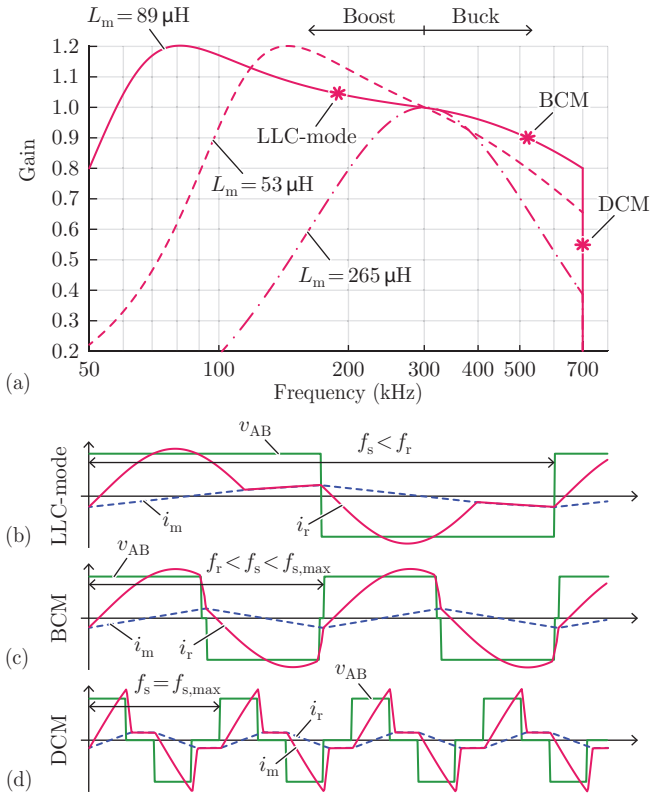

Fig. 5. (a) Plot of the gain function (1) in combination with the expanded tank transfer function (6) for different L_m values. Three operating modes are highlighted in (a) with corresponding time-domain waveforms ($L_m = 89\,\mu H$): **(b)** LLC-mode for boost operation ($f_s < f_r$), and **(c)** BCM ($f_r < f_s < f_{s,max}$) and **(d)** DCM ($f_s = f_{s,max}$) for buck operation.

down to 300 V_{link} but we seek to optimize the efficiency in the nominal V_{link} range.

To shift the nominal operating range closer to the resonant frequency and consequently optimize efficiency, we must properly select nV_o such that $\frac{nV_o}{V_{link}} = 1$ for a V_{link} near or within the nominal range. The Hybrid design places nV_o just below the nominal range minimum (360 V_{link}) and maximizes the $m-1$ ratio, L_m/L_r, and the tank quality factor, Q, to achieve the required gain at 300 V_{link}. These design choices force the Hybrid control to operate in buck mode across the nominal input range ($V_{link} > 360\,V$), and to enter boost mode only in case of mains fault – taking advantage of the B/DCM-control benefits described in **Section II**. Following the efficiency-optimal design guidelines in [12], the LLC design places nV_o at 420 V_{link} and solves for the maximum $(m-1)Q$ product that can maintain regulation down to 300 V_{link}. The values for each design, including the first-generation prototype, are listed in **Table III**, and the transfer function gain for each tank are compared in **Fig. 6(a)**.

Relative to the LLC, the Hybrid design needs much lower boost gain and extends the regulation capability at $f_s > f_r$, resulting in a higher $(m-1)Q$ figure-of-merit and lower circulating currents. The LLC design follows the design guidelines

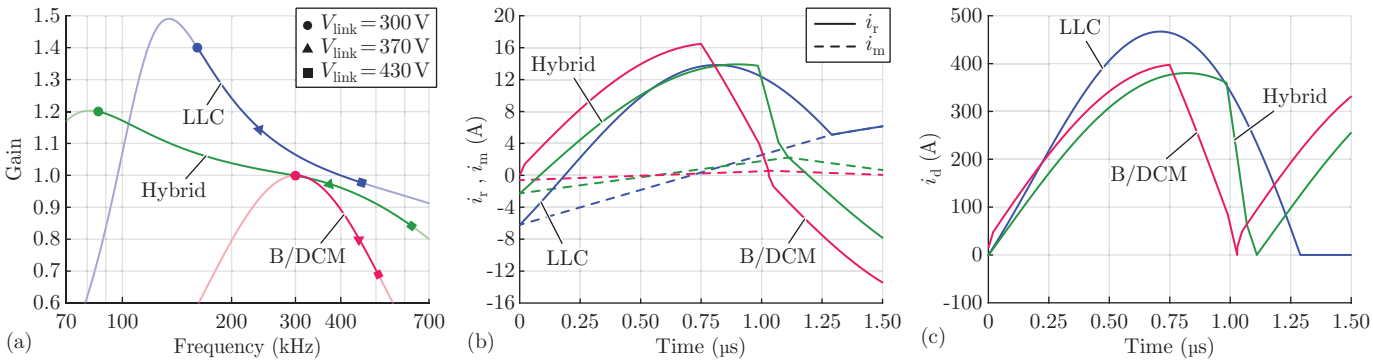

Fig. 6. Operating characteristics for the three proposed designs at maximum load. **(a)** Voltage gain. **(b)** Predicted resonant-tank current (i_r) and magnetizing current (i_m) at $400\,V_{link}$. **(c)** Predicted secondary-side rectified current (i_d) at $400\,V_{link}$.

of [12], where we must tradeoff conduction losses with a lower magnetizing inductance and the width of achievable gain. An efficiency-maximized design yields the LLC gain curve of **Fig. 6(a)**. A comparison between current waveforms at the nominal V_{link} and full output power are shown in **Fig. 6(b,c)**. The small magnetizing inductance in the LLC (again, needed for high boost gain) results in higher primary-side RMS currents for the same output power, increasing conduction losses in the transformer primary windings and full-bridge power devices. The LLC design has also higher secondary-side RMS currents due to a zero-current interval during the "Open" mode (discontinuous conduction on the secondary side [12]), which increases the peak value of that current to compensate for the 0 A interval (cf. **Fig. 6(c)**), leading to higher conduction losses in the SR MOSFETs.

Relative to the B/DCM, the Hybrid design operates closer to the gain-of-1 operating point and has currents with lower peak-to-average ratios. Furthermore, the magnetizing current is larger relative to B/DCM, improving primary-side ZVS at light load at the expense of slightly-higher conduction losses.

The Hybrid design therefore has the potential to outperform both other designs, but a loss analysis is required to confirm this claim and benchmark the achievable efficiency, which is performed below.

D. Analysis Techniques & Loss Models

To compare the three designs across the full range of V_{link} and output power, we numerically calculate the steady-state waveforms at each operating point and use first-order models to estimate the key loss mechanisms, assuming a fixed volume for magnetics and ideal synchronous rectification (i.e. zero body diode conduction).

For each design and at each V_{link}-load operating point, there is a unique set of operating conditions that satisfy periodic steady-state conditions. Unfortunately, with a finite magnetizing inductance and the inclusion of a DCM mode (or "Open" mode in case of LLC), there are no analytical solutions and the sinusoidal approximation is inaccurate for much of our operating range [13]. Numerical techniques are therefore used to find the state variables in steady-state operation, and the full current and voltage waveforms for the converter are then known.

TABLE III
KEY SPECIFICATIONS FOR COMPARED DESIGNS

Parameter	B/DCM	Hybrid	LLC
f_r	300 kHz	300 kHz	400 kHz
$f_{s,min}$	300 kHz	75 kHz	75 kHz
$f_{s,max}$	700 kHz	700 kHz	700 kHz
nV_o	300 V	360 V	420 V
L_r	8 µH	3.7 µH	4.4 µH
C_r	35 nF	76 nF	36 nF
L_m	265 µH	89 µH	48 µH

With the full current and voltage waveforms synthesized, power dissipation in the key components is estimated with first-order loss models. In the primary-side GaN HEMTs, we include conduction losses ($i^2 R_{ds,on}$ losses with $R_{ds,on}$ equal to the datasheet value at 100 °C) and hard-switching losses, and ignore any soft-switching losses from resonantly charging and discharging the parasitic output capacitance, C_{oss}. At 500 kHz, the worst-case error from ignoring these soft-switching losses is around 0.75 W per device [14]. To include hard-switching losses, we first note that the first switching transition per half-cycle will be soft-switched (see **Fig. 3(b)**) if the load current is sufficiently high, and we make this assumption for the full operating space. The hard-switched losses that occur from partial ZVS are calculated using the method in [15], with the current at the switching transition known from the numerical synthesis.

In an LLC-like design, the resonant inductor can be integrated into the same snake-core structure used for the transformer in this design [1]. To do this, the nearly-perfect interleaving between the primary and secondary windings will need to be reduced, which will increase the AC resistance. To calculate conduction losses in the resonant inductor and transformer, we use an AC resistance factor of $\frac{R_{AC}}{R_{DC}} = 1.1$ beyond the DC resistance of the windings. Core losses are calculated using the Generalized Steinmetz fitting [16] based

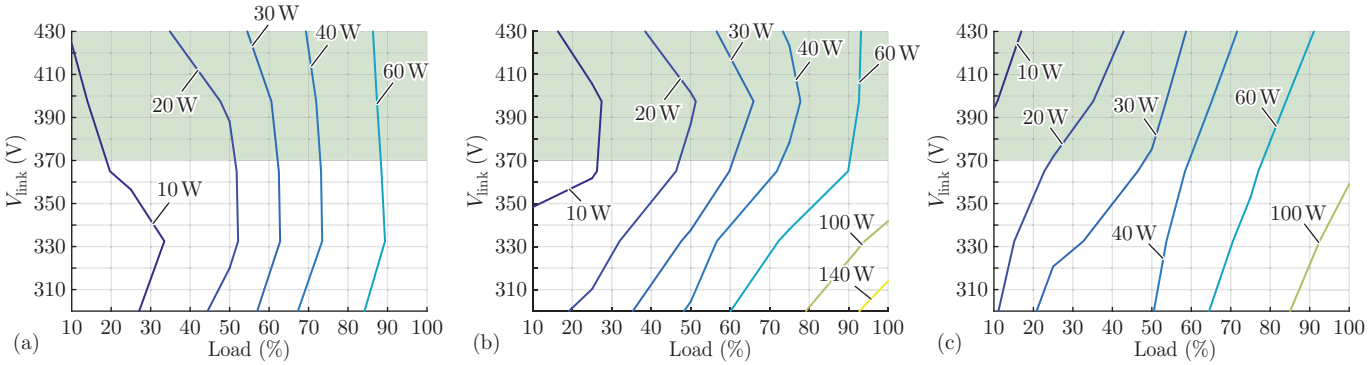

Fig. 7. Modeled losses at all V_{link}-P_{o} operating points for: **(a)** the currently realized B/DCM design (cf. prototype shown in **Fig. 1(a)**), **(b)** the Hybrid-control scheme, and **(c)** the efficiency-optimized traditional LLC design. The "Hybrid" design is the most efficient for the nominal operating conditions (highlighted in green).

on the maximum magnetizing current, and losses in the resonant capacitor (C_{r}) can be comfortably ignored.

Because they operate under ZVS conditions, the secondary-side synchronous rectifier device losses are assumed to only include conduction losses. In this model, we assume perfect synchronous rectification, or zero diode conduction time. Accordingly, a fast, reliable sensing and driving circuit is critical to mitigating any additional losses that occur from diode conduction.

E. Performance Comparison

Fig. 7 shows the calculated converter losses for the prototype converter (B/DCM, cf. **Fig. 1(a)**) and the two potential design improvements (Hybrid and LLC). The B/DCM converter achieves the lowest losses at input voltages that only occur during fault events for this application, and both the Hybrid and B/DCM design outperform the conventional LLC in the nominal input voltage range (green, shaded area). At 400 V_{link} and 3 kW output power, the LLC dissipates 81 W, the Hybrid design dissipates 70 W, and the B/DCM design has 78 W of predicted losses. The required inductance values are more than 50 % lower in the Hybrid design than in the B/DCM design, further improving efficiency for a fixed-volume magnetics design or power density for a fixed-loss design.

For any LLC design, there exists a fundamental tradeoff between nominal efficiency and gain range [7], whereas with the B/DCM control, the Hybrid design can use a lower gain range. The higher circulating currents, shown at one operating point in **Fig. 6(b)**, increase losses throughout the operating region and this analysis confirms the mutual exclusivity of high efficiency and wide voltage range for conventional LLCs. Based on the analysis here, the Hybrid design is necessary to reach the target efficiency of 97.5 % at maximum power in the nominal voltage range.

IV. Next-Iteration Hardware Prototype

The results presented in **Section III** confirm the potential of the Hybrid design to outperform the compared ones, as intuitively justified throughout the section and verified by the loss analysis. Our next-iteration virtual prototype is shown in **Fig. 8**, with dimensions of 3.5 in x 2.7 in x 0.53 in. In this implementation, we split the 3 kW converter into two identical modules of 1.5 kW each, which are then connected in a parallel-input parallel-output configuration. The modular approach significantly enhances the converter's thermal management relative to the first-iteration prototype of **Fig. 1(a)**. Therefore, we expect to achieve 300 W/in^3 in power density, which is less than the current hardware, but we outperform the current system in terms of efficiency, finally reaching the 97.5 % target.

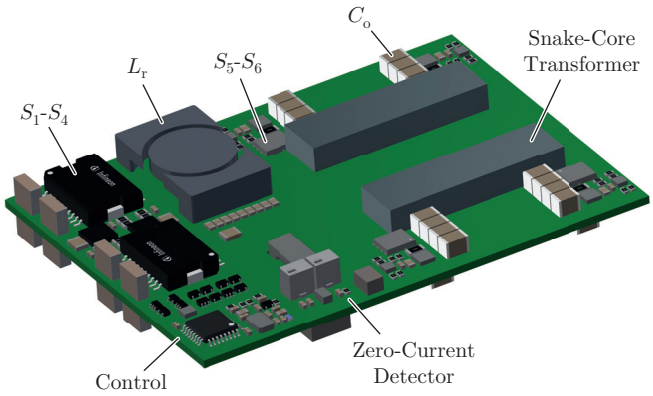

Fig. 8. Virtual hardware prototype of the next-generation, 3 kW dc-dc converter, each module of 1.5 kW measuring 3.5 in x 2.7 in x 0.53 in (300 W/in^3). The design uses the Hybrid-control scheme described in **Section III**, which combines B/DCM and LLC-like modulations.

V. Conclusion

A hardware prototype of a wide-input-voltage-range 400 V to 12 V, 3 kW dc-dc converter is described, which employs B/DCM control and achieves high power density (350 W/in^3) but requires improvements to increase the efficiency beyond the measured 94 %. To adapt the converter for a data center dc-dc application with a target efficiency of $>$ 97.5 %, we

compare predicted losses for three circuit and control combinations, and find the highest efficiency for an improved "Hybrid" design that utilizes both LLC and B/DCM control schemes. A detailed and comprehensive analysis on resonant-tank transfer functions and predicted time-domain current waveforms gives reasoning for the reported higher performance of the Hybrid control. In summary, the converter design takes advantage of the Hybrid-control benefits, and we expect to achieve the targeted efficiency of $97.5\,\%$ at a power density of $300\,\mathrm{W/in^3}$.

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