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Multi-Objective Minimization of Life-Cycle Environmental Impacts of Three-Phase AC-DC Converter Building Blocks

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***Abstract*—The goal of net-zero greenhouse gas emissions by 2050 requires a massive expansion of the use of renewable energy sources like photovoltaics and offshore/onshore wind, and the comprehensive electrification of transportation and upscaling of the industry. The energy transition thus implies an unprecedented scaling-up of the installed power electronic conversion capacity. This motivates an in-depth investigation of the environmental impacts (e.g., greenhouse gas emissions, but also damages to human health, ecosystem quality, or resource availability) of power electronic systems, whereby the entire life cycle and in particular the use phase must be considered. Typically, such Life-Cycle Assessments (LCAs) are carried out only for existing products and not during the early design phase. In this paper, we therefore extend a multi-objective Pareto optimization framework for power electronic converter systems, which today typically considers only efficiency and power density as performance indicators, to include environmental compatibility metrics as additional performance dimensions. After describing the models and the data sources used to estimate the environmental footprint of typical power electronic components like transistors, magnetic components, printed circuit boards, etc., we employ these in a multi-objective optimization of an exemplary 10 kW three-phase ac-dc Power Electronic Building Block (PEBB) considering two-level and multilevel flying-capacitor bridge-legs. First results indicate the importance of the mission profile and the available electricity mix during the use phase, which may justify selecting a converter design with an initially larger environmental burden but better efficiency. Finally, the key challenge of LCAs consists in the lack of comprehensive and high-quality environmental impact data of electronic components, which thus should be addressed by the industry, e.g., by providing such information in future smart datasheets.**

***Index Terms*—Power electronic building blocks, carbon footprint, life-cycle assessment (LCA), multi-objective optimization, environmental impact.**

I. Introduction

Reaching the goal of net-zero anthropogenic greenhouse gas emissions by 2050 requires the full decarbonization of crucial sectors such as, e.g., electric energy generation, industry, and transportation [1], [2]. Maintaining today's standard of living will require a substantial improvement of energy conversion efficiency and a massive increase of renewable electricity generation which, assuming a future global population of 10 billion people with an average power demand of 2.5 kW per capita, totals to 25 000 GW [3]. Power electronics will play a main role in the future grid where electric energy will typically be converted four times between source and the point of use by means of power electronics [4], corresponding to 100 000 GW of worldwide installed power electronics conversion capacity [3], [5], [6]. This represents an unprecedented upscaling of the use of power electronic systems. With a typical service lifetime of typically only 20 to 25 years [7], [8], power electronic converters produced today will be decommissioned by 2050; then, additional electronic waste corresponding to the equivalent of about 5000 GW of installed power converter capacity results annually [5], [6], which also raises concerns regarding scarcity of critical natural resources. Accordingly, the transition from the current linear economy into a future circular economy represents one of the main future challenges in power electronics [6], [9]–[16]. This motivates an in-depth investigation of the environmental footprint of power electronic converter systems over their entire life cycle by means of Life-Cycle Assessments (LCAs) [3], [5], [6], [17]–[21]. An LCA is typically performed for existing products and considers the relevant emissions of the entire value chain (or parts of it), and may include resource extraction, production, transport, operation (use phase), decommissioning, and recycling of a system. The finally considered environmental metrics may include, e.g., Global Warming Potential (GWP) measured in kg of CO_2-equivalent ($CO_{2,eq}$) greenhouse gas emissions, water and land use, release of toxic substances, etc. Thus, high-level Life-Cycle Impact Assessment (LCIA) metrics such as defined by the ReCiPe framework [22], [23] aggregate the weighted impacts of environmental mechanisms into three endpoint categories that correspond to three areas of protection, i.e., human health, the natural environment, and resource scarcity. In contrast to the commonly employed *a-posteriori* LCIAs, this

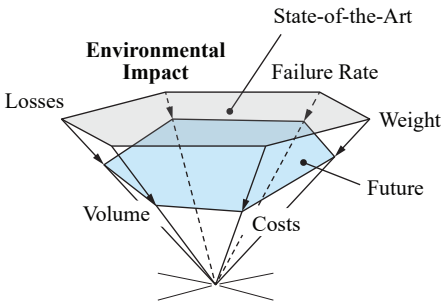

Fig. 1. Performance metrics and performance trends of power electronic converter systems.

paper describes how to include environmental considerations already in the design phase of a power electronic converter [3], [5], [6], i.e., *a priori*, whereby multi-objective Pareto optimization [24]–[28] enables a systematic converter design by considering the trade-offs between multiple performance indicators. So far, the typically considered performance metrics are efficiency and power density (and possibly cost). The design space diversity [29], i.e., the fact that designs with very different values of the design parameters finally show almost identical performance metrics (e.g., the same volume and losses), presents a so far unexplored opportunity to also consider the above-mentioned environmental metrics (and other related aspects such as reliability/lifetime), see **Fig. 1**, and thereby facilitate sustainable converter designs [3], [5], [6].

The paper specifically describes the assessment and modeling of the carbon footprint and/or GWP and the three endpoint impact categories defined by the ReCiPe framework (i.e., Damage to Human Health (DHH), Damage to Eco-System Quality (DESQ), and Damage to Resource Availability (DRA)) [22], [23] of the relevant components of power electronic converters in **Section II**. Then, using a generic 10 kW three-phase ac-dc PEBB (see **Fig. 2**) as an example, **Section III** outlines the developed multi-objective optimization procedure that simultaneously considers efficiency, power density, $CO_{2,eq}$ emissions (i.e., GWP), and the ReCiPe metrics as optimization criteria. The results of the optimization are discussed in detail and several major impact factors on the converter performance limits are investigated, including the component model tolerances, the selected power transistor junction temperature, the modulation strategy, and use-phase-related emissions that depend on the converter's efficiency characteristic and the mission profile. Further, the performance limits, including the environmental impacts, of the simple two-level three-phase ac-dc converter PEBB from **Fig. 2a** are then compared against advanced three-level and seven-level Flying Capacitor (FC) Multilevel (ML) converter topologies. Finally, **Section V** summarizes the main findings of this paper and provides an outlook on research vectors for future power converters with minimum life-cycle environmental footprint.

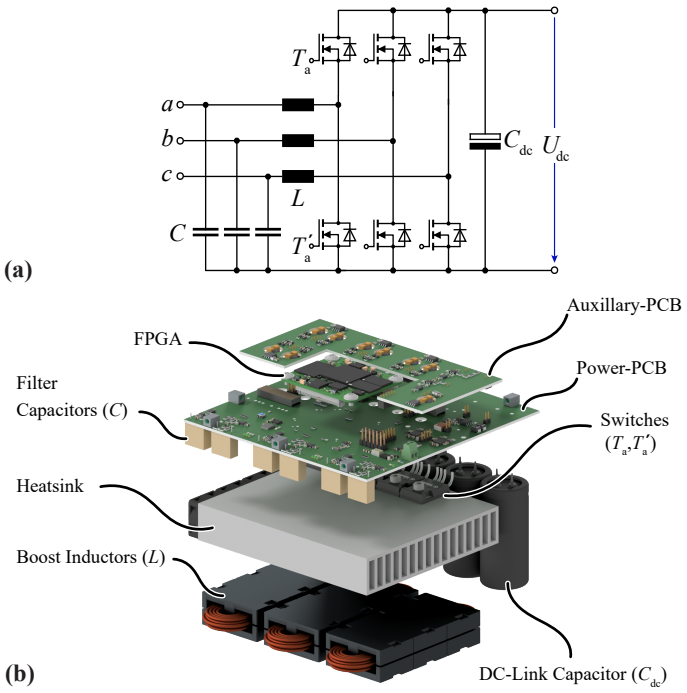

Fig. 2. The considered application example in this paper is a 10 kW three-phase ac-dc PEBB that interfaces a 400 V (RMS line-to-line voltage) three-phase ac voltage and an 800 V dc-link voltage, using 1200 V Silicon Carbide (SiC) power semiconductors: **(a)** Main power circuit and **(b)** 3D rendering of an exemplary prototype system with the key components highlighted.

II. Environmental Impacts of Power Electronic Components

This section describes generic models for the environmental impact of the relevant converter components, which then enable a systematic and holistic, i.e., including the environmental impact, optimization of power electronic converters in **Section III**. Aiming at the goal of net-zero anthropogenic greenhouse gas emissions by 2050, the Global Warming Potential (GWP), i.e., the greenhouse gas emissions measured in CO_2-equivalents according to the IPCC 2021 standard [30], is one of the key performance metrics. GWP is, however, not the only relevant metric; e.g., producing a certain component might also release toxic substances into the environment, require a certain amount of water or critical mineral resources, etc.

Aiming thus at a comprehensive assessment of the environmental footprint, the ReCiPe 2016 [22], [23] framework is considered: The emissions of all involved substances and processes are first grouped into several midpoint categories (e.g., particulate matter emissions, water usage, ozone depletion, GWP, etc.). These are then further aggregated to model the impacts on three endpoint areas of protection, which are: Damage to Human Health (DHH) (years lost or the impairment endured by an individual as a result of illness or accident; measured in disability-adjusted life years, DALY), DESQ (local species loss over time; measured in species·years), and Damage to Resource Availability (DRA) (additional expenses incurred in the extraction of mineral and fossil resources in the future; measured in 2013-equivalent USD). Note that ReCiPe defines three value perspectives that differ regarding the time horizon over which adverse effects are taken into account (20 years for the individualist, 100 years for the hierarchist, and 1000 years for the egalitarian perspective) and result in different weights in the aggregation of the endpoint impacts; here, we consider the egalitarian perspective.

A. Component Models

Databases such as ecoinvent [31] or GaBi [32] provide detailed environmental metrics for materials, components, and processes, etc., which can be used to derive the required generic models for the environmental impact of (power) electronic components.[1] Further, many publications investigate the GWP

[1]Note that the gathering of primary data, e.g., by disassembling components as in [21], is only applicable once a converter has actually been realized using specific components but not *a priori* during the design phase.

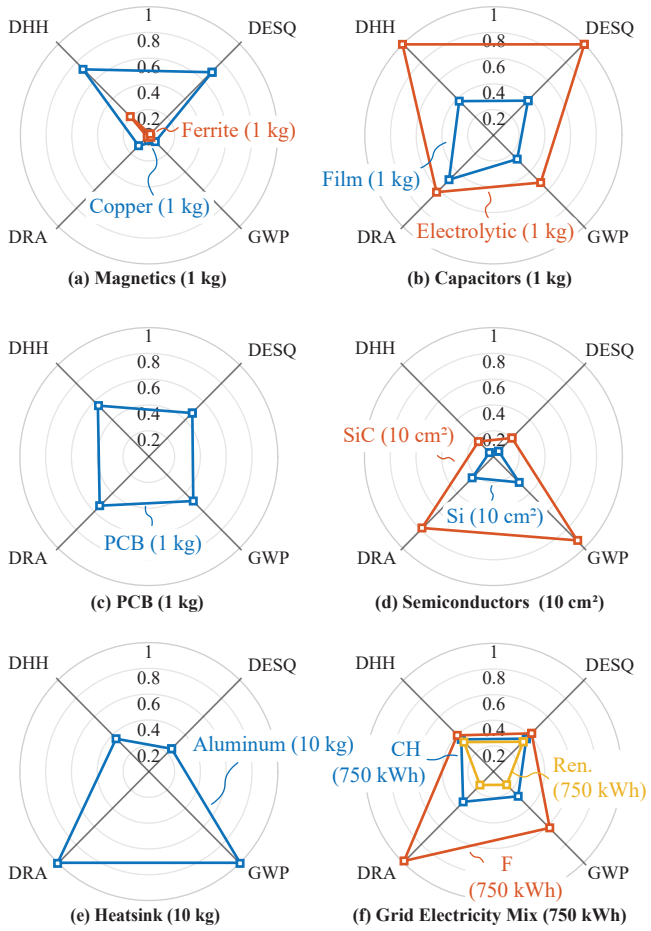

Fig. 3. Environmental impact metrics (Damage to Eco-System Quality (DESQ), Global Warming Potential (GWP) (i.e., $CO_{2,eq}$ emissions), Damage to Resource Availability (DRA), Damage to Human Health (DHH)) of the main components found in a power electronic converter: **(a)** Magnetic components (ferrite core and copper windings per kg of material, **(b)** capacitors (film and electrolytic capacitors per kg of material) **(c)** Printed Circuit Board (PCB) (per kg of material), **(d)** power semiconductors (SiC and Silicon (Si) material per 10 cm^2 of wafer), **(e)** aluminum heatsink (per 10 kg of material). **(f)** Comparison of the environmental impact of different grid electricity mixes (per 750 kW h of consumed energy), i.e., for Switzerland (CH), France (F), and for a purely renewable generation mix (Ren.). All metrics are based on the ecoinvent database [31] and plotted on p.u. scales, as the database license does not allow direct citations of specific values. To allow a qualitative comparison of the impact profiles, identical base values for the axes are used in (a)-(f), though.

footprint of power electronic components [21], [31]–[46]. The values reported by different sources—especially for materials with low production volumes—often vary in a wide range. Therefore, **Section III** also discusses the impact of the modeling uncertainties and/or the data quality/availability on the findings of this work. In contrast to the GWP, fewer data is available in the literature for other environmental impact categories like those defined by the ReCiPe framework; there, we rely on data from the ecoinvent database [31] (this is not explicitly mentioned for every component category discussed in the following).

- **Magnetics:** The environmental impact contributions of the inductor's (or transformer's) magnetic core and winding can be assessed separately: [31], [33] provide the weight-specific GWP emissions for ferrite cores (in $kgCO_{2,eq}/kg$). Similarly, the weight-specific GWP emissions for the copper windings are obtained from [31], [34]–[37].
- **Capacitors:** Power capacitors can be categorized dependent on the dielectric material as film, electrolytic or Multi-Layer Ceramic Capacitors (MLCCs), and the weight-specific GWP emissions are obtained from [21], [31], [47]. Note that due to the lack of more specific data, this is a generic model which does not take into account the impact of the voltage rating and capacitance value on the mass ratio of dielectric and electrode material.
- **PCB:** A PCB comprises several layers of conducting (copper) and insulating (FR-4) materials and [39] states that the GWP footprint is dominated by the FR-4 material (42.3%) and by the PCB production processes (27.3%). The weight-specific GWP emissions are obtained from [21], [31], [38], [39] and the area-density of a PCB is estimated with $\rho_p = 4\,kg/m^2$ (assuming a six-layer PCB with 70 µm copper thickness and 50% copper content).
- **Power transistors:** The processing steps for power semiconductors can be split into (1) substrate/wafer production, (2) front-end processing (anealing/doping), and (3) back-end processing (packaging), with (3) being by far the least energy-intensive process [40]–[42]. Therefore, this paper only considers the processes (1) and (2): The ecoinvent database [31] provides chip-area-specific GWP emissions (in $kgCO_{2,eq}/m^2$) and ReCiPe data for Si Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) and this data is adapted to SiC MOSFETs by scaling the emissions for the process (1) based on the energy demand by about a factor of 80 compared to Si [21]. The energy demand and associated emissions for the front-end processing of Si and SiC MOSFETs (process (2)) is assumed to be identical [21]. The required chip area A_{chip} of a MOSFET is estimated based on the on-state resistance R_{on} as $A_{chip} = k_{R,0} + k_{R,1}/R_{on}$, and $k_{R,0} = 5.26\,mm^2$ $k_{R,1} = 468.3\,mm^2/m\Omega$ was found for 1200 V SiC MOSFETs from Microchip [48].[2]
- **Heatsink:** Forced-air cooling with aluminum heatsinks is considered here, and the weight-specific GWP emissions for aluminum are obtained from [31], [43]–[45]. Note that an aluminum fill factor $k_u = 60\%$ is assumed to account for the air in between the heatsink's fins. The emissions related to the fan(s) are not taken into account in a first step.
- **Auxiliary components:** Apart from the main power components (see **Fig.2**), a plurality of auxiliary components is required to operate a converter: Si Integrated Circuits (ICs) are required for the Digital Signal Processor (DSP) as well as for voltage/current measurements and logic functions. The environmental impact is assessed with weight-specific

[2]For the FC ML bridge-legs discussed in **Section IV-D**, power transistors with lower blocking voltage are considered and the following parameters for the chip area estimation are employed: $k_{R,0} = 2.25\,mm^2$ $k_{R,1} = 393.9\,mm^2/m\Omega$ for 700 V SiC [49] and $k_{R,0} = 0\,mm^2$, $k_{R,1} = 2.6\,mm^2/m\Omega$ for 200 V Si MOSFETs [50].

GWP and ReCiPe data from the ecoinvent database [31]. Further, in addition to the ICs, each auxiliary functional unit requires several low-voltage resistors and capacitors in Surface Mount Device (SMD) packages. The dataset from ecoinvent [31] provides weight-specific GWP emissions and ReCiPe values as well as typical SMD component weights.

- **Electricity:** Finally, as will be discussed below in **Section III**, conversion losses waste electric energy during the use phase of a converter. Each kWh of electricity comes with an associated environmental footprint which varies massively depending on the electricity mix of the considered geographic region/country. The energy-specific GWP (in $kgCO_{2,eq}$/kWh) is obtained from [31], [46].

B. Comparison of Component Environmental Footprints

Fig. 3 compares the relevant environmental impact metrics (DESQ, GWP DRA, DHH) of a power electronic converter's main components on a relative scale (the license of the ecoinvent database [31] does not permit the publication of specific dataset values). Note that the axes in **Figs. 3a-f** are normalized to the same base values, however, and thus a direct (qualitative) comparison of the environmental impact profiles of the different materials/components can be made. Clearly, each component class has a different, specific environmental impact profile (e.g., a ferrite core is problematic in terms of DHH and DESQ, whereas an aluminum heatsink suffers from high DRA and GWP emissions). Therefore, a trade-off situation between the different environmental metrics arises during the design of a power electronic converter, which will be further discussed in **Section III**. Further, **Fig. 3f** compares the environmental footprint of different electricity mixes (per 750 kWh), where again different combinations of electric energy generation methods result in different environmental impact profiles.

III. Multi-Objective Optimization Framework

The goal of multi-objective optimizations is to avoid an "apples-vs.-oranges" comparison of specific converter realizations and instead enable a systematic and fair comparison of converter designs and topologies with respect to a set of performance indices [24]–[28]. Further, the results of a multi-objective optimization show design trade-offs between the considered performance dimensions, which enables identifying Pareto-optimal converter designs suitable for the realization of hardware prototypes. Traditionally, the considered performance metrics are efficiency, power density, and sometimes cost. The component models presented in **Section II** enable also considering environmental impact metrics in the multi-objective optimization and thus pushing towards more sustainable converter designs. This is shown in the following using the exemplary bidirectional three-phase ac-dc converter PEBB depicted in **Fig. 2**.

Fig. 4 shows the flowchart of the implemented multi-objective optimization procedure. The considered converter specifications are for a P_N = 10 kW three-phase ac-dc converter PEBB interfacing a 400 V three-phase ac voltage (U_{ac} = 230 V rms line-to-neutral voltage) and a dc-link voltage U_{dc} = 800 V. The two main converter-level DOF are the switching frequency f_s and the maximum high-frequency boost inductor current ripple amplitude ΔI_{Lp} (i.e., 1/2 of the peak-to-peak current ripple; defined relative to the grid current amplitude):

- Increasing the switching frequency enables to shrink the size of the passive components (filter capacitor C, boost inductor L, dc-link capacitor C_{dc}) but comes at the cost of elevated switching losses [55], thus modifying

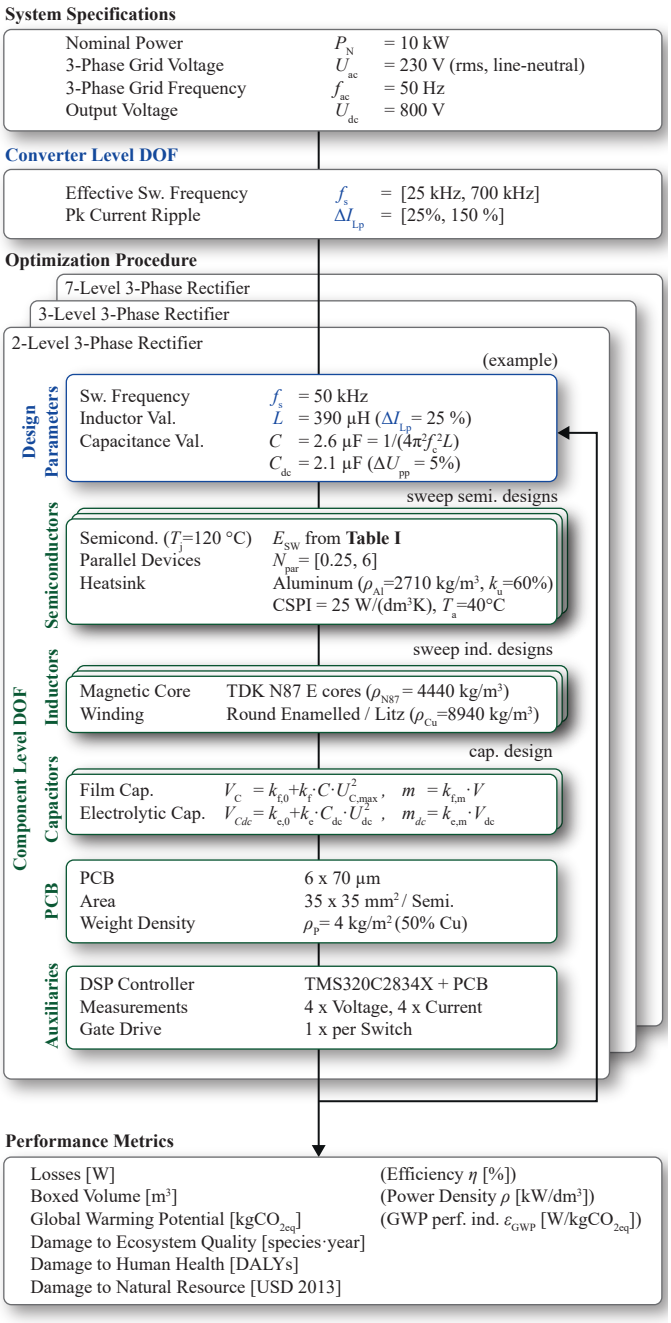

Fig. 4. Flowchart of the multi-objective optimization routine implemented in MATLAB, which considers the relevant converter-level and component-level Degrees of Freedom (DOF) (adapted from [51]).

TABLE: I: CONSIDERED SEMICONDUCTOR DEVICES.

V_{ds}	Mat.	R_{on}	Manuf.	Pt. Number	E_{sw}
1.2 kV	SiC	16 mΩ	Cree	C3M0016120K	Ref. [52]
650 V	SiC	27 mΩ	Infineon	IMZA65R027M1H	Ref. [53]
200 V	Si	9 mΩ	Infineon	IPT111N20NFD	Ref. [54]

the key design trade-off between volume and losses. Here, a wide (effective) switching frequency range of $f_s \in [25\,\text{kHz}, 700\,\text{kHz}]$ is considered to fully explore the design space.

- The boost inductor current ripple ΔI_{Lp} impacts the resulting high-frequency current stresses (conduction losses) and the semiconductor hard-switching turn-on currents. To allow a fair comparison among the converter designs, the cutoff frequency f_c of the second-order input filter formed by the filter capacitor C and the boost inductor L (see **Fig. 2a**) is set to one tenth of the switching frequency f_s such that the switching-frequency emissions are attenuated by -40 dB. Thus, ΔI_{Lp} modifies also the trade-off between the boost inductor L and the filter capacitor C values and volumes.

Note that for a grid-tied rectifier system, an additional Electromagnetic Interference (EMI) filter stage is required to comply with the corresponding emission limits; this is not included here for the sake of brevity but would need to be considered for a more comprehensive analysis.

For a given set of design parameters, i.e., a set of parameters (f_s, L, C, C_{dc}), the electric waveforms are calculated and used to identify suitable component realizations by systematically evaluating the component-level DOF:

- The power transistors (e.g., T_a, T_a' in phase a) need to switch the dc-link voltage $U_{dc} = 800$ V and provide sufficient blocking voltage margin. Cutting-edge 1200 V, 16 mΩ SiC transistors in a TO 247-4 package are considered (see **Tab. I**; for the FC ML topologies discussed in **Section IV-D**, devices with lower voltage ratings can be employed). The conduction losses are calculated considering a design junction temperature of $T_j = 120\,°\text{C}$ (unless otherwise noted) and based on the datasheet on-state resistance, and the hard- and soft-switching energies E_{SW} are calculated based on the calorimetric measurements provided in [52]. The chip area is a powerful DOF to trade off semiconductor switching and conduction losses and thus achieve minimum overall semiconductor losses. Therefore, the number of parallel-connected semiconductors N_p is swept, where also fractional $N_p < 1$ are considered to account for the availability of devices using the same technology but with on-state resistances ≥ 16 mΩ.
- The volume of the required aluminum heatsink is calculated assuming a typical Cooling System Performance (CSPI) [56] of 25 W/(dm^{3}K) (forced-air cooling) and an ambient temperature of $T_a = 40\,°\text{C}$. To assure isolation between the transistor drain pad and the heatsink, a thermal interface material with 5 W/(mK) and 1 mm thickness is employed.
- The boost inductor L is the power component with the largest number of component-level DOF, as different magnetic cores, airgap lengths, and winding types can be combined. These are explored using the design procedure from [29], whereby TDK N87 ferrite cores in various E-core geometries and both, solid round wire and litz wire windings are considered.
- Commercially available film and electrolytic capacitors are considered for the realization of the filter capacitors C and the dc-link capacitor C_{dc}, respectively. Specifically, a fit on a large number of commercially available capacitors is performed (data extracted from Digikey) to obtain a typical relationship between the specified capacitance values and rated voltages and the resulting volume and mass (see **Fig. 4**; the fit parameters are $k_{f,0} = 2.7\,\text{dm}^3$, $k_f = 10.7\,\text{dm}^3/\text{J}$, $k_{e,0} = 9.8\,\text{dm}^3$, $k_e = 0.3\,\text{dm}^3/\text{J}$, and $k_{f,m} = 1191\,\text{kg/m}^3$, $k_{e,m} = 1500\,\text{kg/m}^3$). Typically, the contribution of the capacitor losses in a three-phase ac-dc converter is marginal and thus neglected here.
- The required power PCB area is estimated based on the number of power transistors with an estimated PCB area of $35 \times 35\,\text{mm}^2 (1.4 \times 1.4\,\text{in}^2)$ per device (including the area for the gate-drive circuitry and commutation loop) and at least two devices per half-bridge. The volume and mass is calculated assuming a 6 layer / 70 µm (2 oz/ft^2) PCB and the conduction losses are considered by a lump-sum loss contribution of 5 W, based on experience. Further, a control PCB with a total area of $10\times10\,\text{cm}^2$ ($3.9\times3.9\,\text{in}^2$) is considered to accommodate the DSP and auxiliary circuitry like voltage and current measurements.
- The auxiliary components are split into three groups: First, there is a DSP with a chip mass of 2 g (e.g., TI TMS320C2834X) as well as a set of 60 auxiliary capacitors and 20 resistors in SMD packages. Second, the four required voltage and current measurements (3× grid voltage and currents, 1× dc voltage and current) are modeled assuming a chip weight of 0.3 g for the sensor IC and an associated set of 10 auxiliary capacitors and 10 resistors in SMD packages. Third, the gate-drive circuit required for each power transistor comprises a chip with a mass of 0.1 g and an associated set of 15 auxiliary capacitors and 5 resistors in SMD packages. Note that the contribution of the auxiliary components to the environmental impact is much higher than their small volume might suggest (see [21] and below). The overall auxiliary losses are assumed to be 5 W.

The components for a specific set of design parameters are systematically combined to obtain all feasible converter realizations. The overall performance of each converter realization in terms of conversion losses, volume, and environmental impacts is calculated by summing up the contributions of the individual components (the boxed volume of the converter considers a derating factor of 1.5 to consider the physical arrangement of the components) such that the design trade-offs between

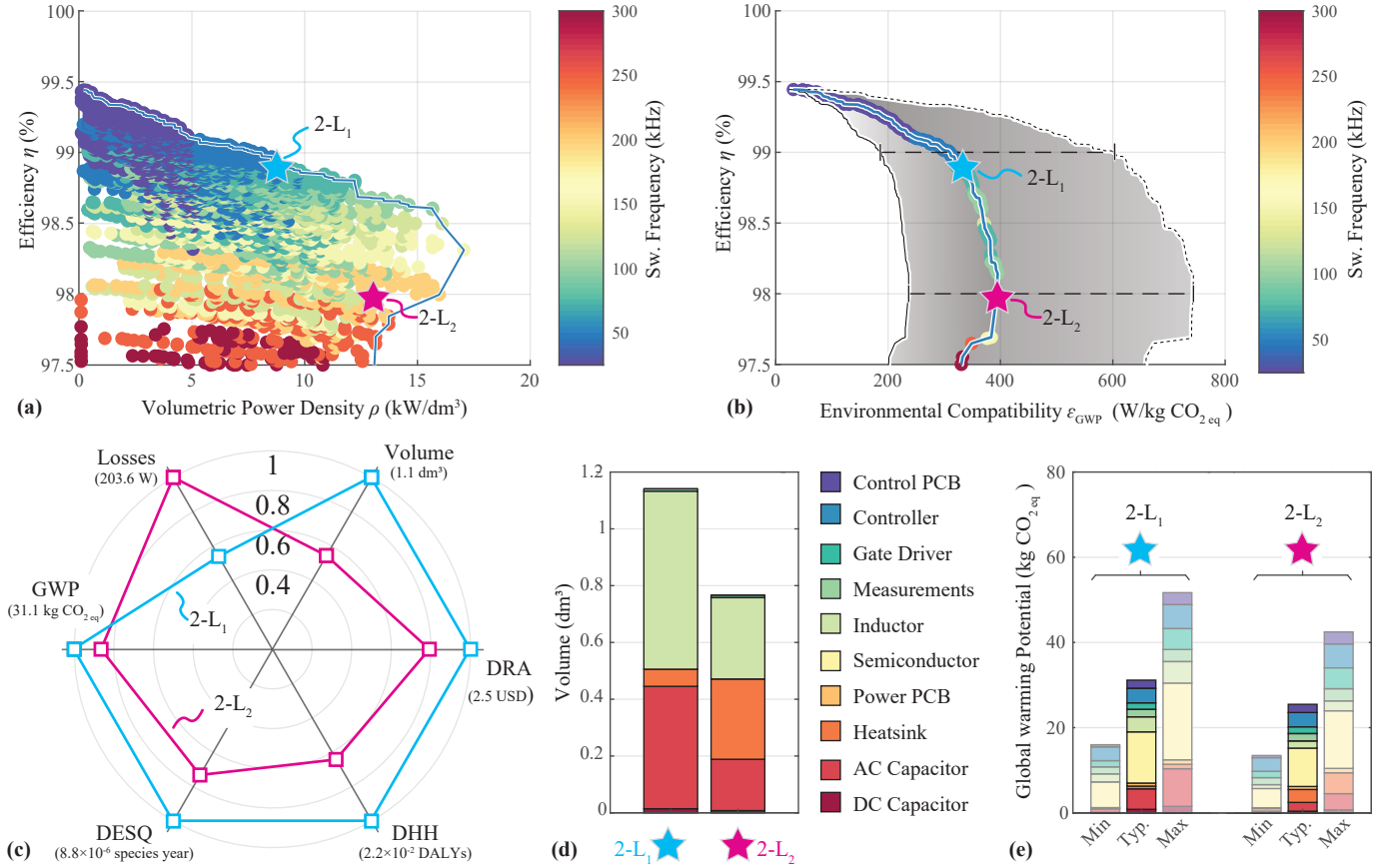

Fig. 5. **(a)** Multi-objective optimization results for the two-level converter PEBB from **Fig. 2a** highlighting the trade-off between conversion efficiency η and power density ρ. The scatter color indicates the switching frequency f_s. **(b)** Multi-objective optimization results comparing the limits in conversion efficiency η and the environmental compatibility index for GWP, $\varepsilon_{GWP} = P_N/GWP$. Here, only the Pareto-optimal designs are shown and the maximum and minimum deviation of ε_{GWP} due to the modeling uncertainties (see **Section II**) is indicated. Two designs with $\eta = 99\%$ and $\eta = 98\%$ are highlighted with a star symbol and **(c)** shows the system-level performance in all six considered dimensions, i.e., losses, boxed volume, Damage to Resource Availability (DRA), Damage to Human Health (DHH), Damage to Eco-System Quality (DESQ), and Global Warming Potential (GWP). Further, **(d)** and **(e)** present the corresponding volume and GWP breakdowns, respectively.

the performance metrics can be visualized and Pareto-optimal designs can be identified.

IV. Multi-Objective Optimization Results

The multi-objective optimization framework presented in **Section III** is a generic optimization tool which is employed in a first step to investigate the performance limits and design trade-offs of the 10 kW two-level three-phase ac-dc converter PEBB shown in **Fig. 2**. Subsequently, different DOF, i.e., the semiconductor junction temperature, advanced modulation strategies, and advanced ML converter topologies, and their impact on the performance metrics are examined. Last, also the impact of the converter's use phase, where the power conversion losses covered by electricity from the power grid cause emissions, on the overall life-cycle environmental footprint is assessed.

A. Performance Limits of a 2-L PEBB

Fig. 5 presents the results of the multi-objective optimization of the 10 kW two-level three-phase ac-dc converter PEBB. Specifically, **Fig. 5a** shows the limits in conversion efficiency η and (volumetric) power density ρ (i.e., the $\eta\rho$-Pareto front) with the scatter color indicating the switching frequency f_s of each design. Increasing the switching frequency f_s enables more compact designs at the cost of higher conversion losses (lower η), where beyond $f_s = 150$ kHz no further volume reduction can be achieved as the improvements concerning the volume of the passive filter components are overcompensated by the increasing (due to switching losses) cooling system volume.

Similarly, **Fig. 5b** shows the trade-off between conversion efficiency η and the environmental compatibility indicator for GWP, ε_{GWP}, i.e., the nominal power divided by the embodied GWP of the design.[3] Here, only the Pareto-optimal (in terms of η and ε_{GWP}) designs are shown. Furthermore, the maximum and minimum deviation of ε_{GWP} due to the modeling/data uncertainties mentioned in **Section II** is highlighted with a

[3]The environmental compatibility indicator ε_{GWP} is defined such that larger values imply better performance, as is the case for the efficiency η, power density ρ, etc. Note that equivalent environmental compatibility indicators could be defined and corresponding Pareto fronts be plotted for the other environmental impact categories (DHH, DRA, and DESQ); here, we focus the discussion on ε_{GWP} for the sake of conciseness.

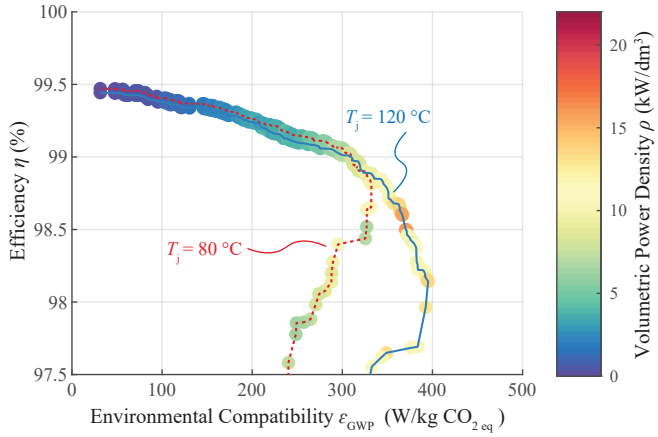

Fig. 6. Impact of the selected semiconductor junction temperature T_j on the limits in conversion efficiency η and environmental compatibility indicator ε_{GWP} of the two-level PEBB (**Fig. 2a**). The scatter color indicates the power density ρ of each design.

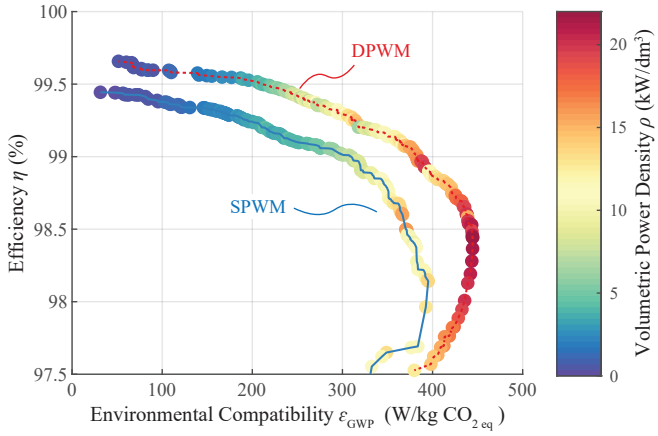

Fig. 7. Impact of the considered modulation strategies, i.e., Sinusoidal Pulse-Width Modulation (SPWM) and Discontinuous Pulse-Width Modulation (DPWM), on the limits in conversion efficiency η and environmental compatibility indicator ε_{GWP} of the two-level PEBB (**Fig. 2b**). The scatter color indicates the power density ρ of each design.

shaded area which varies for some designs by approximately ±100% with respect to the "typical" values.

Two designs on the $\eta\varepsilon_{GWP}$-Pareto front with η = 99% (2-L_1) and η = 98% (2-L_2) are selected[4] for further investigation and **Fig. 5c** indicates all considered performance dimensions. Whereas the more efficient design 2-L_1 features only approximately half the losses of design 2-L_2, it employs substantially larger components with adverse impact on the environmental performance indicators. **Fig. 5d** further provides the detailed volume breakdown of the two systems, where the design 2-L_2 achieves a substantially lower passive component volume at the cost of a larger heatsink, which still results in an overall volume reduction compared to design 2-L_1.

The components' contributions to the converters' GWP emission distribution is presented in **Fig. 5e**, where two characteristics should be noted: First, note the large spread resulting from employing the min., typ. and max. GWP data[5] in the component models (see also **Fig. 5b**): if considering the best-case scenarios (min. emissions), the more efficient design 2-L_1 may reach very similar GWP values as the less efficient design 2-L_2. Hence, data availability/quality represents a major challenge for such analyses, and future component datasheets should disclose information on embodied $CO_{2,eq}$ emissions and ideally provide a complete environmental footprint. Second, the typ. results with approximately 25 kg$CO_{2,eq}$ for a 10 kW system indicate room for substantial reductions of the GWP compared to the state of the art [6], [21], even given that here only the core PEBB is considered and further components such as an EMI filter and a housing will be required for a commercial product.

[4]Specifically, within a tolerance band of ±0.1% around the specified value of η and the maximally achievable value of ε_{GWP}, the most compact design is selected.

[5]Typically, various data sources per component are available regarding the GWP footprint. As these, however, differ significantly, we characterize the corresponding range by min., max. and typical (typ.) values.

B. Impact of the Junction Temperature

For the optimization results shown in **Fig. 5**, the cooling system was designed such that a semiconductor junction temperature of T_j = 120 °C results for nominal power operation. The choice of T_j, however, impacts the system performance, and thus, **Fig. 7** investigates the limits in conversion efficiency η and environmental compatibility indicator ε_{GWP} of the PEBB for T_j = 120 °C and T_j = 80 °C: As the power transistors' on-state resistance decreases with a decreasing T_j, lower conduction losses and thus slightly higher efficiencies result for T_j = 80 °C. However, at the same time a larger heatsink volume is required, such that with T_j = 80 °C the system is constrained to lower values of the environmental compatibility indicator ε_{GWP}.

Note that the ε_{GWP} of low-junction-temperature designs improves once also the use-phase-related emissions are considered (see **Section IV-E**), which scale with the conversion losses. Further, the higher lifetime of power transistors operating with lower junction temperature [8], [57] may extend the converter system's useful life and offset the initially higher environmental impact due the larger cooling system.

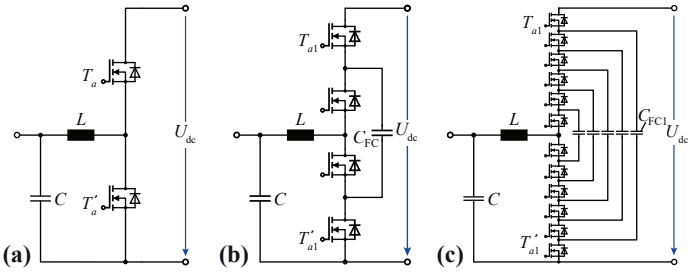

Fig. 8. Considered three-phase ac-dc converter PEBB bridge-leg structures: **(a)** standard two-level, as well as FC ML [58], [59] bridge-leg realizations with **(b)** three levels and **(c)** seven levels; For the design of both FC ML converters a relative FC voltage ripple of ΔU_{pp} = 2.5% is considered.

C. Impact of the Modulation Strategy

So far, the standard Sinusoidal Pulse-Width Modulation (SPWM) was considered, where all three converter phases are continuously switched at high frequency. Alternatively, e.g., the advanced Flat Top (FT) Discontinuous Pulse-Width Modulation (DPWM) [60] enables substantial efficiency gains by injecting a low-frequency common-mode voltage component in the three-phase switch node voltage references such that the phase with the instantaneously highest absolute grid current value (i.e., the phase with the highest turn-on currents) ceases switching at high frequency and is clamped to either the positive or the negative dc-link rail within a sixty-degree interval of the grid period. Thus, only two out of three converter phases are switched at high frequency at any given point in time and thereby the semiconductor switching losses are reduced by at least 33%.

Thus, **Fig. 7** investigates the impact of the considered modulation strategy on the limits in conversion efficiency η and the environmental compatibility indicator $\varepsilon_{\mathrm{GWP}}$ of the two-level PEBB. In contrast to a lower semiconductor junction temperature, DPWM reduces semiconductor losses *and*, in consequence, also the required heatsink volume, such that simultaneously better performance in both, η *and* $\varepsilon_{\mathrm{GWP}}$ can be achieved. Hence, the converter modulation strategy represents a powerful tool to enable more environmentally friendly converter realizations, especially considering that the higher η also reduces use-phase emissions.

D. Multi-Level Converter Topologies

Flying Capacitor (FC) Multilevel (ML) converters enable elevated effective switching frequencies and higher bridge-leg output voltage level counts, thus facilitating more compact and more efficient converter realizations compared to two-level converters [58], [59]. Here, the limits in conversion efficiency η and GWP performance index $\varepsilon_{\mathrm{GWP}}$ of a standard three-phase ac-dc converter PEBB with two-level bridge-legs is compared with PEBB realizations that employ three-level (**Fig. 8b**) or seven-

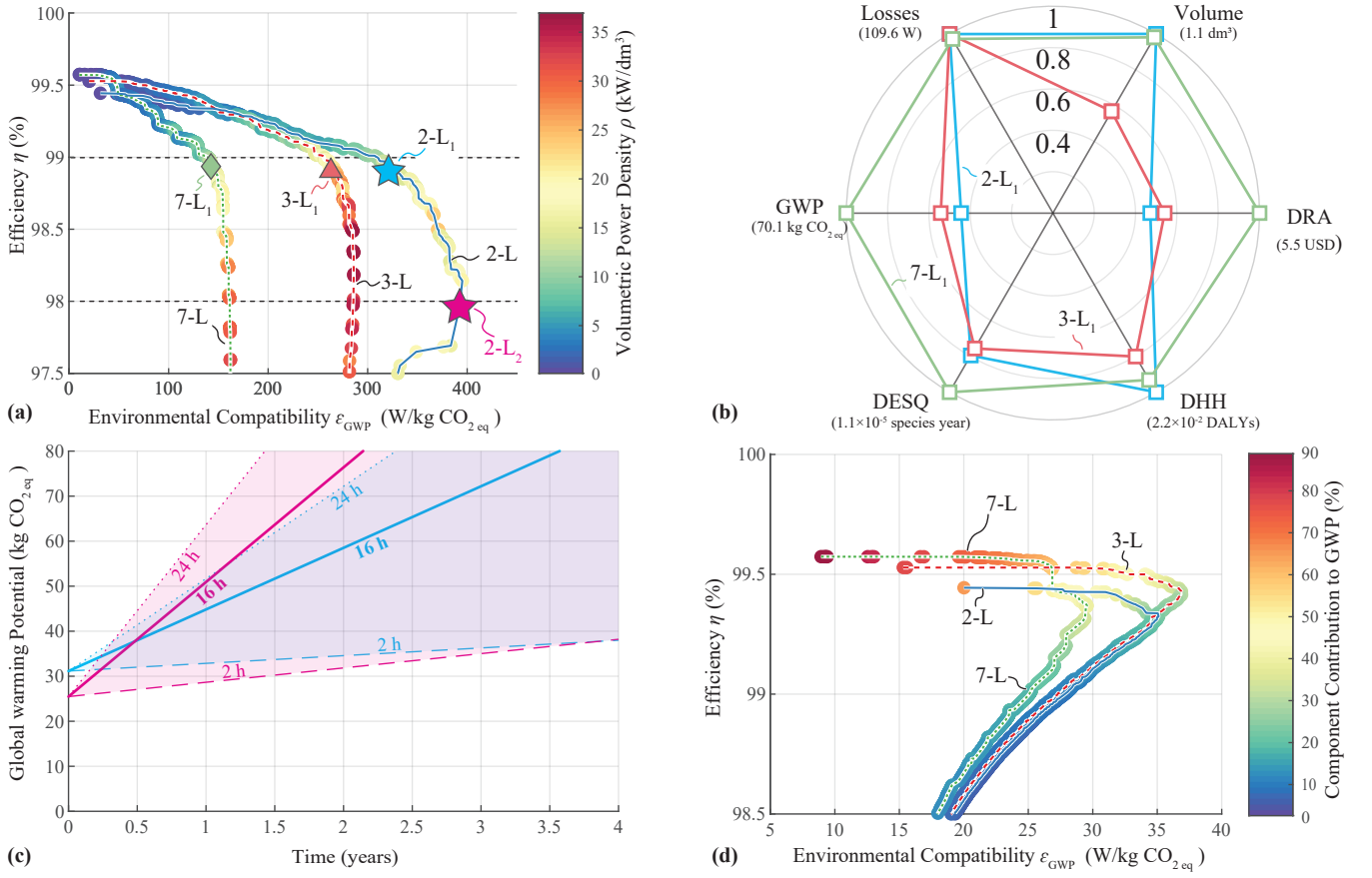

Fig. 9. (a) Multi-objective optimization results comparing the limits in conversion efficiency η and environmental compatibility indicator $\varepsilon_{\mathrm{GWP}}$ of different bridge-leg realizations used in the three-phase ac-dc converter PEBB. The scatter color indicates the power density ρ of each design. The considered bridge-leg topologies are the standard two-level (2-L) half-bride, and the three-level (3-L) and seven-level (7-L) FC ML bridge-legs (see **Fig. 8**). For each topology, a design with $\eta = 99\%$ is highlighted and **(b)** shows their system-level performance in all six considered dimensions, i.e., losses, boxed volume, Damage to Resource Availability (DRA), Damage to Human Health (DHH), Damage to Eco-System Quality (DESQ), and Global Warming Potential (GWP). **(c)** Impact of the use phase on the overall GWP footprint of the two two-level designs with $\eta = 99\%$ and $\eta = 98\%$ operating with the Swiss electricity mix (112 $\mathrm{gCO_{2,eq}}$/kWh [46]) for different mission profiles (nominal power operation during 2 h, 16 h and 24 h per day). **(d)** Limits in conversion efficiency η and environmental compatibility indicator $\varepsilon_{\mathrm{GWP}}$ of three-phase ac-dc converter PEBB employing different bridge-leg realizations (the scatter color indicates the power density ρ), including the use-phase contributions assuming nominal power operation in the Swiss electricity grid for 8 h per day during ten years.

level (**Fig. 8c**) FC ML bridge-leg realizations. Note that power semiconductors with 600 V and 200 V are sufficient for the three-level and the seven-level FC ML bridge-legs, respectively, and the considered semiconductors are listed in **Tab. I**. In particular, the seven-level FC ML bridge-legs are realized with Si instead of SiC transistors.

Fig. 9a presents the optimization results, where both, the seven-level and the three-level FC ML converter achieve higher peak efficiencies than the two-level converter. In terms of the maximum achievable values of the environmental compatibility indicator $\varepsilon_{\mathrm{GWP}}$, the FC ML converters remain, however, limited compared to the two-level converter, as the larger number of components diminishes the gains obtained by the filter volume minimization that results from the higher effective switching frequency and the multilevel voltage waveforms. **Fig. 9b** further compares three converter designs with approximately $\eta = 99\%$ and the respectively best environmental compatibility indicator $\varepsilon_{\mathrm{GWP}}$ in all six performance dimensions. Interestingly, the environmental footprints of the three designs are quite different: As discussed in **Section II**, each type of component has a different environmental footprint (i.e., some components are particularly disadvantageous in terms of DHH, whereas others might be problematic regarding GWP). Converters employing the considered bridge-leg configurations from **Fig. 8** achieve the selected efficiency level of $\eta = 99\%$ by employing different numbers of active and passive components (and also different component values and realizations). Hence the different environmental profiles of the components are weighted differently in the converters' environmental footprints, which explains the different shapes of the resulting radar plots.

E. Impact of the Use Phase

Finally, once built, a converter will be used in a certain application with a specific mission profile for a certain number of years, typically until its end of life or until it reaches obsolescence. With $\eta < 100\%$, a converter inevitably wastes electric energy during the use phase. As each wasted kWh of electricity comes with its region-specific environmental footprint (see **Section II**), the conversion losses during the use phase contribute to the life-cycle environmental footprint of a converter PEBB. Note that also the converter weight or volume may impact the use-phase emissions in case of airborne or land-based mobile applications.

Fig. 9c presents the GWP footprint of the two two-level designs highlighted in **Fig. 9a** with $\eta = 99\%$ (2-L_1) and $\eta = 98\%$ (2-L_2) over time. Operation in the Swiss electricity grid (112 $gCO_{2,eq}$/kWh [46]) and three (simplified) mission profiles, i.e., nominal-load operation during either 2 h, 16 h or 24 h per day, are considered. Note that depending on the mission profile, i.e., the intensity of use during the use phase, the more efficient design 2-L_1 with an initially higher GWP offset can outperform a less efficient design 2-L_2 within less than half a year. Therefore, it is of great importance to also include the converter use phase in the multi-objective optimization.

Thus, **Fig. 9d** compares again the limits in conversion efficiency η and the environmental performance indicator $\varepsilon_{\mathrm{GWP}}$ for PEBBs with the three bridge-leg structures from **Fig. 8**, but now includes the use-phase contributions to the overall GWP considering again the Swiss electricity mix and a mission profile with nominal-power operation for 8 h per day during ten years. Now, the three-level FC ML bridge-leg-based designs can outperform the two-level designs regarding $\varepsilon_{\mathrm{GWP}}$, because essentially they can achieve better efficiency with a smaller GWP offset. In contrast, the even higher efficiency values η of certain seven-level converter designs cannot compensate their larger GWP offsets for the considered use-case scenario.

All in all, it is important to highlight that the selection of a converter design with minimum environmental impact depends heavily on the duration and intensity (i.e., the mission profile) of the use phase, as well as on the geographic location which determines the environmental profile of the electricity mix. Note, however, that the ongoing transition towards more sustainable electric energy generation will increase the relative importance of the environmental footprint of the converter and its components themselves (before taking into account the use phase).

V. Conclusion

Achieving the net-zero greenhouse gas emission target by 2050 requires a rather complete transition towards renewable energy and large-scale electrification of transportation and industry, which implies a massive expansion of the installed power electronic conversion capacity. All these power converters ultimately end up as electronic waste at the end of their useful life unless they are designed for compatibility with a circular economy. As a first step towards design-for-circularity, the environmental impact of a power converter (e.g., the greenhouse gas emissions and the damage to ecosystems, human health or resource availability its production and use causes) should thus be assessed in the early concept-evaluation and design phase.

Therefore, this paper includes environmental compatibility indicators as new performance dimensions (in addition to efficiency and power density typically considered today) in a multi-objective optimization framework. Using a 10 kW three-phase ac-dc PEBB with an LC filter as an example, design trade-offs are illustrated, e.g., between employing SiC-based two-level, FC ML three-level and seven-level (Si-based) bridge-legs. In particular, the application-specific mission profile and the geographic location (which determines the environmental footprint of the electricity mix used to cover the conversion losses) of the use phase are found to have a significant impact on the selection of the converter design with the lowest environmental impact over its life cycle.

Whereas the proposed method is quite universal, the accuracy and comparability of results obtained by different actors hinges on the availability of high-quality data for the environmental footprints of power electronic components. Given today's scarcity of such data, the results presented herein should be considered exemplary and not absolute in nature. There is thus an urgent need for component manufacturers to provide high-quality environmental footprint data for their products

and for standardization of how such data must be obtained and reported, for example in future smart datasheets and/or digital component passports.

Finally, future work should address how design for reusability, repairability, and recyclability influences design decisions; similarly, life-cycle costs should be considered, also in view of upcoming monetary incentives (like CO_2 emission taxes) for minimizing environmental impacts of products and systems.

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