Novel Bidirectional Single-Stage Isolated Three-Phase Buck-Boost PFC Rectifier System

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***Abstract*—Future three-phase ac-dc converter systems ideally allow for bidirectional power flow, provide high-frequency isolation, and feature buck-boost capability. Further, high efficiency and high compactness and the applicability of standard half-bridge and/or three-phase full-bridge (B6) semiconductor arrangements are crucial aspects. This Paper proposes a novel converter concept that employs B6-type circuits on the input and on the output side and a low-complexity Discontinuous Conduction Mode (DCM)-type or a Dual Active Bridge (DAB)-type modulation strategy, thereby enabling single-stage isolated three-phase ac-dc power conversion with sinusoidal grid currents and controlled dc output voltage. The converter operation is detailed on the switching-frequency and on the grid-frequency time scale and verified by means of circuit simulations. The converter control characteristic and the main power component stresses are discussed and design guidelines for a 6.6 kW prototype system with an expected efficiency $\eta > 98\%$ are presented. Finally, an outlook on future research related to the practical realization and advanced modulation of the topology is provided.**

***Index Terms*—ac-dc converter, bidirectional operation, high-frequency isolation, single-stage power conversion.**

I. Introduction

Power-electronic energy conversion between a three-phase ac and a dc voltage system is mandatory in applications such as server supplies, solar inverters, or Electric Vehicle (EV) battery chargers. There, three-phase Power Factor Correction (PFC) rectifiers enable sinusoidal grid currents with low distortion and controlled dc output. Applications with wide dc voltage ranges (e.g., varying battery or solar panel dc voltages) may have overlapping input/output voltage ranges (dc voltage relative to the peak grid line-to-line voltage), such that a converter system with buck-boost capability is required. Traditionally, this is realized with a PFC rectifier front-end and an additional dc-dc converter stage which, however, leads to a two-stage energy conversion. Hence, phase-modular converters with inherent buck-boost capability and (quasi)-single-stage High-Frequency (HF) power conversion gained significant interest in literature [1] and **Fig. 1a** depicts the main power circuit of a modular non-isolated buck-boost Y-rectifier [2], [3]. Often, however, galvanic isolation is a strict requirement, e.g., for safety reasons or voltage level adaption, which is traditionally realized with dedicated HF isolated dc-dc converters (typically a Series-Resonant Converter (SRC) operated as dc transformer [4] or a Dual Active Bridge (DAB) converter [5]). This allows for a compact realization [6]–[8] but results again in a two-stage power conversion.

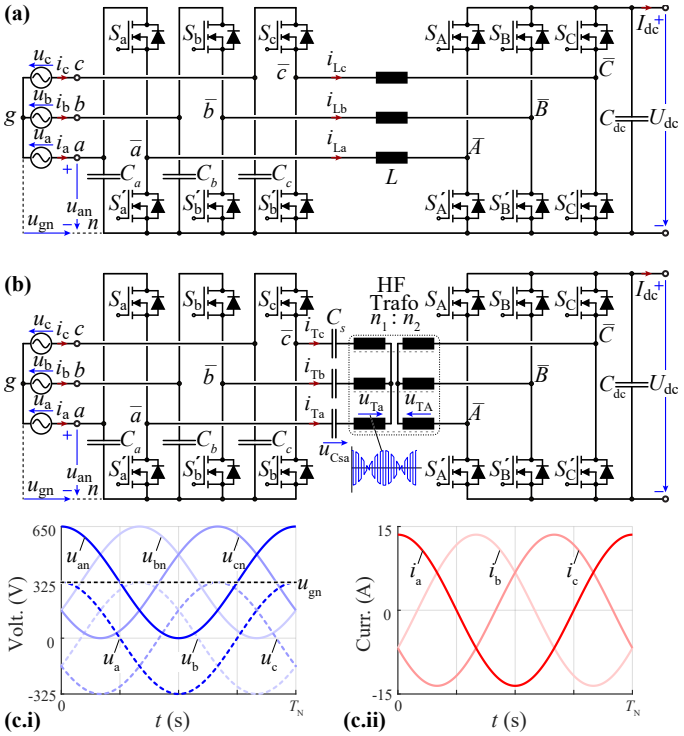

Fig. 1. Main power circuits of **(a)** the Y-rectifier employing three star-connected (Y) converter modules [2], [3] and **(b)** the proposed three-phase Y-type ac-dc converter with integrated HF isolation, interfacing the European low-voltage grid ($U_\mathrm{N} = 230\,\mathrm{V_{rms}}$) and a dc source (e.g., a solar panel) or load (e.g., an EV battery or a general load / subsequent converter stage). The ac input voltages with respect to the grid neutral terminal g ($u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$) and with respect to the converter input-stage starpoint n ($u_\mathrm{an}, u_\mathrm{bn}, u_\mathrm{cn}$ comprising an offset voltage u_gn) are shown in **(c.i)** and the grid currents ($i_\mathrm{a}, i_\mathrm{b}, i_\mathrm{c}$) are depicted in **(c.ii)** for a system with $P_\mathrm{N} = 6.6\,\mathrm{kW}$ rated power (i.e., $I_\mathrm{N} = 10\,\mathrm{A_{rms}}$).

Table I: System Specifications.

Designator	Description	Value
U_N	Grid voltage (line-to-neutral)	$3 \times 230\,\mathrm{V_{rms}}$
I_N	Grid phase current	$3 \times 9.6\,\mathrm{A_{rms}}$
f_N	Grid frequency	50 Hz
P_N	Nominal system power	6.6 kW
U_dc	dc output voltage	400 V
f_s	Switching frequency	72 kHz
n_1:n_2	Transformer turns ratio	1:1

Ideally, in future power converter systems the HF potential separation should be integrated into the PFC ac-dc converter stage to realize single-stage power conversion. Such converter concepts are known in literature [9]–[16] but suffer from several shortcomings: Matrix type approaches with DAB-type isolation enable the use of a single main magnetic component [9]–[11] but require semiconductors with bidirectional blocking capability and complex modulation strategies. Modular or semi-modular isolated converter structures also exist [12], [13], but suffer from a relatively large realization effort. A further approach is described in [14], [15] and advantageously utilizes a low number of primary-side switches and features a straightforward input power regulation by means of Space Vector Modulation (SVM) of the secondary-side three-phase full-bridge (B6) stage, but shows a relatively low transformer utilization and high transient primary-side semiconductor switching voltage stresses.

Given the shortcomings of existing converter structures, this paper proposes a new three-phase ac-dc converter with integrated HF isolation (see **Fig. 1b**) based on the phase-modular buck-boost Y-rectifier [2], [3] (see **Fig. 1a**): The reference potentials of the Y-rectifier input- and output-stage are separated, the buck-boost inductors L are replaced by an HF transformer and series Low-Frequency (LF) voltage blocking capacitors C_s are added. Advantageously, and similar to [16], the B6-type realizations of the Y-rectifier input stage and of the output stage, both employing unidirectional semiconductors with a clearly defined commutation loop and direct switch voltage limitation [17], is maintained. The primary-side converter stage is operated such that amplitude modulated (with the grid frequency) HF transformer voltages result in each module (see **Fig. 1b**). The power transfer adjustment and the shaping of the grid-side input currents can be realized with either Discontinuous Conduction Mode (DCM)-type [18]–[20] or DAB-type [14], [15] modulation of the secondary-side converter stage.

This paper describes the main aspects of the proposed converter system, and **Section II** presents the primary-side converter stage LF and HF voltage formation. **Section III** then discusses the two considered secondary-side converter stage modulation strategies and is accompanied by simulation results. Then, **Section IV** provides a guideline for the selection of the main converter component values and compares the secondary-side converter stage modulation strategies with respect to the component stresses. Finally, **Section V** summarizes the main findings and provides an outlook on future research topics.

II. Primary-Side Converter Stage Modulation

The goal of the modulation of the proposed topology's primary-side converter stage (see **Fig. 1b**) is to translate the LF grid input voltages $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$ into HF transformer voltages, thereby enabling the utilization of a compact HF transformer. The desired PFC operation with sinusoidal grid currents is then realized by the secondary-side converter stage, which is discussed in **Section III**.

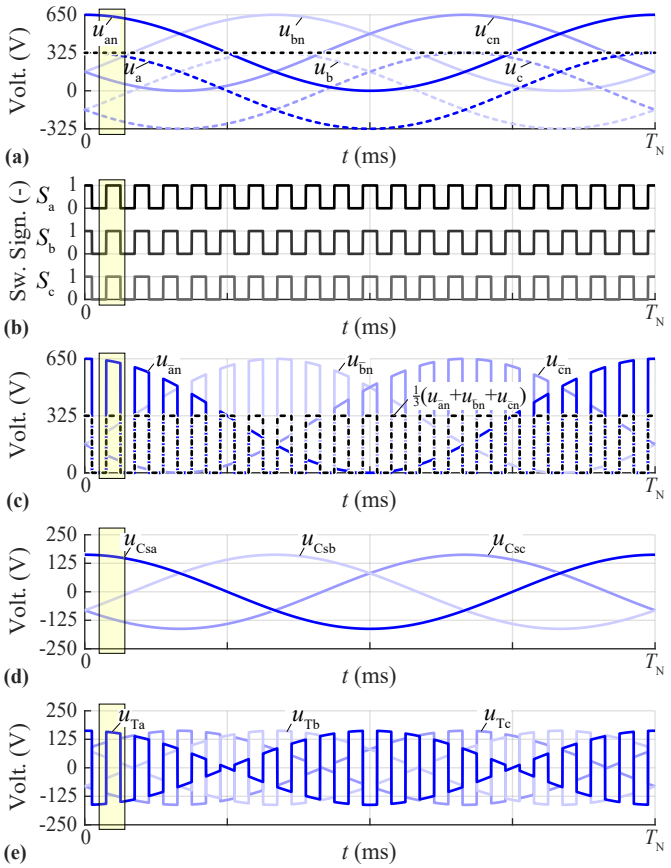

Fig. 2. Illustration of the primary-side HF transformer voltage formation of the proposed isolated PFC rectifier depicted in **Fig. 1b**: **(a)** ac input voltages $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$ with respect to the grid neutral terminal g and input capacitor voltages $u_\mathrm{an}, u_\mathrm{bn}, u_\mathrm{cn}$ comprising an offset voltage u_gn. **(b)** Control signals of the primary-side high-side semiconductors S_a,S_b,S_c which are turned on and off simultaneously; the low-side semiconductors S'_a,S'_b,S'_c (not shown) are switched complementarily. **(c)** Resulting primary-side switch-node $\bar{a}, \bar{b}, \bar{c}$ voltages $u_{\bar{a}\mathrm{n}}, u_{\bar{b}\mathrm{n}}, u_{\bar{c}\mathrm{n}}$ with respect to the input-stage starpoint n, the Common-Mode (CM) component $1/3 \cdot (u_{\bar{a}\mathrm{n}} + u_{\bar{b}\mathrm{n}} + u_{\bar{c}\mathrm{n}})$ is indicated with a dashed line. **(d)** LF Differential-Mode (DM) switch-node voltage components $u_\mathrm{Csa}, u_\mathrm{Csb}, u_\mathrm{Csc}$ applied to the LF-blocking series capacitors C_s. **(e)** HF DM components applied to the transformer primary-side terminals $u_\mathrm{Ta}, u_\mathrm{Tb}, u_\mathrm{Tc}$. Note that a low pulse number (i.e., ratio of switching f_s and grid frequency f_N) is selected here for illustration purposes. Further, a switching period at a grid angle $\alpha_\mathrm{N} = 2\pi f_\mathrm{N} t = 20°$ is highlighted and will be discussed in more detail in **Fig. 3**.

The input terminals a, b, c of the considered converter depicted in **Fig. 1b** are subject to sinusoidal DM voltages u_a,u_b,u_c (with amplitude $\hat{U}_\mathrm{N}$ and frequency $f_\mathrm{N} = 1/T_\mathrm{N}$) which are impressed by the grid. Similar to a Y-rectifier (see **Fig. 1a**), the grid star point g is not connected to the input-stage starpoint n and an offset voltage u_gn is established [2], [3] such that the input capacitor voltages $u_\mathrm{an}, u_\mathrm{bn}, u_\mathrm{cn}$ are strictly positive (i.e., comprise a CM offset voltage $u_\mathrm{gn} = \frac{1}{3}\sum u_\mathrm{an,bn,cn}$) and hence, advantageously, standard semiconductors with unidirectional voltage-blocking capability can be employed. In the most simple case, the offset voltage is constant and equal to the grid line-to-neutral voltage amplitude $\hat{U}_\mathrm{N} = 325\,\mathrm{V}$ as presented in **Fig. 2a**.

As mentioned, the goal of the primary-side converter stage modulation is to translate the LF grid input voltages into HF

transformer voltages. This can be realized by synchronously operating the primary-side converter stage semiconductors as highlighted in **Fig. 2b**, where S_a,S_b,S_c are turned on simultaneously with a constant Pulse Width Modulation (PWM) duty cycle $d_\mathrm{ac} = 0.5$ and S'_a,S'_b,S'_c are controlled complementarily.

The resulting primary-side switch-node $\bar{a},\bar{b},\bar{c}$ voltages $u_{\bar{a}\mathrm{n}}, u_{\bar{b}\mathrm{n}}, u_{\bar{c}\mathrm{n}}$ with respect to the input-stage starpoint n are shown in **Fig. 2c**. It is important to highlight that the selected primary-side synchronous (i.e., CM) switching pattern translates the input capacitor CM offset voltage u_gn in **Fig. 2a** into a CM switch-node voltage $1/3 \cdot (u_{\bar{a}\mathrm{n}} + u_{\bar{b}\mathrm{n}} + u_{\bar{c}\mathrm{n}})$ which does not create any currents in the open-starpoint transformer primary-side windings.

Further, the primary-side switch-node $\bar{a},\bar{b},\bar{c}$ voltages $u_{\bar{a}\mathrm{n}}, u_{\bar{b}\mathrm{n}}, u_{\bar{c}\mathrm{n}}$ comprise two DM components which result from the convolution (in the frequency domain) of the synchronous HF switching signals of S'_a,S'_b,S'_c with the LF DM component of the input capacitor voltages $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$. Assuming that the impedance of the transformer leakage inductance Z_Ls is small compared to the series capacitor impedance Z_Cs at LF, i.e., $Z_\mathrm{Ls}(f_\mathrm{N}) \ll Z_\mathrm{Cs}(f_\mathrm{N})$, and vice versa at HF, i.e., $Z_\mathrm{Ls}(f_\mathrm{s}) \gg Z_\mathrm{Cs}(f_\mathrm{s})$, the following voltage sharing results (the sizing of C_s and L_s is discussed in **Section IV**):

- The LF voltage components of the primary-side switch-node $\bar{a},\bar{b},\bar{c}$ voltages $u_{\bar{a}\mathrm{n}}, u_{\bar{b}\mathrm{n}}, u_{\bar{c}\mathrm{n}}$ are blocked by the series capacitors C_s showing voltages $u_\mathrm{Csa}, u_\mathrm{Csb}, u_\mathrm{Csc}$ (with, e.g., $u_\mathrm{Csa} = d_\mathrm{ac} \cdot u_\mathrm{a} = \frac{1}{2} u_\mathrm{a}$), see **Fig. 2d**. Note that saturation of the HF transformer's magnetic core would result in the absence of the LF blocking capacitors.
- The HF DM voltage components $u_\mathrm{Ta}, u_\mathrm{Tb}, u_\mathrm{Tc}$ of the primary-side switch-node $\bar{a},\bar{b},\bar{c}$ voltages $u_{\bar{a}\mathrm{n}}, u_{\bar{b}\mathrm{n}}, u_{\bar{c}\mathrm{n}}$ are applied to the primary-side transformer terminals. The transformer primary-side terminal voltages $u_\mathrm{Ta}, u_\mathrm{Tb}, u_\mathrm{Tc}$ are amplitude modulated by the respective grid voltages u_a,u_b,u_c as can be seen in **Fig. 2e**.

The primary-side transformer voltages $u_\mathrm{Ta}, u_\mathrm{Tb}, u_\mathrm{Tc}$ within two switching periods $T_\mathrm{s} = 1/f_\mathrm{s}$ are highlighted in **Fig. 3a**. The switching frequency is significantly higher than the mains frequency f_N, i.e., $f_\mathrm{s} = 1/T_\mathrm{s} \gg f_\mathrm{N}$, such that the grid voltages are approximately constant within one switching period $T_\mathrm{s} = 1/f_\mathrm{s}$. Accordingly, e.g., for phase a the transformer voltage alternates with HF between two values $u_\mathrm{Ta} = \pm\frac{1}{2} \cdot u_\mathrm{a}(t)$ with equal duration ($d_\mathrm{ac} = 50\,\%$) of both states (1) and (2).

The Space Vector (SV) representation of the three transformer primary-side voltages $u_\mathrm{Ta}, u_\mathrm{Tb}, u_\mathrm{Tc}$ is depicted in **Fig. 3b**: The voltage SV $\underline{u}_\mathrm{Tabc}$ equals the grid voltage SV $\underline{u}_\mathrm{abc}$ scaled by $50\,\%$ during the first switching half-period (1), i.e., it rotates with the grid angle $\alpha_\mathrm{N} = 2\pi f_\mathrm{N} t$; however, its polarity reverses (i.e., the phase jumps by $180°$) during the second switching half-period (2).

III. Secondary-Side Converter Stage Modulation

The secondary-side converter stage switch nodes $\bar{A},\bar{B},\bar{C}$ (see **Fig. 1b**) are directly connected to the transformer

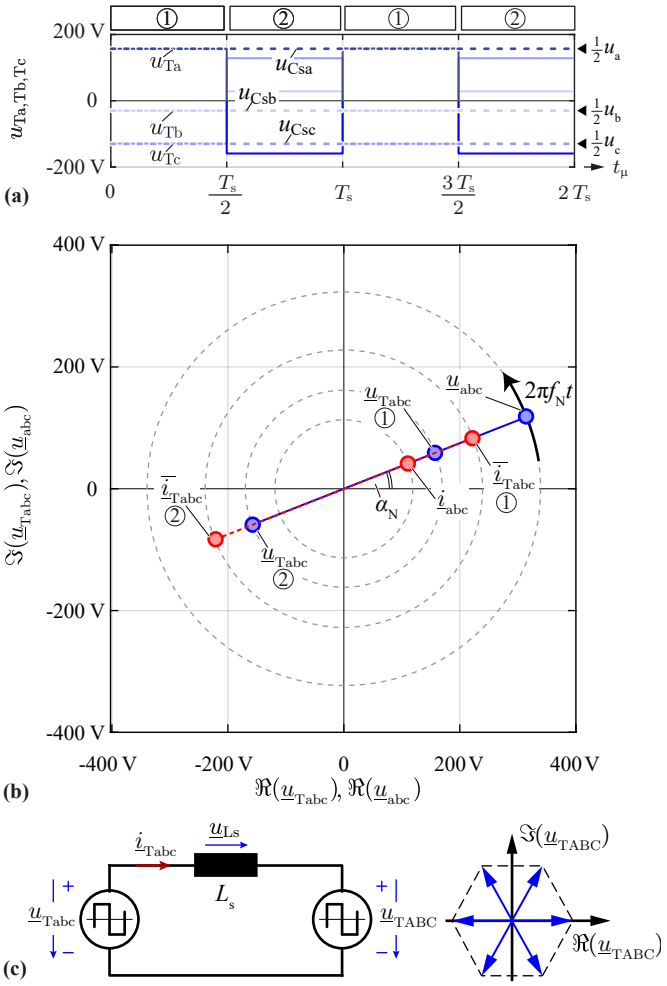

Fig. 3. **(a)** Primary-side transformer voltage waveforms $u_\mathrm{Ta}, u_\mathrm{Tb}, u_\mathrm{Tc}$ of the proposed three-phase Y-type ac-dc converter with integrated HF isolation presented in **Fig. 1b** for the operating point highlighted in **Fig. 2** (i.e., for a grid angle $\alpha_\mathrm{N} = 2\pi f_\mathrm{N} t = 20°$). **(b)** Space Vector (SV) $\underline{u}_\mathrm{Tabc}$ representation of the transformer voltage waveforms presented in (a). **(c)** HF DM Space Vector (SV) equivalent circuit of the converter depicted in **Fig. 1b** and illustration of the six active voltage SVs $\underline{u}_\mathrm{TABC}$ that the secondary-side converter stage can apply to the HF transformer's secondary-side terminals.

secondary-side terminals and the goal of the secondary-side converter stage operation is thus to apply secondary-side transformer voltages $u_\mathrm{TA}, u_\mathrm{TB}, u_\mathrm{TC}$ which result in HF transformer currents $i_\mathrm{Ta}, i_\mathrm{Tb}, i_\mathrm{Tc}$ corresponding to (ideally, and after filtering) sinusoidal grid currents $i_\mathrm{a}, i_\mathrm{b}, i_\mathrm{c}$ (with an amplitude $\hat{I}_\mathrm{N}$ according to the specified power flow P) that are in phase with the respective grid voltages $u_\mathrm{a}, u_\mathrm{b}, u_\mathrm{c}$.

The HF DM SV equivalent circuit of the converter is presented in **Fig. 3c**, and the difference of the primary-side voltage SV $\underline{u}_\mathrm{Tabc}$ and the secondary-side voltage SV $\underline{u}_\mathrm{TABC}$ is applied across the transformer leakage inductance L_s, which results in a transformer *current* SV $\underline{i}_\mathrm{Tabc}$. Hence, sinusoidal grid currents can be realized if the local average (across one half switching period $T_\mathrm{s}/2$) transformer current SV $\bar{\underline{i}}_\mathrm{Tabc}$ is in phase with the primary-side transformer voltage SV $\underline{u}_\mathrm{Tabc}$ within each half-switching period (1) and (2) as highlighted in **Fig. 3b**.

Two possible secondary-side converter stage modulation

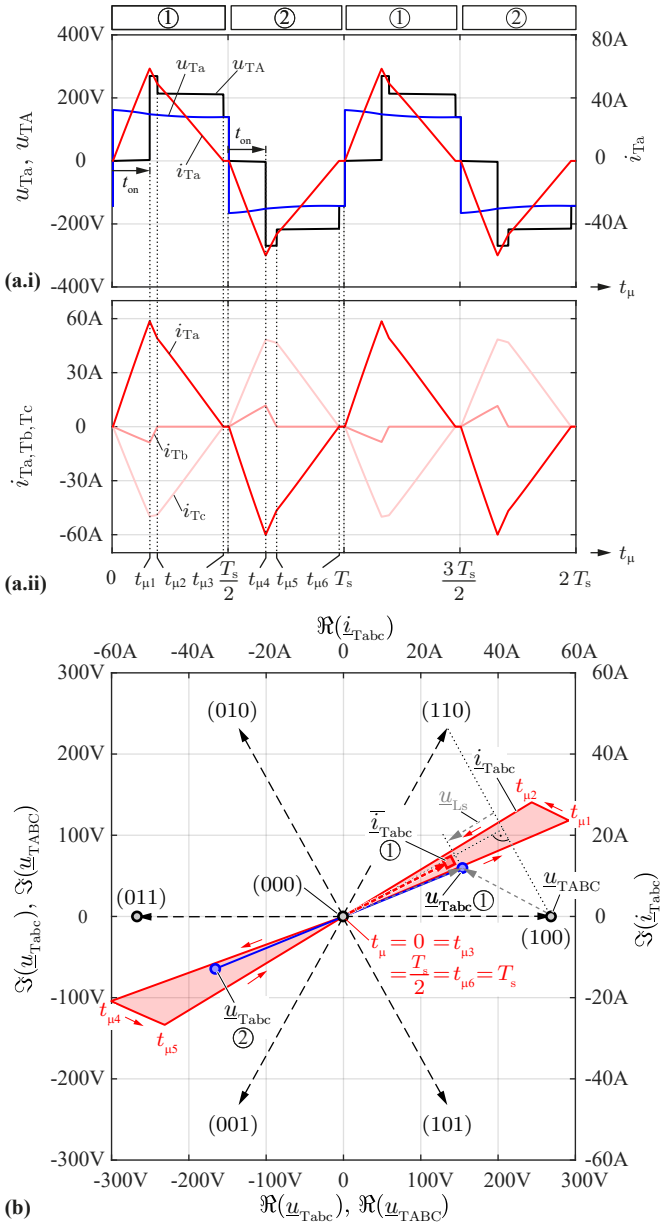

Fig. 4. Main DCM switching-frequency waveforms for the operating point highlighted in **Fig. 2** (i.e., $U_{\mathrm{dc}} = 400\,\mathrm{V}$, $U_{\mathrm{N}} = 230\,\mathrm{V_{rms}}$, and a grid angle $\alpha_{\mathrm{N}} = 2\pi f_{\mathrm{N}} t = 20°$): **(a)** Time-domain waveforms of module a, i.e., the transformer primary- and secondary-side voltages u_{Ta} and u_{TA}, and the transformer current i_{Ta}. **(b)** Space-vector representation of the three-phase voltages and currents during one switching period. The switching frequency is $f_{\mathrm{s}} = 72\,\mathrm{kHz}$, the transformer leakage inductance $L_{\mathrm{s,DCM}} = 5.8\,\mu\mathrm{H}$, and the secondary-side turn-on time is $t_{\mathrm{on}} = 2.2\,\mu\mathrm{s}$ ($\delta_{\mathrm{on}} = 0.3$).

concepts, based on DCM and DAB operation, are considered here and discussed in detail in the following.

A. Modulation Concept I (DCM)

Aiming at a simple modulation concept, the secondary-side converter stage can be operated with DCM similar to [18]–[20]: The secondary-stage high-side semiconductors are turned off permanently, i.e., in **Fig. 1b** S_{A}=S_{B}=$S_{\mathrm{C}} = 0$, and current flow is only possible through the respective body diodes.

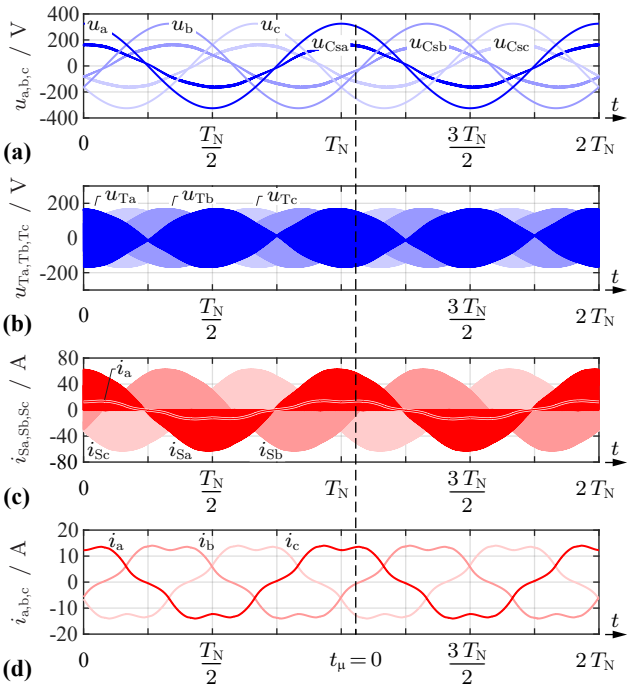

Fig. 5. Main DCM operation waveforms for two grid periods T_{N} with $U_{\mathrm{N}} = 230\,\mathrm{V_{rms}}$, $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and $P = 6.6\,\mathrm{kW}$: **(a)** Grid ($u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}}$) and series capacitor voltages $u_{\mathrm{Csa}}, u_{\mathrm{Csb}}, u_{\mathrm{Csc}}$, **(b)** transformer primary-side voltages $u_{\mathrm{Ta}}, u_{\mathrm{Tb}}, u_{\mathrm{Tc}}$ which are grid-frequency amplitude modulated HF signals, **(c)** primary-side high-side semiconductor currents $i_{\mathrm{Sa}}, i_{\mathrm{Sb}}, i_{\mathrm{Sc}}$, and **(d)** grid currents $i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}}$ The switching frequency is $f_{\mathrm{s}} = 72\,\mathrm{kHz}$, the transformer leakage inductance $L_{\mathrm{s,DCM}} = 5.8\,\mu\mathrm{H}$ and $t_{\mathrm{on}} = 2.2\,\mu\mathrm{s}$ ($\delta_{\mathrm{on}} = 0.3$).

Alternatively, the switches S_{A},S_{B},S_{C} could also be replaced with diodes.

At the beginning of each switching half-period $T_{\mathrm{s}}/2$ (i.e., at each leading or falling edge of the primary-side transformer voltages in **Fig. 3a**) the low-side semiconductors S'_{A},S'_{B},S'_{C} are turned on synchronously, thereby shorting the secondary-side switch nodes $\bar{A}, \bar{B}, \bar{C}$ via the negative dc-link rail such that the transformer secondary-side voltages are forced to zero. This state is kept for a constant on-time t_{on}, which is typically expressed relative to $T_{\mathrm{s}}/2$ as

$$\delta_{\mathrm{on}} = \frac{t_{\mathrm{on}}}{T_{\mathrm{s}}/2}. \tag{1}$$

The main switching-frequency waveforms of module a for the operating point highlighted in **Fig. 2** (i.e., for a grid angle $\alpha_{\mathrm{N}} = 2\pi f_{\mathrm{N}} t = 20°$) are presented in **Fig. 4a.i**, and **Fig. 4a.ii** further highlights the three transformer currents $i_{\mathrm{Ta}}, i_{\mathrm{Tb}}, i_{\mathrm{Tc}}$. Here, a relative on-time $\delta_{\mathrm{on}} = 0.3$ is considered, and during the initial secondary-side on-state interval the transformer currents $i_{\mathrm{Ta}}, i_{\mathrm{Tb}}, i_{\mathrm{Tc}}$ increase as the primary-side transformer voltages $u_{\mathrm{Ta}}, u_{\mathrm{Tb}}, u_{\mathrm{Tc}}$ are applied across the transformer leakage inductances L_{s}. Starting from initially zero current in DCM, a local peak transformer current value of, e.g., for phase a

$$i_{\mathrm{Ta,pk}}(t) = \delta_{\mathrm{on}} \frac{T_{\mathrm{s}} u_{\mathrm{a}}(t)}{4 L_{\mathrm{s}}}, \tag{2}$$

is reached within the on-state interval, depending on the transformer leakage inductance L_{s} (see **Fig. 3c**). Advantageously

$i_{\mathrm{Ta,pk}}(t)$ is directly proportional to the respective grid voltage, and the resulting transformer current SV $\underline{\bar{i}}_{\mathrm{Tabc}}$ in **Fig. 4b** shows the desired phase relationship to the primary-side voltage SV $\underline{u}_{\mathrm{Tabc}}$ for sinusoidal grid currents within the on-state interval.

When the on-time expires, the semiconductors S'_{A},S'_{B},S'_{C} are turned off such that the transformer currents $i_{\mathrm{Ta}}, i_{\mathrm{Tb}}, i_{\mathrm{Tc}}$ flow through the diodes of the secondary-side high-side and low-side semiconductors according to the current direction. Accordingly, the inductances L_{s} are demagnetized by the differences of the dc-link voltage U_{dc} and the secondary-side-referred HF transformer voltages. In the considered operating point, the transformer current of phase b is the first to reach zero at the time instance $t_{\mu 2}$. Thus, the body diode of the semiconductor S'_{B} stops conducting and the current slope of the two remaining phases a, c changes due to the change in the secondary-side stage voltage SV. It is important to highlight that the transformer current SV $\underline{i}_{\mathrm{Tabc}}$ is no longer in phase with the primary-side voltage SV $\underline{u}_{\mathrm{Tabc}}$ during the demagnetization process. Inevitably, thus, the local average transformer current SV $\underline{\bar{i}}_{\mathrm{Tabc}}$ is not fully in phase with $\underline{u}_{\mathrm{Tabc}}$ with the phase shift varying (and changing sign) over each sector of the grid period. Therefore, LF grid current distortions result. Finally, at $t = t_{\mu 3} < T_{\mathrm{s}}/2$ all transformer currents reach zero. In the subsequent switching half-period (2), the process repeats accordingly, and negative peak transformer currents with inverted signs compared to (2) result due to the inverted transformer primary-side voltage SV $\underline{u}_{\mathrm{Tabc}}$.

Fig. 5 shows the simulated converter waveforms for two grid periods T_{N} with $\delta_{\mathrm{on}} = 0.3$ corresponding to a transferred power $P = P_{\mathrm{N}} = 6.6\,\mathrm{kW}$, where the discussed LF grid current distortion can be observed. Note that the current distortion depends on the modulation index M defined as

$$M = \frac{U_{\mathrm{dc}}}{\sqrt{3}(\frac{\hat{U}_{\mathrm{N}}}{2})}, \tag{3}$$

with $M = 1.42$ for the considered specifications in **Tab. I**. Improved grid current quality results for larger values of M [19] and fully sinusoidal grid currents can be enabled by means of advanced modulation techniques [20] which are not discussed in detail here. Further, the secondary-side converter stage diode conduction losses during the demagnetization interval can be reduced by employing synchronous rectification.

Fig. 6 presents the simulated dependence of the transferred power P on the relative secondary-side converter stage turn-on time δ_{on} in DCM operation, which is limited to positive values of P (i.e., power flow from the grid to the dc output) because of the diode behavior of the disabled secondary-side high-side semiconductors S_{A},S_{B},S_{C}. Due to the distorted grid currents, the instantaneous transferred power $p(t)$ fluctuates within each $\pi/6$-interval of the grid angle $\alpha_{\mathrm{N}} = 2\pi f_{\mathrm{N}} t$ and the average power P is a function of the modulation index M and the converter specifications with [19]

$$P = \frac{1}{\pi/6}\int_0^{\frac{\pi}{6}} p(\alpha_{\mathrm{N}}, M, L_{\mathrm{s}}) d\alpha_{\mathrm{N}} \approx k_{\mathrm{DCM}} \cdot \frac{\delta_{\mathrm{on}}^2}{2\pi f_{\mathrm{s}} L_{\mathrm{s}}}, \tag{4}$$

and can be approximated with a quadratic relationship to the relative on-time δ_{on} (following the derivation from [19],

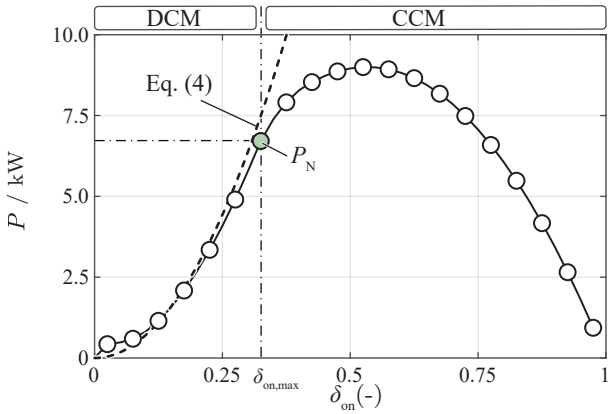

Fig. 6. Simulated dependence of the transferred power P on the relative secondary-side converter stage turn-on time δ_{on} in DCM operation for $U_{\mathrm{dc}} = 400\,\mathrm{V}$, $U_{\mathrm{N}} = 230\,\mathrm{V_{rms}}$, $f_{\mathrm{s}} = 72\,\mathrm{kHz}$ and $L_{\mathrm{s,DCM}} = 5.8\,\mu\mathrm{H}$. The dashed line represents the calculated power flow according to (4). Note that this modulation strategy is limited to power flow from the grid to the dc output (i.e., unidirectional). Further, for $\delta_{\mathrm{on}} > \delta_{\mathrm{on,max}} = 0.3$, Discontinuous Conduction Mode (DCM) operation is lost and the converter temporarily enters a Continuous Conduction Mode (CCM); the system is designed, however, to achieve nominal power $P_{\mathrm{N}} = 6.6\,\mathrm{kW}$ at the upper end of the DCM range.

$k_{\mathrm{DCM}} = 186\,083\,\mathrm{W\Omega}$ can be obtained for the considered specifications in **Tab. I**).

It is worth highlighting that in contrast to the traditional non-isolated DCM system [18]–[20] current controllability is not lost in case the relative on-time δ_{on} exceeds the maximum value for DCM [19]

$$\delta_{\mathrm{on,max}} = 1 - M^{-1}, \tag{5}$$

with $\delta_{\mathrm{on,max}} = 0.3$ for the considered specifications in **Tab. I**. In case $\delta_{\mathrm{on}} > \delta_{\mathrm{on,max}}$ not all of the three transformer currents return to zero within one switching half-period $T_{\mathrm{s}}/2$. Due to the polarity reversal of the primary-side transformer voltages in each switching half-period $T_{\mathrm{s}}/2$ (see **Fig. 4a.i**), the local average transformer currents within one full switching period T_{s} are maintained at zero and the converter can thus safely transition to Continuous Conduction Mode (CCM) operation (see **Fig. 6**), which, however, comes at the cost of elevated current stresses.

B. Modulation Concept II (DAB)

It is important to highlight that the HF DM equivalent circuit in **Fig. 3c** represents the SV equivalent of a standard dc-dc DAB such that a DAB-type modulation seems an obvious candidate for the secondary-side converter stage operation. Here, the modulation approach described in [14], [15] is employed, where the secondary-side converter stage is operated by means of SVM generating a voltage SV $\underline{u}_{\mathrm{TABC}}$ that, on average over half a switching period $T_{\mathrm{s}}/2$, is equal to the secondary-side-referred value of the voltage SV $\underline{u}_{\mathrm{Tabc}}$ generated by the primary-side converter stage.

In particular, the secondary-side converter stage is operated with a defined sequence of states such that symmetrical voltage characteristics within each switching half-period $T_{\mathrm{s}}/2$ result as highlighted for module a in **Fig. 7a**. For the first $60°$ sector of the grid period T_{N}, i.e., $0 < 2\pi f_{\mathrm{N}} t < 60°$, this is realized with

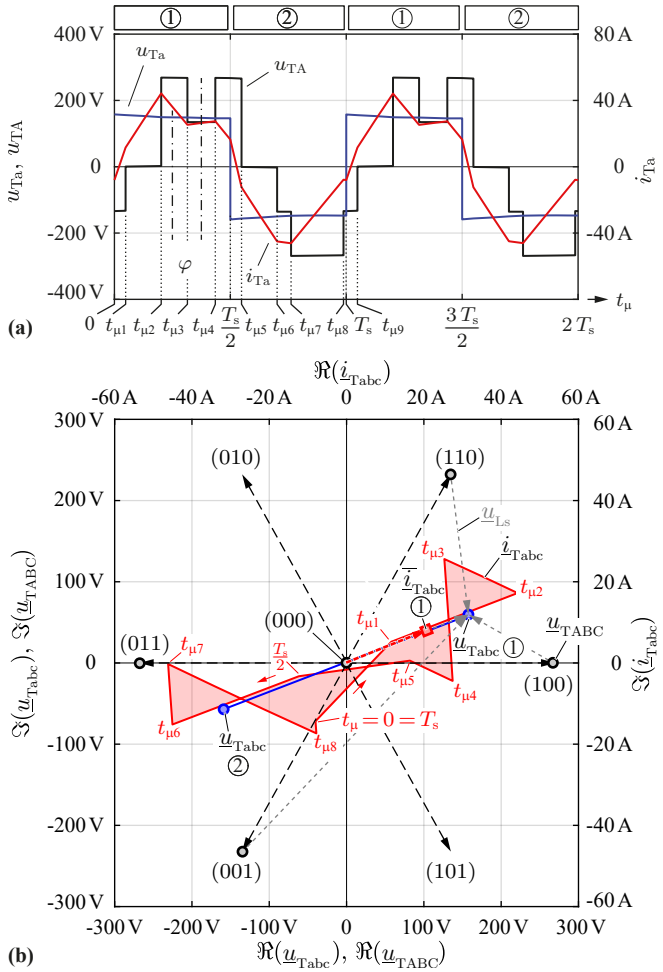

Fig. 7. Main DAB switching-frequency waveforms for the operating point highlighted in **Fig. 2** (i.e., $U_{\mathrm{dc}} = 400\,\mathrm{V}$, $U_{\mathrm{N}} = 230\,\mathrm{V_{rms}}$, and a grid angle $\alpha_{\mathrm{N}} = 2\pi f_{\mathrm{N}} t = 20°$): **(a)** Time-domain waveforms of module a, i.e., the transformer primary- and secondary-side voltages u_{Ta} and u_{TA}, and the transformer current i_{Ta}. **(b)** Space-vector representation of the three-phase voltages and currents. The switching frequency is $f_{\mathrm{s}} = 72\,\mathrm{kHz}$, the transformer leakage inductance $L_{\mathrm{s,DAB}} = 10.8\,\mu\mathrm{H}$, and the phase shift between primary- and secondary-side PWM carriers is $\varphi = \frac{\pi}{4}$.

the following sequence of secondary-side switching states (see **Fig. 7b**),

$$\begin{aligned}(000) \rightarrow (100) \rightarrow (110) \rightarrow (100) \rightarrow (000)\\ \rightarrow (001) \rightarrow (011) \rightarrow (001) \rightarrow (000),\end{aligned} \tag{6}$$

where the notation $(S_{\mathrm{A}} S_{\mathrm{B}} S_{\mathrm{C}})$ is used here, and the low-side switching signals $S'_{\mathrm{A}}, S'_{\mathrm{B}}, S'_{\mathrm{C}}$ are set complementarily. In order to achieve symmetry, the durations of the states considered in (6) are selected according to

$$\frac{d_1 T_{\mathrm{s}}}{2} = 2(t_{\mu 3} - t_{\mu 2}) = 2(t_{\mu 5} - t_{\mu 4}) = t_{\mu 8} - t_{\mu 7}, \tag{7}$$

$$\frac{d_2 T_{\mathrm{s}}}{2} = t_{\mu 4} - t_{\mu 3} = 2(t_{\mu 7} - t_{\mu 6}) = 2(t_{\mu 9} - t_{\mu 8}), \tag{8}$$

$$t_{\mu 2} - t_{\mu 1} = t_{\mu 6} - t_{\mu 5}, \tag{9}$$

where $t_{\mu 1}$ to $t_{\mu 9}$ refer to the time instants defined in **Fig. 7a**.

In order to transmit a certain power P from the grid to the secondary side, the generation of the secondary-side voltages needs to be delayed by a small time delay Δt (which is a fraction of a switching half-period $T_{\mathrm{s}}/2$) resulting in a PWM carrier phase shift

$$\varphi = 2\pi \frac{\Delta t}{T_{\mathrm{s}}}, \tag{10}$$

as illustrated in **Fig. 7a,b** for $\varphi = \pi/4$.

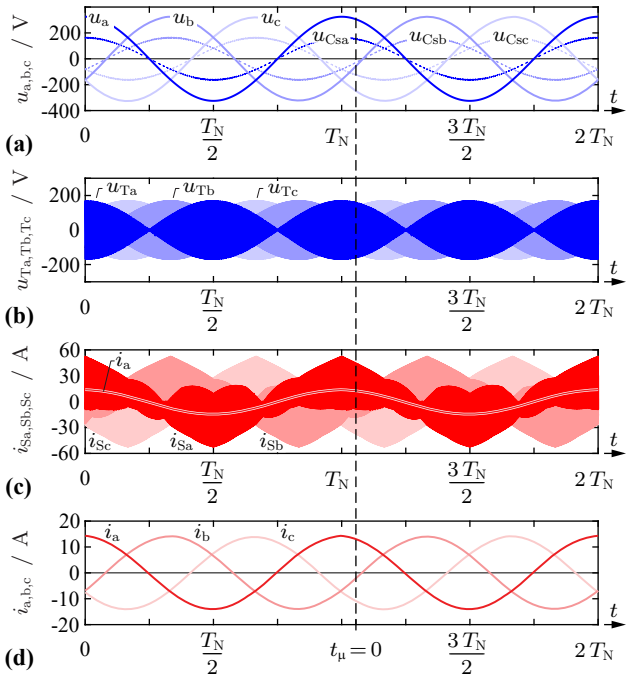

Fig. 8. Main DAB operation waveforms for two grid periods T_{N} with $U_{\mathrm{N}} = 230\,\mathrm{V_{rms}}$, $U_{\mathrm{dc}} = 400\,\mathrm{V}$ and $P = 6.6\,\mathrm{kW}$: **(a)** Grid $(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}})$ and series capacitor voltages $u_{\mathrm{Csa}}, u_{\mathrm{Csb}}, u_{\mathrm{Csc}}$, **(b)** transformer primary-side voltages $u_{\mathrm{Ta}}, u_{\mathrm{Tb}}, u_{\mathrm{Tc}}$ which are grid-frequency amplitude modulated HF signals, **(c)** primary-side high-side semiconductor currents $i_{\mathrm{Sa}}, i_{\mathrm{Sb}}, i_{\mathrm{Sc}}$, and **(d)** sinusoidal grid currents $i_{\mathrm{a}}, i_{\mathrm{b}}, i_{\mathrm{c}}$. The switching frequency is $f_{\mathrm{s}} = 72\,\mathrm{kHz}$, the transformer leakage inductance $L_{\mathrm{s,DAB}} = 10.8\,\mu\mathrm{H}$ and $\varphi = \frac{\pi}{4}$.

Fig. 8 shows the simulated converter waveforms for two grid periods T_{N} with $\varphi = \frac{\pi}{4}$ corresponding to a transferred power $P = P_{\mathrm{N}} = 6.6\,\mathrm{kW}$, where (in close approximation) ideally sinusoidal grid currents can be observed.

The PWM carrier phase shift can be selected within $\varphi \in [-\pi, \pi]$ and power transfer from the secondary side to the primary side is achieved by delaying the generation of the primary-side voltages by means of a negative value of φ. **Fig. 9** presents the converter control characteristic, i.e., the dependence of the transferred power P on the PWM carrier phase shift $\varphi \in [-\pi, \pi]$ between primary and secondary side. The transferred power can be approximated according to a sine relationship with the PWM carrier phase shift φ and

$$P \approx k_{\mathrm{DAB}} \cdot \frac{\sin \varphi}{2\pi f_{\mathrm{s}} L_{\mathrm{s}}}, \tag{11}$$

with $k_{\mathrm{DAB}} = 42\,876\,\mathrm{W\Omega}$ for the considered specifications in **Tab. I**. Note that similar to a standard dc-dc DAB, the maximum power is transferred for $\varphi = \pm\pi/2$ and elevated current stresses result for $\varphi > \pi/2$.

As a final remark, it is worth noting that the SVM from [15] employed here does not permit any further optimization of the

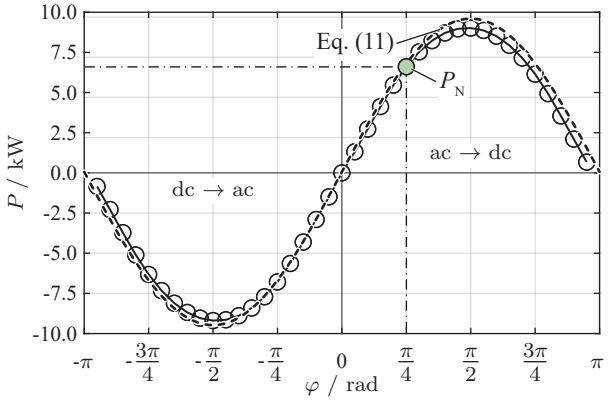

Fig. 9. Simulated dependence of the transferred power P on the PWM carrier phase shift $\varphi \in [-\pi, \pi]$ between primary and secondary side for $U_\mathrm{dc} = 400\,\mathrm{V}$, $U_\mathrm{N} = 230\,\mathrm{V_{rms}}$, $f_\mathrm{s} = 72\,\mathrm{kHz}$ and $L_\mathrm{s,DAB} = 10.8\,\mu\mathrm{H}$. The dashed line represents the calculated power flow according to (11). Note that bidirectional power flow is possible and $\varphi > 0$ corresponds to a power flow from the grid to the dc output.

switching sequences and respective time durations. The reason for this is the fact that all three available control parameters are strictly defined as d_1 and d_2 by (7) and (8), respectively, and φ is used to adjust the transmitted power P according to (11).

Therefore, to facilitate a possible optimization of the modulation scheme, it would be necessary to increase the number of degrees of freedom of the modulation. In this context, a more flexible generation of the secondary-side converter SV $\underline{u}_\mathrm{TABC}$ could be allowed. Accordingly, the conditions defined by (7), (8), and/or (9) would no longer be met and certain symmetries of the voltage waveforms at the input of the rectifier would be violated. However, this allows the number of degrees of freedom to be increased from three to up to a total number of seven. A further increase in the number of degrees of freedom could be achieved if the primary-side half-bridges were allowed to generate square-wave voltages with a duty cycle unequal to $50\,\%$.

The now possible optimization of the control process could, for example, aim at minimizing certain quality indices, such as the rms values of the transformer currents or switching losses (e.g., to maximize the range where Zero-Voltage Switching (ZVS) is achieved) which are discusses in more detail in **Section IV-B**. However, in order to allow the use of a global optimization tool, which may be necessary due to the possibly high number of degrees of freedom, a reliable and fast computation of these quality indices is required. The obtained optimization results will enable a comparative evaluation of the above optimization objectives that are obtained for different modulation methods. In this context, such optimization will serve to gain a deeper understanding in terms of optimal operation of the studied system. Accordingly, investigations in this regard are the subject of future research on the presented system.

IV. Component Stresses and Design

This section is dedicated to, first, the selection of suitable component values (**Section IV-A**) and, second, the comparative evaluation in terms of converter functionality and main component stress indices (**Section IV-B**) for both considered secondary-side converter stage modulation strategies, i.e., DCM and DAB operation.

A. Component Selection

The key passive component value to be defined during the converter design is the transformer leakage inductance L_s which limits the maximally transferable power. The considered converter specifications are listed in **Tab. I** with a nominal system power of $P = P_\mathrm{N} = 6.6\,\mathrm{kW}$ and a switching frequency $f_\mathrm{s} = 72\,\mathrm{kHz}$.

1) Series inductance: In case of DCM operation, a small value of L_s corresponds to long zero-current intervals (see **Fig. 4**) and hence a poor utilization of the power components. Hence, L_s is selected such that the nominal system power according to (4) occurs at the boundary of DCM and CCM (i.e., $\delta_\mathrm{on} = \delta_\mathrm{on,max}$) resulting in $L_\mathrm{s} = 5.8\,\mu\mathrm{H}$ (i.e., the value considered in **Section III-A**). Note that a certain overload capability with CCM operation is realized (see **Fig. 6**).

In contrast, a small value of L_s in DAB operation corresponds to ideally square-wave shaped transformer currents and high power component utilization (see **Fig. 7**). However, similar to standard dc-dc DAB converters, small values of L_s are accompanied by extremely high $\mathrm{di/dt}$ values (and hence extremely low PWM carrier phase-shift values φ) associated to poor power controllability and fault behavior. Hence, a typical value of $\varphi = \frac{\pi}{4}$ is selected here for the nominal system power, resulting with (11) in $L_\mathrm{s,DAB} = 10.8\,\mu\mathrm{H}$ (i.e., the value considered in **Section III-B**), again allowing for a certain overload capability (see **Fig. 9**).

2) Series capacitor: The derivation of the primary-side transformer voltage waveforms in **Section II** is based on the assumption that at the switching frequency f_s (and above) the impedance of the series capacitor $Z_\mathrm{Cs}(f_\mathrm{s})$ is small compared to the transformer leakage inductance $Z_\mathrm{Ls}(f_\mathrm{s})$. Here, a factor of ten in impedance difference is selected, i.e.,

$$C_\mathrm{s} = \frac{10}{(2\pi f_\mathrm{s})^2 L_\mathrm{s}}, \tag{12}$$

is selected. Therefore, the series capacitor values C_s required for DCM operation are almost a factor of two higher compared to those for DAB operation, as stated in **Tab. II**. This renders the DAB operation more favorable in terms of a compact primary-side series capacitor C_s realization.

3) Power semiconductors: Last, a maximum input-stage voltage of $2 \cdot \hat{U}_\mathrm{N} = 650\,\mathrm{V}$ requires the utilization of semiconductors with $900\,\mathrm{V}$ blocking voltage to ensure sufficient voltage margin during transients, and $900\,\mathrm{V}$ / $10\,\mathrm{m\Omega}$ Silicon Carbide (SiC) MOSFETs [21] from Cree are considered here. For both secondary-side converter stage modulation strategies the output stage dc voltage is $U_\mathrm{dc} = 400\,\mathrm{V}$ and the same $900\,\mathrm{V}$ power semiconductors as for the primary-side converter stage are employed here to maximize the number of equal parts and also to allow operation with a higher dc output voltage.

B. Component Stress Comparison

In the following, the two presented modulation strategies, i.e., DCM and DAB operation, are compared with respect to the

TABLE II: CONVERTER PARAMETERS AND COMPONENT STRESS INDICES OF MODULE a.

Param.	DCM	DAB	DCM : DAB
P	6.6 kW	6.6 kW	-
L_s	5.8 µH	10.7 µH	0.5
C_s	8.4 µF	4.6 µF	1.8
THD_{40}	13.3 %	1.6 %	8.5
I_a	10.0 $\mathrm{A_{rms}}$	9.9 $\mathrm{A_{rms}}$	1.0
I_Ca	14.9 $\mathrm{A_{rms}}$	12.3 $\mathrm{A_{rms}}$	1.2
$I_\mathrm{Ta} = I_\mathrm{Csa}$	24.5 $\mathrm{A_{rms}}$	22.3 $\mathrm{A_{rms}}$	1.1
I_Sa	17.3 $\mathrm{A_{rms}}$	15.7 $\mathrm{A_{rms}}$	1.1
$I_\mathrm{Sa'}$	17.3 $\mathrm{A_{rms}}$	15.6 $\mathrm{A_{rms}}$	1.1
I_SA	13.8 $\mathrm{A_{rms}}$	12.3 $\mathrm{A_{rms}}$	1.1
$I_\mathrm{SA'}$	20.2 $\mathrm{A_{rms}}$	18.4 $\mathrm{A_{rms}}$	1.1
$P_\mathrm{Sa,C}$ ($P_\mathrm{Sa,s}$[1])	3.0 W (12.0 W)	2.5 W (1.9 W)	-
$P_\mathrm{Sa',C}$ ($P_\mathrm{Sa',s}$[1])	3.0 W (12.0 W)	2.4 W (5.1 W)	-
$P_\mathrm{SA,C}$ ($P_\mathrm{SA,s}$[1])	1.9 W (0.0 W)	1.5 W (2.6 W)	-
$P_\mathrm{SA',C}$ ($P_\mathrm{SA',s}$[1])	4.1 W (13.2 W)	3.4 W (3.4 W)	-

[1] Switching loses calculated based on [21].

converter functionality and component stress indices with the key performance indices for nominal power operation ($P_\mathrm{N} = 6.6\,\mathrm{kW}$) summarized in **Tab. II**.

It is immediately clear from the operating concepts discussed in **Section III** that the DAB operation is favorable in terms of functionality, as it allows bidirectional power flow and purely sinusoidal grid currents (see **Fig. 8**), compared to DCM operation with unidirectional power flow and a LF grid current distortion (see **Fig. 5**). This also manifests in a grid current Total Harmonic Distortion (THD) value which is elevated by more than a factor of 5 (which also results in an elevated LF grid rms current I_a) with DCM compared to DAB operation (see **Tab. II**). This, however, could be avoided by means of an advanced DCM modulation concept [20].

For both modulation strategies the HF transformer is subject to current stresses $I_\mathrm{Ta} = I_\mathrm{Csa}$ elevated by approximately a factor of two compared to the nominal grid current I_N, hence also causing increased current stresses in the power semiconductors of the primary- and secondary-side converter stages. The high HF transformer current stresses I_Ta are mainly a consequence of the fact that the transformer primary-side terminal voltages are reduced by a factor of two compared to the grid voltage as highlighted in **Fig. 3a**, where I_Ta is further increased by approximately 10 % with DCM compared to DAB operation due to the discontinuous current flow (see **Tab. II**).

Fig. 10 further depicts the local rms currents (across one switching half-period $T_\mathrm{s}/2$) of module a's primary-side (S_a,S'_a) and secondary-side (S_A,S'_A) power semiconductors within one grid period T_N, showing elevated current stresses for DCM compared to DAB operation. This results in the global rms current stresses (across one grid period T_N) of the semiconductors listed in **Tab. II**. Similar to the transformer, the semiconductor current stresses are relatively high compared to the nominal grid current I_N. However, the availability of low-on-state-resistance WBG semiconductors allows efficient converter realizations with low conduction losses. Thus, **Tab. II** also lists the calculated semiconductor conduction losses $P_\mathrm{x,C}$ of module a, which remain below 5 W (assuming synchronous rectification also for DCM operation). Note that

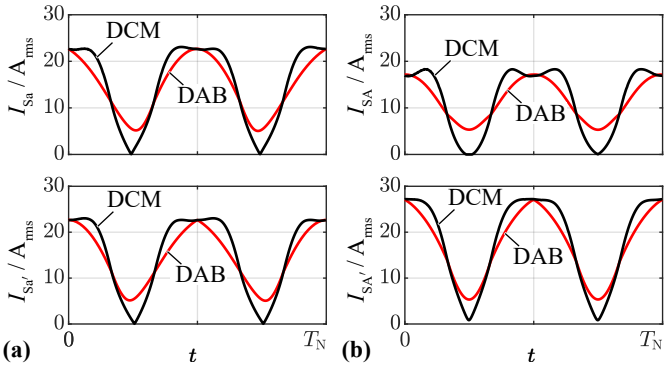

Fig. 10. Local (across one switching half-period $T_\mathrm{s}/2$) rms current stresses of **(a)** the primary-side S_a,S'_a and **(b)** the secondary-side S_A,S'_A power semiconductors of module a within one grid period T_N for nominal power operation and the component values stated in **Tab. II**.

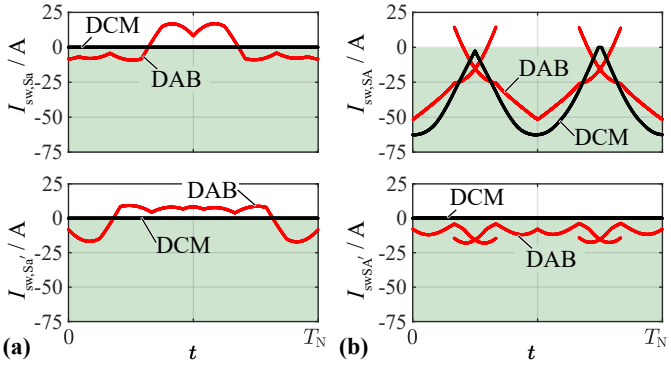

Fig. 11. Turn-on current values of **(a)** the primary-side S_a,S'_a, and **(b)** the secondary-side S_A,S'_A power semiconductors of module a within one grid period T_N for nominal power operation and the component values stated in **Tab. II**. Switched current values $< 0\,\mathrm{A}$ correspond to a soft-switching (i.e., Zero-Voltage Switching (ZVS)) turn-on event with substantially reduced switching losses compared to a hard-switching turn-on event [21]. Further, note that for DAB operation the secondary-side semiconductors S_A,S'_A switch twice within each switching period T_s (i.e., two turn-on current values exist in (b)) during two 60° intervals of the grid period T_N.

for DCM operation the maximum conduction losses result for the secondary-side converter stage low-side semiconductors $S'_\mathrm{A}, S'_\mathrm{B}, S'_\mathrm{C}$, which is a consequence of the fact that they conduct the transformer currents during the on-time interval (see **Section III-A**). A more even conduction stress distribution could be realized by turning on the secondary-side converter stage high-side semiconductors $S_\mathrm{A}, S_\mathrm{B}, S_\mathrm{C}$ during every second on-time interval instead.

Last, **Fig. 11** depicts the turn-on current values of the module a primary-side (S_a,S'_a) and secondary-side (S_A,S'_A) power semiconductors within one grid period T_N. There, switched current values $< 0\,\mathrm{A}$ correspond to a soft-switching (i.e., Zero-Voltage Switching (ZVS)) turn-on event with substantially reduced switching losses compared to a hard-switching turn-on event and the switching losses (including turn-on and turn-off transitions) in **Tab. II** are calculated from the switched voltage and current values using the calorimetric switching loss measurement data provided in [21].

Advantageously, the primary-side semiconductors (S_a,S'_a) are fully soft-switched in the vicinity of the peak input capacitor voltage in DAB operation such that the losses are

reduced by up to a factor of 6 compared to DCM operation, where the semiconductors are continuously hard-switched at zero current (i.e., Zero-Current Switching (ZCS)). Note that for DAB operation the secondary-side semiconductors (S_A,S'_A) switch twice within each switching period T_s (i.e., two turn-on current values exist in **Fig. 11b**) during two $60°$ intervals of the grid period T_N due to the considered SVM switching pattern discussed in **Section III-B**. Despite the extra switching events, the DAB secondary-side switching losses remain small compared to the ZCS losses of S'_A resulting in DCM operation. Note that the switched current in **Fig. 11b** for DCM operation represents the commutation current in the body diode of S_A (or the soft-switching turn-on current of S_A in case of synchronous rectification) according to (2).

Hence, assuming a typical transformer efficiency of $99.5\,\%$, an overall converter efficiency of $\eta_\mathrm{DCM} > 97\,\%$ and $\eta_\mathrm{DAB} > 98\,\%$ can be expected for DCM and DAB operation, respectively. Experimentation to verify these numbers is currently in progress.

In closing, it can be stated that the DAB operation of the secondary-side converter stage is advantageous with respect to all investigated stress and functionality indices. However, as key property of DCM operation remains its simplicity with respect to the realization in a prototype system, such that the selection of the operating mode depends on the application-specific importance of performance and complexity.

V. Conclusion

Future ac-dc converter systems are ideally bidirectional, feature integrated single-stage HF isolation and buck-boost capability, and employ standard semiconductor building blocks. This paper proposes a novel ac-dc converter system providing all of these desirable converter properties. The functionality of the topology concerning power flow controllability and sinusoidal input current generation based on Discontinuous Conduction Mode (DCM) operation and Space Vector Modulation (SVM) / Dual Active Bridge (DAB) operation is derived and verified by means of simulations. Design guidelines for the main power components are provided and the considered modulation strategies are compared based on functionality and component stress indices.

The results indicate the feasibility of a $6.6\,\mathrm{kW}$ grid-connected isolated single-stage converter system operating with a nominal efficiency of $\eta > 98\,\%$ if the DAB-type modulation and $900\,\mathrm{V}$ SiC transistors are employed. The experimental verification of the introduced converter concepts and the associated modulation strategies based on a hardware prototype is currently conducted. Subsequently, the goal will be to design and build an optimized converter system based on a multi-objective Pareto optimization, which also includes an Electromagnetic Interference (EMI) filter to assure compliance with the relevant conducted EMI emission standards. Last, it is important to highlight that this paper introduces two basic approaches for the secondary-side converter stage operation. Future research could focus on the investigation of advanced modulation strategies considering all degrees of freedom that the switching stages provide, thereby enabling, e.g., lower switching losses or component current stresses and/or increased power conversion efficiency.

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