electronics

MDPI

Article

Experimental Efficiency Evaluation of Stacked Transistor Half-Bridge Topologies in 14 nm CMOS Technology

Pedro André Martins Bezerra [1,†], Florian Krismer [1,*], Johann Walter Kolar [1], Riduan Khaddam-Aljameh [2], Stephan Paredes [2], Ralph Heller [2], Thomas Brunschwiler [2], Pier Andrea Francese [2], Thomas Morf [2], Marcel André Kossel [2] and Matthias Braendli [2]

[1] Power Electronic Systems Laboratory, ETH Zürich, 8092 Zurich Switzerland; bezerra@lem.ee.ethz.ch (P.A.M.B.); kolar@lem.ee.ethz.ch (J.W.K.)
[2] IBM Research Zürich, 8803 Rüschlikon, Switzerland; rid@zurich.ibm.com (R.K.-A.); spa@zurich.ibm.com (S.P.); rhr@zurich.ibm.com (R.H.); tbr@zurich.ibm.com (T.B.); pfr@zurich.ibm.com (P.A.F.); tmr@zurich.ibm.com (T.M.); mko@zurich.ibm.com (M.A.K.); mbr@zurich.ibm.com (M.B.)
* Correspondence: krismer@lem.ee.ethz.ch
† Work done while at IBM Research.

Abstract: Different Half-Bridge (HB) converter topologies for an Integrated Voltage Regulator (IVR), which serves as a microprocessor application, were evaluated. The HB circuits were implemented with Stacked Transistors (HBSTs) in a cutting-edge 14 nm CMOS technology node in order to enable the integration on the microprocessor die. Compared to a conventional realization of the HBST, it was found that the Active Neutral-Point Clamped (ANPC) HBST topology with Independent Clamp Switches (ICSs) not only ensured balanced blocking voltages across the series-connected transistors, but also featured a more robust operation and achieved higher efficiencies at high output currents. The IVR achieved a maximum efficiency of 85.3% at an output current of 300 mA and a switching frequency of 50 MHz. At the maximum measured output current of 780 mA, the efficiency was 83.1%. The active part of the IVR (power switches, gate-drivers, and level shifters) realized a high maximum current density of 24.7 A/mm^2.

Keywords: IVR; CMOS; stacked transistors; half-bridge; multi-phase; 14 nm technology; ANPC

Citation: Bezerra, P.A.M.; Krismer, F.; Kolar, J.W.; Khaddam-Aljameh, R.; Paredes, S.; Heller, R.; Brunschwiler, T.; Francese, P.A.; Morf, T.; Kossel, M.A.; et al. Experimental Efficiency Evaluation of Stacked Transistor Half-Bridge Topologies in 14 nm CMOS Technology. *Electronics* **2021**, *10*, 1150. https://doi.org/10.3390/electronics10101150

Academic Editors: Thaiyal Naayagi Ramasamy and Padmanabhan Balasubramanian

Received: 13 April 2021
Accepted: 8 May 2021
Published: 12 May 2021

1. Introduction

Modern high-performance microprocessors feature tens of processor cores [1], operate with clock frequencies up to 5 GHz [2], and, with this, achieve previously unmatched computational performance. However, this performance increase is accompanied by an increase of the required power, which can exceed 150 W per device [3]. In this context, the concept of Dynamic Voltage and Frequency Scaling (DVFS), in combination with a granular power delivery system that features independent Voltage Domains (VDs) for different cores or parts of cores, can achieve an effective reduction of the power demand [4]. By way of example, it was found in [5] that a video decoder test chip, which employs multiple different VDs with configurable supply voltages (two defined voltages: 1.6 V and 2.2 V), can achieve a reduction of the supplied power by 55% to 61%. In addition, it is desirable to reduce the high package currents of modern microprocessors. Reduced package current and adjustable supply voltages for the different VDs can be achieved with buck-type Integrated Voltage Regulators (IVRs) that are located in the package of the microprocessor or on the microprocessor die [6]. Table 1 summarizes the main specifications of the considered IVR.

Common topologies for IVRs are Switched Capacitor Converters (SCCs) and buck converters with output inductors. Numerous examples of SCCs are documented in the literature, e.g., a standalone SCC topology with regulated output voltage (using pulse

frequency modulation) [7], an SCC with a low dropout regulator in parallel to achieve low output voltage ripple [8], and a hybrid DC–DC converter, which comprises a 2:1 SCC and a 0.8 nH output inductor to achieve soft switching in order to increase the efficiency of the SCC [9]. The absence of inductors renders SCC topologies attractive with regard to chip integration, to avoid the challenges related to magnetic components (losses and required footprint area [10], the integration of magnetic materials [11], and, depending on the realization, the need for through silicon vias [12]). However, the topologies of SCCs are subject to a predefined voltage conversion ratio and generate increased losses when operated with input-to-output voltage ratios that deviate from the predefined ratio (for example, this can be observed in Figure 6 in [7], which depicts efficiency curves for an input voltage of 5 V and output voltages ranging from 3.2 V down to 2.6 V). Accordingly, inductor-type buck converters are often preferred if the ratio of input-to-output voltage is variable. Documented realizations include multi-phase buck converters with on-die inductors with a magnetic core [12], on-package air core inductors [13], and discrete inductors [6]. In addition, numerous improvements have been presented in the literature, e.g., the use of discontinuous conduction mode [14] and the implementation of a small SCC that is connected in parallel to the output of the buck converter [15], to achieve increased efficiencies under medium- and light-load conditions, respectively.

Table 1. Main specifications of the IVR.

Parameter	Value
Input voltage, V_{in}	1.6 V
Range of output voltage, V_{out}	0.8 V to 1.2 V
Maximum output current, $I_{out,max}$	800 mA
Switching frequency range, f_{sw}	50 MHz to 150 MHz

This paper presents an evaluation of an inductor-based buck-type IVR, whose power stage is comprised of four converter phases (half-bridges) that are operated in parallel with interleaving. The power stage was implemented in the high-end 14 nm CMOS technology node of the microprocessor, in order to allow for on-die integration, and employed short-channel transistors, instead of long-channel devices, to take advantage of their low conduction and switching losses [16]. With this, a high switching frequency of up to 150 MHz can be achieved, which enables a fast transient response that is needed for microprocessor applications [17]. However, short-channel transistors are subject to a reduced breakdown voltage. For this reason, the power switches of each half-bridge were realized with stacked transistors (CMOS Half-Bridges with Stacked Transistors (HBSTs)) [18], depicted in Figure 1a, in order to reduce the voltage applied to each power transistor to half of the input voltage of the CMOS HBST. (Please note that all circuits depicted in Figure 1 refer to Phase 1 of the four-phase IVR and include level-shifters, which are needed to provide the correct voltage levels for the gate drivers connected to TP_2 and TN_3.)

The CMOS HBST has been used in IVRs of commercial microprocessors in modern technology nodes built in the most recent tri-gate technology nodes, e.g., 22 nm [13] and 14 nm [19]. Although, high efficiencies are achievable using the CMOS HBST, e.g., 88% in [14], the blocking voltages of the stacked transistors can be unequal, which leads to reduced reliability and increased losses [20]. To achieve equal blocking voltages, the CMOS HBST with Active Neutral Point Clamping (CMOS ANPC HBST), depicted in Figure 1b, was considered, which adds clamp switches to the CMOS HBST to actively clamp the potential between the stacked transistors to a middle potential [21]. The CMOS ANPC HBST uses common gate drivers for the main switches and the respective clamp switches. Therefore, the clamp switches TN_3 and TP_3 are both turned on if TP_2 and TN_2 are both turned off. In addition, TP_1 starts to conduct if its gate-to-drain voltage is less than −0.3 V and TN_1 starts to conduct for a gate-to-drain voltage higher than 0.3 V, which is found in Section 2, in the course of the investigation of the simulation results.

For this reason, the output of the power stage cannot be switched to high impedance. Accordingly, phase shedding, which is used to increase part-load efficiency in multi-phase converters [22], is not possible. The CMOS ANPC HBST with Independent Clamp Switches (ICSs) of Figure 1c eliminates this shortcoming by using separate gate drivers for the clamp switches [20]. Please note that Figure 1c defines all currents and voltages of the waveforms discussed in Section 2. Furthermore, the symbols $\overline{ck_{\mathrm{GP,H,1}}}$, $ck_{\mathrm{GN,H,1}}$, $\overline{ck_{\mathrm{GP,L,1}}}$, and $ck_{\mathrm{GN,L,1}}$ in Figure 1c refer to digital gate signals that stem from the circuitry explained in Section 3.

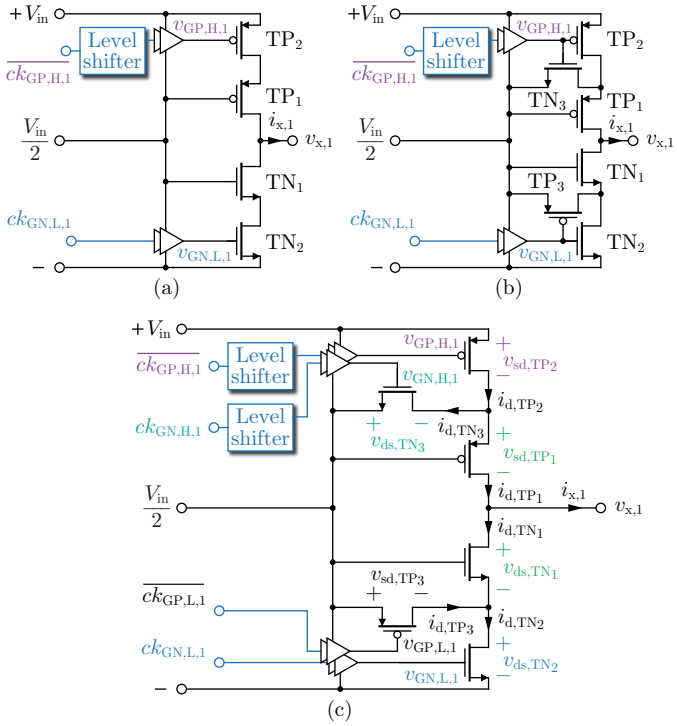

Figure 1. (**a**) CMOS Half-Bridge with Stacked Transistors (CMOS HBSTs). (**b**) CMOS Active Neutral Point Clamped (ANPC) HBST. (**c**) CMOS ANPC HBST with Independent Clamp Switches (ICSs). Adapted from [6,20,23]. Copyright © 2017 by IEEE. Adapted with permission.

The three investigated topologies, HBST, ANPC HBST, and ANPC HBST with ICS, mainly differ with regard to their behavior during switching. Accordingly, the switching operations are inspected in a first step in Section 2 based on simulation results in order to gain a deeper understanding of the different topologies. However, the conducted simulations disregard different loss components, e.g., due to the Power Distribution Network (PDN) and the metal layers of the chip. In order to provide a robust comparison of the three topologies, experimental efficiency results are used to assess the topologies. In this regard, Section 3 summarizes the implementation details of the realized IVR. Section 4 presents the results of the experimental evaluation. Section 5 provides a final discussion. With this, the paper provides the two key contributions listed below.

1. first, the experimental validation of a CMOS ANPC HBST with ICS that is realized in 14 nm CMOS technology;
2. a comparative evaluation of the conventional CMOS HBST, the conventional CMOS HBST ANPC, and the CMOS HBST ANPC with ICS based on measured efficiencies.

2. Investigation of the Switching Operations

This section investigates the switching operations of the three considered circuit topologies, i.e., the CMOS HBST in Section 2.1 and the CMOS ANPC HBST, as well as the CMOS ANPC HBST with ICS in Section 2.2, using simulated waveforms, and presents a related discussion of the main findings in Section 2.3. All simulations were conducted with the circuit simulator that is part of the Virtuoso Custom IC Design Environment by

Cadence (Version ICADV12.1), which, for the employed 14 nm CMOS technology, was the only software tool for simulation that was available to our research group in the scope of this work. By way of example, Converter Phase 1 of the four-phase IVR was selected for this purpose. With this, it provides a knowledge basis for the discussions presented in the subsequent sections of this paper. This section summarizes the findings of a previous conference publication [20].

Figure 2 presents typical gate voltages that are used to generate an output voltage, $v_{x,1}$, with a defined duty cycle at the switching node of the buck converter. Figure 2a depicts the gate voltages $v_{GP,H,1}$ and $v_{GN,L,1}$ that are applied to the transistors TP_2 and TN_2, respectively. These waveforms are valid for all three topologies shown in Figure 1. Figure 2b shows the additional gate voltages, $v_{GN,H,1}$ and $v_{GP,L,1}$, for the clamping switches TN_3 and TP_3 of the CMOS ANPC HBST with ICS. The presented gate voltages are measured with respect to the minus terminal of the power stage. (Please note that TP_1, TP_2, and TP_3 are p-type MOSFETs; for this reason, negative gate-to-source voltages are needed to turn on TP_1, TP_2, and TP_3. In addition, the gate voltages of TP_2 and TN_3, $v_{GP,H,1}$ and $v_{GN,H,1}$, feature an offset of $V_{in}/2$, which is needed to keep the transistors' gate-to-source voltages within the allowable voltage range.) In the case of the CMOS HBST, solely the switching states of TP_2 and TN_2 determine the switching states of TP_1 and TN_1, respectively, e.g., if TP_2 is in the on-state and TN_2 in the off-state (with an assumed drain-to-source voltage of $V_{in}/2$), the gate-to-source voltages of TP_1 and TN_1 are equal to $-V_{in}/2$ and zero, respectively. Accordingly, TP_1 is in the on-state and TN_1 in the off-state. Figure 2a,b reveals the dead times between subsequent turn-off and turn-on events, to avoid short-time short circuits in the HBST, and Figure 2c illustrates the waveform of the voltage at the switching node, $v_{x,1}$, that results for the gate voltages of Figure 2a (and Figure 2b in the case of the CMOS ANPC HBST with ICS) and a positive output current, $i_{x,1}$. During the voltage transitions between zero and V_{in}, the actual waveform of the switched voltage depends on the topology as explained in Sections 2.1 and 2.2.

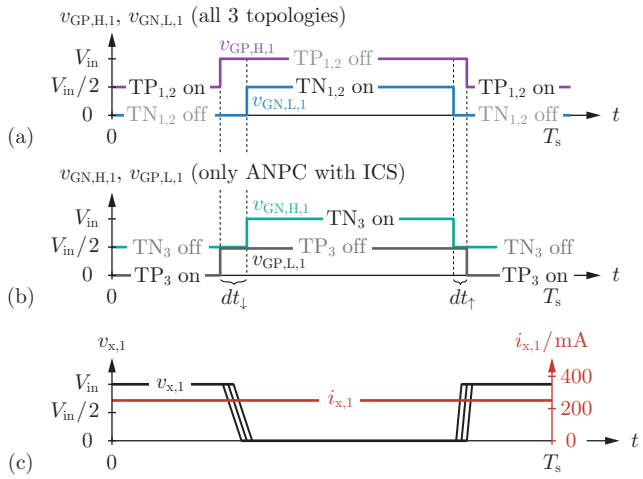

Figure 2. Waveforms of the gate voltages for a programmed duty cycle of 50%. (**a**) Gate voltages $v_{GP,H,1}$ and $v_{GN,L,1}$. (**b**) Gate voltages $v_{GN,H,1}$ and $v_{GP,L,1}$. (**c**) Resulting waveform of the switched output voltage, $v_{x,1}$, for a positive output current, e.g., $i_{x,1} = 250\,\mathrm{mA}$.

The simulated waveforms of the transistor currents and drain-source voltages during the time intervals where $v_{x,1}$ changes from V_{in} to zero and vice versa are presented in Figures 3–5 for the CMOS HBST, the CMOS ANPC HBST, and the CMOS ANPC HBST with ICS topologies, respectively. All simulations considered the settings of Table 1 and a constant output current of 250 mA (i.e., a negligible output current ripple was assumed) and disregarded the implications of the metal layers and the power distribution network of the IVR's Power Management IC (PMIC) on the waveforms.

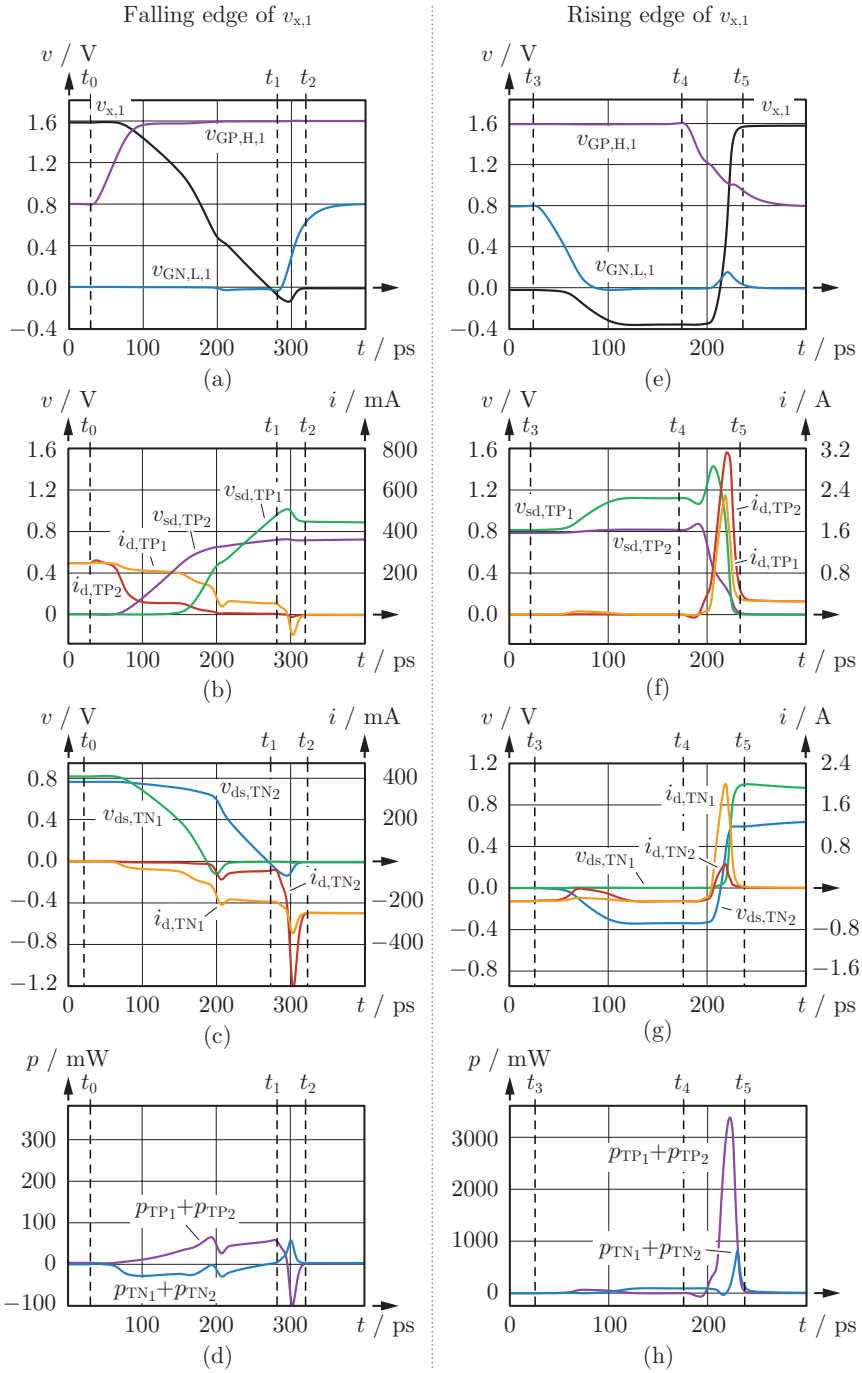

Figure 3. Currents and voltages in the transistors of a conventional HBST simulated with Cadence for the settings listed in Table 1 and $i_{x,1} = 250\,\text{mA}$: (**a**–**d**) falling edge of $v_{x,1}$; (**e**–**h**) rising edge of $v_{x,1}$. Subfigures (**d**) and (**h**) show the instantaneous powers in the power transistors of the HBST. Adapted from [20]. Copyright © 2017 by IEEE. Adapted with permission.

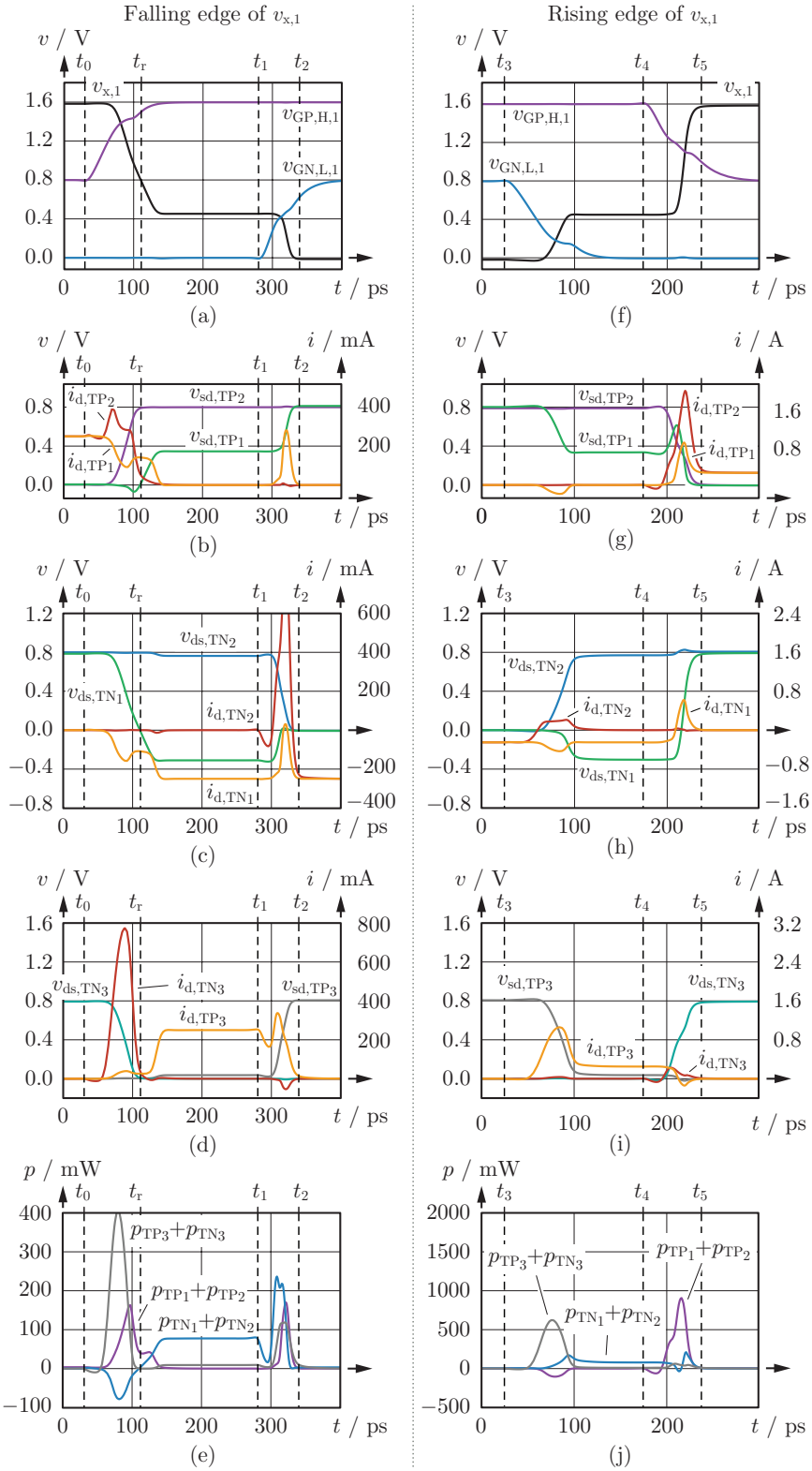

Figure 4. Currents and voltages in the transistors of an ANPC HBST simulated with Cadence for the settings listed in Table 1 and $i_{x,1} = 250\,\text{mA}$: (**a**–**e**) falling edge of $v_{x,1}$; (**f**–**j**) rising edge of $v_{x,1}$. Subfigures (**e**) and (**j**) show the instantaneous powers in the power transistors of the HBST. Adapted from [20]. Copyright © 2017 by IEEE. Adapted with permission.

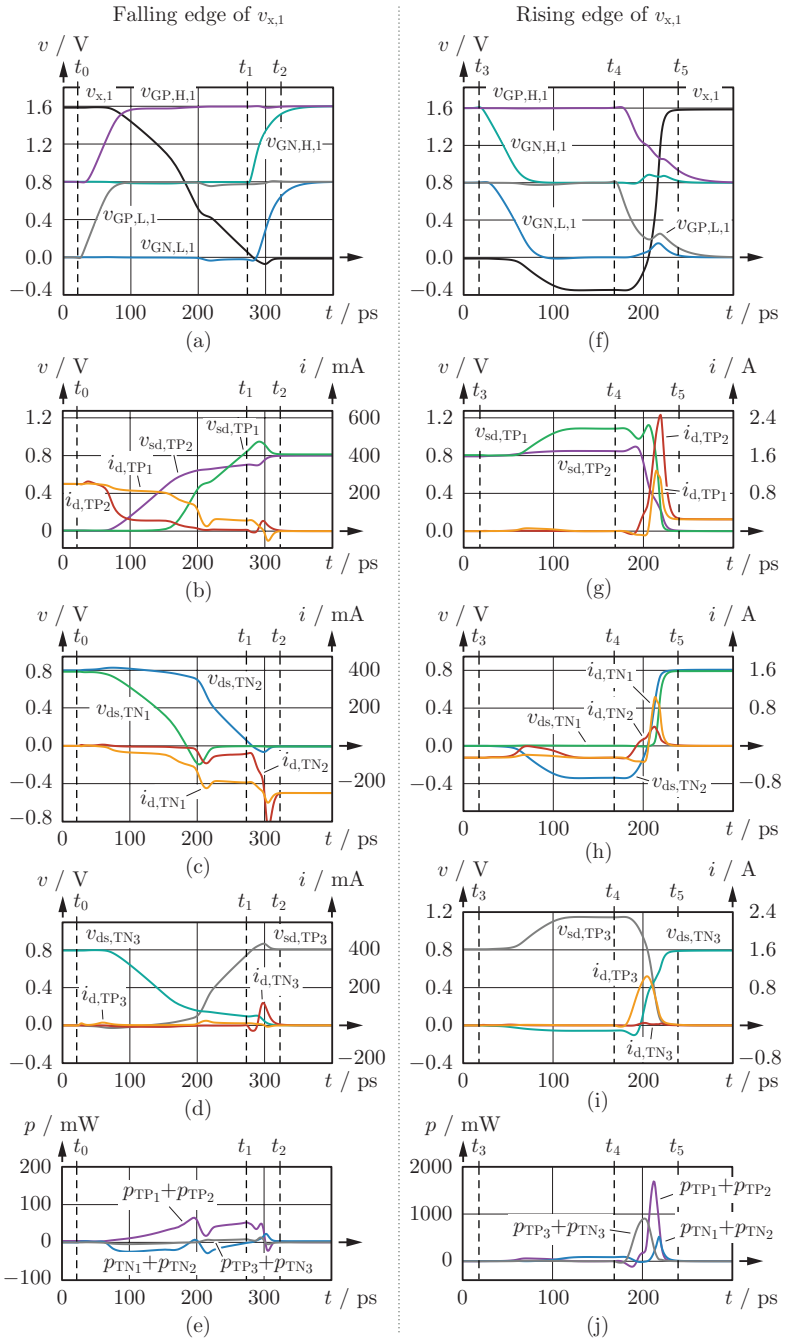

Figure 5. Currents and voltages in the transistors of an ANPC HBST with ICS simulated with Cadence for the settings listed in Table 1 and $i_{x,1} = 250\,\text{mA}$: (**a**–**e**) falling edge of $v_{x,1}$; (**f**–**j**) rising edge of $v_{x,1}$. Subfigures (**e**) and (**j**) show the instantaneous powers in the power transistors of the HBST. Adapted from [20]. Copyright © 2017 by IEEE. Adapted with permission.

2.1. Conventional HBST

The conventional *CMOS HBST* is considered in a first step. In the case of a falling edge of $v_{x,1}$, first, TP_2 is commanded to switch off at $t = t_0$, as shown in Figure 3a (please note that the definitions of all currents and voltages used in Figure 3 are given in Figure 1c). The constant output current charges the output capacitance of TP_2, and $v_{sd,TP2}$ increases, which is depicted in Figure 3b. As a consequence, the gate-to-source capacitance of TP_1 is discharged, and subsequently, TP_1 is turned off. With increasing source-to-drain voltages of TP_2 and TP_1, the drain-to-source voltages of TN_1 and TN_2 decrease, as shown in Figure 3c, in order to keep the sum $v_{sd,TP2} + v_{sd,TP1} + v_{ds,TN1} + v_{ds,TN2}$ equal to the input voltage.

Accordingly, very small turn-on losses can be achieved during $t_1 < t < t_2$, if the dead time is sufficiently large, such that $v_{ds,TN1}$ and $v_{ds,TN2}$ reach zero before TN_2 is commanded to turn on at $t = t_1$. Figure 3d depicts the instantaneous losses of the four power transistors, that is the products of drain-source voltages and drain currents (not considering the gate driver losses). This result reveals that a large part of the stored energy can be recycled, leading to low total switching losses. However, after the switching operation has elapsed, for $t > t_2$, the simulation computes unequal source-to-drain voltages for TP_1 and TP_2, i.e., $v_{sd,TP1} \neq v_{sd,TP2}$ applies.

The rising edge of $v_{x,1}$ is initiated by commanding TN_2 to turn off at $t = t_3$, which is depicted in Figure 3e. During the dead time interval, $t_3 < t < t_4$, TN_1 remains in the on-state, and the high-side transistors TP_1 and TP_2 remain off. As a consequence, TN_1 conducts the output current, $i_{x,1}$, which charges the output capacitance of TN_2 until $v_{ds,TN2}$ reaches approximately $-0.4\,V$; cf. Figure 3g. With this, the gate-to-drain voltage of TN_2, $v_{gd,TN2}$, reaches approximately $0.4\,V$, which leads to a turn-on of TN_2, i.e., TN_2 conducts the output current. As a result, increased conduction losses occur in TN_2 during the dead time. Furthermore, the negative value of $v_{ds,TN2}$ leads to an overvoltage condition for TP_1. (The current that charges the output capacitance of TP_1, $i_{d,TN1}$ in Figure 3g, finds a low impedance path (to $V_{in}/2$) in the large input capacitance of TP_1. For this reason, only negligible charging current remains for TP_2, leading to a negligible overvoltage across TP_2 during the dead time interval.) At $t = t_4$, TP_2 is commanded to turn on. The associated turn-on processes force $v_{sd,TP2}$ and $v_{sd,TP1}$ to decrease to zero, as shown in Figure 3f. During turn-on, large spikes are observed in the drain currents of TN_1, TP_1, and TP_2. Figure 3h depicts the instantaneous losses in the transistors, which are particularly high for TP_1 and TP_2. According to Figure 3g, TN_1 and TN_2 are subject to unequal drain-to-source voltages after the switching operation has elapsed, i.e., for $t > t_5$.

2.2. ANPC HBST without and with ICS

Figure 4 depicts the transistors' currents and voltages that result for the *CMOS ANPC HBST* for a falling edge of $v_{x,1}$ in Figure 4a,b,c,d,e and a rising edge of $v_{x,1}$ in Figure 4f–j. Figure 4 depicts the waveforms of the same physical variables as Figure 3 and, in addition, also shows the drain-to-source voltages and the drain currents of the clamping switches, TN_3 and TP_3 in Figure 4d,i. Compared to the CMOS HBST, the clamping switches TN_3 and TP_3 are both turned on during the dead time and define the drain potentials of TP_2 and TN_2 during this time.

In case of a negative slope of $v_{x,1}$, the turn-on of TN_3 leads to increased switching losses during $t_0 < t < t_r$ and the turn-on of TN_2 to increased switching losses during $t_1 < t < t_2$. In addition, an increased forward voltage drop across TN_1, which conducts the output current during the dead time, of $v_{ds,TN1} \approx -0.3\,V$, is found during $t_r < t < t_1$, which leads to increased conduction losses during this time interval. (The constant output current charges the output capacitance of TN_1 until $v_{ds,TN1} \approx -0.3\,V$ applies, which increases the gate-to-drain voltage of TN_1 to approximately $0.3\,V$, since TP_3 is turned on. As a consequence, TN_1 is forced to conduct the output current (via TP_3) during the dead time interval, $t_r < t < t_1$.) In the case of a positive slope of $v_{x,1}$, the turn-on losses are found to be less than for the HBST topology, because the active clamp switches enforce a reduction of $v_{sd,TP1}$ during the dead time $t_3 < t < t_4$, which also decreases the value of $v_{sd,TP1}$ during the turn-on time interval, $t_4 < t < t_5$, as shown in Figure 4g. Furthermore, equal blocking voltages are achieved after both switching operations, i.e., $v_{sd,TP1} = v_{sd,TP2}$ for $t > t_2$ in Figure 4b and $v_{ds,TN1} = v_{ds,TN2}$ for $t > t_5$ in Figure 4h.

The waveforms of the transistor voltages and currents simulated for the *CMOS ANPC HBST with ICS* are depicted in Figure 5. Compared to the CMOS ANPC HBST without ICS, the main switches and the clamp switches are commanded to turn off during every dead time. This can be seen in Figure 5a,f, which presents the transistors' gate signals for a falling and a rising edge of $v_{x,1}$, respectively. For this reason, the switching operations are the same as for the conventional HBST described in Section 2.1 during $t_0 < t < t_1$

and $t_3 < t < t_4$. However, at the end of the dead time interval, either TN_3 (at $t = t_1$ in Figure 5a) or TP_3 (at $t = t_4$ in Figure 5f) is turned on in addition to the two main switches (TN_1 and TN_2 or TP_1 and TP_2, respectively). With this, equal drain-to-source voltages of the main power switches are enforced as soon as the respective clamp switch is in the on-state, i.e., for $t > t_2$ in Figure 5b and for $t > t_5$ in Figure 5h.

2.3. Discussion

A comparison of the instantaneous switching losses during the rising edge of $v_{x,1}$ of the ANPC HBST without and with ICS revealed lower losses of 46 pJ for the ANPC HBST without ICS, compared to 55 pJ for the ANPC HBST with ICS (for the instantaneous power waveforms depicted in Figures 4j and 5j). However, in the case of a falling edge of $v_{x,1}$, the ANPC HBST without ICS is subject to higher losses of 37 pJ (Figure 4e), compared to 5 pJ for the ANPC HBST with ICS (Figure 5e). In addition, the switching losses depend on the dead times, $dt_\uparrow$ and $dt_\downarrow$. Accordingly, it is not directly possible to draw a meaningful conclusion. For this reason, the characteristics of the overall simulated efficiencies of the three investigated topologies are compared to each other in Figure 6. The efficiencies were determined for different dead times during the falling edge of $v_{x,1}$, $dt_\downarrow$, for the settings listed in Table 1, $D = 50\%$, $I_{x,1} = 250\,\text{mA}$, $f_{sw} = 150\,\text{MHz}$, and the minimum configurable dead time during the rising edge of $v_{x,1}$, $dt_\uparrow$, of 40 ps, which leads to minimum switching losses during the rising edge of $v_{x,1}$. As expected, the conventional ANPC HBST featured the best results for very small values of $dt_\downarrow$, due to the additional losses during the dead time, as shown in Figure 4. The efficiency characteristics of the conventional HBST and the ANPC HBST with ICS were approximately parallel, which was attributed to the similar processes that occur during the corresponding dead times. However, the conventional HBST generated higher losses in TP_1 and TP_2 than the ANPC HBST with ICS during the rising edge of $v_{x,1}$; cf. Figures 3h and 5j. In summary, the ANPC HBST with ICS achieved the highest efficiency for $dt_\downarrow = 200\,\text{ps}$ overall; for $dt_\downarrow < 200\,\text{ps}$, the efficiency decreased due to increasing turn-on losses (during $t_1 < t < t_2$ in Figure 5) and for $dt_\downarrow > 200\,\text{ps}$ due to increased conduction losses during the dead time.

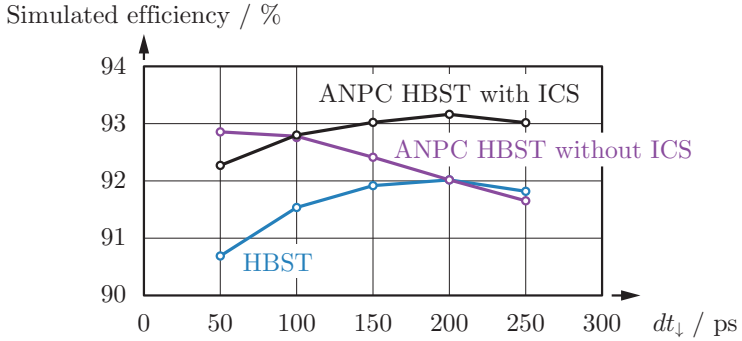

Figure 6. Efficiencies obtained from Cadence simulations for the specifications listed in Table 1, $D = 0.5$, $I_{x,1} = 250\,\text{mA}$, $f_{sw} = 150\,\text{MHz}$, $dt_\uparrow = 40\,\text{ps}$, and variable dead time $dt_\downarrow$. Adapted from [20]. Copyright © 2017 by IEEE. Adapted with permission.

3. Realized IVR

The realized hardware demonstrator was a four-phase IVR, which was comprised of the Power Management IC (PMIC) that was bonded to a PCB. Figure 7a shows a picture of the hardware demonstrator. The PCB contains the PMIC, four discrete output inductors (one PFL1005-36NMR device, manufactured by Coilcraft, for each converter phase), and additional buffer capacitors. The PMIC contains four power stages, all gate drivers (each gate driver consists of a three-stage gate driver circuit, as explained in [6]), a high-frequency digital PWM, a configurable load resistor that emulates the power dissipation of a microprocessor, and limited internal buffer capacitances to stabilize the voltages at the input terminal (V_{in}) and the mid-point terminal (V_m), both with respect to the ground. Figure 7b

depicts the chip layout of the power stage of one converter phase. The Front-End-Of-Line (FEOL) area of the HB is 0.0081 mm^2. The switching frequency, f_{sw}, can be adjusted between 50 MHz and 150 MHz. A detailed explanation of the realized demonstrator was given in [6].

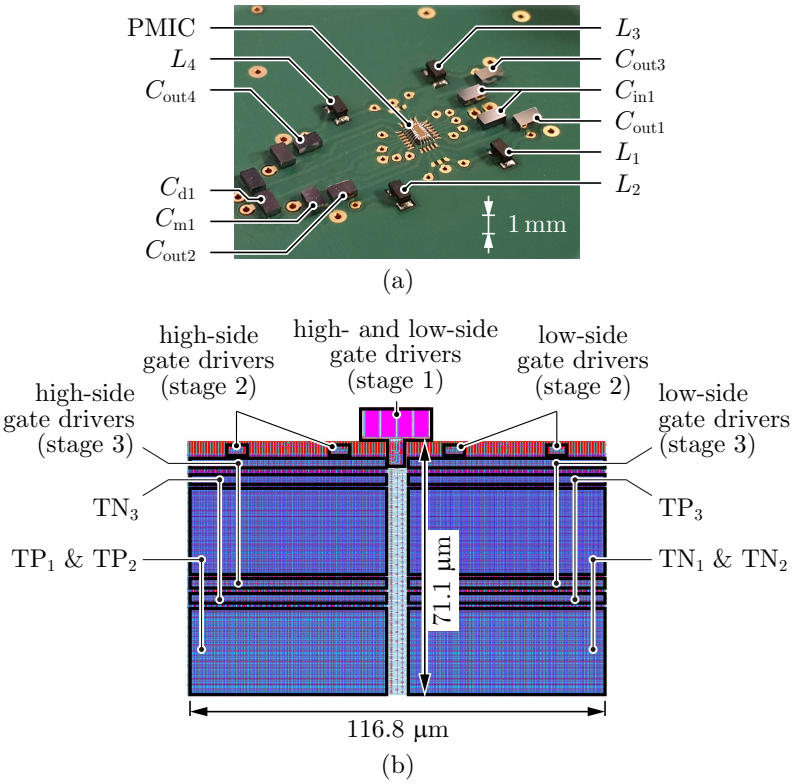

Figure 7. (**a**) Picture of the PCB-based hardware demonstrator. (**b**) Layout of the designed CMOS ANPC HBST with ICS; cf. Figure 1c. Adapted from [6].

Figure 8 depicts the functional blocks that generate the gate signals for the power transistors, i.e., the digital PWM unit (Figure 8a), configurable dead time generation units (Figure 8b), and gate signal multiplexers (Figure 8c). The circuitries shown in Figure 8b,c were separately implemented for each converter phase. The PWM unit receives the input clock from the clock signal ck_{in} and generates a PWM signal, ck, that features 16 discrete duty cycles. The output of the PWM unit is connected to the configurable delay block, which realizes the phase-shifted gate signals $ck_{\{1,2,3,4\}}$, in order to enable interleaving. Each dead time generation unit uses one output signal of the configurable delay block, e.g., ck_1 in the case of Converter Phase 1, to generate the gate signals depicted in Figure 8a and includes an output enable logic that is controlled by en_1 to allow for the deactivation of selected converter phases (phase shedding). Two four-bit values, which represent $dt_{\uparrow}$ and $dt_{\downarrow}$, are used to configure the respective dead times. Finally, the multiplexer circuit employs the two-bit configuration signal *cfg_out* to configure how the gate signals for the clamp switches are generated. With this, the three investigated topologies can be emulated: HBST (Position 1), ANPC HBST (Position 2), and ANPC HBST with ICS (Position 3).

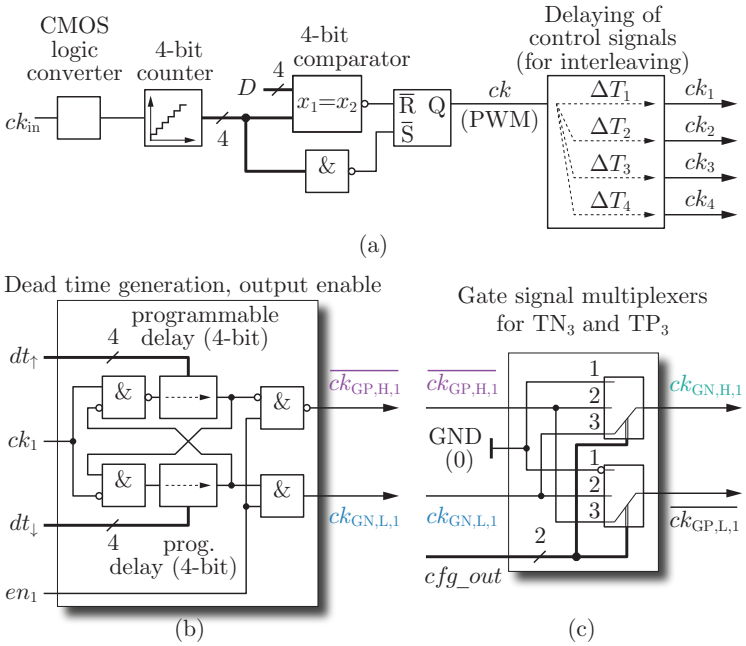

Figure 8. Digital control signal generation unit for all 4 converter phases. (**a**) Digital Pulse Width Modulator (PWM) unit and configurable delay block. (**b**) Configurable dead time generation unit and output-side enable function for the example of Phase 1. (**c**) Multiplexers for the gate signals of TN_3 and TP_3 (Phase 1).

4. Experimental Results

4.1. Experimental Setup

The experimental setup used to measure the efficiency of the first converter phase of the four-phase IVR is shown in Figure 9. All currents and voltages were measured with a precision data acquisition unit (34,970 by Keysight). The chip provides a Kelvin-pad at the input ($V_{in,k}$ in Figure 9) that allows for a measurement of the chip-internal input voltage, i.e., without the voltage drops on the input-side bond wire and PCB tracks. Accordingly, the voltage between $V_{in,k}$ and ground (gnd) estimates the voltage across the half-bridge more accurately than the voltage between $V_{in,p}$ and gnd. Reference [6] gave a detailed description of this measurement setup.

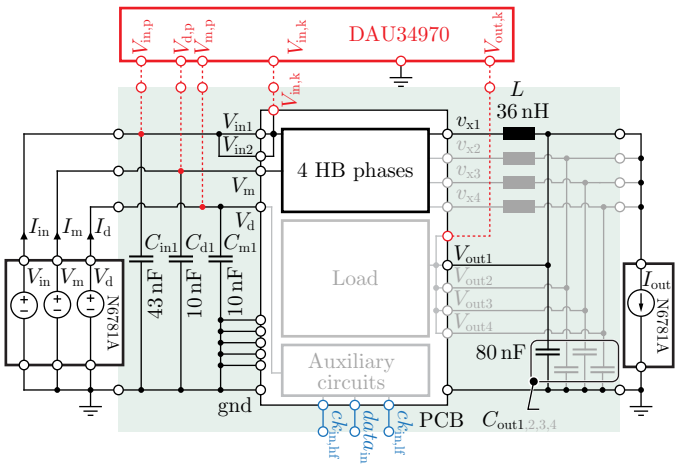

Figure 9. Experimental setup used for the efficiency measurement. Adapted from [6].

4.2. Output Voltage Characteristic

The measured ratios of the output voltage-to-input voltage,

$$M_{\mathrm{k}} = \frac{V_{\mathrm{out,k}}}{V_{\mathrm{in,k}}}, \tag{1}$$

for the HBST and the ANPC HBST with ICS at f_{sw} = 150 MHz are depicted in Figure 10. In most operating regions, $M_{\mathrm{k}}(D, I_{\mathrm{out}})$ is proportional to the duty cycle, D. However, at an output current of I_{out} = 260 mA, M_{k} of the HBST is non-linear for $D \in [50\%, 80\%]$, which is similar to the result obtained in [24]. This is presumably due to an unstable chip-internal supply voltage of the HB and was solved in [24] by using a capacitive interposer that reduces the parasitic inductances between on-chip and off-chip buffer capacitances. The ANPC HBST with ICS is more robust in this regard, i.e., M_{k} remains proportional to D, since the clamp switch TP_3 can take over a part of the excess current in the commutation loop during the rising edge of the switched voltage, $v_{\mathrm{x},1}$; cf. Figure 3f (HBST) and Figure 3g (the peak of $i_{\mathrm{d,TP2}}$ decreases from 3.2 A to 2.5 A). This leads to a reduction of the current peaks in the on-chip input capacitor that is connected between $V_{\mathrm{in1,2}}$ and ground.

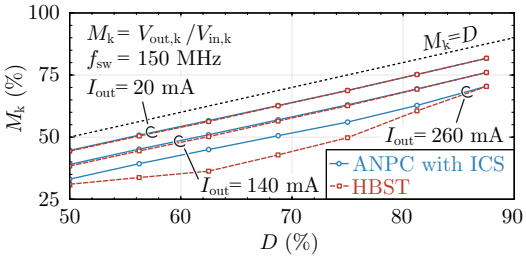

Figure 10. Measured conversion ratio, M_{k}, of the PCB-attached IVR (f_{sw} = 150 MHz).

4.3. Impact of Dead Time on Efficiency

The characteristics of the converter efficiencies with respect to the dead times $dt_{\downarrow}$ and $dt_{\uparrow}$ are shown in Figure 11a,b, respectively. The general characteristics depicted in Figure 11a are similar to the simulated characteristics shown in Figure 6; however, the absolute values of the measured efficiencies are substantially lower, due to the additional conduction losses in the PDN and the metal layers of the chip. These relatively high conduction losses are inherent to the employed 14 nm CMOS technology, since PDN and metal layers use very thin conductors [6]. With regard to a falling edge of $v_{\mathrm{x},1}$, maximum efficiency is obtained for $dt_{\downarrow} = dt_{\downarrow,\mathrm{opt}}$. For a rising edge, the minimum possible dead time leads to the highest efficiency, since any increase of $dt_{\uparrow}$ increases the conduction losses during the dead time. The standard ANPC HBST (without ICS) achieves only a comparably low maximum efficiency. For this reason, the efficiency evaluation given in the next subsection considers only the HBST and the ANPC HBST with ICS.

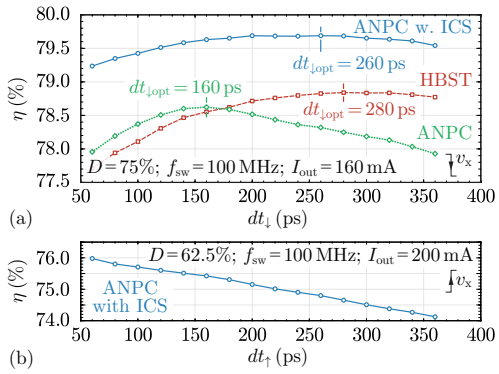

Figure 11. Impact of dead times on efficiency. (**a**) Efficiencies of the considered topologies for different dead times during the falling edge of $v_{\mathrm{x},1}$ and (**b**) during the rising edge of $v_{\mathrm{x},1}$.

4.4. Efficiency Results

The efficiencies measured for optimal dead times, different input-to-output voltage ratios,

$$M = \frac{V_{\text{out,k}}}{V_{\text{in,p}}} = \{0.5, 0.7\}, \tag{2}$$

and for $f_{\text{sw}} = \{50\,\text{MHz}, 150\,\text{MHz}\}$ are presented in Figure 12. (Reference [6] described how the measurement uncertainties shown in Figure 12 were calculated.) Due to the internal resistances of the IVR, the output voltage decreases with increasing output current. Furthermore, the duty cycle is subject to 16 discrete values, as explained in Section 3. Accordingly, steps are observed in the measured efficiencies whenever the duty cycle is changed in order to adjust the output voltage such that the output voltage remains within a certain tolerance band. For example, the duty cycle is increased from 12/16 to 13/16 if I_{out} is increased from 260 mA to 280 mA at $M = 0.7$ in Figure 12a.

A single converter phase achieves a peak efficiency of 83.7% at f_{sw} = 50 MHz and I_{out} = 160 mA. The efficiency could be improved with advanced packaging technologies, e.g., flip-chip bonding of the chip to an interposer that contains the inductors and the capacitors. At high output currents, the results reveal a higher efficiency for the ANPC HBST with ICS, which indicates a possible relation between an increase of the losses of the HBST and the non-linear dependency of the output voltage on the duty cycle at high output currents; cf. Figure 10. The efficiency increases by up to 3% in the case of $M = 0.5$ and $f_{\text{sw}} = 50\,\text{MHz}$ and by up to 7% for $M = 0.5$ and $f_{\text{sw}} = 150\,\text{MHz}$.

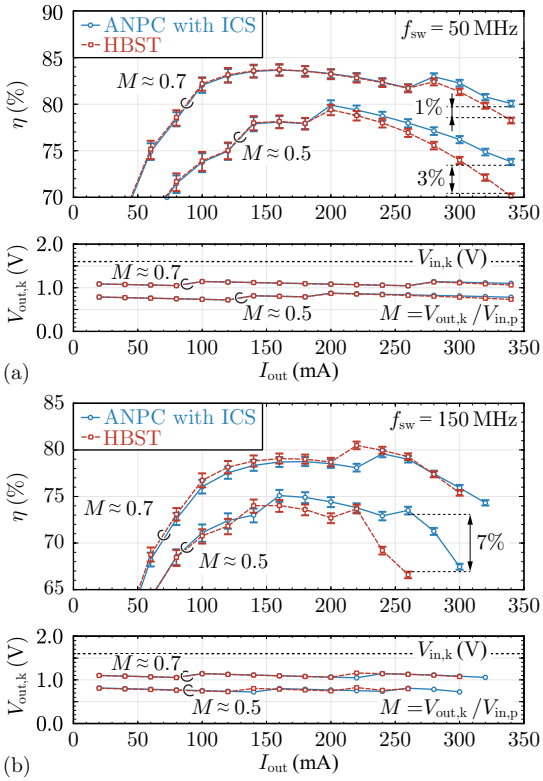

Figure 12. Measured efficiencies and output voltages of the PCB-attached IVR: (**a**) $f_{\text{sw}} = 50\,\text{MHz}$, (**b**) $f_{\text{sw}} = 150\,\text{MHz}$.

Finally, the measured efficiency with phase-shedding is depicted in Figure 13 for the ANPC HBST with ICS and a total output current that ranges from zero to 780 mA ($V_{\text{in}} = 1.6\,\text{V}$, $M \approx 0.7$ and $f_{\text{sw}} = 50\,\text{MHz}$ apply; the observed steps in the efficiency are related to the change of the discrete duty cycle to maintain $M \approx 0.7$). (Reference [6] described how the measurement uncertainties shown in Figure 13 were calculated.) The

result reveals the great efficiency improvements that are feasible with phase shedding if the IVR is operated at reduced output power levels. By way of example, at $I_{out} = 140\,mA$, the efficiency increases from 72% (four active converter phases) to 80% (two active phases) to 83.4% if only a single converter phase is active. The maximum achieved efficiency is 85.3% for two active phases, and $I_{out} = 300\,mA$; at a maximum output current of 780 mA, the efficiency is 83.1% (for all four phases being active).

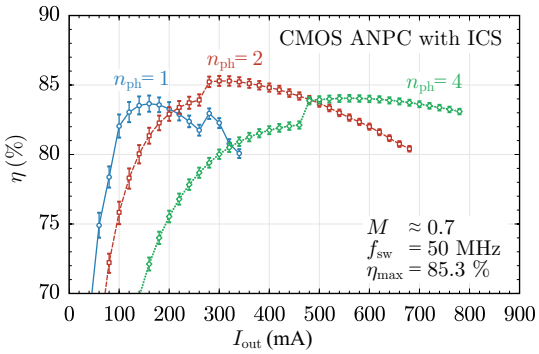

Figure 13. Efficiencies measured for the ANPC HBST with ICS topology for one, two, or four phases being operational ($V_{in} = 1.6\,V$, $M \approx 0.7$, $f_{sw} = 50\,MHz$).

5. Discussion

The footprint area of the Power Management IC (PMIC) of the investigated IVR is comparably small, which enables a very high current density of $24.7\,A/mm^2$. (In this paper, the current density of the PMIC was defined as the maximum output current of the IVR divided by the area of the enabled power switches, gate drivers, and level shifters.) In comparison, the realization presented in [14], which is also based on a 14 nm CMOS technology and operates the buck converter in discontinuous conduction mode, reveals a current density of approximately $10\,A/mm^2$ (estimated based on Figure 8.5.7 in [14]).

The maximum achieved efficiency of 85.3% is in a similar range as the efficiencies achieved in [11,12,14] (84% for 1.5 V:1.15 and $f_{sw} = 100\,MHz$ in [11], 80% for 1.2 V:0.93 V and $f_{sw} = 90\,MHz$ in [12], and 88% for 1.6 V:1.2 V and $f_{sw} = 70\,MHz$ in [14]). The decreased efficiency values are due to substantial conduction losses in the thin conductors of the metal layers and the power distribution network of the 14 nm CMOS technology node [6]. Accordingly, IVRs realized in more mature CMOS technology nodes can achieve higher maximum efficiencies, e.g., in [25], a peak efficiency of 91.5% was reported for an IVR realized in a 40 nm technology (3.3 V:2.4 V, $f_{sw} = 100\,MHz$). Conversely, the interconnects in CMOS nodes with higher integration levels, e.g., 7 nm, will be even thinner and, thus, more prone to generate even higher conduction losses. For this reason, future research is expected to increasingly address alternative realizations of the IVR's PMIC that are not directly integrated into the die of the microprocessor, e.g., 3D realizations as presented in [26].

6. Conclusions

This paper presented an experimental evaluation of chip-integrated HBST, ANPC HBST, and ANPC HBST with ICS topologies, using a high-end 14 nm CMOS technology. Compared to the conventional HBST, the ANPC HBST topologies guarantee the same voltages across the stacked transistors. The standard ANPC HBST is subject to increased switching losses and is less suitable for a multi-phase converter (no phase shedding possible). The ANPC HBST with ICS eliminates the shortcomings of the standard ANPC HBST. Compared to the HBST, it requires 14% more chip area; in return, it is more robust and achieves a higher efficiency at high output currents.

Author Contributions: Conceptualization, P.A.M.B.; methodology, P.A.M.B.; software, R.K.-A., S.P., R.H., P.A.F., T.M., M.A.K., and M.B.; validation, P.A.M.B., F.K., R.K.-A., S.P., and R.H.; formal analysis, P.A.M.B.; investigation, P.A.M.B.; resources, T.B., P.A.F., and T.M.; writing—original draft preparation, P.A.M.B.; writing—review and editing, F.K. and J.W.K.; supervision, J.W.K.; project administration, T.B.; funding acquisition, T.B. All authors read and agreed to the published version of the manuscript.

Funding: Part of this work was carried out within the European CarrICool Project under the Seventh Framework Program for Research and Technological Development (FP7-ICT-619488).

Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available due to internal policies of the industry research partner.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Tam, S.M.; Muljono, H.; Huang, M.; Iyer, S.; Royneogi, K.; Satti, N.; Qureshi, R.; Chen, W.; Wang, T.; Hsieh, H.; et al. SkyLake-SP: A 14 nm 28-core Xeon R processor. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 34–36.
2. Berry, C.; Bell, B.; Jatkowski, A.; Surprise, J.; Isakson, J.; Geva, O.; Deskin, B.; Cichanowski, M.; Hamid, D.; Cavitt, C.; et al. IBM z15: A 12-core 5.2 GHz microprocessor. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 54–56.
3. Lopez-Novoa, U. Exploring performance and energy consumption differences between recent Intel processors. In Proceedings of the IEEE SmartWorld, Ubiquitous Intelligence & Computing, Advanced & Trusted Computing, Scalable Computing & Communications, Cloud & Big Data Computing, Internet of People and Smart City Innovation (SmartWorld/SCALCOM/UIC/ATC/CBDCom/IOP/SCI), Leicester, UK, 19–23 August 2019; pp. 263–267.
4. Kim, W.; Gupta, M.S.; Wei, G.-Y.; Brooks, D. System level analysis of fast, per-core DVFS using on-chip switching regulators. In Proceedings of the IEEE International Symposium on High Performance Computer Architecture (HPCA), Salt Lake City, UT, USA, 16–20 February 2008; pp. 123–134.
5. Cheng, C.-H. Using a voltage domain programmable technique for low-power management cell-based design. *J. Low Power Electron. Appl.* **2011**, *1*, 303–326.
6. Bezerra, P.A.M.; Krismer, F.; Kolar, J.W.; Aljameh, R.K.; Paredes, S.; Heller, R.; Brunschwiler, T.; Francese, P.A.; Morf, T.; Kossel, M.A.; et al. Electrical and thermal characterization of an inductor-based ANPC-type buck converter in 14 nm CMOS technology for microprocessor applications. *IEEE Open J. Power Electron.* **2020**, *1*, 456–468.
7. Jeon, H.; Kim, K.K.; Kim, Y.-B. Fully integrated on-chip switched DC-DC converter for battery-powered mixed-signal SoCs. *Symmetry* **2017**, *9*, 18.
8. Lee, J.-Y.; Kim, G.-S.; Oh, K.-I.; Baek, D. Fully integrated low-ripple switched-capacitor DC–DC converter with parallel low-dropout regulator. *Electronics* **2019**, *8*, 98.
9. Choi, M.; Jeong, D.-K. Design of soft-switching hybrid DC-DC converter with 2-phase switched capacitor and 0.8 nH inductor for standard CMOS process. *Electronics* **2020**, *9*, 372.
10. Lambert, W.J.; Hill, M.J.; Radhakrishnan, K.; Wojewoda, L.; Augustine, A.E. Package inductors for intel fully integrated voltage regulators. *IEEE Trans. Components Packag. Manuf. Technol.* **2016**, *6*, 3–11.
11. Krishnamurthy, H.K.; Weng, S.; Matthew, G.E.; Saraswat, R.; Ravichandran, K.; Tschanz, J.; De, V. A digitally controlled fully integrated voltage regulator with on-die solenoid inductor with planar magnetic core in 14 nm tri-gate CMOS. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 336–338.
12. Krishnamurthy, H.K.; Vaidya, V.; Kumar, P.; Jain, R.; Weng, S.; Kim, S.T.; Matthew, G.E.; Desai, N.; Liu, X.; Ravichandran, K. A digitally controlled fully integrated voltage regulator with 3-D-TSV-based on-die solenoid inductor with a planar magnetic core for 3-D-stacked die applications in 14-nm tri-gate CMOS. *IEEE J. Solid-State Circuits* **2018**, *53*, 1038–1048.
13. Burton, E.A.; Schrom, G.; Paillet, F.; Douglas, J.; Lambert, W.J.; Radhakrishnan, K.; Hill, M.J. FIVR—Fully integrated voltage regulators on 4th generation Intel© Core™ SoCs. In Proceedings of the IEEE Applied Power Electronics Conference (APEC), Houston, TX, USA, 16–20 March 2014; pp. 432–439.
14. Schaef, C.; Desai, N.; Krishnamurthy, H.; Weng, S.; Do, H.; Lambert, W.; Radhakrishnan, K.; Ravichandran, K.; Tschanz, J.; De, V. A fully integrated voltage regulator in 14nm CMOS with package-embedded air-core inductor featuring self-trimmed, digitally controlled variable on-time discontinuous conduction mode operation. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 17–21 February 2019; pp. 154–156.
15. Baek, J.; Lee, H.-M.; Shin, S.-U. Triple-mode switched-inductor-capacitor DC-DC buck converter with reusable flying capacitor and bang-bang zero-current detector for wide load current range. *Electronics* **2020**, *9*, 1202.
16. Neveu, F.; Martin, C.; Allard, B.; Bevilacqua, P.; Voiron, F. Design of a highly integrated, high frequency, low power DC-DC converter with cascode power stage with a 2.5D approach. In Proceedings of the International Conference on Integrated Power Electronics Systems (CIPS), Nuremberg, Germany, 8–10 March 2016.

17. Haj-Yahya, J.; Rotem, E.; Mendelson, A.; Chattopadhyay, A. A comprehensive evaluation of power delivery schemes for modern microprocessors. In Proceedings of the International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, 6–7 March 2019; pp. 123–130.
18. Kursun, V.; Schrom, G.; De, V.K.; Friedman, E.G.; Narendra, S.G. Cascode buffer for monolithic voltage conversion operating at high input supply voltages. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCS), Kobes, Japan, 23–26 May 2005; pp. 464–467.
19. Nalamalpu, A.; Kurd, N.; Deval, A.; Mozak, C.; Douglas, J.; Khanna, A.; Paillet, F.; Schrom, G.; Phelps, B. Broadwell: A family of IA 14nm processors. In Proceedings of the IEEE Symposium on VLSI Circuits (VLSI), Kyoto, Japan, 17–19 June 2015; pp. C314–C315.
20. Bezerra, P.A.M.; Aljameh, R.K.; Krismer, F.; Kolar, J.W.; Sridhar, A.; Brunschwiler, T.; Toifl, T. Analysis and Comparative Evaluation of Stacked Transistor Half-bridge Topologies Implemented with 14 nm Bulk CMOS Technology. In Proceedings of the IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), Padova, Italy, 25–28 July 2017.
21. Page, S.; Wajda, A.; Hess, H. High voltage tolerant stacked MOSFET in a buck converter application. In Proceedings of the IEEE Workshop on Microelectronics and Electron Devices (WMED), Boise, ID, USA, 20 April 2012; pp. 37–40.
22. Michal, V. Optimal peak-efficiency control of the CMOS interleaved multi-phase step-down DC-DC converter with segmented power stage. *IET Power Electron.* **2016**, *9*, 2223–2228.
23. Brunschwiler, T.; Schlottig, G.; Sridhar, A.; Bezerra, P.; Ruch, P.; Ebejer, N.; Oppermann, H.; Kleff, J.; Steller, W.; Jatlaoui, M.; et al. Towards cube-sized compute nodes: advanced packaging concepts enabling extreme 3D integration. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 3.7.1–3.7.4.
24. Neveu, F. Design and Implementation of High Frequency 3D DC-DC Converter. Ph.D. Thesis, Institut National des Sciences Appliquées, Lyon, France, December 2015.
25. Neveu, F.; Allard, B.; Martin, C.; Bevilacqua, P. A 100 MHz 91.5% peak efficiency integrated buck converter with a three-MOSFET cascode bridge. *IEEE Trans. Power Electron.* **2016**, *31*, 3985–3988.
26. Vivet, P.; Guthmuller, E.; Thonnart, Y.; Pillonnet, G.; Moritz, G.; Miro-Panadès, I.; Fuguet, C.; Durupt, J.; Bernard, C.; Varreau, D.; et al. A 220 GOPS 96-core processor with 6 chiplets 3d-stacked on an active interposer offering 0.6 ns/mm latency, 3 Tb/s/mm^2 inter-chiplet interconnects and 156 mW/mm^2 @ 82%-peak-efficiency dc-dc converters. In Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 46–48.