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***Abstract*—Solid-State Transformers (SSTs) are considered important building blocks of a future Smart Grid, where they will replace conventional transformers and provide enhanced functionality and controllability. To deal with the medium-voltage levels at the input of an SST for distribution applications, commonly cascaded cells converter topologies are proposed. This paper presents a detailed analysis of the common-mode currents appearing in cascaded cells converter systems as a consequence of steep changes of the cells' potentials caused by the individual cells' switching actions. Common-mode chokes placed at the AC terminals of each individual cell are identified as the most feasible way of mitigating these common-mode current disturbances. Detailed, analytic design guidelines are provided and applied to a 1 MVA, 10 kV/400 V SST.**

***Keywords*—Cascaded Cells Converters, Common-Mode Currents, Multilevel Converters, Solid-State Transformers.**

I. Introduction

With the increasing need of substituting conventional energy sources such as fossil fuel and nuclear fission by renewables, which often involves geographical dispersion of the power sources, completely new demands on the future power grid, especially on the distribution level, arise. These can be summarized in the requirement that the grid needs to transition towards a so-called "smart-grid", which allows for a precise distributed control of sources, loads, voltage levels and power flows. However, such functionality cannot be provided by passive components such as line-frequency transformers, which are ubiquitous in today's distribution grids. While power electronic equipment is used to, at least partly, overcome the limits of passive transformers, e. g., with FACTS or STATCOM devices, complete power electronic replacements could integrate higher functionality and therefore offer much more flexibility.

Solid-State Transformers (SSTs) are such power electronic systems that could replace line-frequency transformers at the interfaces between medium-voltage (MV) and low-voltage (LV) levels. An SST interfaces either grid by means of a combination of power electronic converter systems, provides galvanic isolation using medium-frequency (MF) transformers and, most prominently, enables control of the active power flows of the phases, independent reactive power compensation on both sides, active filtering of harmonics, and features a LV DC bus to interface energy storage systems or a local DC distribution infrastructure, etc. The first patent of an "electronic transformer" has been issued already in 1970 [1], however, only in recent years the concept has been scaled up to higher voltage and power ratings for grid [2]–[6] and traction applications [7]–[10].

TABLE I
Specifications of the considered SST.

Rated power	1 MVA
MV grid voltage (line-line, rms)	10 kV
LV grid voltage (line-line, rms)	400 V
Cell rectifier stage switching frequency	1 kHz
Cell MV DC link voltage	2×1100 V
Cell LV DC link voltage	800 V

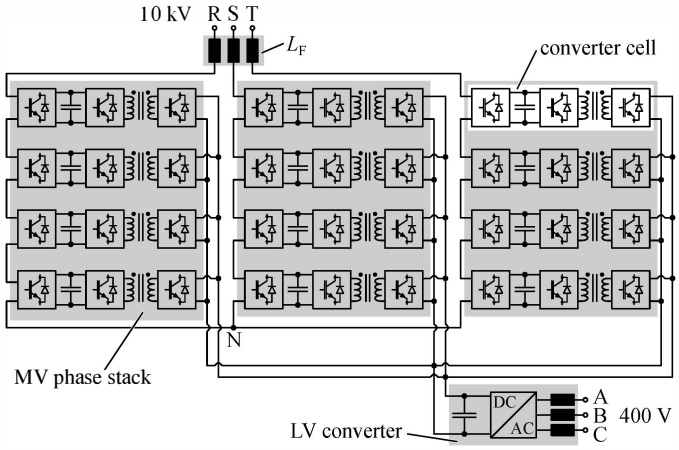

Fig. 1. Overview on the considered SST topology.

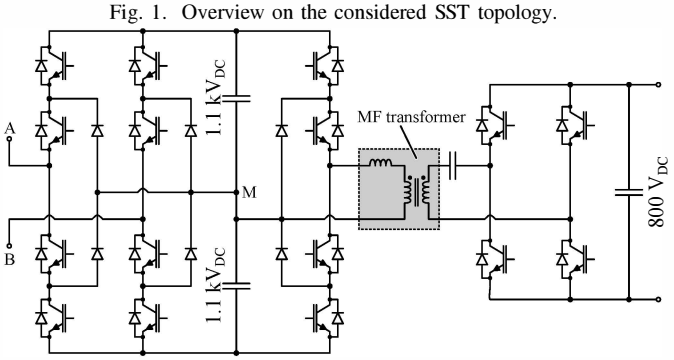

Fig. 2. Power circuit of a single MVAC-LVDC converter cell.

Since the blocking voltage ratings of today's power semiconductors are limited, usually cascaded converter systems are used to interface the MV grid. The choice of the blocking voltage and hence the number of cascaded cells is an important design parameter. For the voltage and power ratings considered here (cf. Table I), it has been shown that systems based on low-voltage power devices, i. e., 1700 V IGBTs, are Pareto-optimal regarding efficiency and power density [11]. Fig. 1 shows a corresponding example SST system, which employs

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four cascaded cells per phase on its MV side and Fig. 2 shows the power circuit of a single cell, consisting of a single-phase neutral-point-clamped (NPC) rectifier stage and an isolated, resonant DC/DC converter [12].

While there are many publications dealing with the reduction of common-mode voltages at the cascaded cells converter's output, which is important for, e. g., drive systems, by means of special modulation schemes [13]–[15], so far only a single paper discusses another common-mode-related phenomenon inherent to cascaded cells converter systems [16]: the potential of a cascaded cell's MV side with respect to ground cannot be fixed, instead it changes during every switching transition of any subjacent cell in the same phase stack. Each cell, however, has a certain capacitance to ground arising from, e. g., transformer windings, heatsinks, etc., that needs to be charged or discharged for the cell's midpoint potential to change, which gives rise to common-mode currents. Furthermore, it has been shown that severe oscillations between these parasitic ground capacitances and parasitic inductances of the cell interconnections can occur [16].

This paper provides a more detailed analysis of the phenomenon in Sections II and III, and discusses mitigation means in Section IV, where also comprehensive design guidelines for the most promising solution, i. e., common-mode chokes at each cell's AC terminals, are given.

II. Common-Mode Equivalent Circuit

In this and the next section, an analytical description of the common-mode currents arising in the cascaded cells converter is presented, where the analysis confines to a single phase without loss of generality, since the star point, N, is assumed to be solidly grounded. To start, suitable equivalent circuits are derived.

A. Common-Mode Equivalent Circuit of a Converter Cell

A single converter cell's power circuit as shown in Fig. 2 can be simplified for common-mode analysis purposes, as for example suggested in [13]. To do so, the MV side switches and DC link capacitors are replaced by stepped voltage sources with amplitude $V_{\mathrm{dc}} = 1100\,\mathrm{V}$ (corresponding to one half of the total MV side DC link voltage), which results in the equivalent circuit shown in Fig. 3(a). The grayed-out capacitances, $C_{\mathrm{sc,I}}$ and $C_{\mathrm{sc,D}}$, represent capacitances between semiconductor dies and the heatsink, which is connected to the MV side midpoint, M. Any switching causes "local" common-mode currents through these capacitances. However, these currents flow only within a single cell and are no different from those present in any switching power converter. Therefore, these "local" common-mode currents are not considered further.

In contrast, any switching of the voltage source v_{B}, or of any other voltage source subjacent in the phase stack, will move the potential of the cell midpoint, M, with respect to ground. This will give rise to a current flow through the capacitance between the transformer winding (note that one end of the MV winding is connected to the midpoint) and ground, C_{T}, as well as through C_{HS}, the capacitance between the cell structures on

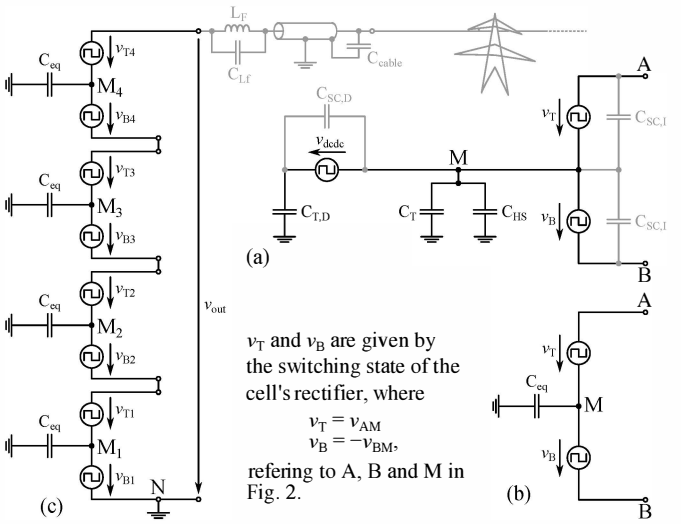

Fig. 3. Common-mode equivalent circuit of the converter cell shown in Fig. 2, including "local" common-mode effects and the DC/DC converter (a), reduced version suitable for the analysis of "global" common-mode effects (b), and corresponding common-mode equivalent circuit of a complete phase stack (c).

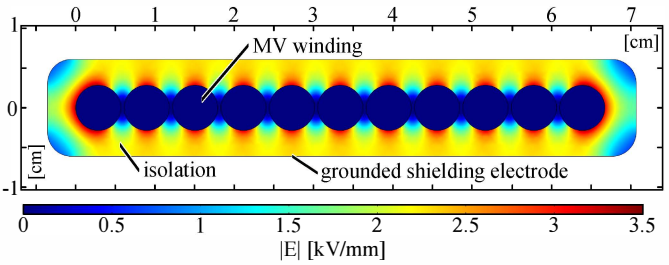

Fig. 4. Electrostatic FEM simulation of the transformer MV winding.

midpoint potential, such as the heatsink, and adjacent grounded parts such as cabinet walls. Additionally, also the switching of the DC/DC converter, represented by v_{dcdc}, causes common-mode currents through the capacitance between the transformer winding and ground, $C_{\mathrm{T,D}}$. However, these are independent of the cell's position in the phase stack and therefore non-specific to cascaded cells systems; thus the DC/DC converter is not considered any further. Applying these simplifications yields the common-mode equivalent circuit of one converter cell as shown in Fig. 3(b), where C_{eq} summarizes C_{T} and C_{HS}.

Due to the close geometric proximity of the MV winding on cell potential and grounded parts such as the core, which is mandatory to achieve good magnetic and thermal performance of the MF transformer, C_{T} can be assumed to dominate C_{eq}. Finite element simulation has been used to determine the parasitic capacitance of a transformer designed for the system under consideration. Fig. 4 shows the corresponding electric field distribution, from which $C_{\mathrm{eq}} \approx C_{\mathrm{T}} = 650\,\mathrm{pF}$ is obtained.

B. Common-Mode Equivalent Circuit of a Phase Stack

Fig. 3(c) finally shows the common-mode equivalent circuit of a complete SST phase stack. The neutral point, N, is assumed to be solidly grounded, or at least directly connected to the aforementioned structures such as cabinet walls or transformer cores. In this second case, no direct ground connection of the star point would be required, however, for safety reasons the voltage between N and ground would have to be kept small

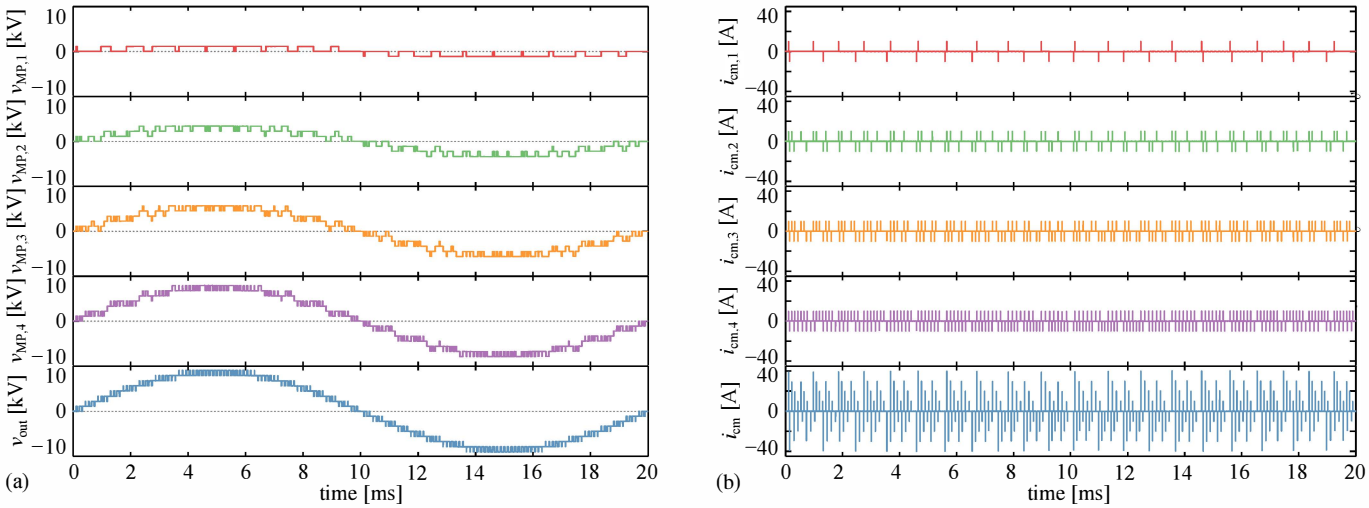

Fig. 5. Full-system simulation results for one SST phase. (a) shows the voltages between the cell midpoints and ground as well as the total phase stack output voltage, v_{out}, and (b) shows the corresponding common-mode currents flowing through the cell's parastitic capacitances to ground, and also the total common-mode current, i_{cm}, flowing back through the node N.

by suitable means.

Note that, in addition to C_{eq}, there is also a capacitive path to ground from the phase terminal via the parasitic capacitance of the filter inductor and the cable capacitance of a possibly connected MV cable. However, while these capacitances might be in the same order of magnitude as C_{eq} and need to be charged or discharged at every switching of any converter cell, the corresponding current spikes do not appear as common-mode current inside the converter structure, but only as a minor addition to the load current.

III. Analytical Description of Common-Mode Currents

The idealized equivalent circuit (not considering any parasitic inductances) depicted in Fig. 3(c) is now used to derive a basic analytic description of the common-mode currents flowing in the system.

The power semiconductors are impressing a high dv/dt during their switching transitions, $dv/dt = 15\,\mathrm{kV/\mu s}$ being a typical value for the IGBTs considered here. Assuming a constant dv/dt, the corresponding charging current for a cell's parasitic capacitance is given as

$$\hat{I}_{\mathrm{cm}} = C_{\mathrm{eq}} \frac{dv}{dt}. \tag{1}$$

A constant current with this magnitude flows until the capacitor is charged to the new voltage level. The current spike is therefore rectangular with magnitude $\hat{I}_{\mathrm{cm}}$ and a duration of

$$\Delta t = \frac{V_{\mathrm{dc}}}{\frac{dv}{dt}}, \tag{2}$$

where $V_{\mathrm{dc}} = 1100\,\mathrm{V}$, which is the voltage change resulting from any switching transition.

Consider now a cell at position k in the stack, where $1 \leq k \leq 4$ in the example system. If the voltage source $v_{\mathrm{B,k}}$ or the voltage source $v_{\mathrm{T,(k-1)}}$ is changing its voltage value as a result of corresponding switching actions, the midpoint potentials of cell k and of all cells at positions $l > k$ will change, requiring a current flow through their respective common-mode capacitances as described above.

Using PWM with phase-shifted carriers creates the desired multilevel output voltage waveform but implies that all cells are continuously switching with the same frequency, f_{s}. Thus, the higher a cell is positioned in the stack, the more common-mode current pulses it experiences per time.

A. RMS Common-Mode Current of Cell k

More precisely, every voltage source shown in Fig. 3(c) switches twice during a switching period, $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$. Therefore, the midpoint of cell k experiences $2\cdot(2k-1)$ potential changes during T_{s}. The rms common-mode current flowing through the common-mode capacitance of cell k is thus given as

$$\tilde{i}_{\mathrm{cm,k}} = \sqrt{\frac{1}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}} i_{\mathrm{cm,k}}(t)^2\,dt} = \sqrt{\frac{1}{T_{\mathrm{s}}}\sum_{\mathrm{j}=1}^{(4k-2)} \Delta t \hat{I}_{\mathrm{cm}}^2}$$
$$= C_{\mathrm{eq}} \cdot \sqrt{f_{\mathrm{s}} V_{\mathrm{DC}} \frac{dv}{dt}} \cdot \sqrt{4k-2}. \tag{3}$$

Note that therefore an effective capacitance for a cell at position k in the stack could be defined as $C^*_{\mathrm{eq,k}} = C_{\mathrm{eq}} \cdot \sqrt{4k-2}$, which is increasing for cells at higher stack positions.

B. Total RMS Common-Mode Current

The common-mode currents of all cells flow back through the ground connection at node N in Fig. 3(c). The magnitude of these current pulses depends on which cell, denoted by its position in the stack, k, is switching, namely $\hat{i}_{\mathrm{cm}\leftarrow\mathrm{k}} = (N-k+1)\cdot\hat{I}_{\mathrm{cm}}$. As mentioned above, there are two switching transitions of each voltage source in the equivalent circuit during one switching period. For $k > 1$ a switching transition of $v_{\mathrm{B,k}}$ has the same effect as one of $v_{\mathrm{T,(k-1)}}$, resulting in four corresponding current pulses per switching period. Thus, the total common-mode rms current becomes

$$\tilde{i}_{\mathrm{cm}} = \sqrt{f_{\mathrm{s}} V_{\mathrm{DC}} C_{\mathrm{eq}}^2 \frac{dv}{dt} \cdot \left(2N^2 + \sum_{\mathrm{k}=2}^{N} 4\cdot(N-k+1)^2\right)}$$
$$= C_{\mathrm{eq}} \cdot \sqrt{f_{\mathrm{S}} V_{\mathrm{DC}} \frac{dv}{dt} \cdot \left(\frac{4}{3}N^3 + \frac{2}{3}N\right)}. \tag{4}$$

TABLE II
CALCULATED AND SIMULATED RMS COMMON-MODE CURRENTS.

	calc. [mA]	sim. [mA]	error [%]
cell 1	118.1	119.5	-1.17
cell 2	204.5	206.7	-1.06
cell 3	264.0	266.7	-1.01
cell 4	312.4	315.6	-1.01
total	783.2	790.9	-0.96

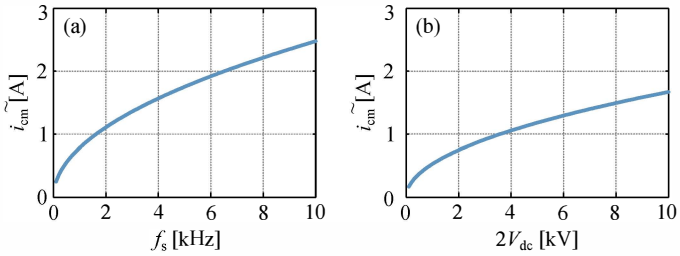

Fig. 6. Dependence of the total rms common-mode current, $\tilde{i}_{cm}$, on the cells' switching frequency, f_S, at $V_{dc} = 1.1\,kV$ (a), and on the cells' DC link voltage, V_{dc}, at $f_S = 1\,kHz$ (b).

C. Verification

A complete simulation model of a single MV phase stack, featuring four cascaded cells including the DC/DC converter stages, has been implemented in GeckoCICRUITS [17] to verify the above calculations. Note that the fixed simulation time-step has to be chosen according to (2) in order to obtain a desired dv/dt. Fig. 5(a) shows the simulated cell midpoint voltages to ground and Fig. 5(b) shows the corresponding common-mode currents. The calculated and simulated rms common-mode currents are listed in Table II, confirming the accuracy of the analytic calculations.

D. Parameter Influences

The validated analytic expressions allow to investigate the influence of certain system parameters on these common-mode currents. From (4) it can directly be seen that $\tilde{i}_{cm} \propto \sqrt{f_s}$ and $\tilde{i}_{cm} \propto \sqrt{V_{dc}}$, which is illustrated by Fig. 6. Note that if instead of a constant dv/dt a constant switching time for the voltage to rise from 0 V to V_{dc} was considered, a linear dependency, $\tilde{i}_{cm} \propto V_{dc}$, would result.

Furthermore, there is a linear dependence on the parasitic capacitance, i. e., $\tilde{i}_{cm} \propto C_{eq}$ as shown in Fig. 7. There, also the fact that the rms common-mode current increases with higher position of a cell in the stack, corresponding to increasing k, is clearly visible.

E. Influence of the Number of Cascaded Converter Cells

The choice of the optimum number of cascaded converter cells, N, for a given grid voltage level has been discussed in [11]. It is thus interesting to assess the influence of N on the common-mode current stress in the system.

It has been shown that the following relations hold for a given output filter and constant output current ripple, i. e.,

$$V_{dc} = V_{dc,0}\frac{N_0}{N} \quad \text{and} \quad f_s = f_{s,0}\frac{N_0^2}{N^2}, \tag{5}$$

where $V_{dc,0}$, $f_{s,0}$ and N_0 are the parameters of a reference cascaded cells system. Coarsely approximated, the scaling behavior of the transformer stray capacitance is as follows:

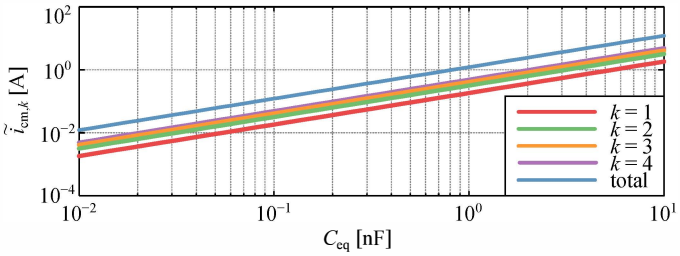

Fig. 7. Dependence of the individual cells' rms common-mode currents, $\tilde{i}_{cm,k}$, and of the total rms common-mode current, $\tilde{i}_{cm}$, on C_{eq}.

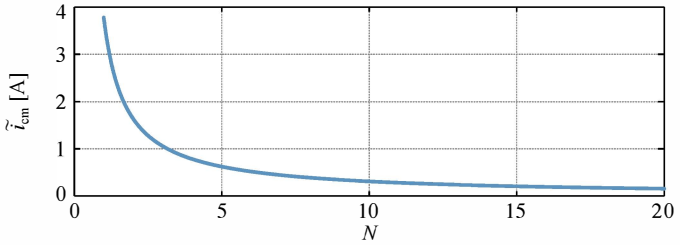

Fig. 8. Total rms common-mode current, $\tilde{i}_{cm}$, as a function of the number of cascaded converter cells, N.

the cell power scales with $1/N$, but so does the cell DC voltage, resulting in the transformer current being independent of N, i. e., the required copper cross section remains constant and the same holds for the isolation distances, essentially leaving the cross section shown in Fig. 4 unchanged, assuming an equivalent number of turns. Assuming further a constant switching frequency of the DC/DC stage, the required core area scales with $1/N$ since the applied voltage-time area does so. Consequently, the third dimension of the transformer scales with $1/N$, corresponding to an according reduction of the stray capacitance, i. e.,

$$C_{eq} = C_{eq,0}\frac{N_0}{N}. \tag{6}$$

Inserting these dependencies in (4) yields

$$\tilde{i}_{cm}(N) = \sqrt{f_S \frac{N_0^2}{N^2} V_{DC} \frac{N_0}{N} C_{eq}^2 \frac{N_0^2}{N^2} \frac{dv}{dt} \cdot \left(\frac{4}{3}N^3 + \frac{2}{3}N\right)}, \tag{7}$$

which is plotted in Fig. 8. Even though the approximations are coarse and for example a scaling of the dv/dt with the switch voltage rating is not considered, the qualitative notion that an increasing number of cascaded cells results in lower total rms common-mode current stress is very pronounced, since $\tilde{i}_{cm}(N) \propto \sqrt{N^3/N^5} \propto 1/N$.

F. Parasitic Inductances and Common-Mode Oscillations

So far, an idealized situation has been used to introduce the basic relations. However, additional parasitic elements, most prominentely series inductances of the interconnections of the cells, are present in a real system. Fig. 9(a) shows a common-mode equivalent circuit extended accordingly, where the series inductances are summarized as $L_{eq} = 100\,nH$. Severe oscillations between the parasitic common-mode capacitances and these series inductances have been described in [16]. Here, a more detailed theoretical analysis is presented.

Considering a single switching transition of the source $v_{B,3}$ from 0 V to V_{dc}, the circuit from Fig. 9(a) can be redrawn

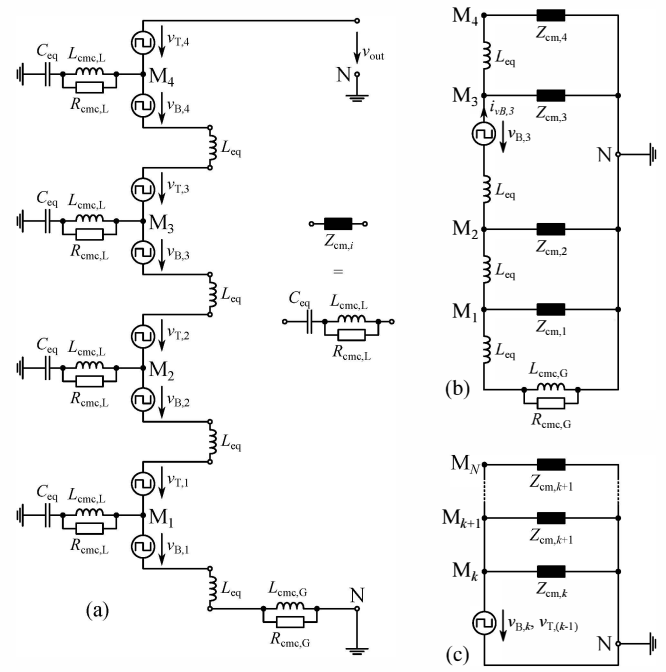

Fig. 9. (a) Common-mode equivalent circuit including parasitic inductances as well as local, i. e., per cell, common-mode chokes, $L_{\mathrm{cmc,L}}$, and a global, i. e., per phase, common-mode chocke, $L_{\mathrm{cmc,G}}$. (b) Corresponding equivalent circuit for the case of a switching transition of the equivalent source $v_{\mathrm{B},3}$. (c) Simplified and generalized equivalent cicuit suitable for designing the local common-mode chokes.

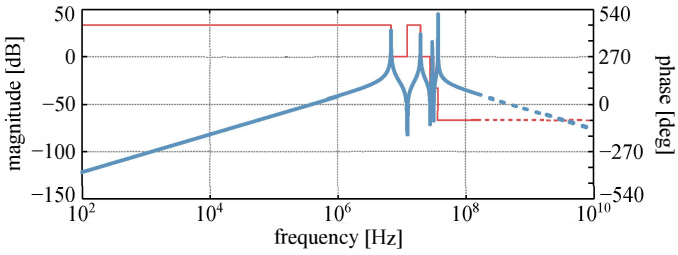

Fig. 10. Bode plot of the transfer function $G_3(s)$ for $L_{\mathrm{eq}} = 100\,\mathrm{nH}$ and without any common-mode chokes, i. e., $L_{\mathrm{cmc,G}} = L_{\mathrm{cmc,L}} = 0$.

to obtain Fig. 9(b), where for now $L_{\mathrm{cmc,L}} = L_{\mathrm{cmc,G}} = 0$ is assumed. Fig. 10 shows the Bode diagram of the transfer function

$$G_3(s) = \frac{I_{\mathrm{vB},3}(s)}{V_{\mathrm{B},3}(s)} = \frac{1}{Z_{\mathrm{T},3}(s)}, \tag{8}$$

i. e., the transfer function from the voltage step to the resulting current flow through the switching voltage source, where $Z_{\mathrm{T},3}(s)$ is the total impedance seen by the source in the circuit of Fig. 9(b), including L_{eq}. As expected, severe resonances in the MHz-range are present. Although series resistances, e. g., semiconductor on-state resistances, etc., are not considered, these are required to be small from an efficiency point-of-view and therefore the provided damping is only minor.

IV. Common-Mode Current Reduction Strategies

The analysis presented so far provides the basis to evaluate means for reducing the common-mode currents circulating in the system and to suppress the severe common-mode oscillations indicated in Fig. 10.

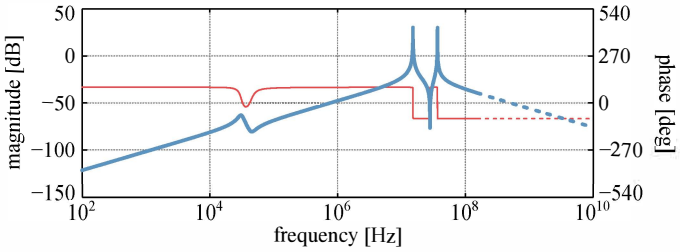

Fig. 11. Bode plot of the transfer function $G_3(s)$ for $L_{\mathrm{eq}} = 100\,\mathrm{nH}$, a global common-mode inductance of $L_{\mathrm{cmc,G}} = 10\,\mathrm{mH}$ and a parallel damping resistor of $R_{\mathrm{cmc,G}} = 10\,\mathrm{k\Omega}$.

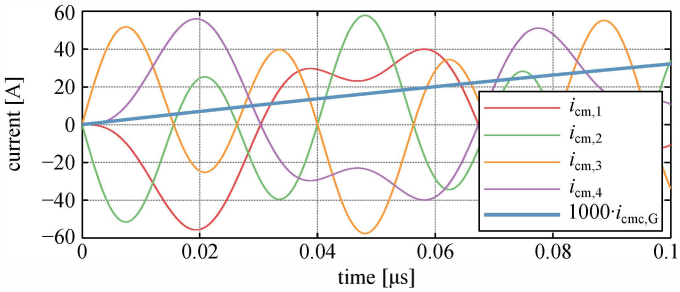

Fig. 12. Step responses of the common-mode currents, $i_{\mathrm{CM,k}}$, and the current through the common-mode impedance, $i_{\mathrm{cmc,G}}$, for $L_{\mathrm{eq}} = 100\,\mathrm{nH}$, $L_{\mathrm{cmc,G}} = 10\,\mathrm{mH}$ and $R_{\mathrm{cmc,G}} = 10\,\mathrm{k\Omega}$.

Regarding the dependency of $\tilde{i}_{\mathrm{cm}}$ on the switching frequency, an obvious solution to mitigate common-mode currents would be to reduce the switching frequency, e. g., by using other modulation methods based on fundamental switching frequency at least for most of the cells [18]. However, such measures inevitably require increased passive filtering efforts to comply with harmonic standards.

Another approach would be to use dv/dt filters, as known from drive systems and described in, e. g., [19], [20], at the outputs of the individual converter cells. The downside of such filters is their differential-mode nature, which makes them potentially quite bulky.

Therefore, the most promising third option for reducing common-mode currents in the SST, common-mode choking, is investigated closer in the following.

A. Global Common-Mode Choke

A first approach could be to place a common-mode choke (CMC) at the output terminals of the complete phase stack. Such a CMC, including a parallel damping resistor, appears in the common-mode equivalent circuit from Fig. 9(b) as $L_{\mathrm{cmc,G}}$ and $R_{\mathrm{cmc,G}}$. Fig. 11 shows the Bode plot of the accordingly adjusted transfer function $G_3(s)$. The high common-mode inductance creates a second, damped resonance at a much lower frequency, and increases the common-mode impedance at the stack output, however, it does hardly affect some of the internal high-frequency resonances occurring between the common-mode capacitances, C_{eq}, and the parasitic inductances, L_{eq}, within the phase stack, which is in accordance with the findings reported in [16].

Similar to $G_3(s)$, transfer functions from the step voltage change to the common-mode currents flowing in the parasitic capacitances, C_{eq}, can be derived and Fig. 12 shows the

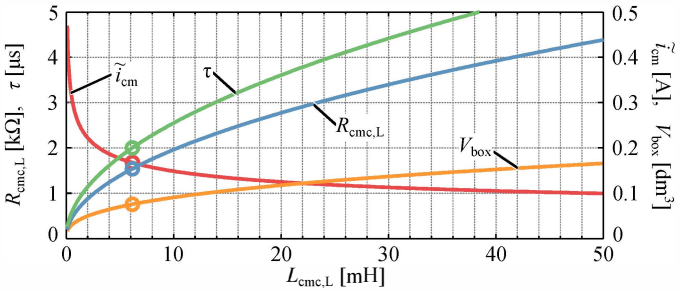

Fig. 13. Required damping resistor, $R_{\mathrm{CMC,L}}$, resulting time constant, τ, and rms common-mode current, $\tilde{i}_{\mathrm{cm}}$, as functions of $L_{\mathrm{cmc,L}}$. The estimated box volume of the CMC, V_{box}, is also shown.

corresponding step responses. As expected, nearly undamped oscillations occur, where it should be noted that the initial current flow in the common-mode capacitances of the cells residing at lower stack positions than the switching voltage source is in the negative direction, i. e., discharging these capacitances, which results in an undesired lowering of these cells' midpoint potentials. This is a result of $L_{\mathrm{cmc,G}}$ very effectively suppressing the common-mode current flowing back through node N; the only other path for the required charging current inevitably involves the common-mode impedances of those cells initially not affected by the switching.

All in all, the above shows that common-mode choking at the phase stack terminals is not a feasible solution for mitigating common-mode current flows inside an SST.

B. Local Common-Mode Chokes at Cell Inputs

Another option is to place "local" CMCs between the AC terminals of each individual cell, which appear as $L_{\mathrm{cmc,L}}$ and $R_{\mathrm{cmc,L}}$ in the equivalent circuit from Fig. 9(a). This solution has been proposed in [16], but without consideration of the components design. Therefore, a detailed design guideline is provided in the following.

1) Design Equations: The full transfer function, $G_3(s)$ given in (8), is a very complicated expression. However, since the parasitic inductances, L_{eq}, are much smaller than the common-mode inductances, $L_{\mathrm{cmc,L}}$, they can be neglected to reduce complexity and enable the derivation of straightforward design equations. In addition, no global CMC is present, which allows to reduce the equivalent circuit to that shown in Fig. 9(c), where a generalized case is shown. With these simplifications, the simplified total impedance, $Z_{\mathrm{T,s,k}}$, seen by the switching source $v_{\mathrm{B,k}}$ (or, equivalently, $v_{\mathrm{T,(k-1)}}$), is given as

$$Z_{\mathrm{T,s,k}} = \frac{Z_{\mathrm{CM}}}{N-k+1}, \text{ where}$$
$$Z_{\mathrm{CM}} = \frac{1}{sC_{\mathrm{eq}}} + \frac{R_{\mathrm{cmc,L}} \cdot sL_{\mathrm{cmc,L}}}{R_{\mathrm{cmc,L}} + sL_{\mathrm{cmc,L}}}. \tag{9}$$

The simplified transfer function from the voltage step to the total common-mode current flowing through the voltage source is thus

$$G_{\mathrm{s,k}}(s) = \frac{1}{Z_{\mathrm{T,s,k}}(s)} = \frac{(N-k+1)(s^2 C_{\mathrm{eq}} L_{\mathrm{cmc,L}} + sR_{\mathrm{cmc,L}} C_{\mathrm{eq}})}{s^2 C_{\mathrm{eq}} L_{\mathrm{cmc,L}} R_{\mathrm{cmc,L}} + sL_{\mathrm{cmc,L}} + R_{\mathrm{cmc,L}}}, \tag{10}$$

which describes a second-order system.

With respect to reducing EMI, no oscillations are desired. On the other hand, while an overdamped response features a faster decay rate, this comes at the price of higher peak current values (and thus increased rms current), since the total amount of charge that needs to be transferred is given by C_{eq} and the applied voltage step. Therefore, critical damping should be aimed at for an optimum design, which corresponds to the imaginary part of the poles of (10) being zero, i. e.,

$$L_{\mathrm{cmc,L}} = 4C_{\mathrm{eq}} R_{\mathrm{cmc,L}}^2. \tag{11}$$

Applying this condition to $G_{\mathrm{s,k}}(s)$, the response to a voltage step of source $v_{\mathrm{B,k}}$ (or $(v_{\mathrm{T,(k-1)}})$ with magnitude V_{dc} can be calculated as

$$i_{\mathrm{cm,T,k}}(t) = \frac{(N-k+1)V_{\mathrm{dc}}}{4R_{\mathrm{cmc,L}}^2 C_{\mathrm{eq}}} \left(4C_{\mathrm{eq}} R_{\mathrm{cmc,L}} - t\right) \mathrm{e}^{-\frac{t}{2C_{\mathrm{eq}} R_{\mathrm{cmc,L}}}}. \tag{12}$$

Note that the time integral of such a current pulse directly corresponds to the amount of charge required to increase the voltage of all affected, i. e., $(N-k+1)$, common-mode capacitances by V_{dc},

$$\int_0^\infty i_{\mathrm{cm,T,k}}(t)dt = (N-k+1) \cdot C_{\mathrm{eq}} V_{\mathrm{dc}}. \tag{13}$$

The step response described by (12) features a time-constant

$$\tau = 2C_{\mathrm{eq}} R_{\mathrm{cmc,L}}, \tag{14}$$

and a peak value of

$$\hat{I}_{\mathrm{T,k}} = (N-k+1)\frac{V_{\mathrm{dc}}}{R_{\mathrm{cmc,L}}}. \tag{15}$$

Following the same procedure as in the idealized case (cf. (3) and (4)), the resulting rms common-mode current flowing through node N can be calculated by replacing the rectangular current blocks with such of shape $i_{\mathrm{cm,T,k}}(t)$. Defining

$$X(k) := \int_0^\infty i_{\mathrm{cm,T,k}}(t)^2 dt = \frac{5}{8}(N-k+1)^2 \frac{C_{\mathrm{eq}} V_{\mathrm{dc}}^2}{R_{\mathrm{cmc,L}}}, \tag{16}$$

the desired total rms common-mode current becomes

$$\tilde{i}_{\mathrm{cm}} = \sqrt{f_{\mathrm{S}} \cdot \left[2X(1) + \sum_{\mathrm{k}=2}^{N} 4X(k)\right]} = \sqrt{f_{\mathrm{s}} \cdot \frac{5}{8}\frac{C_{\mathrm{eq}} V_{\mathrm{dc}}^2}{R_{\mathrm{cmc,L}}} \cdot \left[\frac{4}{3}N^3 + \frac{2}{3}N\right]}. \tag{17}$$

Similarly, the rms value of the common-mode current in cell l for $l \geq k$ is given by

$$\tilde{i}_{\mathrm{cm,l}} = \sqrt{f_{\mathrm{S}} \cdot (4l-2) \cdot \frac{5}{8}\frac{C_{\mathrm{eq}} V_{\mathrm{dc}}^2}{R_{\mathrm{cmc,L}}}}. \tag{18}$$

Using the current divider rule, the current flowing in $R_{\mathrm{cmc,L}}$ can be calculated as

$$\tilde{i}_{\mathrm{R,l}} = \sqrt{f_{\mathrm{s}} \cdot (4l-2)\frac{C_{\mathrm{eq}} V_{\mathrm{dc}}^2}{2R_{\mathrm{cmc,L}}}}. \tag{19}$$

Therefore, the power dissipated in the damping resistor becomes

$$P_{\mathrm{l,R}} = \tilde{i}_{\mathrm{l,R}}^2 \cdot R_{\mathrm{cmc,L}} = f_{\mathrm{s}} \cdot (2l-1) C_{\mathrm{eq}} V_{\mathrm{dc}}^2, \tag{20}$$

which is independent of the CMC and damping resistor, and amounts to negligible 5.5 W for $l = N = 4$ in the example system. The power dissipation in the CMC's series resistance, i. e., the windings, is anyway dominated by the differential-mode load current and will be addressed in the next section.

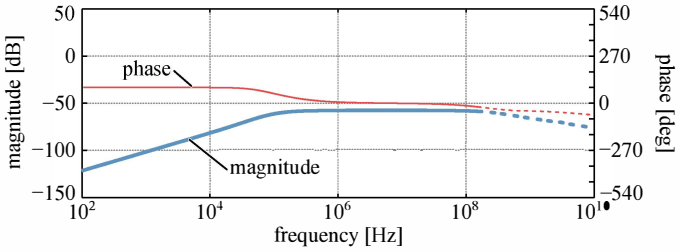

Fig. 14. Bode diagramm of $G_3(s)$ considering the designed local CMCs and $L_{\mathrm{eq}} = 100\,\mathrm{nH}$.

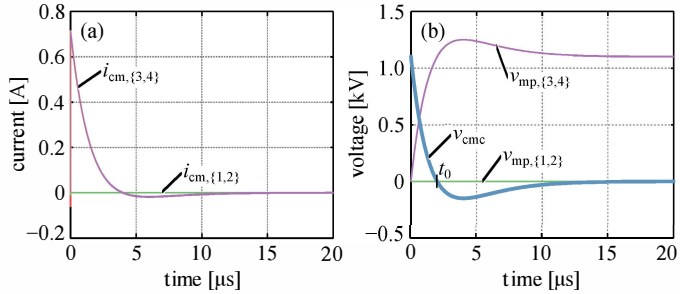

Fig. 15. Step responses of the common-mode currents (a) and the corresponding midpoint voltages (b), where also the voltage across a local CMC, v_{cmc}, is shown. Note that $L_{\mathrm{eq}} = 100\,\mathrm{nH}$ is considered in addition to the designed local CMCs.

2) Example Design: Eq. (17) serves together with (11) as design equation for the local CMCs and Fig. 13 illustrates the design trade-offs. However, to choose a specific value of $L_{\mathrm{cmc,L}}$, an additional specification is required. In order for the common-mode current pulses to be short compared with the PWM pulses, the requirement $\tau \leq 0.2\,\% \cdot T_{\mathrm{s}} = 2\,\mu\mathrm{s}$ could be introduced. This results in $L_{\mathrm{CMC,L}} = 6.2\,\mathrm{mH}$, $R_{\mathrm{CMC,L}} = 1.539\,\mathrm{k\Omega}$ and $\tilde{i}_{\mathrm{cm}} = 167\,\mathrm{mA}$, as is indicated also in Fig. 13. Note that the rms common-mode current is reduced by almost a factor of 5 when compared to the initial case (cf. Table II); a further reduction would come at the cost of very high $L_{\mathrm{cmc,L}}$ values.

Fig. 14 shows the Bode plot of $G_3(s)$, i. e., the full transfer function including L_{eq}, where the above values for $L_{\mathrm{cmc,L}}$ and $R_{\mathrm{cmc,L}}$ are used. The high-frequency resonances are successfully removed by the critically damped CMCs. This is also visible in Fig. 15(a) and (b), where the corresponding responses of the common-mode currents and cell midpoint voltages to a step transition of the voltage source $v_{\mathrm{B},3}$ are shown.

3) Verification: Fig. 16 shows waveforms of the output voltage and total common-mode current (i. e., flowing through the ground connection at node N) obtained from a full-system simulation including the designed local CMCs. A massive reduction of the common-mode currents compared to those shown in Fig. 5(b) is obvious. Table III compares calculated and simulated rms common-mode current values, which confirms the accuracy of the proposed analytic modeling including the assumption $L_{\mathrm{eq}} \approx 0$.

C. Common-Mode Choke Design

With the required values of the local CMCs now being calculable, this section discusses the resulting size and losses of possible actual realizations. A key design parameter is

TABLE III
CALCULATED AND SIMULATED RMS COMMON-MODE CURRENTS WITH LOCAL CMCS.

	calc. [mA]	sim. [mA]	error [%]
cell 1	25.3	25.2	0.352
cell 2	43.8	43.5	0.717
cell 3	56.5	56.2	0.571
cell 4	66.9	66.6	0.411
total	167.7	166.7	0.615

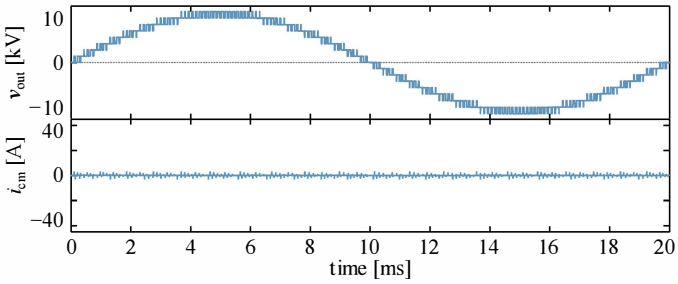

Fig. 16. Simulated phase stack output voltage, v_{out}, and total common-mode current, i_{cm}, for the case of optimally damped local CMCs.

the applied voltage-time integral, which follows from $v_{\mathrm{cmc}}(t)$ shown in Fig. 15(b) as

$$(vt) = \int_0^{t_\bullet} v_{\mathrm{cmc}}(t)dt = \sqrt{L_{\mathrm{cmc,L}}C_{\mathrm{eq}}}V_{\mathrm{dc}}\mathrm{e}^{-1}, \qquad (21)$$

where v_{cmc} is the difference between the applied voltage step and the voltage across the parasitic capacitance. Note that the simplified step response resulting from $G_{\mathrm{s,k}}(s)$ has been used to obtain this analytic result. However, the deviation from numerical integration of the full step response shown in Fig. 15(b) is only about 0.35 % for the values used here.

The two well-known inductor design equations become thus

$$\hat{B} = \frac{\sqrt{L_{\mathrm{cmc,L}}C_{\mathrm{eq}}}V_{\mathrm{dc}}\mathrm{e}^{-1}}{NA_{\mathrm{c}}} \quad \text{and} \qquad (22)$$

$$J_{\mathrm{rms}} = \frac{2NI_{\mathrm{rms}}}{k_{\mathrm{w}}A_{\mathrm{w}}}, \qquad (23)$$

where the factor 2 in (23) accounts for the second CMC winding. From these equations, the area product can be derived as

$$A_{\mathrm{c}}A_{\mathrm{w}} = \frac{2\sqrt{L_{\mathrm{cmc,L}}C_{\mathrm{eq}}}V_{\mathrm{dc}}\mathrm{e}^{-1}I_{\mathrm{rms}}}{\hat{B}k_{\mathrm{w}}J_{\mathrm{rms}}} \propto \sqrt{L_{\mathrm{cmc,L}}}. \qquad (24)$$

Commonly, CMCs are realized using toroidal cores with an area product of (cf. Fig. 17(a))

$$\begin{aligned} A_{\mathrm{c}}A_{\mathrm{w}} &= (h \cdot (r_{\mathrm{a}} - r_{\mathrm{i}})) \cdot (\pi r_{\mathrm{i}}^2) \\ &= \pi s_{\mathrm{h}} s_{\mathrm{r}}^2 (1 - s_{\mathrm{r}}) \cdot r_{\mathrm{a}}^4, \end{aligned} \qquad (25)$$

where $s_{\mathrm{r}} = r_{\mathrm{i}}/r_{\mathrm{a}} = 0.7$ and $s_{\mathrm{h}} = h/r_{\mathrm{a}} = 0.7$, as found from averaging a range of suitable toroidal cores, are introduced to establish a dependency between the area product and the box volume of the resulting CMC. Neglecting the winding, the box volume of a toroidal coil is thus given by

$$V_{\mathrm{box}} = (2r_{\mathrm{a}})^2 \cdot h = (2r_{\mathrm{a}})^2 \cdot s_{\mathrm{h}} r_{\mathrm{a}}. \qquad (26)$$

Solving (25) for r_{a} and inserting in (26) yields an estimate of the required CMC volume as a function of the area product,

$$V_{\mathrm{box}} = 4s_{\mathrm{h}} \left(\frac{A_{\mathrm{c}}A_{\mathrm{w}}}{\pi s_{\mathrm{h}} s_{\mathrm{r}}^2 (1 - s_{\mathrm{r}})} \right)^{3/4}, \qquad (27)$$

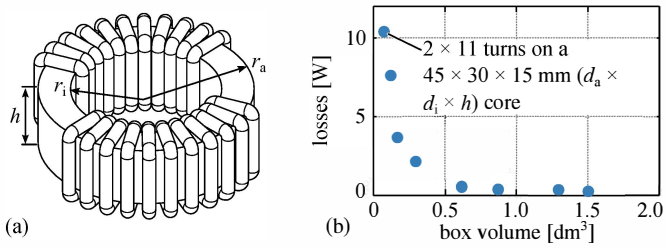

Fig. 17. (a) Geometric dimensions of the considered CMC and (b) thermally feasible CMC designs based on standard Vitroperm cores.

and substituting $A_c A_w$ with the expression from (24) leads to a direct dependence on the system parameters and the desired $L_{cmc,L}$ value:

$$V_{box} = 4 s_h \left(\frac{2\sqrt{L_{cmc,L} C_{eq}} V_{dc} e^{-1} I_{rms}}{\hat{B} k_w J_{rms} \pi s_h s_r^2 (1 - s_r)} \right)^{3/4} \propto L_{cmc,L}^{3/8} \tag{28}$$

Assuming $J_{rms} = 5\,\mathrm{A/mm^2}$, $\hat{B} = 0.7\,\mathrm{T}$ for nanocrystalline core material such as Vitroperm [21], $k_w = 0.1$ for a single-layer winding, and $I_{rms} = 56.6\,\mathrm{A}$ corresponding to the phase current resulting from the specifications in Table I, yields the curve shown in Fig. 13 and a volume estimate of $V_{box} = 0.076\,\mathrm{dm^3}$ for the designed CMC with $L_{cmc,L} = 6.2\,\mathrm{mH}$.

To back-up these approximations, a number of CMCs for $L_{cmc,L} = 6.2\,\mathrm{mH}$ have been designed based on standard toroidal Vitroperm cores from VAC [21]. For each core geometry, the required number of turns to meet the above stated peak flux density has been calculated. Together with the requirement for a minimum spacing between the two windings (isolation requirements), the maximum possible wire diameter for single-layer windings and hence the losses caused by the load current can be calculated. Core losses are neglected due to the moderate peak flux density and the comparably low switching frequencies. Finally, the box volume is calculated taking into account also the windings. To account for thermal limitations, the box surface area, a heat transfer coefficient of $\alpha = 20\,\mathrm{W/Km}$ for natural convection, a maximum surface temperature of $100\,^\circ\mathrm{C}$ and an ambient temperature of $50\,^\circ\mathrm{C}$ are used to calculate the maximum allowable power dissipation, and any design exceeding this value is discarded.

Fig. 17 shows the resulting designs in a loss-vs.-volume plot, which confirms that a design with a volume of roughly $0.1\,\mathrm{dm^3}$ and about $10\,\mathrm{W}$ power dissipation is possible (cf. example design details in Fig. 17) and the estimate of the CMC volume based on $L_{cmc,L}$ presented above gives acceptable results.

Even though fifteen such CMCs are required for the complete three-phase SST, the additional volume and losses are negligible. Therefore, local CMCs designed as described above are a feasible means to suppress common-mode currents and associated resonant phenomena in cascaded cells converter systems.

V. Conclusion

Due to the high grid voltage levels, commonly multi-cell systems are employed in the medium-voltage interface of solid-state transformers. Without proper countermeasures, the steeply changing potentials within such cascaded cells converter systems give rise to high common-mode currents flowing through parasitic capacitances and potentially resonating with parasitic inductances. An analytic description of these effects as well as of the mitigation thereof by means of common-mode choking has been presented. In accordance with literature, placement of common-mode chokes at the AC terminals of each individual converter cell has been identified as the most feasible solution and a detailed design guideline for such common-mode chokes has been presented. Furthermore, the impact of the additional volume and losses has been shown to be negligible considering the overall SST system.

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