Novel Hybrid 12-Pulse Line-Interphase-Transformer Boost-Type Rectifier with Controlled Output Voltage and Sinusoidal Utility Currents

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Keywords: 12-pulse hybrid rectifier, sinusoidal input current, controlled output voltage, aircraft applications

Passive rectifiers are advantageous compared to active rectifiers concerning efficiency, low complexity, EMC, and reliability. Furthermore, for high input frequency applications, such as aircraft and micro gas turbine systems, the magnetic components occupy a smaller volume. On the other hand, hybrid rectifiers can compensate drawbacks of passive rectifiers such as ensuring a controlled output voltage. In this paper, a novel control scheme of the hybrid rectifier is proposed for achieving purely sinusoidal input currents. Furthermore, the control scheme is verified with numerical simulations and experimental results.

The main circuit configuration of the hybrid rectifier, which composes a voltage-type 12-pulse passive rectifier and DC-DC converters, is shown in Fig. 1. The output voltage can be controlled by the power transistors T_1 and T_2. The input current shape depends on only the output voltages of the diode bridges and the turns ratio (w_B/w_A=0.366) of the line interphase transformers (LIT). The input currents can therefore be controlled by using variable duty cycles of T_1 and T_2. From space vector equations the optimum voltage modulation in order to achieve purely sinusoidal input currents can be derived as

$$\begin{aligned} u_1 &= \frac{3}{2}\hat{u}'(\cos\varphi_N + (2+\sqrt{3})\sin\varphi_N) \\ u_2 &= \frac{3}{2}\hat{u}'(\cos\varphi_N - (2+\sqrt{3})\sin\varphi_N) \end{aligned} \quad \cdots\cdots\cdots (1)$$

where u_1 and u_2 are the local average values of voltages across T_1 and T_2 respectively and $\hat{u}'$ is the peak input phase voltage. The waveforms u_1 and u_2 are close to having a trianglar shape that that varies between zero and the output voltage for the angle $\varphi_N = (+15°, -15°)$. The triangular shape can be realized by changing duty cycle of T_1 and T_2.

Fig. 2 shows the experimental input currents of a 10 kW prototype controlled by the conventional constant duty cycle (a) and by triangular modulation (b), which approximates well u_1 and u_2 according to (1). By applying the proposed modulation scheme, sinusoidal input currents are realized. The THD is reduced from 6.1% to 2.0% and the power factor is improved from 0.968 to 0.976. The input inductor L is designed to fulfill the requirements of low-order input current harmonics for aircraft applications. Since low-order input current harmonics can be significantly reduced by the proposed control scheme, the inductance of L can be reduced. However, the flux density through the LIT is increased if the proposed control scheme is applied.

In this paper a novel control scheme to achieve purely sinusoidal input currents for a voltage-type hybrid 12-pulse rectifier has been proposed. In further work, the application of the control scheme will be studied for current-type multi-pulse hybrid rectifier systems.

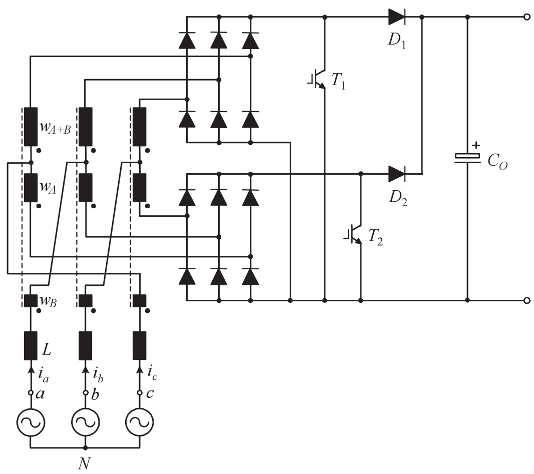

Fig. 1. Novel hybrid 12-pluse LIT rectifier with controlled output voltage and purely sinusoidal input currents

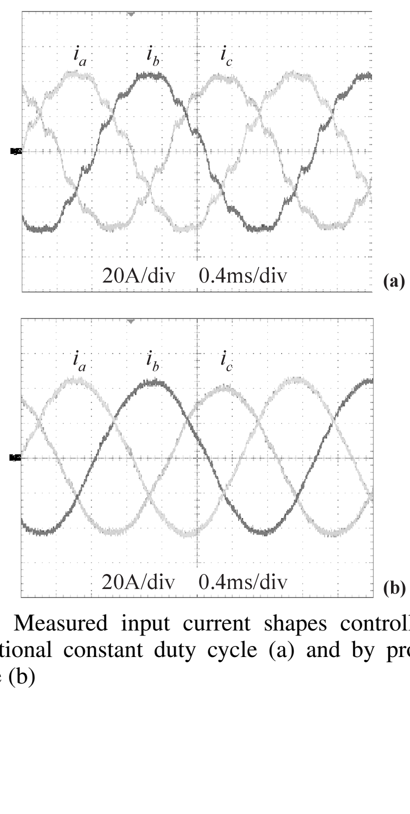

Fig. 2. Measured input current shapes controlled by conventional constant duty cycle (a) and by proposed scheme (b)

Paper

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A novel injection scheme to improve the input current harmonics of a hybrid 12-pulse line-interphase-transformer rectifier with controlled output voltage by a two-switch boost-type output stage is presented in this paper. A theoretical derivation of the modulation for achieving purely sinusoidal input currents is introduced. Finally, the proposed scheme is analyzed and verified by numerical simulations and experimental results.

Keywords: 12-pulse hybrid rectifier, sinusoidal input current, controlled output voltage, aircraft applications

1. Introduction

Various 12-pulse passive rectifier concepts which comprise of isolated and/or non-isolated phase shifting transformers, diodes, and inductors have been proposed in the literature [1]. Passive rectifiers are advantageous concerning efficiency, complexity, EMC, and reliability. Furthermore, for high input frequency applications like aircraft and micro gas turbine systems, the magnetic components have a lower volume.

For future More-Electric-Aircraft the conventional fly-by-wire hydraulic flight control surface actuation will be partly replaced by power-by-wire electro-hydrostatic actuators (EHAs) [2]–[4]. Various rectifier concepts were compared for powering an EHA and it was identified that a passive 12-pulse rectifier system with line-interphase-transformers (LIT) [11][12] is competitive with an active three-level PWM rectifier with respect to efficiency and power density [6]. However, a drawback of the passive system is the dependency of the output voltage on the mains voltage level, mains frequency, and output power, especially if the voltage and frequency of the power source show large fluctuations. In order to avoid this drawback, hybrid 12-pulse rectifiers with controlled output voltage (Fig. 1) have been proposed [5][6] and analytically and experimentally evaluated [7].

A remaining disadvantage of the proposed rectifiers compared to active PWM rectifiers is the staircase shape of the input currents, which cannot be eliminated by the input EMI filter and results in low-frequency mains current harmonics.

Three-phase passive and hybrid rectifier topologies are classified in Fig. 2. Hybrid rectifiers are defined as a combination of a passive rectifier and turn-off power semiconductor(s). Both passive and hybrid rectifiers can be classified as being either voltage-type and current-type. Several current injection schemes like the Minnesota Rectifier [16] invented by Prof. Mohan and auxiliary current generators [19]–[21], which can improve the input current quality in current-type rectifiers, have been proposed. The voltage-type rectifier proposed by Niermann [11][12] shows a lower VA rating of the LIT (e.g. 13.4% for 12-pulse rectifier). However, a voltage injection scheme is necessary to improve input current harmonics in voltage-type systems [10]–[13] and no solution has been

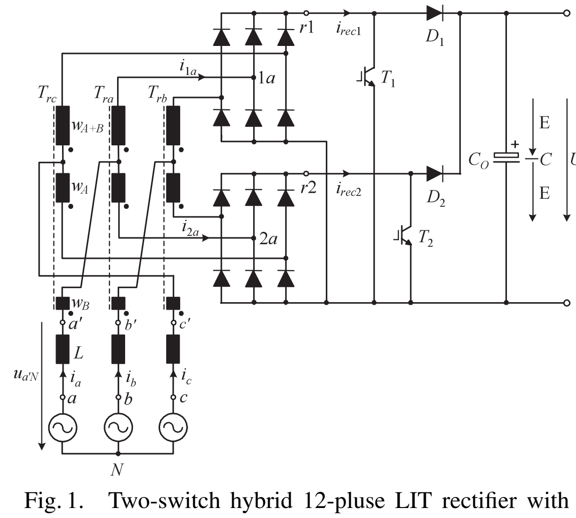

Fig. 1. Two-switch hybrid 12-pluse LIT rectifier with controlled output voltage

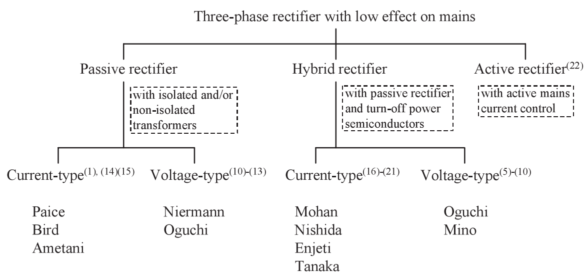

Fig. 2. Classification of three-phase rectifiers concept with low effect on the mains

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proposed so far.

In this paper a novel control scheme for improving the input current quality and/or for lowering the amplitudes of low frequency current harmonics of a hybrid voltage-type 12-pulse LIT rectifier is presented. The system is formed by combining a 12-pulse passive rectifier with two DC/DC boost converters (c.f. Fig. 1) ensuring a controlled output voltage.

In section 2 a theoretical derivation for the optimum operating condition to achieve purely sinusoidal input current is shown. The proposed control scheme is verified and compared to conventional constant duty cycle control by numerical simulations in section 3. Finally, the proposed control scheme is experimentally evaluated in section 4.

2. Derivation of the Modulation Functions for Achieving Purely Sinusoidal Input Currents

For passive operation, continuous input current shape and constant output voltage U_o of the rectifier system the LIT input voltages $u_{a'N}$, $u_{b'N}$, $u_{c'N}$ exhibit a staircase shape. There, the different voltage levels are directly determined by U_o and the LIT turns ratios. Accordingly, a purely sinusoidal LIT input voltage shape and/or a related space vector

$$\underline{u'} = \hat{u}'(\cos\varphi_N + j\sin\varphi_N) \quad \cdots\cdots (1)$$

($\varphi_N = \omega_N t$, where ω_N is the mains angular frequency, φ_N is the phase of the mains current space vector $\underline{i}_N$ and $\hat{u}'$ is the peak input phase voltage) could be achieved in the average over a pulse period by proper modulation of the rectifier bridge output voltages u_{T1} and u_{T2}. This would result in a purely sinusoidal current drawn from the mains, i.e. the low frequency harmonics of the input current would be eliminated.

For the calculation of the corresponding time behavior of u_{T1} and u_{T2} the considerations can be restricted to a 30°-wide interval of the mains period due to the 12-pulse property of the circuit, e.g. only $\varphi_N = [+15°, -15°)$ is considered. The (purely sinusoidal) mains current $\underline{i}_N$ is split into two current space vectors $\underline{i}_1$ and $\underline{i}_2$ which are displaced in phase by ±15° (with respect to $\underline{i}_N$) and occur at the LIT outputs. Accordingly, we have for the input voltage space vectors of the diode bridges in the φ_N interval considered

$$\begin{aligned}\underline{u}_1 &= \frac{2}{3}u_1 \\ \underline{u}_2 &= \frac{2}{3}u_2\end{aligned} \quad \cdots\cdots (2)$$

($i_{1a}, i_{2a} > 0, i_{1b}, i_{2b}, i_{1c}, i_{2c} < 0$) where u_1 and u_2 are the local average values of u_{T1} and u_{T2}. This results in the LIT input voltage space vector

$$\underline{u'} = \underline{u}_2 - (\underline{u}_2 - \underline{u}_1)\left(\frac{w_A}{2w_A + w_B}\right) + \underline{u}_{wB} \quad \cdots\cdots (3)$$

($w_B/w_A = 0.366$) where $\underline{u}_{wB}$ is the space vector of the voltages across the windings w_B of the LIT, which are related to the voltage difference ($\underline{u}_2 - \underline{u}_1$) present across w_A and w_{A+B} by

$$\underline{u}_{wB} = (\underline{u}_2 - \underline{u}_1)\left(\frac{w_B}{2w_A + w_B}\right)e^{-j\frac{2\pi}{3}} \quad \cdots\cdots (4)$$

There, the cyclic changing of the phases has been considered by a phase shift of −120°. Combining (1)–(4) results in

$$\begin{aligned}u_1 &= \frac{3}{2}\hat{u}'(\cos\varphi_N + (2 + \sqrt{3})\sin\varphi_N) \\ u_2 &= \frac{3}{2}\hat{u}'(\cos\varphi_N - (2 + \sqrt{3})\sin\varphi_N)\end{aligned} \quad \cdots\cdots (5)$$

with

$$\begin{aligned}u_1 &= (1 - d_1)U_o \\ u_2 &= (1 - d_2)U_o\end{aligned} \quad \cdots\cdots (6)$$

(d_1 and d_2 are the local duty cycles of the power transistors). As can be seen from a graphical representation of u_1 and u_2 and/or from $u_{2,\varphi N=-15°} = u_{1,\varphi N=+15°} = 0$, $u_{2,\varphi N=0°} = u_{1,\varphi N=0°} = 1.5\hat{u}'$, and $u_{2,\varphi N=+15°} = u_{1,\varphi N=-15°} \approx 2.9\hat{u}'$ the actual shape of u_1 and u_2 can be approximated linearly with sufficient accuracy using

$$\begin{aligned}u_1 &= 3\hat{u}'\left(\frac{1}{2} - \frac{6}{\pi}\varphi_N\right) \\ u_2 &= 3\hat{u}'\left(\frac{1}{2} + \frac{6}{\pi}\varphi_N\right)\end{aligned} \quad \cdots\cdots (7)$$

which results in a triangular shape of u_1 and u_2 over the mains period (u_1 exhibits a phase shift of 180° with respect to u_2). Considering (8) in section 3.3 and $\hat{u}' \approx \hat{u}_a$ the global average value of the duty cycle of T_1 and T_2 has to be selected as $D_{avg} = 50\%$ corresponding to an output voltage of $U_o \approx 3\hat{u}_a$.

3. Numerical Simulation

In this section the proposed modulation scheme is verified by numerical simulations and compared to constant duty cycle operation.

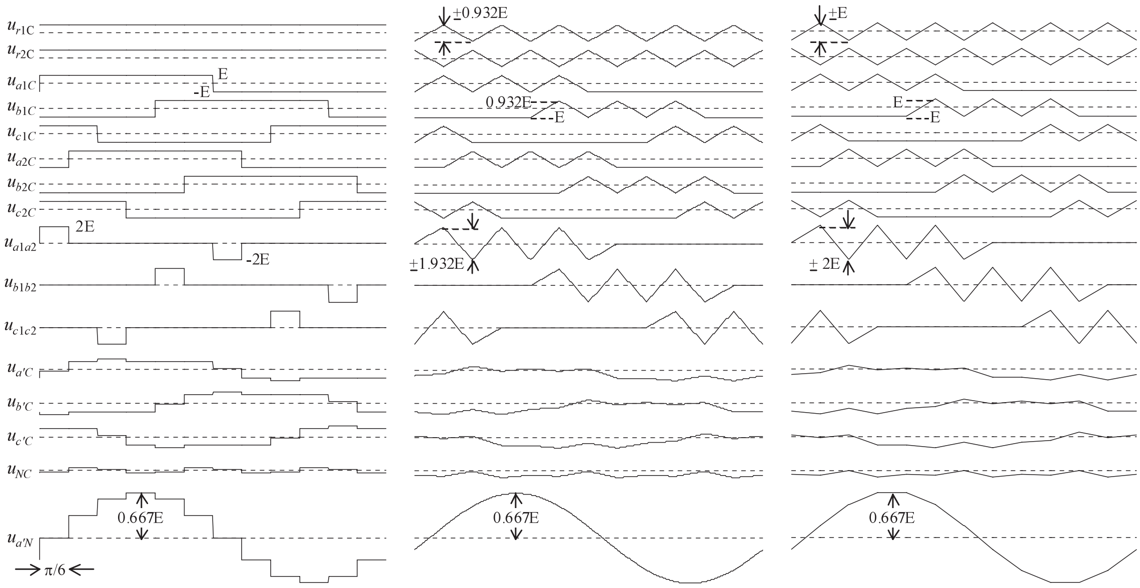
3.1 Simulated Operating Conditions To easily generate the modulation functions, triangular waveforms are used in the numerical simulations as a approximation of the actual time behavior of the modulation functions. The following parameters are defined with reference to aircraft applications:

Input phase voltage:	U_N = 115 Vrms ± 15%
Input frequency:	f_N = 400 Hz
Nominal output power:	P_O = 10 kW
Switching frequency:	f_S = 33 kHz
Output voltage:	U_O = 480 V at D_{avg} = 50%.

Table 1 lists the rectifier circuit parameters. The inductance of the input inductors is selected to endure that the admissible amplitudes of the 11th and 13th input current harmonics at constant duty cycle or passive operation [4][6] (where power transistors T_1 and T_2 remaining in the turn-off state) are less than the required aircraft standards. The switching frequency is defined such that the peak-to-peak switching frequency input current ripple is kept below 10% of the fundamental current amplitude [4][6]. The turns ratio of the LIT

Table 1. Simulation circuit parameters of the two-switch hybrid 12-pulse LIT rectifier with controlled output voltage

Component	Symbol	Parameter
Input inductor	L	188μH
LIT	T_{ra}, T_{rb}, T_{rc}	w_B/w_A=0.366
Output capacitor	C_O	1mF



(a) Constant duty cycle (b) Optimum modulation (c) Triangular modulation

Fig. 3. Simulated operating behavior of the voltage-type hybrid 12-pulse rectifier

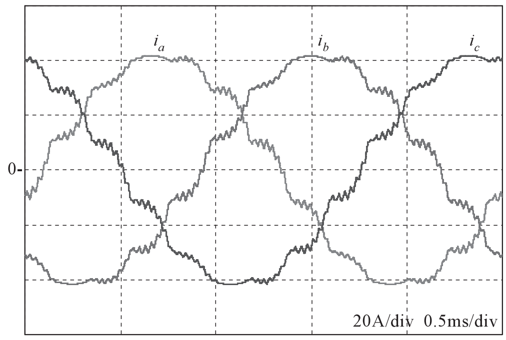
is selected to achieve the necessary ±15° phase shift of i_{1a} and i_{2a}. The power transistors T_1 and T_2 are driven in an interleaved manner in order to reduce the switching frequency input current ripple.

The simulation results are shown in Fig. 3 where the local average value of discontinuous quantities is shown instead of the actual shape in order to clearly represent the system operating behaviors. It is verified that the input currents simulated by the optimum modulation to achieve purely sinusoidal input current and the triangular modulation (triangular approximation of the optimum modulation functions) are improved compared to using a constant duty cycle.

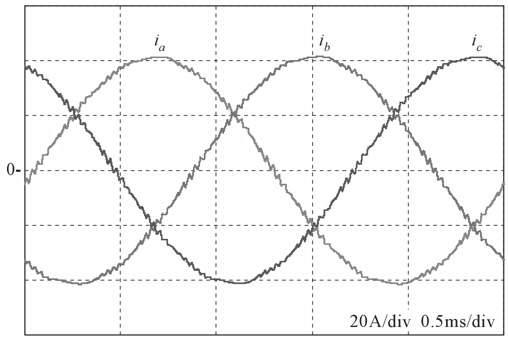
3.2 Comparison of Low-Order Input Current Harmonics The simulated input current waveforms and the corresponding low-order input current harmonics resulting from constant duty cycle and variable duty cycle operation are shown in Fig. 4 and Fig. 5. It has to be noted that injected control signals of T_1 and T_2 are inverted waveforms of u_{r1C} and u_{r2C} (see Fig. 3(c)) because a high (low) duty cycle results in a low (high) local average value of voltage u_{r1C} and/or u_{r2C}.

By employing the 6th harmonic modulation, i.e. by triangular shaping of the local average value of the rectifier stage output voltages, the input current waveforms are improved (cf. Fig. 4 (a) and (b)) and the low-order harmonic components are significantly reduced (cf. Fig. 5(a) and (b)). The THD of the input current is improved from 6.8% to 0.8%.

3.3 Comparisons of Current and Voltage Stresses The output currents of the diode bridges i_{rec1} and i_{rec2} are depicted in Fig. 6. The current stresses resulting from a constant duty cycle and from triangular modulation are approximately equal. The selected turns ratio of the LIT results in an equal distribution of the input phase currents, e.g. of i_a to the inputs of the diode bridges i_{1a} and i_{2a} with phase shift of ±15°. Therefore, the improved input current waveforms causes a slight variation of i_{rec1} and i_{rec2} waveforms for both control schemes (see Fig. 6(a) and (b)). However, the proposed modulation scheme does not cause significant



(a) Constant duty cycle control



(b) Triangular modulation at D_{avg} = 50%

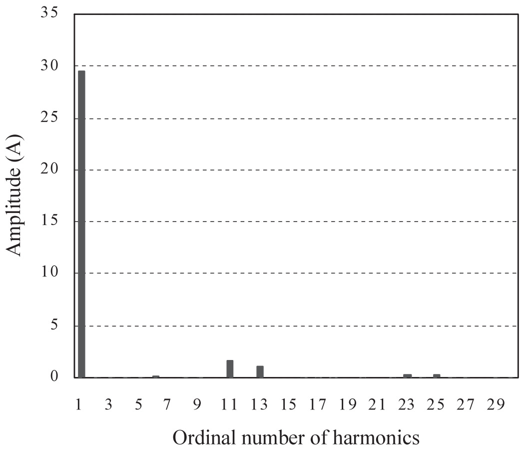
Fig. 4. Simulated input current waveforms

influence on current stresses in the main components.

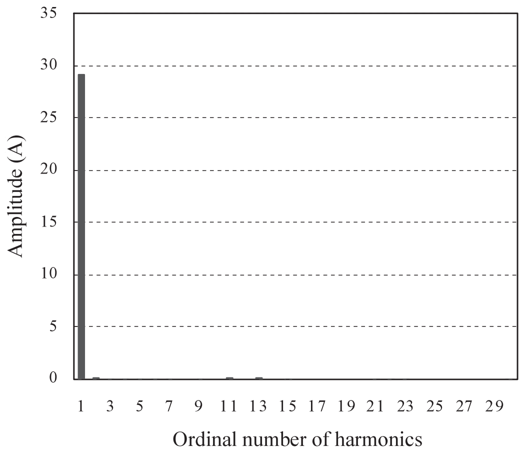
Since the average duty cycles of both control schemes are equal, the output voltages must also be equal. The output voltage can be expressed as [4][6]

$$U_o = \frac{1.52\hat{u}_a}{1 - D_{avg}} \quad \cdots\cdots (8)$$

where $\hat{u}_a$ and D_{avg} denote the amplitude of the input phase voltage and the average duty cycle respectively. It should be noted that the conduction voltage drops across the semiconductors and the inductors are neglected and no leakage

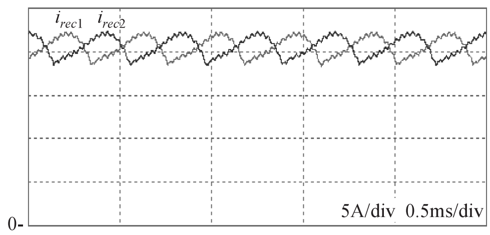


(a) Constant duty cycle control

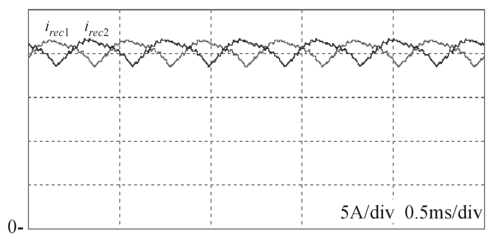


(b) Triangular modulation at D_{avg} = 50%

Fig. 5. Simulated low-order harmonics of the input currents as in Fig. 4



(a) Constant duty cycle control



(b) Triangular modulation

Fig. 6. Simulated output currents of the diode bridges of the 12-pulse hybrid rectifier system as in Fig. 4

inductance is considered and ideal coupling of the LIT windings is assumed. Equation (8) is identical with the simulation results (as shown in Fig. 7) and is valid for both control schemes. The resulting output voltage immediately determines the blocking voltage stress on the power semiconductors.

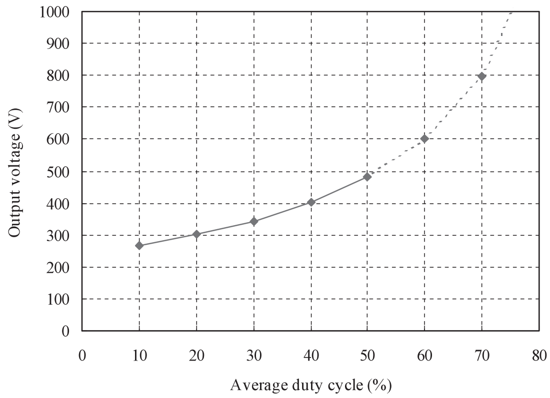


Fig. 7. Simulated output voltage resulting in dependency on average duty cycle for 10 kW output power

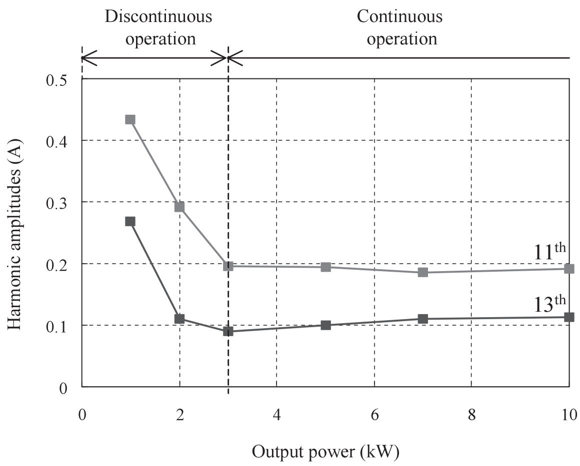


Fig. 8. Simulated amplitudes of the 11th and 13th input current harmonics in dependency on the output power for triangular modulation at D_{avg} = 50%

3.4 Dependency of Input Current Harmonics and Output Voltage on Output Power and Average Duty Cycle

The simulated dependency of the amplitude of the 11th and 13th input current harmonic on the output power is depicted in Fig. 8. The 11th and 13th input current harmonics increase in the range of low output power (P_O < 3 kW). In this output power range the input currents to the diode bridges are discontinuous, which causes a low-frequency distortion of phase voltages at the input of the LIT (e.g. of voltage $u_{a'N}$). However, the proposed control scheme ensures low 11th and 13th input current harmonics within a wide operating power range.

The dependency of the THD on the average duty cycle is illustrated in Fig. 9. The average duty cycle of the optimum modulation, which varies from 0 to 100%, is 50%. Since the modulation and/or duty cycle range is 0 to 100% the optimum modulation to improve the input current can only be realized for D_{avg} = 50%. For D_{avg} < 50% the duty cycle variation is within the range 0 to 2D_{avg} and from 2D_{avg} − 100% to 100% within the range D_{avg} > 50%. Despite this a low THD is achieved within the whole operating range as compared to constant duty cycle control (see Fig. 8). The THD in the range D_{avg} > 50% is lower compared to the range D_{avg} < 50% due to the high output voltage.

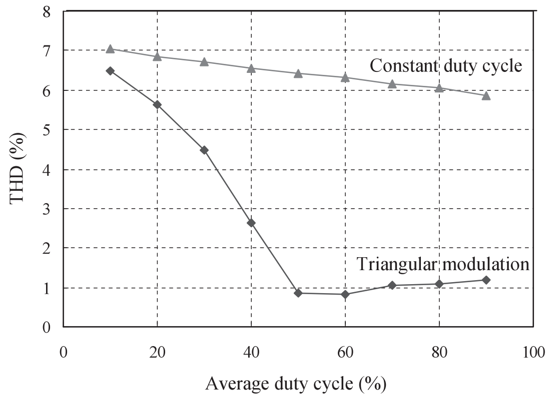
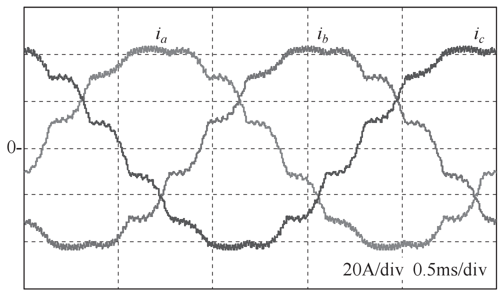
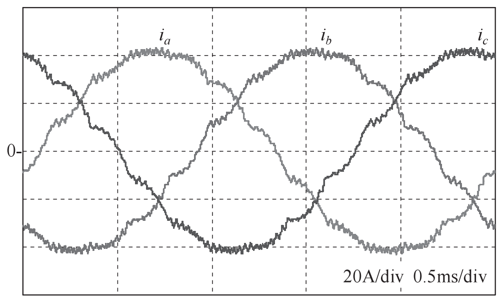


Fig. 9. Simulated dependency of the THD on the average duty cycle for an output power of 10 kW

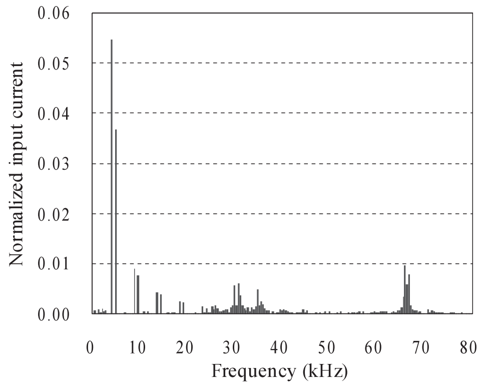


(a) Constant duty cycle

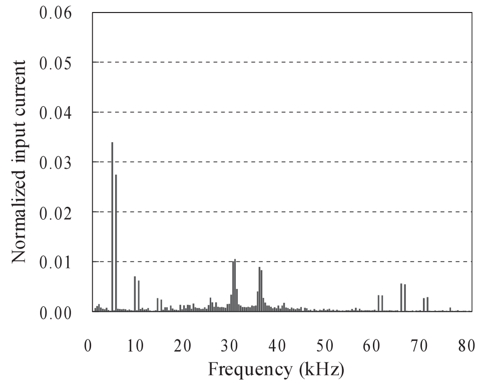


(b) Triangular modulation

Fig. 10. Simulated input current at D_{avg} = 30%



(a) Constant duty cycle



(b) Triangular modulation

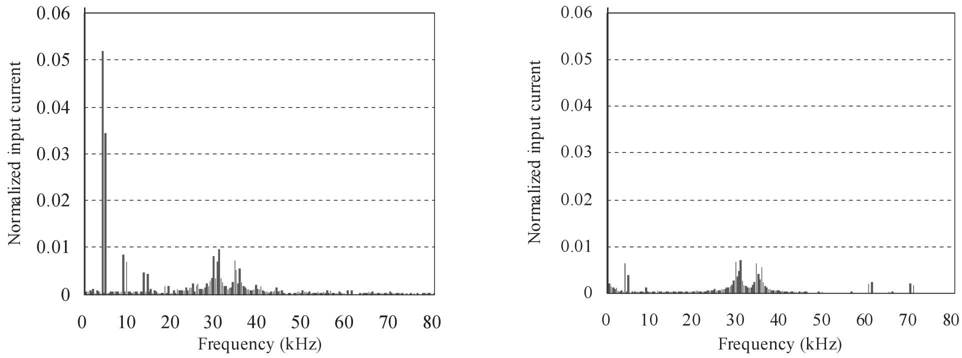
Fig. 11. Simulated input current spectrum; (a) and (b) as for Fig. 10

3.5 Comparisons of High-Order Input Current Harmonics and Output Voltage Ripple For D_{avg} = 50% the output voltage is around 480 V_{dc} in case of 200 V_{ac} input voltage. Therefore, for employing 600 V power semiconductors the voltage margin would not be sufficient, especially if input voltage tolerances would be considered.

With respect to future more electronic aircraft applications the output voltage has to be set to 350 Vdc [4][6] and/or D_{avg} = 30% has to be selected. The input current waveforms and the current spectrum for D_{avg} = 30% are shown in Fig. 10 and Fig. 11 respectively. The switching frequency current ripple resulting for constant duty cycle operation is relatively low due to the interleaved switching of T_1 and T_2 [4][6]. The switching frequency current ripple resulting for triangular modulation is higher due to the different duty cycles of T_1 and T_2 which makes the interleaving less effective. The input current quality is slightly lowere than D_{avg} = 50% (cf. Fig. 10(b) and Fig. 4(b)) because the optimum triangular modulation around Davg = 50% as shown in Fig. 8 can not be realized at D_{avg} = 30%.

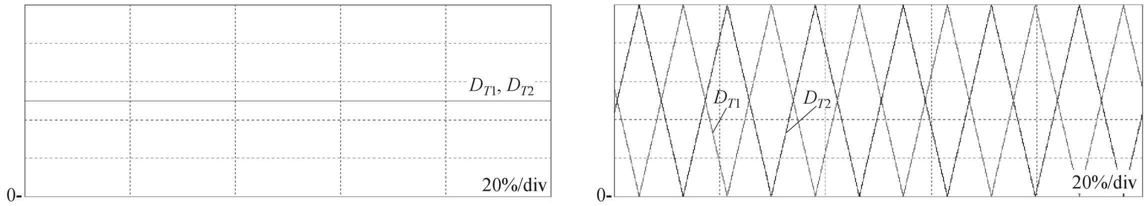
Fig. 12 and Fig. 13 show high-order harmonics of the input current and characteristic voltage shapes for constant duty cycle and the triangular modulation at Davg = 50%. In case of D_{avg} = 50% with triangular modulation the switching frequency current ripple is lower compared to constant duty cycle operation (cf. Fig. 12(a) and (b)) because the pulse width of $u_{a'N}$ and $u_{a'a}$ with the triangular modulation can gradually change (cf. Fig. 13(c) and (d), (e) and (f)). The amplitude of each generated voltage is theoretically equal. However, the pulse width of the inductor voltage $u_{a'a}$ for triangular modulation is smaller compared to the case of constant duty cycle when high amplitudes of $u_{a'a}$ are generated (cf. Fig. 13(e) and (f)). This causes lower switching frequency current ripple and lower output voltage U_O of high frequency components (cf. Fig. 13(g) and (h)). It is noted that the phase angle and the frequency of the modulation should be adjusted and synchronized to the input current. Any difference in phase angle or frequency would cause low frequency output voltage ripple.

3.6 Comparison of Magnet Components The LIT voltage u_{1a2a} and the integrated LIT voltage $u_{1a2a,\mathrm{int}}$ are depicted in Fig. 14. u_{1a2a} and $u_{1a2a,\mathrm{int}}$ are varying over a half mains period [6]. As compared to the constant duty cycle control, the peak amplitude of $u_{1a2a,int}$ resulting for triangular modulation is two times higher (cf. Fig. 14(a) and (b)). Furthermore, $u_{1a2a,\mathrm{int}}$ oscillates with the frequency of the triangular modulation, i.e. with six times of the mains frequency within a 150°-wide interval. This causes higher maximum flux density, volume, and core loss of the LIT. On the other hand, the inductance of the input inductors, which is selected for compliance to limits given for the amplitudes of the 11$^{\mathrm{th}}$



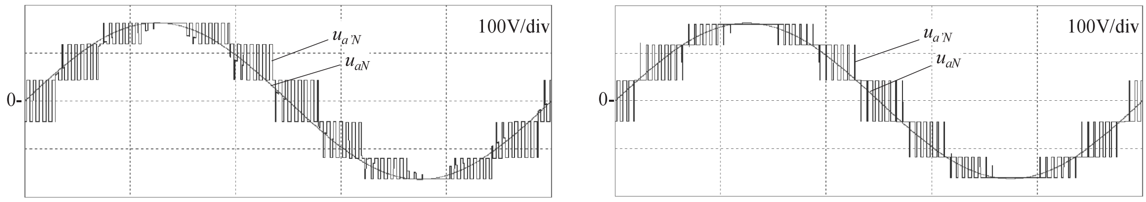
(a) Constant duty cycle **(b)** Triangular modulation

Fig. 12. Simulated high-order harmonics of the input current at D_{avg} = 50%



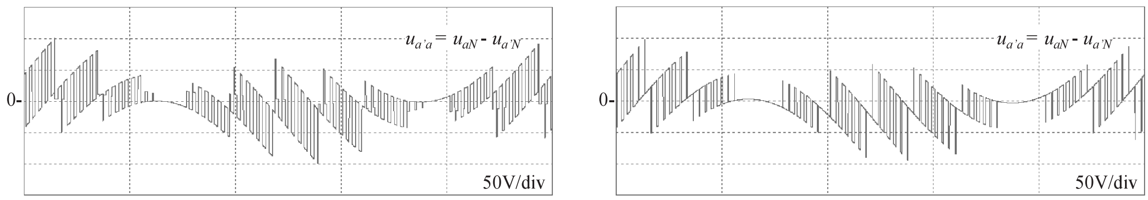
(a) Duty cycle of D_{T1} and D_{T2} (with constant duty cycle)

(b) Duty cycle of D_{T1} and D_{T2} (with triangular modulation)



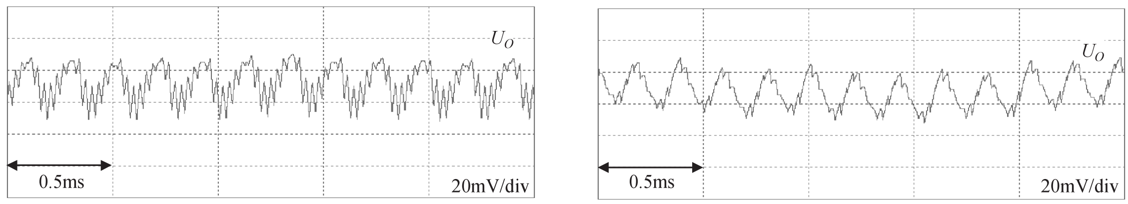
(c) Input phase voltage u_{aN} and corresponding input phase voltage $u_{a'N}$ between N and a' (with constant duty cycles D_{T1} and D_{T2})

(d) Input phase voltage u_{aN} and corresponding input phase voltage $u_{a'N}$ between N and a' (with triangular modulation D_{T1} and D_{T2})



(e) Input inductor voltage $u_{a'a}$ (with constant duty cycles D_{T1} and D_{T2})

(f) Input inductor voltage $u_{a'a}$ (with triangular modulation D_{T1} and D_{T2})



(g) Output voltage U_O (with constant duty cycles D_{T1} and D_{T2})

(h) Output voltage U_O (with triangular modulation D_{T1} and D_{T2})

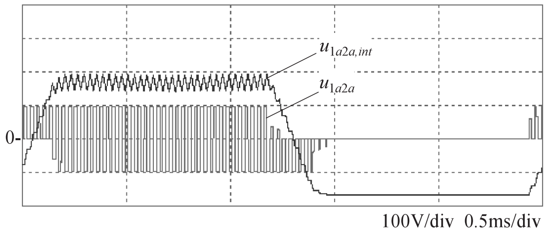
Fig. 13. Simulated operating behavior for constant duty cycles and triangular modulation of D_{T1} and D_{T2}

and 13th current harmonics [4][6], can be significantly reduced for the proposed modulation scheme. For example, using D_{avg} = 30% the inductance could be reduced from 188 μH to 55 μH for same low-order input current harmonics what results in a significant reduction of the inductor weight and volume.

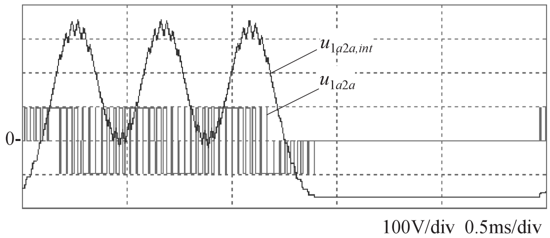
4. Experimental Evaluation

The proposed control scheme is evaluated by using a 10kW prototype. The control circuit, the main circuit components, and the experimental results are described in this section.

4.1 Control Circuit The control circuit diagram is depicted in Fig. 15. In order to generate the synchronized triangular signal, an input voltage (e.g u_a, u_b, or u_c) is detected and used as the input of the triangular signal generator. The triangular signal is then added to the constant control signals that are generated from the feed back control of U_o and the average current control of i_{rec1} and i_{rec2}. Zero sequence



(a) Constant duty cycle



(b) Triangular modulation

Fig. 14. Simulated LIT voltage u_{1a2a} and integrated voltage $u_{1a2a,\mathrm{int}}$ of u_{1a2a} at D_{avg} = 50%

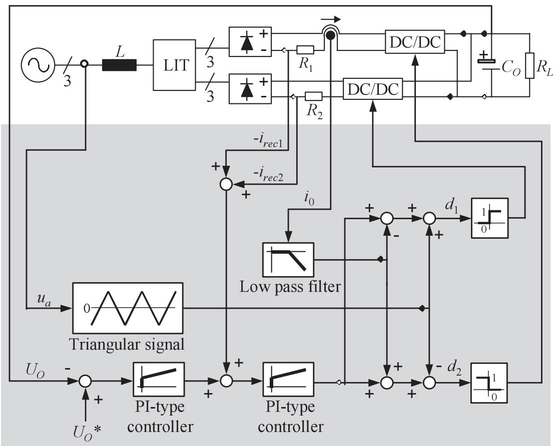


Fig. 15. Control block diagram including the triangular modulation

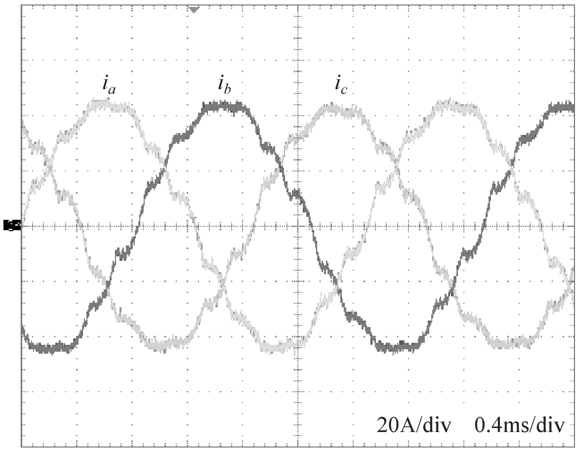
current i_0 is detected from both positive and negative output currents of a diode bridge. In (6) a low cost zero sequence current control which detects currents flowing to shunt resistors during turn-on period of a power transistor has been proposed. However, the low cost zero sequence current control scheme is not suitable for the triangular modulation due to the variable duty cycle i.e. i_0 can not be detected when the local duty cycle is around zero. Accordingly, a current transducer is employed in order to detect i_0. For the current measurements of i_{rec1} and i_{rec2} for the average current control shunt resistors R_1 and R_2 are employed.

4.2 Main Circuit Components Table 2 lists the main circuit components of the 10 kW prototype. Since the maximum output voltage is 569 Vdc at the maximum input voltage according to (8) neglecting the conduction voltage drops on the power semiconductors and the inductors and consideration of an ideal transformer of LITs), 900 V IGBTs as T_1 and T_2 and 1200 V fast recovery diodes as D_1 and D_2 are employed.

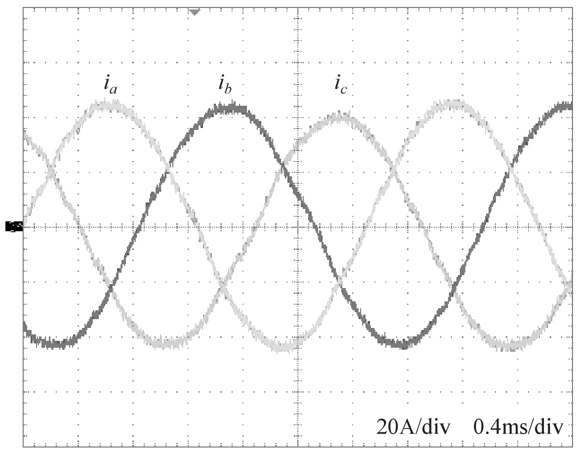
4.3 Experimental Results The measured input current waveforms from using constant duty cycle control and triangular modulation at D_{avg} = 50% are shown in Fig. 16.

Table 2. Main circuit components of the 10 kW prototype

Component	Symbol	Parameter
Input inductor	L	Value: 188μH, Number of turns: 45 Core: 10JNEX900, CS125, 0.1mm, Nippon steel
LIT	T_{ra}, T_{rb}, T_{rb}	w_A+w_B : w_A : w_B = 29 : 21 : 8 Core: 23P100, SL7500, 0.23mm, JFE steel
Diode bridge		800V/50A, 6RIE50-80, Fuji Electric Device Technology
IGBT	T_1, T_2	900V/50A × 2 in parallel, IRG4PF50W, International Rectifier
Output diode	D_1, D_2	1200V/50A, RHRG50120, Fairchild
Output capacitor	C_O	470μF/400Vdc, 2 in series, 2 in parallel, Rubycon



(a) Constant duty cycle

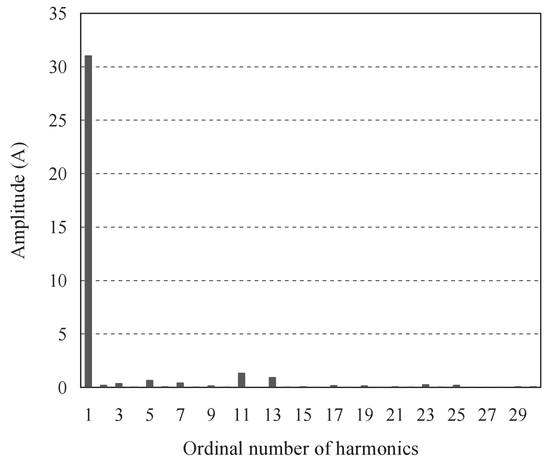


(b) Triangular modulation

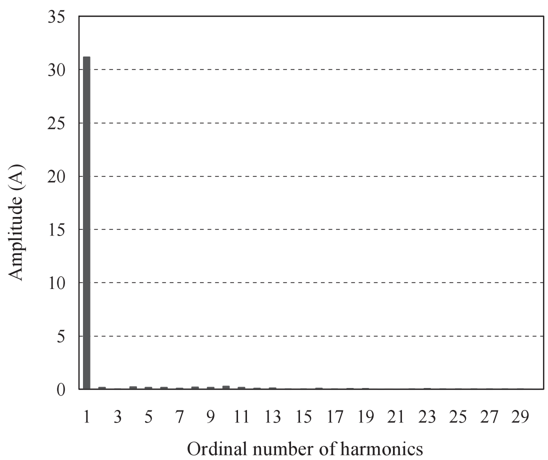
Fig. 16. Measured input current waveforms at D_{avg} = 50% and the norminal condition

By applying the proposed control scheme the input current waveforms are now near sinusoidal. The experimental waveforms are comparable to those of the simulation results (c.f. Fig. 4). The low-order input current harmonics are clearly reduced as one can be seen in Fig. 17. As compared to the constant duty cycle, the THD is improved from 6.1% to 2.0%.

The power factor characteristics are illustrated in Fig. 18. In case of the triangular modulation the low-order input current harmonics are increased in the range of the low output



(a) Constant duty cycle



(b) Triangular modulation

Fig. 17. Measured low-order harmonics of the input currents (Fig. 16)

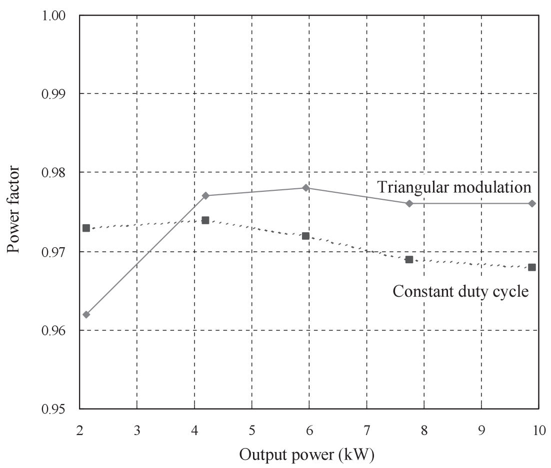


Fig. 18. Measured power factor in dependency on the output power at D_{avg} = 50%

power (c.f. Fig. 8). Accordingly, the power factor is lower compared to the constant duty cycle. However, the power factor is increased in the middle and high output power range by applying the proposed modulation scheme. The power factor is improved from 0.968 to0.976 at nominal output power. The improved power factor is not closed to 1. This is caused by the phase displacement of input current and input voltage resulting from the voltage drops across the input inductors. It should be noted that sinusoidal input currents are realized except in the low output power range. The power factor could be improved by combination of reduced inductance of the input inductors and the proposed control scheme. On the other hand, the efficiency at the nominal condition is 92%. High switching losses are generated due to the high switching frequency $f_p = 33\,\mathrm{kHz}$. Especially, behavior of reverse recovery causes high reverse recovery loss in D_1 and D_2 and high turn-on loss in S_1 and S_2. The efficiency could be improved by using the latest power diodes, such as silicon carbide Schottky diodes.

5. Conclusions

A novel 6th harmonic modulation scheme for hybrid 12-pulse voltage-type line-interphase-transformer (LIT) rectifiers has been proposed in this paper. The optimum function for achieving purely sinusoidal input currents is theoretically derived. The circuit operation and performance for the proposed control scheme are analyzed and compared to constant duty cycle control by numerical simulations and the experimental results. This shows that low-order input current harmonics can be significantly reduced. By applying the proposed modulation scheme, the volume of the LIT will be increased slightly compared to the conventional constant duty cycle scheme. However, the inductance and volume of the input inductors can be significantly reduced. This leaves room for a minimization of the overall system volume and/or efficiency. In summary, almost purely sinusoidal input currents can be realized by using the proposed control scheme with a low realization effort.

In further work the application of a modulation of the output quantity of the rectifier stages will be studied also for current-type multi-pulse passive rectifier systems.

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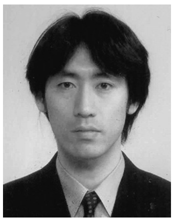

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