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Novel Motor-Kinetic-Energy-Based Power Pulsation Buffer Concept for Single-Phase-Input Electrolytic-Capacitor-Less Motor-Integrated Inverter System

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Abstract: The motor integration of singe-phase-supplied Variable-Speed Drives (VSDs) is prevented by the significant volume, short lifetime, and operating temperature limit of the electrolytic capacitors required to buffer the pulsating power grid. The DC-link energy storage requirement is eliminated by using the kinetic energy of the motor as a buffer. The proposed concept is called the Motor-Integrated Power Pulsation Buffer (MPPB), and a control technique and structure are detailed that meet the requirements for nominal and faulted operation with a simple reconfiguration of existing controller blocks. A 7.5 kW, motor-integrated hardware demonstrator validated the proposed MPPB concept and loss models for a scroll compressor drive used in auxiliary railway applications. The MPPB drive with a front-end CISPR 11/Class A EMI filter, PFC rectifier stage, and output-side inverter stage achieved a power density of 0.91 kW L^{-1} (15 W in^{-3}). The grid-to-motor-shaft efficiency exceeded 90% for all loads over 5 kW or 66% of nominal load, with a worst-case loss penalty over a conventional system of only 17%.

Keywords: single-phase; electrolytic capacitor-less; VSD; PFC operation; single-phase to three-phase AC/AC converter; motor integration

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1. Introduction

Mobility, transportation, and industrial systems are increasingly electric, from the drivetrain to the auxiliaries, driven by improvements in battery performance and lifetime, government and private mandates to reduce greenhouse gas emissions, and an improved user experience. This electrification includes the traction systems in electric vehicles, but the auxiliary systems must also be electrified with power-dense, efficient, and reliable power conversion stages under unique operating conditions and constraints. In particular, electromechanical systems—including pumps, compressors, and blowers—are required on nearly every vehicle and require VSDs for efficient operation.

An on-board compressor system for the air brakes of railway vehicles was considered here, as shown in Figure 1a. This oil-free scroll compressor [1]—selected for high pressure, low noise, and long maintenance intervals (see [2] for a comparison of compressors)—was used to charge the pressure tank that supplies the air brakes, pantograph, and other critical loads driven by air pressure, necessitating ultra-high reliability. As such, the compressor system is supplied from a tertiary traction transformer winding during normal operation ("grid operation"), as is typical for auxiliary railway applications [3], and from an on-board battery during startup or extended grid interruptions, with a reduced output power. The key specifications for this particular application are given in Table 1. While, in this work, the focus was on the single-phase to three-phase VSD power conversion system for this particular application, the requirements for single-phase to three-phase variable-speed conversion are quite general (e.g., a 10 kW, 230 Vrms, single-phase VSD in [4], or a single-phase to three-phase VSD with Power Factor Correction (PFC) operation in [5]).

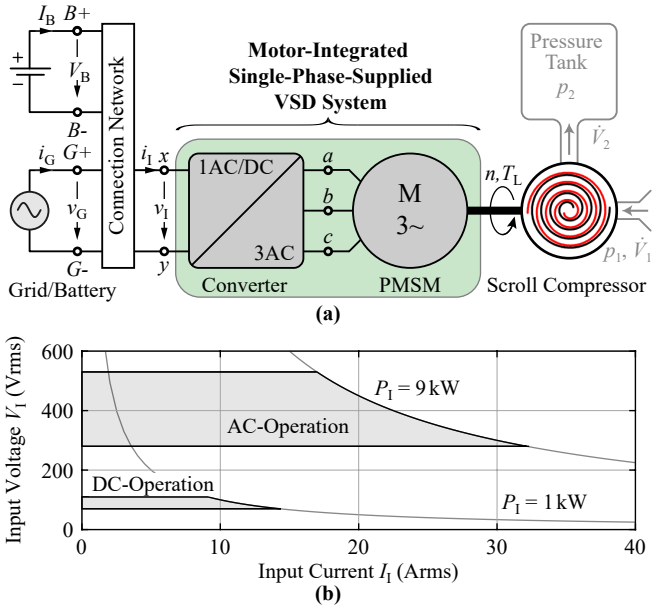

Figure 1. (**a**) Motor-integrated single-phase-supplied Variable-Speed Drive (VSD) system to drive the compressor of an air brake system for railway vehicles. The system can be supplied either from the tertiary winding (AC) of the traction transformer or an on-board battery (DC-supplied operation). (**b**) Required converter input range, including reduced power for DC-supplied operation.

With a VSD system required to increase compressor performance [6], the application needs a power electronics system to convert the single-phase AC—or DC, under battery operation—input voltage into a symmetrical three-phase voltage system, where the magnitude and frequency can be adjusted to control the motor speed (and, accordingly, output power). A three-phase Permanent Magnet Synchronous Motor (PMSM) was selected for high torque, low weight, high efficiency, and compactness [7]. The VSD was designed for 9 kW of output power (see Figure 1b), to meet the required 7.5 kW of mechanical output power (Table 1) while accounting for system losses and acceleration, must comply with CISPR 11/Class A [8], and must operate under unity power factor operation to minimize harmonic distortion and reactive grid power [9].

Table 1. Key system specifications.

Air Flow Rate at Pressure	850 L min^{-1}, 0.83 MPa
Nominal Speed (n_N)	3700 rpm
Nominal Mech. Power, Grid ($P_{0,N}$)	7.5 kW
Nominal Mech. Power, Batt. ($P_{0DC,N}$)	1.0 kW
Nominal Grid Voltage ($V_{G,N}$)	400 Vrms
Grid Voltage Range (V_G)	280 Vrms to 530 Vrms
Grid Frequency (f_G)	50 Hz
Battery Voltage Range (V_B)	70 Vdc to 120 Vdc
EMI Standard (Input)	CISPR 11/Class A [8]

Conventionally, these power conversion systems are realized with a two-stage system [10] comprising a front-end PFC rectifier, an electrolytic DC-link capacitor to buffer the power pulsation from the single-phase grid supply, and a VSD inverter to drive the motor and compressor [11]. For auxiliary motor drive applications, though, efficiency is not the primary concern—due to the low duty-cycle of operation—and the power density should be maximized for the space- and weight-constrained mobility application. The highest-power-density solution, in the end, is a motor-integrated drive system [12], which eliminates expensive shielded cables [13] and cable reflections [14], which allows for higher

slew rates of the inverter stage power semiconductor switching voltage transitions and/or lower switching losses, exhibits better Electromagnetic Interference (EMI) behavior [12] from integration in a single housing, and allows for combined cooling of the electronics and motor [15]. Motor-integrated VSDs, in sum, result in lower installation and operating costs, but require the integration of all drive components—even the EMI input filter [16]. The requirement for electrolytic capacitors as the single-phase power buffer, though, prevents motor integration, with the elevated operating temperatures [17] of the integrated converter (85 °C to 105 °C) [18] degrading lifetime [19] and/or requiring substantial overdimensioning of these large capacitors.

For the highly desired motor integration of the converter system for these single-phase to three-phase drive applications, then, alternatives to the traditional two-stage approach with an electrolytic capacitor are required. Solutions that synergistically employ the components are considered first. Ultra-low-cost implementations use the grid voltage effectively as one of the motor line-to-line voltages and employ four power MOSFETs and a TRIAC [20], but do not allow a wider range of speed control. To utilize the motor star point as one of the connecting points to the single-phase grid, the motor leakage inductance may be utilized as a boost inductor [21], but this results in unacceptably high voltage stresses (twice the grid peak voltage) for this application, which already features a high-grid-input voltage. The same issue occurs in a low-cost implementation that employs a front-end PFC rectifier with only one bridge-leg and a split DC-link [22]. Coupled power electronics (rectifier to inverter) approaches, such as Z-source-based concepts [23] or matrix converters [24], typically feature an (integrated) active buffer for power decoupling [25], a basic requirement since the matrix converter does not include energy storage [26], which drives the complexity and high component stresses. Current-source structures [27], in the end, only replace the boost inductor with a DC-link inductor (since voltage-source inverters do not require an output filter here) while requiring bidirectional switches, and therefore do not improve the potential for integration. The synergistic approaches, then, do not hold the promise of eliminating the large energy storage components required to buffer the single-phase power pulsation—and if they do start to alleviate the requirement, the penalties appear unacceptably high.

Accordingly, this work proposes to use the motor (and load) inertia as a power buffer, eliminating the need for power buffering in the DC-link capacitors, an approach called the MPPB and introduced in [28]. A conventional two-stage structure was utilized, with a single-phase front-end PFC rectifier and a three-phase VSD inverter, with the power flow for a conventional system and the MPPB system shown in Figure 2a. Although particular rectifier and inverter topologies were selected and demonstrated here, the findings are applicable to any specific implementation of the rectifier and inverter.

The MPPB concept was previously proposed with the PFC rectifier omitted and the inverter stage directly supplied from a single-phase-grid diode bridge rectifier [29]. This concept results in a rectifier sine wave voltage at the DC-link, so the input current is only sinusoidal if the motor voltage stays below the rectified input voltage [30]. This concept, then, is limited to motors with a low back Electromotive Force (EMF) and/or applications where a large speed variation is acceptable—but in both cases, a unity power factor cannot be achieved. In [31], a solution to this problem was proposed, where a reactive current component was injected into the motor to keep the back EMF of the motor below the input voltage. Here, the PFC rectifier can indeed be omitted, but the small motor inductance leads to large motor currents and excessive losses. With this constraint and the large fluctuating DC-link voltage, which increase the system complexity, applications for this approach are restricted to drive systems with special low-voltage motors that do not operate at common voltages.

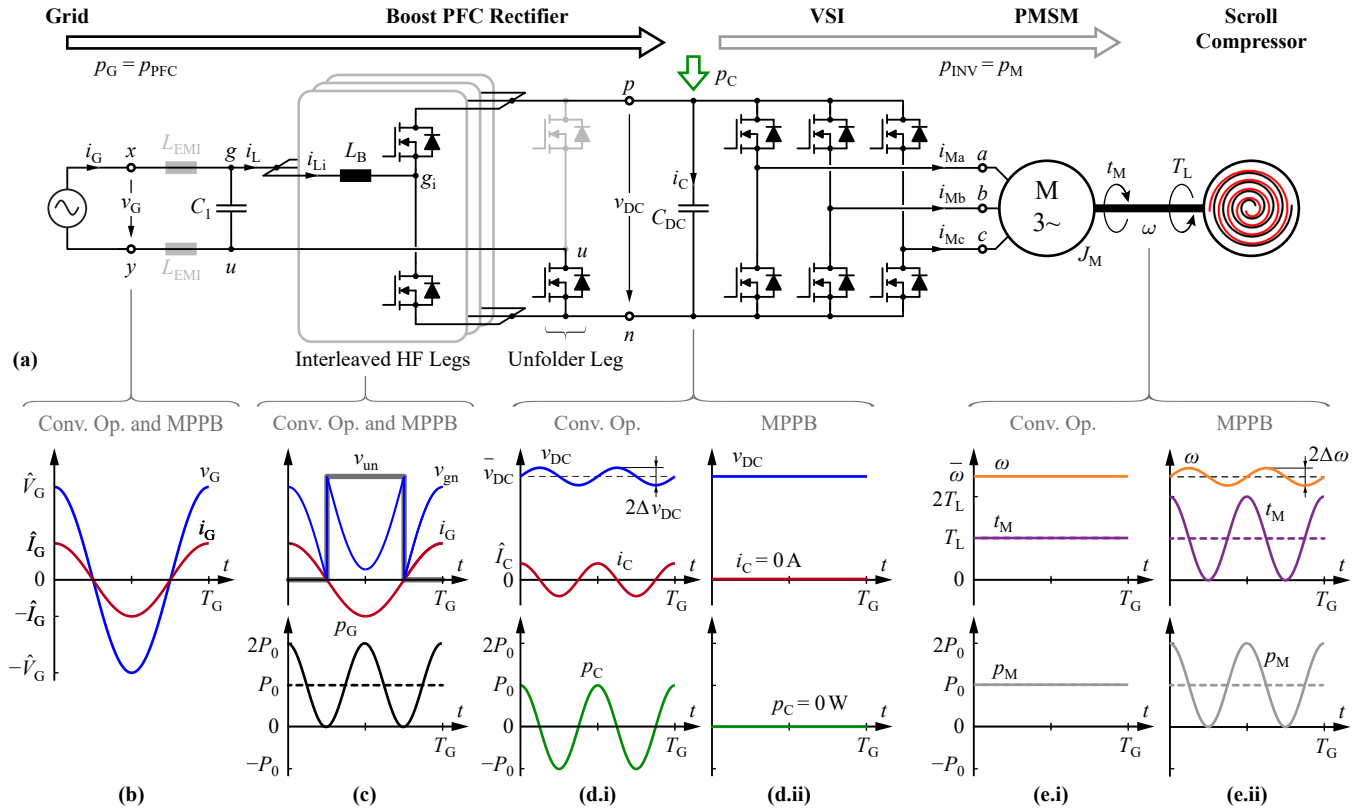

Figure 2. (**a**) Circuit diagram of the selected converter implementation, with a single-phase boost-type totem-pole PFC rectifier to achieve a sinusoidal input current and a conventional two-level three-phase variable-speed inverter that enable the speed control of the associated PMSM. The two converter stages are high-frequencywise, decoupled by a DC-link capacitor C_{DC}. The power flow is indicated with arrows. (**b**–**e**) Characteristic voltage, current, speed, torque, and power waveforms (**d.i**,**e.i**) for conventional operation with an electrolytic capacitor C_{DC}, which buffers the pulsating power drawn from the grid and (**d.ii**,**e.ii**) for the proposed MPPB concept, where the input power pulsation is buffered by the inertia of the motor and no electrolytic capacitor is needed. t_M denominates the inner motor torque. In DC-supplied operation, the battery is connected to the input terminals x and y. © 2018 IEEE. Adapted, with permission, from [28].

In this work, a single-phase-supplied electrolytic-less VSD system with dedicated rectifier and inverter stages that realizes a high lifetime and reduced volume for motor integration is designed, modeled, and implemented. In Section 2, the rectifier and inverter topologies are selected, introduced, and evaluated with the concept and control of the novel proposed MPPB approach to eliminate electrolytic capacitors. In this section, the operational limits for the proposed approach are evaluated for different load cases. The novel control concept for MPPB operation is derived and explained in detail, with verification based on circuit simulation, and finally, the phase currents are investigated in detail to compare the performance of the novel MPPB approach to a conventional system. Section 3 details the implementation of the motor-integrated drive system with volume and loss distributions, including showcasing the motor integration that is uniquely enabled by the novel, proposed MPPB approach. Section 4 verifies the system operation in the time domain for the steady-state and transients, loss models across the full torque range, and EMI requirements and compares the system losses between the MPPB and conventional systems. In Section 5, the extended functionality required for the considered application is demonstrated, including ride-through and battery-supplied operation. The novel control structure can also be employed for DC-supply operation with a single structure that simplifies the implementation and maintenance effort of the system. Section 6 concludes and summarizes the MPPB approach and results of the work, with Appendices that specifically

investigate low-speed operation in the context of the proposed approach (Appendix A), controller design and future enhancements (Appendix B) to reduce the DC-link voltage ripple (including novel feedforward terms), and the detailed phase currents under MPPB operation (Appendix C).

2. Topology Selection and Proposed MPPB Concept and Control

2.1. Topology

Although the proposed MPPB concept is applicable to a broad range of inverter and rectifier topologies, a particular configuration for the demonstration was selected in this paper to explain and, later, showcase the MPPB concept. Conventional systems in these applications utilize a two-stage design with a single-phase PFC rectifier, a large low- and high-frequency-decoupling DC-link capacitor, and a three-phase VSD inverter. A similar two-stage topology was desired here for a straightforward comparison and implementation of the MPPB concept relative to the state-of-the-art.

A single-phase PFC rectifier can be implemented with multiple topologies, components, and control schemes, and these options were reviewed extensively in [32]. A unidirectional boost PFC rectifier with a diode bridge, boost inductor, and transistor and diode pair is widely used for simplicity and low-cost [33]; here, instead, a totem-pole PFC with an unfolder bridge-leg (see Figure 2a) was selected to improve the performance by avoiding the diode conduction losses [34]. While Zero-Voltage Switching (ZVS) triangular-current-mode schemes could further reduce the semiconductor switching losses [35], a simple Pulse-Width-Modulation (PWM) scheme with a constant switching frequency is preferred for the simplicity of interleaving and operation across a wide AC input voltage range (see Figure 1b). Finally, with a DC-link voltage above 750 V (the peak voltage of the maximum grid voltage), 1200 V power semiconductors must be used, and Silicon Carbide (SiC) Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) were chosen over Insulated Gate Bipolar Transistors (IGBTs) for the lower loss characteristics.

Similarly, a straightforward two-level, three-phase inverter utilizing SiC MOSFETs and directly connected to the motor [36] was selected for the power topology. With SiC MOSFETs and no output filter, a voltage slew rate limitation was required to prevent motor insulating aging [37], with the options and tradeoffs for this slew rate value and implementation highlighted in [38].

The resulting structure with the indicated power flow is shown in Figure 2a, with the grid and rectifier input waveforms under conventional operation shown in Figure 2b,c (see [34] for a more detailed explanation). This structure also supports the necessary DC-input operation, with the battery terminals directly connected to x and y. In this mode, the PFC rectifier operates as a conventional DC/DC boost converter.

2.2. MPPB Concept

At the single-phase grid input, the unity power factor operation dictates that the drive system behaves as an ohmic load with a sinusoidal input current $i_G(t) = \hat{I}_G \cos(2\pi f_G t)$ in phase with the grid voltage $v_G(t) = \hat{V}_G \cos(2\pi f_G t)$, as shown in Figure 2b. The instantaneous input power, however, varies as:

$$p_G(t) = v_G(t)\, i_G(t) = P_0 + \tilde{p}_G(t), \tag{1}$$

with $P_0 = \hat{V}_G \hat{I}_G/2$ (see Figure 2c). A lossless system implies that $p_G(t) = p_{PFC}(t)$ and $p_M(t) = p_{INV}(t)$, and an instantaneous power balance results in:

$$p_G(t) = p_C(t) + p_M(t). \tag{2}$$

Thus, the twice-grid-frequency pulsation $\tilde{p}_G(t) = P_0 \cos(2\pi f_P t)$ with $f_P = 2f_G$ is then forwarded to the DC-link capacitor C_{DC}, under conventional operation, or, under the proposed MPPB approach, through the DC-link and the inverter to the motor.

2.2.1. Conventional Operation with an Electrolytic Capacitor

First, system operation with a conventional approach, utilizing a large electrolytic capacitor at the DC-link, is outlined. The waveforms are shown in Figure 2(d.i),(e.i) for each stage.

Under constant speed $\omega(t) = \bar{\omega}$ and constant torque $t_M(t) = T_L$ operation, the motor power is constant ($p_M(t) = \omega(t)\, t_M(t) = p_{INV}(t) \equiv P_0$), as shown in Figure 2(e.i). With this constant power P_0 and the twice-line-frequency power pulsation, from the grid input, a large intermediate DC-link capacitor C_{DC} was used to cover the active power mismatch between the two stages, where the instantaneous capacitor power is:

$$p_C(t) \equiv p_G(t) - p_M(t) = \tilde{p}_G(t) = P_0 \cos(2\pi f_P t) \tag{3}$$

and the average capacitor power is zero, $P_C = \bar{p}_C(t) = 0\,\text{W}$, as it must be for the periodic steady-state (see Figure 2(d.i)).

With a nearly constant DC-link voltage $v_{DC}(t) \approx \bar{v}_{DC}$ and under the power balance of the capacitor $p_C(t) = v_{DC}(t)\, i_C(t)$, the capacitor current must have an approximately sinusoidal waveform $i_C \approx \tilde{p}_G(t)/\bar{v}_{DC}$ with amplitude $\hat{I}_C \approx P_0/\bar{v}_{DC}$. This capacitor current causes a voltage ripple with amplitude Δv_{DC}, which is typically limited to a certain percentage of the DC-link voltage v_{DC} to provide a nearly constant voltage (as previously assumed) to the inverter. The required capacitance value C_{DC} is:

$$C_{DC} = \frac{P_0}{2\pi f_P} \frac{1}{\bar{v}_{DC} \Delta v_{DC}}, \tag{4}$$

and for this application, a value in the mF range is required. This large capacitance value is, therefore, typically realized with electrolytic capacitors. The capacitor current, in addition to causing the voltage ripple, also results in a low-frequency Root Mean Square (RMS) current stress of the capacitor of $I_{C,LFrms} = \hat{I}_C/\sqrt{2} = P_0/\bar{v}_{DC}\, 1/\sqrt{2}$.

For the nominal operating point of $f_G = 50\,\text{Hz}$, $\bar{v}_{DC} = 650\,\text{V}$ (see Table 2), $P_0 = 8\,\text{kW}$, and a selected $\Delta v_{DC} = 20\,\text{V}$ (see Figure 2(d.i)), the required capacitance is $C_{DC} = 0.98\,\text{mF}$ with a current stress of $I_{C,LFrms} = 8.7\,\text{A}$. This DC-link capacitance can be realized with four 1 mF capacitors *B43742A6108M000* [39] (rated for 500 V and 4.9 A at 105 °C), which are connected in a 2×2 array. This DC-link capacitor alone corresponds to a box volume of 1 L (61 in^3) and 6 W of losses before including the PFC and VSD high-frequency currents. This large—and required—electrolytic DC-link capacitor is a major limitation for power density, motor integration, and converter lifetime [40].

Table 2. Nominal operating point.

Nominal Speed (n_N)	3700 rpm
Nominal Mech. Power, Grid ($P_{0,N}$)	7.5 kW
Nominal Grid Voltage ($V_{G,N}$)	400 Vrms
Grid Frequency (f_G)	50 Hz
DC-Link Voltage (V_{DC})	650 Vdc

To overcome these limitations, alternate capacitor-based Power Pulsation Buffer (PPB) buffer concepts have been proposed in the literature [41]. These circuits all contain an active switching stage and a buffer capacitor stage [42] (often separate, in series [43], or in parallel [44], from the existing DC-link capacitor) with a capacitor cycled with a large voltage ripple Δv_C. With a larger voltage ripple, the required capacitance value is much smaller (according to Equation (4)) and enables foil- or ceramic-based capacitor implementations, but the additional active switching stages incur significant realization effort, complexity, and cost for the overall drive system.

2.2.2. Motor Power Pulsation Buffer Concept

Rather than adding complexity to the drive system's electronics, the pulsating power component $\tilde{p}_G$ can be removed from the converter system by enforcing $p_C(t) \equiv 0\,W$, rather than only enforcing the periodic steady-state condition $\bar{p}_C(t) \equiv 0\,W$. This condition is shown in Figure 2(d.ii). With this constraint and the power balance of Equation (2), the only possible result is to forward to complete the input power through the DC-link and the inverter to the motor [28]. The motor, then, is no longer operated with a constant output power, but with the pulsating grid power itself as $p_M(t) = \omega(t)\, t_M(t) \equiv p_G = P_0[1 + \cos(2\pi f_P t)]$.

Due to the motor inertia J_M (and any additional load inertia), the speed ω changes slowly ($\omega(t) \approx \bar{\omega}$), resulting in a pulsating torque $t_M(t) \approx p_G(t)/\bar{\omega}$ at twice the grid frequency (Figure 2(e.ii)). When the instantaneous input power is larger than the average power, positive torque is applied to the inertia, and the rotating mass is accelerated (speed increases), with the excessive power stored as an increase in kinetic energy $e_{KIN} = J_M\omega^2/2$. In the other part of the mains period, when the input power drops below the average power, negative torque is applied and the rotating mass is decelerated. This causes a pulsating rotational speed $\omega(t)$ with an average $\bar{\omega}$, analogous to the DC-link voltage in the conventional system, where the amplitude of the speed ripple $\Delta\omega$ is (and recalling $P_0 = \bar{\omega}T_L$, where T_L is the load torque):

$$\Delta\omega \approx \frac{1}{2\pi f_P}\,\frac{P_0}{\bar{\omega}J_M} = \frac{1}{2\pi f_P}\,\frac{T_L}{J_M}. \tag{5}$$

This concept buffers the pulsating power in the inertia of the motor, an approach called the Motor-Integrated Power Pulsation Buffer. The basic operation is similar to the working principle of conventional single-phase motors [45], although with the VSD capabilities required here and for most modern motors.

Another way to conceive of the approach, then, is that the motor acts as both a drive and a flywheel, which are used independently for peak power reduction in traction systems [46], peak power supply within railway grids [47], smoothing of the output power of renewable power sources such as wind power [48], or within dynamic voltage restorers [49]. Because low-speed motors have a large moment of inertia J_M and high-speed motors have high rotational speeds ω, the stored kinetic energy of the mechanical system is typically orders of magnitude larger than the required energy to buffer the electric power pulsation at the input, leading to a very small variation in the rotational speed ω around its average value $\bar{\omega}$ (for J_M according to Table 3, $\Delta\omega = 7.3\,rad/s = 70\,rpm$ or 1.9%). Analogous to the capacitor current, though—although here with a DC offset of the average torque—the MPPB concept results in a large twice-line-frequency variation in the mechanical torque between zero and twice the average torque value. The MPPB concept offers a fundamental simplicity with the potential to significantly reduce or, theoretically, even eliminate the DC-link capacitor as the energy storage.

In Equation (5), a linear relationship between the speed ripple amplitude $\Delta\omega$ and the load torque T_L is observed, and the validity of the MPPB concept across the complete range of motor speeds must be investigated. Under variable speed operation, the load torque may also depend on the current speed based on the load torque speed characteristic. This relationship is defined around the nominal load torque $T_{L,N}$ at a nominal average speed ω_N, with an exponential dependence between torque and speed as $T_L = T_{L,N}(\bar{\omega}/\omega_N)^k$. The speed ripple under the MPPB operation can then be defined as:

$$\Delta\omega \approx \frac{1}{2\pi f_P}\,\frac{T_{L,N}}{J_M\omega_N^k}\,\bar{\omega}^k. \tag{6}$$

For $k > 1$, which includes fans, blowers, or centrifugal pumps ($k = 2$), the load torque and speed ripple grow faster than the average speed ($\Delta\omega \propto \bar{\omega}^2$), so the worst-case ripple in both absolute and relative terms occurs at the nominal speed and nominal torque operating

point. For $k = 1$, the ripple amplitude scales linearly with speed ($\Delta\omega \propto \bar{\omega}$), resulting in a constant relative ripple. It is important to point out that in both cases, i.e., for $k \geq 1$, the speed ripple will be much less than the average speed ($\Delta\omega << \bar{\omega}$) at all operating points—including speeds close to zero—if the condition is met at the nominal operating point, and the time-varying speed is defined as $\omega(t) \approx \bar{\omega}$.

For applications where $0 \leq k < 1$, however, the absolute speed ripple grows slower than the average speed ($\Delta\omega \propto \bar{\omega}^k$). This may occur for a constant torque load T_L (the $k = 0$ condition), for which an application could be a compressor with constant back pressure [50]—the use case considered in this paper. In this case, the absolute speed ripple amplitude is in a first approximation (see Equation (6)) independent of the speed and constant. This condition results in a lower limit on the average speed, since an instantaneous negative speed needs to be prevented for the MPPB operation (to avoid a transfer of energy from the motor to the DC-link). To a first approximation, this implies a lower absolute speed limit of $\bar{\omega} - \Delta\omega = 0\,\mathrm{rad/s}$ and a lower speed limit for continuous operation of $\bar{\omega}_{\min} \approx \Delta\omega$ (this limit does not apply to transient operation). In the vicinity of $\bar{\omega}_{\min}$, however, the approximation $\omega(t) \approx \bar{\omega}$ is no longer valid. Therefore, this lower speed limit is investigated in detail in Appendix A.

2.3. Control

Relative to the conventional control technique for a two-stage system, the MPPB control can be realized with identical high-frequency current control and a modification of only the coupling in the top-level structure between the PFC rectifier and the inverter. Therefore, the control structure of a conventional system is detailed first before moving to the needed modifications for the MPPB technique.

2.3.1. Conventional Control Overview

In conventional single-phase-supplied VSD systems, the PFC rectifier and the inverter stage are decoupled from one another by the large intermediate DC-link capacitor. The control structures are also mostly decoupled, as shown in Figure 3a.

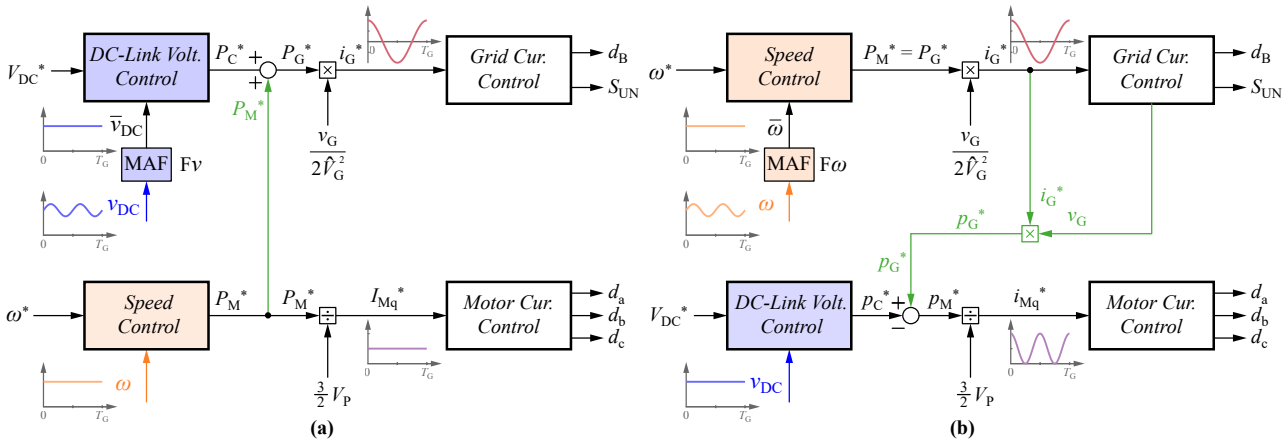

Figure 3. Simplified control structure of (**a**) a conventional implementation of a single-phase-supplied VSD with an electrolytic capacitor and (**b**) the proposed MPPB concept without an electrolytic capacitor. Feedforward signals improve the control quality and are highlighted in green, with characteristic waveforms over one grid period shown adjacent to the relevant control signals. © 2018 IEEE. Adapted, with permission, from [28].

The PFC rectifier control provides a constant DC-link voltage while drawing a sinusoidal current from the grid. Firstly, the power-pulsation-associated voltage ripple in the measured signal is eliminated, either by a Moving-Average Filter (MAF) [51] (shown here) or a conventional low-pass filter. The output of this filter, the obtained average value $\bar{v}_{DC}$, is then compared to the reference V^*_{DC}, and the DC-link voltage control derives the average

capacitor power P_C^*, which can be taken as the average grid power P_G^*, and is then used to generate the input current reference i_G^* for the grid current controller [52]. This results in the duty-cycle for the boost stage d_B and the corresponding switching state of the unfolder leg S_{UN}.

The task of the inverter control is to track the speed reference ω^*, a target that is typically accomplished with a control structure in the dq-coordinate system [53]. The speed control results in the reference motor torque T_M^*, or as shown here, in the reference motor power $P_M^* = \omega^* T_M^*$. Considering a rotor field-oriented control in a rotating dq-reference frame [54], this request can be translated to the torque-generating current I_{Mq}^* by the torque constant k_T or, based on the power balance $P_M^* = 3V_P I_{Mq}^*/2$, where V_P is the induced voltage (assumed proportional to the reference speed and aligned with the q-axis), and the dq-quantities correspond to the phase amplitudes. The motor current control, in the end, determines the duty-cycles d_a, d_b and d_c of the inverter switching stages.

In the conventional approach, the DC-link capacitor compensates the difference of the instantaneous grid power $p_G(t)$ and motor power P_M, so only the average power of the grid P_G and the inverter P_M have to be equal. To achieve this, the conventional control structure typically employs a feedforward of the average motor power P_M^*, where the inverter stage directly informs the rectifier stage about the needed output power (Figure 3a) and thus improves the control performance of the PFC rectifier. For PFC operation, P_G^* is not allowed to vary within a grid period T_G, which requires a slow DC-link voltage control and a bandwidth-limited feedforward (or this could be achieved with an additional low-pass filter, which is not shown here).

2.3.2. MPPB Control Overview

For the proposed MPPB control structure, the average grid power P_G must still match the average motor power P_M, as $P_G = P_M = P_0$. Here, though, the power pulsation is buffered by the motor inertia, causing a (small) speed ripple that should be eliminated in the signal measurement, as the DC-link voltage ripple was in the conventional control scheme.

The speed controller, then—which drives the required average motor power P_M^* from the difference between the reference speed ω^* and average speed $\bar{\omega}$—defines the grid power $P_M^* = P_G^*$ and, therefore, the grid current i_G^* (see Figure 3b). Again, P_G^* must be bandwidth limited (here, slow speed control) to prevent a distortion of the grid current.

The instantaneous input power $p_G^* = v_G i_G^*$ is derived and feed-forwarded to the motor control, resulting in the time-varying q-current i_{Mq}^*, which causes the torque pulsation. Here, though, a stable DC-link voltage v_{DC} must be ensured, and the DC-link voltage control block achieves this by deriving the instantaneous reference power p_C^* from the reference value V_{DC}^* and the unfiltered measurement v_{DC}.

According to the power balance Equation (2), this quantity is then subtracted for the instantaneous motor power request:

$$p_M^*(t) = p_G^*(t) - p_C^*(t). \tag{7}$$

The elegance of the MPPB approach, then, is the utilization of identical control blocks that are simply connected in a different configuration. The MPPB control, then, can be implemented with only software modifications and could even be retrofitted into existing deployments.

2.3.3. MPPB Control Details

In the proposed approach, the primary challenge is that the speed control defines the average grid power, but the inverter must ensure that the *instantaneous* input power is forwarded to the motor; otherwise, with a small DC-link capacitance, the difference could charge the DC-link capacitor rapidly and lead to catastrophic failures. To address this critical challenge and highlight the other details of the MPPB control technique, the

simplified control structure of Figure 3b is extended and shown together with the power topology in Figure 4.

To achieve a high quality for both the power and current alongside a high dynamic control at the output, the control structures were realized in a cascaded fashion. The outer loops for speed and DC-link voltage control provide the current setpoints for the grid and motor current control inner loops, with the motor current control implemented in the dq-coordinate system [53] using the mechanical rotor angle ε [54] provided by the encoder of the PMSM.

This encoder angle is also used to derive the instantaneous speed ω, shown at the bottom of Figure 4, which is then filtered by a MAF [51] with $T_{\mathrm{MAF}} = T_{\mathrm{P}} = T_{\mathrm{G}}/2$ to eliminate the speed ripple in the measured signal. Inside the speed control block, $\bar{\omega}$ is compared to the reference ω^*, and the speed controller Rω derives the reference average motor torque T_{M}^*, which results in the reference average motor power $P_{\mathrm{M}}^* = T_{\mathrm{M}}^* \omega^*$ and the average grid power as $P_{\mathrm{G}}^* = P_{\mathrm{M}}^*$.

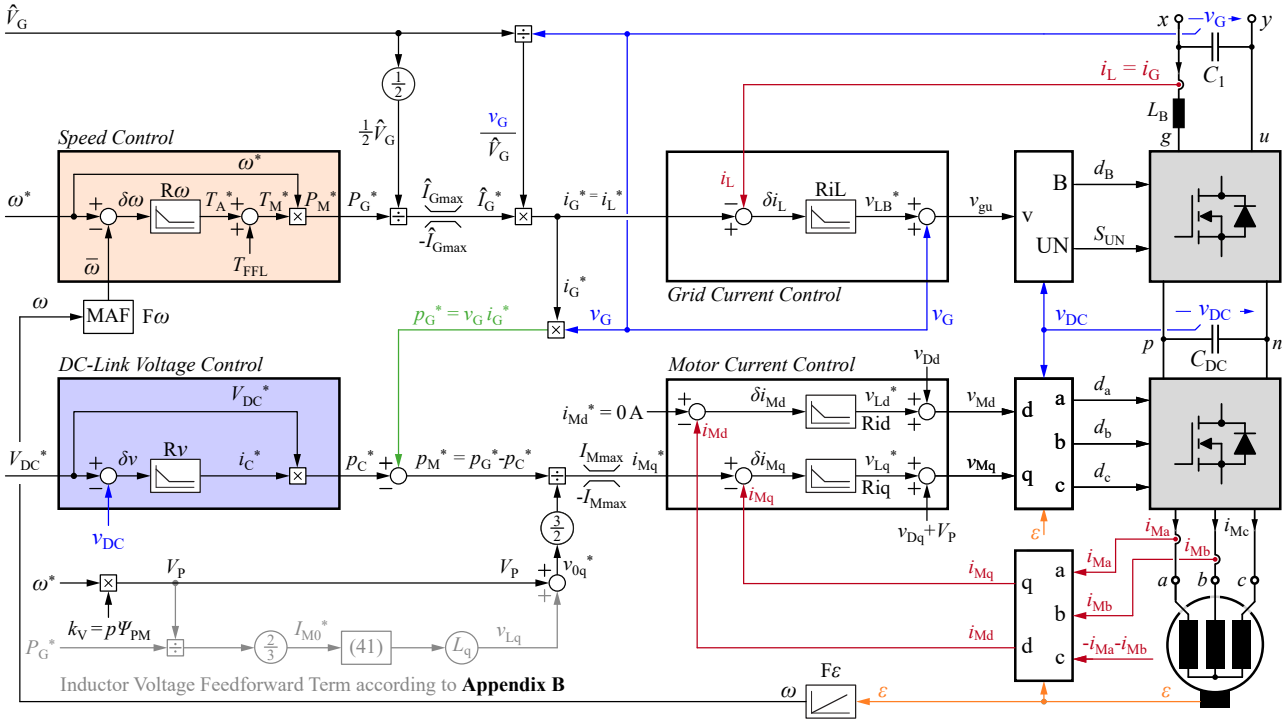

Figure 4. Control structure of Figure 3b with full implementation details, indicating the cascaded controller blocks, the dq-coordinate motor current control, and all required measurements. The addition of an inductor voltage feedforward term is described in Appendix B. © 2018 IEEE. Adapted, with permission, from [28].

The grid current controller requires the grid current reference as an input, which is translated from P_{G}^* using the power balance of the grid $\hat{I}_{\mathrm{G}}^* = 2P_{\mathrm{G}}^*/\hat{V}_{\mathrm{G}}$. This result is then limited to a maximum current amplitude $\hat{I}_{\mathrm{Gmax}}$, which is the minimum of (*a*) the maximum rectifier input current and (*b*) the current amplitude that corresponds to the power the inverter can deliver to the motor (the sum of the instantaneous mechanical output power and the system losses). The instantaneous grid current request, then, results from $i_{\mathrm{G}}^* = v_{\mathrm{G}}\hat{I}_{\mathrm{G}}^*/\hat{V}_{\mathrm{G}}$ and equals the inductor current as $i_{\mathrm{L}}^* = i_{\mathrm{G}}^*$. The grid current controller RiL compares the requested current to the measured inductor current, adds the the resulting boost inductor voltage v_{LB}^* to the measured terminal voltage v_{G}, and translates this sum to the boost duty-cycle d_{B} and the switching state of the unfolder S_{UN}. For interleaved boost bridge-legs, an additional balancer control unit would need to be included [55].

The power feedforward term $p_{\mathrm{G}}^* = v_{\mathrm{G}} i_{\mathrm{G}}^*$ to the motor current control block, subsequently, is derived from the measured terminal voltage v_{G} and the reference grid current

i^*_G. This feedforward term significantly reduces the control effort of the DC-link voltage controller, where the capacitor power request p^*_C is derived from the DC-link voltage reference V^*_{DC} and the measured and unfiltered DC-link voltage v_{DC}. The reference motor power p^*_M, the input to the motor current controller, results then from Equation (7).

The motor current controller, here, avoids field weakening [56] for simplicity; therefore, $i^*_{Md} = 0\,A$ is selected, and the produced torque is only proportional to the q-current i_{Mq}. The motor power balance results in $p^*_M = 3v^*_{0q}i^*_{Mq}/2$ as $i^*_{Md} = 0\,A$, with $v^*_{0q} \approx V_P = p\Psi_{PM}\omega^*$ as the induced voltage, which is dependent on the speed, the number of pole pairs p, and the permanent magnet flux Ψ_{PM} (or, more conventionally, the product of the latter two, the motor constant $k_V = V_P/\omega^* = p\Psi_{PM}$).

Inside the motor current controller, the current setpoints $i^*_{Md} = 0\,A$ and i^*_{Mq} are compared to the the instantaneous current values i_{Md} and i_{Mq}, which are derived from the phase current measurements by the Park transform. The current controllers Rid and Riq then derive the reference motor inner inductor voltages v^*_{Ld} and v^*_{Lq}, which are translated to the inverter duty-cycles d_a, d_b, and d_c after including the motor voltage feedforward V_P and the decoupling terms $v_{Dd} = -\omega pL_q i^*_{Mq}$ and $v_{Dq} = \omega pL_d i^*_{Md}$ (which depend on the reference currents and the motor inductances L_d and L_q) for the required motor voltages v_{Md} and v_{Mq}. The motor current control supports the inclusion of an additional Common-Mode (CM) voltage component for overmodulation [57], if desired.

2.3.4. Simulation Results

With the concept and the detailed control structure for the proposed MPPB concept each outlined, the approach was verified through simulation for the nominal operating point of Table 2. The circuit parameters of Table 3 were used, highlighting especially that only 60 µF of the DC-link capacitance is required for an 8 kW system. The controller design for the simulation (and later, for the implementation) is described in further detail in Appendix B.

The corresponding waveforms at a mechanical output power of 7.5 kW and 3700 rpm are shown in Figure 5, where the grid current i_G is in phase with the grid voltage v_G for unity power factor operation and the product of the grid current and grid voltage resulting in pulsating input power, translated to a torque pulsation. The torque t_M pulsated, as expected, around the average of $T_L = 19.4\,Nm$. When $t_M(t) > T_L$, the motor speed increased, and when $t_M(t) < T_L$, the motor speed decreased, resulting here in a symmetric speed ripple amplitude of $\Delta n = \pm 61$ rpm around the average of 3700 rpm. The DC-link voltage contains a low-frequency peak-to-peak ripple of around 34 Vpkpk, a direct consequence of the limited control bandwidth of the DC-link voltage control and a limitation that can be addressed through the improvements discussed in Appendix B. Overall, the simulation results verified the correct and expected operation, and next, the performance of the MPPB-operated system was evaluated.

2.4. Performance Evaluation

Aside from the significant reduction in required DC-link capacitance, the MPPB concept has no effect on the performance of the PFC rectifier or on the performance of the EMI filter. The effect of the proposed concept can be analyzed on only the motor and the inverter, then starting with the time-domain impact and subsequently moving to an analysis of the losses.

2.4.1. Time-Domain Waveforms

Under conventional operation, the magnitude of the q-current is given by $I_{M0} = 2P_0/(3V_P)$, and thus, $i_{Md}(t) \equiv 0\,A$ and $i_{Mq}(t) = I_{M0}$. The phase currents are derived using the inverse Park transform [54] with $\varepsilon = p\bar{\omega}t + \varepsilon_0$:

$$\begin{bmatrix} i_{Ma} \\ i_{Mb} \\ i_{Mc} \end{bmatrix} = \begin{bmatrix} \cos(\varepsilon) & -\sin(\varepsilon) \\ \cos\left(\varepsilon - \frac{2\pi}{3}\right) & -\sin\left(\varepsilon - \frac{2\pi}{3}\right) \\ \cos\left(\varepsilon + \frac{2\pi}{3}\right) & -\sin\left(\varepsilon + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_{Md} \\ i_{Mq} \end{bmatrix} \tag{8}$$

This results in three purely sinusoidal and symmetrical phase currents, each with the peak value I_{M0}, as shown in Figure 6a. These phase currents are evaluated—and later, compared to the same values under MPPB operation—by the absolute average current I_{PH0avg}, the RMS value I_{PH0rms}, and the peak current I_{PH0pk} as (with T the minimum period of the signal):

$$I_{PH0avg} = \frac{1}{T}\int_0^T |i_{Ma}(\tau)|d\tau = \frac{2}{\pi}I_{M0} \quad (9)$$

$$I_{PH0rms} = \sqrt{\frac{1}{T}\int_0^T i_{Ma}^2(\tau)d\tau} = \frac{1}{\sqrt{2}}I_{M0} \quad (10)$$

$$I_{PH0pk} = \max i_{Ma}(t) = I_{M0}. \quad (11)$$

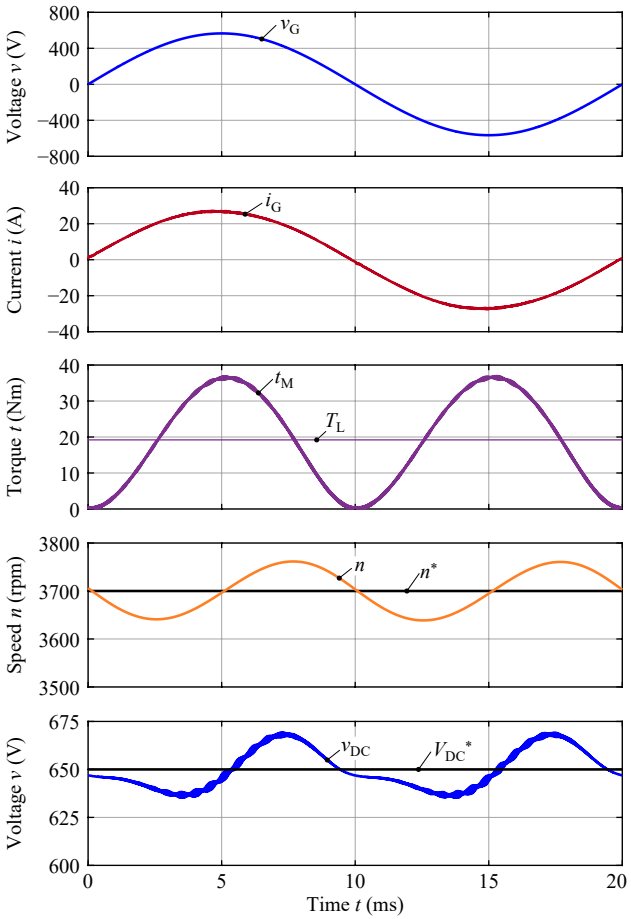

Figure 5. Simulated waveforms of the grid voltage v_G, grid current i_G, motor torque t_M, rotational speed n, and DC-link voltage v_{DC} during steady-state, nominal operation, verifying the proposed MPPB concept and control structure. © 2018 IEEE. Adapted, with permission, from [28].

To analyze the proposed MPPB operation, constant speed (with $\omega(t) \approx \bar{\omega}$) was assumed, which resulted in a constant induced voltage $V_P = k_V\omega \approx k_V\bar{\omega}$, and the instantaneous q-current was $i_{Mq}(t) = 2p_M(t)/(3V_P)$. Using $p_M(t) = P_0[1 + \cos(2\pi f_P t)]$, the q-current proportional relationship to the instantaneous torque is:

$$i_{Mq}(t) \approx I_{M0}[1 + \cos(2\pi f_P t)] \propto t_M(t), \quad (12)$$

where the magnitude I_{M0} is the same as under conventional operation.

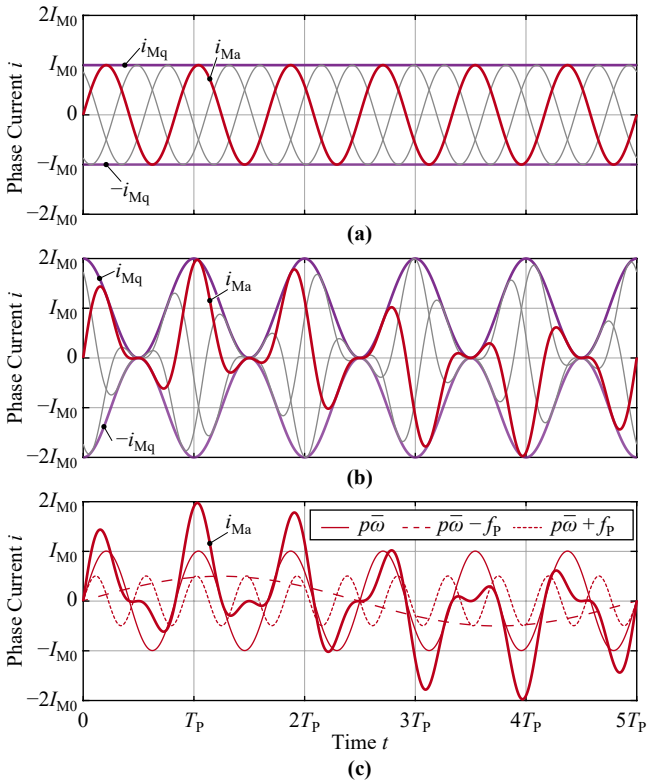

Figure 6. Phase currents i_{Ma}, i_{Mb}, and i_{Mc} and the enveloping currents $\pm i_{Mq}$ for the (**a**) conventional and (**b**) MPPB operation for $f_P = 100\,\text{Hz}$ and $p\bar{\omega}/(2\pi) = 120\,\text{Hz}$. (**c**) Spectral decomposition of the first phase current i_{Ma} under MPPB operation. © 2018 IEEE. Adapted, with permission, from [28].

Because the q-current is now, under MPPB operation, pulsating at twice line frequency, the phase currents i_{Ma}, i_{Mb} and i_{Mc} into the motor are no longer purely sinusoidal. These phase currents were found by applying the inverse Park transform to the q-current and are shown in Figure 6b for $f_P = 100\,\text{Hz}$ and $p\bar{\omega} = 2\pi\,120\,\text{Hz}$. The phase current, more precisely, is then $i_{Ma} = -i_{Mq}\sin(p\bar{\omega}t + \varepsilon_0)$, or:

$$\begin{aligned} i_{Ma}(t) &= -I_{M0}\sin(p\bar{\omega}t + \varepsilon_0) \\ &\quad -\frac{I_{M0}}{2}[\sin(p\bar{\omega}t + 2\pi f_P t + \varepsilon_0) + \sin(p\bar{\omega}t - 2\pi f_P t + \varepsilon_0)]. \end{aligned} \tag{13}$$

In addition to the fundamental $p\bar{\omega}$ frequency, the phase currents now contain two additional harmonic components at the frequencies $|p\bar{\omega} + 2\pi f_P|$ and $|p\bar{\omega} - 2\pi f_P|$ with amplitude $I_{M0}/2$, as shown with the spectral decomposition of the phase current for phase *a* in Figure 6c. For certain frequency ratios, these individual sines may collapse into a single frequency, become DC components, or even result in standing waves and an asymmetric phase stress. The precise effect of different frequency ratios is discussed in Appendix C, with the result that such effects occur only in the vicinity of certain speed values $\bar{\omega}$, which are all below or equal to the angular pulsation frequency $\omega_P = 2\pi f_P$, and the assumption $|p\bar{\omega}| > \omega_P$ was used for the remaining analysis here.

Only the sinusoid with frequency $p\bar{\omega}$ is phase aligned with the induced voltage of the corresponding phase, and therefore, only this component generates average torque to drive the load. Because this component is not influenced by the pulsating q-current, there is, as expected, no degradation in the mechanical average torque—but the additional components do increase current stress in the inverter and motor. The RMS current stress was calculated by a superposition of the purely sinusoidal waveforms, with a $\sqrt{3/2}$ factor increase in RMS current. The average current remains unchanged while the peak current doubles as a result of the pulsating q-current. This large increase in peak current has a

limited effect on the iron in the motor, since motors are typically designed in the thermal (rather than the saturation) limit and the flux is primarily defined by the permanent magnet Ψ_{PM}. The key current equations are summarized below, and the relative increase of each current is shown in Figure 7a.

$$I_{PHavg} = \frac{1}{T}\int_0^T |i_{Ma}(\tau)|d\tau = \frac{2}{\pi}I_{M0} \quad (14)$$

$$I_{PHrms} = \sqrt{\frac{1}{T}\int_0^T i_{Ma}^2(\tau)d\tau} = \frac{1}{\sqrt{2}}\sqrt{\frac{3}{2}}I_{M0} \quad (15)$$

$$I_{PHpk} = \max i_{Ma}(t) = 2I_{M0}. \quad (16)$$

With the key current ratios defined, the relative inverter and motor losses between conventional and MPPB operation were analyzed.

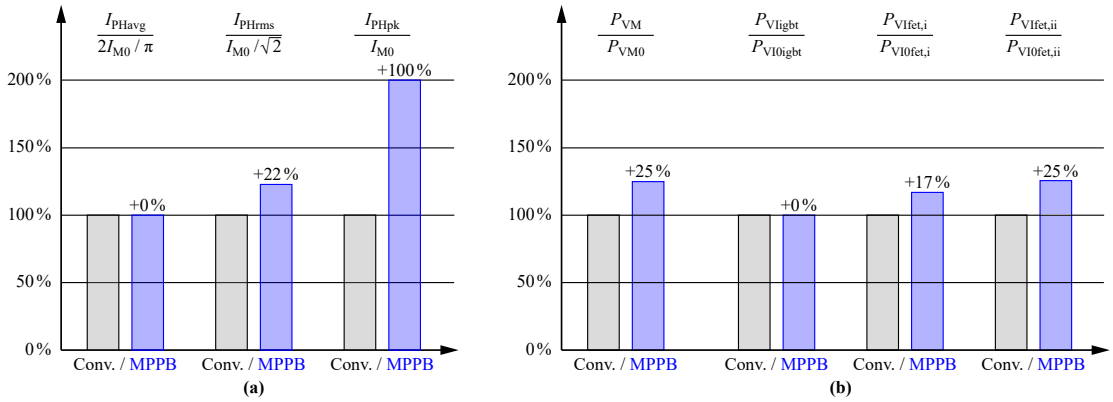

Figure 7. Comparison of (**a**) loss characteristic currents and (**b**) losses under conventional and MPPB operation at the nominal operating point. The loss penalty of the MPPB is evaluated for three inverter realizations: IGBT-based (P_{VIigbt}), MOSFET-based with external Miller capacitors to limit the dv_{DS}/dt of the switching transitions ($P_{VIfet,i}$), and MOSFET-based with the explicit LC output filter stage designed for the dv/dt-limitation of the voltage applied to the motor terminals [58] or full-sine-wave output voltage shaping ($P_{VIfet,ii}$).

2.4.2. Motor Loss Analysis

The motor losses P_{VM} include both speed-dependent no-load losses P_{VMnl} and load-dependent conduction losses $P_{VMcond} = 3R_s I_{PHrms}^2$, with R_s as the stator winding resistance. The motor losses under conventional operation P_{VM0} and under the proposed MPPB operation P_{VM} are:

$$P_{VM0} = P_{VMnl} + \frac{3}{2}R_s I_{M0}^2 \quad (17)$$

$$P_{VM} = P_{VMnl} + \frac{9}{4}R_s I_{M0}^2, \quad (18)$$

where the MPPB operation incurs a 50% loss increase in conduction losses due to the increase in the RMS current. If an equal loss distribution between the no-load losses and the load-dependent conduction losses at the nominal operation point is assumed, which is typically close to an optimum design, MPPB operation incurs a motor loss penalty of only 25%. This loss ratio, along with the inverter loss ratios of the next section, is shown in Figure 7b.

2.4.3. Inverter Loss Analysis

The inverter semiconductor losses P_{VI} comprise conduction P_{VIcond} and switching losses P_{VIsw}. The conduction losses are, most generally, written as $P_{VIcond} = 3V_f I_{PHavg} + 3R_{on} I_{PHrms}^2$, where V_f is the on-state voltage drop and R_{on} is the (differential) on-resistance. The switching losses are written with a quadratic loss function $e_{sw}(i) = k_0 + k_1 i + k_2 i^2$ [59],

which leads to $P_{\mathrm{VIsw}} = 3f_{\mathrm{Isw}}\left(k_0 + k_1 I_{\mathrm{PHavg}} + k_2 I_{\mathrm{PHrms}}^2\right)$ with the inverter switching frequency f_{Isw}. A quick review of these equations shows that the MPPB concept would only affect the ohmic part of the conduction losses and the quadratic part of the switching losses, both with an increase of 50%, through the increase in the RMS current.

If the semiconductors are implemented as IGBTs, conduction losses are given—to a first approximation—by the on-state voltage drop, and the switching losses can be approximated by the linear part alone. For an IGBT-implemented inverter, then, the inverter losses are identical between conventional (P_{VI0igbt}) and MPPB operation (P_{VIigbt}):

$$P_{\mathrm{VI0igbt}} = \frac{6}{\pi} V_{\mathrm{f}} I_{\mathrm{M0}} + 3f_{\mathrm{Isw}} \frac{2}{\pi} k_1 I_{\mathrm{M0}} = P_{\mathrm{VIigbt}}. \tag{19}$$

IGBTs, however, suffer from high overall losses [60], and inverters with SiC MOSFET-based bridge-legs and a $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ limitation should be considered as well.

For a SiC MOSFET-based bridge-leg and external Miller capacitors to limit the voltage slew rate, the conduction losses can be considered ohmic, and the switching losses are described well by the constant and linear part [61], for inverter losses under conventional ($P_{\mathrm{VI0fet,i}}$) and MPPB operation ($P_{\mathrm{VIfet,i}}$), as:

$$P_{\mathrm{VI0fet,i}} = \frac{3}{2} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3f_{\mathrm{Isw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} \right) \tag{20}$$

$$P_{\mathrm{VIfet,i}} = \frac{9}{4} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3f_{\mathrm{Isw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} \right). \tag{21}$$

The motor acts as a resistive–inductive load with a reactive power demand and, therefore, requires a current commutation path for the freewheeling current. The high voltage drop of the body diode of the utilized SiC MOSFETs is typically overcome with an anti-parallel SiC Schottky diode, but the MOSFET itself can also be utilized as a synchronous rectifier. In this case, the freewheeling diode only conducts during the dead time, and the additional losses from the body diode conduction can be neglected (this assumption was extensively analyzed in [62] and verified in Section 3). In this context, it should be also mentioned that early high-voltage SiC MOSFETs were associated with bipolar degradation on their intrinsic body diodes [63], but this problem has been solved for state-of-the-art 1.2 kV devices [64].

Conduction losses increase by 50% under the proposed MPPB operation. If each loss contribution (conduction, constant switching losses, and current-dependent switching losses) is assumed to be 1/3 of the overall inverter losses [61] at nominal operation, the inverter loss penalty is around 17% for MPPB operation with a SiC MOSFET-based bridge-leg and external Miller capacitors to limit the voltage slew rate.

Finally, a realization with a hard-switching SiC MOSFET-based bridge-leg with an LC output filter designed for a $\mathrm{d}v/\mathrm{d}t$-limitation of the voltage applied to the motor terminals [58] or full-sine-wave output voltage shaping was analyzed. The doubling of the peak current will negatively impact the performance of the filter inductor. Here, conduction losses remain ohmic and the switching losses contain all of the terms, for conventional ($P_{\mathrm{VI0fet,ii}}$) and MPPB inverter losses ($P_{\mathrm{VIfet,ii}}$) of:

$$P_{\mathrm{VI0fet,ii}} = \frac{3}{2} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3f_{\mathrm{Isw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} + \frac{1}{2} k_2 I_{\mathrm{M0}}^2 \right) \tag{22}$$

$$P_{\mathrm{VIfet,ii}} = \frac{9}{4} R_{\mathrm{on}} I_{\mathrm{M0}}^2 + 3f_{\mathrm{Isw}} \left(k_0 + \frac{2}{\pi} k_1 I_{\mathrm{M0}} + \frac{3}{4} k_2 I_{\mathrm{M0}}^2 \right). \tag{23}$$

If an equal loss contribution is assumed for all four loss components (conduction losses and the three switching loss terms) at nominal operation, MPPB operation carries a 25% loss penalty over conventional operation for the inverter, similar to the penalty in the motor.

A summary of these inverter loss penalties for different bridge-leg implementations is shown in Figure 7b, where, although the MPPB concept increases the conduction losses by 50%, the maximum total loss penalty is 25%—while realizing a potential volume reduction of up to 1 L (or 61 in^3) by eliminating the DC-link electrolytic capacitors.

3. System Design and Implementation

With the power density improvements—and the possibility of motor integration—of the MPPB-operated system attractive, the system proposed in Figure 2a was next designed and implemented. This hardware demonstrator allows a direct comparison between conventional and MPPB systems on the volume and loss distributions. The motor-integrated converter system is the focus of this section, with brief guidelines given for motor selection and PFC rectifier and inverter designs.

3.1. Motor Selection and Characterization

With the output power $P_{0,N} = 7.5\,\text{kW}$ and speed requirements $n_N = 3700\,\text{rpm}$ leading to a torque specification of $T_{L,N} = 19.4\,\text{Nm}$, the *1FT7-084* from Siemens [65] was selected.

At nominal operation $n_N = 3700\,\text{rpm}$, the motor frequency with $p = 5$ is $p\omega_N = 2\pi 308\,\text{Hz}$, which is sufficiently above $f_P = 100\,\text{Hz}$ to guarantee symmetric phase stresses in the motor and inverter (see Appendix C). The motor inertia of $J_M = 4.5\,\text{mkgm}^2$ corresponds to a speed ripple amplitude, using Equation (5), of $\Delta\omega = 7.3\,\text{rad/s} = 70\,\text{rpm}$, or 1.9% of the nominal speed. The minimal achievable speed in stationary operation for constant torque $T_L(\omega) = T_{L,N}$ is, according to Appendix A, $\bar{\omega}_{min} = 5\,\text{rad/s} \approx 50\,\text{rpm}$. The torque constant is given with $k_T = T/I_{M0} = 0.92\,\text{Nm/A}$ and the given speed constant k_V, which relates the induced pole-wheel peak voltage V_P to the speed n as $k_V = V_P/n = 67.8\,\text{mV/rpm}$, resulting in a nominal phase voltage amplitude of $V_{P,N} = 250\,\text{Vpk}$. The nominal DC-link voltage can then be selected as $V_{DC,N} = 650\,\text{V}$ (cf. Table 2, allowing boost PFC operation up to the nominal input voltage of $V_{G,N} = 400\,\text{Vrms}$ with a 15% margin. For input voltages above nominal, the DC-link voltage is linearly increased up to 800 V at $V_{Gmax} = 530\,\text{Vrms}$, or a peak voltage of 750 Vpk.

The motor was measured to validate the datasheet and build a complete loss model. The stator phase resistance was measured at $R_s = 0.2\,\Omega$ at 40 °C (close to ambient since the winding temperature does not significantly increase during short-time operation and was also respected for the experimental analyses), and the motor inductances were measured at $L_d \approx L_q \approx 3.0\,\text{mH}$, both within 10% of the datasheet values. The speed-dependent, no-load losses from iron losses and friction [66] were measured with the motor driven mechanically and the torque measured at nominal speed n_N, resulting in a no-load torque of $T_{Mnl} = 0.765\,\text{Nm}$ and no-load losses of $P_{VMnl} = \omega_N T_{Mnl} = 296\,\text{W}$.

At nominal speed, the motor current amplitude is $I_{M0} = (T_L + T_{Mnl})/k_T$, which at nominal load is $I_{M0,N} = 21.9\,\text{A}$. Under conventional operation, this RMS phase current is $I_{PH0rms,N} = I_{M0,N}/\sqrt{2} = 15.5\,\text{Arms}$ (cf. Equation (10)), and under the proposed MPPB operation, the phase current is $I_{PHrms,N} = \sqrt{3}I_{M0,N}/2 = 19\,\text{Arms}$ (cf. Equation (15)). With the no-load losses summed with the conduction losses for the total motor losses, $P_{VM} = P_{VMnl} + P_{VMcond}$, or:

$$P_{VM} = \omega_N T_{Mnl} + \frac{9}{4} R_s \left(\frac{T_L + T_{Mnl}}{k_T} \right)^2. \tag{24}$$

The no-load torque increases the motor losses P_{VM} twice—once directly, through the P_{VMnl} term, and additionally by increasing the motor current as T_{Mnl}/k_T and, therefore, increasing the conduction losses $P_{VMcond} = 9R_s I_{M0}^2/4$.

The MPPB-operated motor losses at the average torque are shown in Figure 8, with the nominal losses under MPPB operation of $P_{VM,N} = 517\,\text{W}$ compared to 443 W under conventional operation. This motor loss increase is 16.7%, less than the 25% predicted in Figure 7b since the no-load losses comprise more than half of the total motor losses.

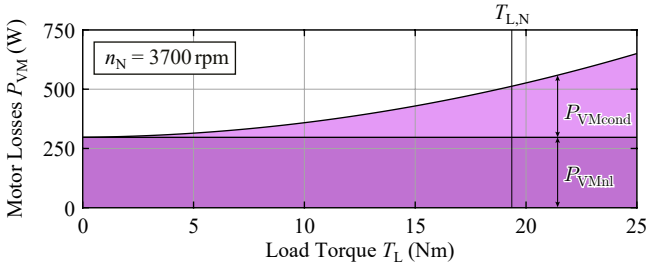

Figure 8. Characterized motor losses P_{VM} under MPPB operation at load torque, comprising speed-dependent no-load losses P_{VMnl} and torque/current-dependent conduction losses P_{VMcond}.

3.2. Converter Design

The complete converter topology is shown in Figure 9 with the components of Table 3, and here, the key pieces of the component selection are highlighted.

3.2.1. Inverter Design

The inverter switching frequency must be outside the audible range (above 16 kHz [67]), but is determined more strictly by the control bandwidth. With a pulsation frequency of $f_P = 100$ Hz, the DC-link voltage control bandwidth was designed to be 5× higher at 500 Hz, the motor current control bandwidth 5× higher than that at 2500 Hz, and the inverter switching frequency 10× higher for an inverter switching frequency of $f_{Isw} \approx 25$ kHz. Due to EMI considerations [68], $f_{Isw} = 24$ kHz was selected.

The 1200 V power semiconductors are required to withstand a DC-link voltage that will be as high as 800 V (plus low- and high-frequency voltage ripple), and SiC MOSFETs are employed instead of IGBTs for high performance [60]. These MOSFETs operate at high voltage slew rates, or dv_{DS}/dt values, which can lead to an unequal distribution of the voltage across the motor windings and partial discharge phenomena [69], resulting in progressive aging of the motor winding insulation [37]. Different solutions to this challenge were discussed and compared in [38], with gate drive modifications preferred [61], for motor-integrated drives that support dv_{DS}/dt values as high as 15 V ns^{-1} (since there are no cable reflections to consider).

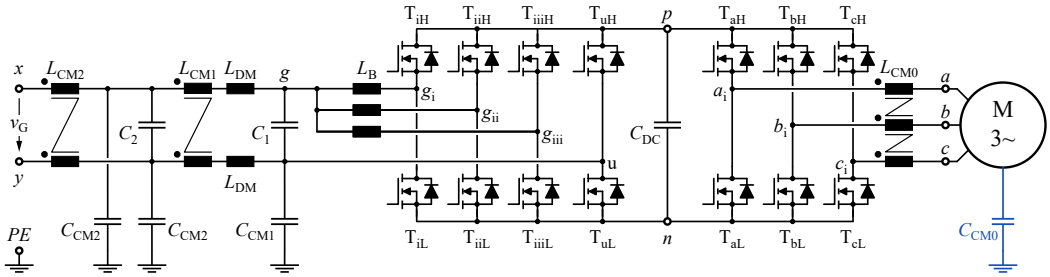

Figure 9. Complete powertrain, with all included components, for the realized motor-integrated VSD system. The component list is detailed below, in Table 3.

Table 3. Component list.

Motor Inertia	J_M	4.5 mkgm^2	Siemens *1FT7-084* [65]
CM-Motor Capacitance	C_{CM0}	1.9 nF	Siemens *1FT7-084* (measured)
Inverter Transistors	T_{aH}, T_{aL}, T_{bH}, T_{bL}, T_{cH}, T_{cL}	16 mΩ/1.2 kV	Cree *C3M0016120K* [70]
PFC Unfolder Transistors	T_{uH}, T_{uL}	16 mΩ/1.2 kV	Cree *C3M0016120K* [70]
PFC Boost Transistors	T_{iH}, T_{iL}, T_{iiH}, T_{iiL}, T_{iiiH}, T_{iiiL}	32 mΩ/1.2 kV	Cree *C3M0032120K* [71]
DC-Link Capacitance	C_{DC}	3 × 20 µF/900 V	Epcos *B32776E9206K000*, Foil
Boost Inductor	L_B	428 µH (each)	4 E-Cores/30 Turns Flat Wire

Table 3. *Cont.*

DM-Filter Capacitance	C_1	$4 \times 1\,\mu F$	Epcos *B32914A5105M000*, X1
DM-Filter Capacitance	C_2	$1\,\mu F$	Epcos *B32914A5105M000*, X1
DM-Filter Inductance	L_{DM}	$4.7\,\mu H$ (each)	Wuerth *74436410470*
CM-Filter Capacitance	C_{CM1}	$2 \times 20\,nF$	Vishay *440LS20-R*, Y1
CM-Filter Capacitance	C_{CM2}	$2 \times 20\,nF$ (each)	Vishay *440LS20-R*, Y1
CM-Filter Inductance	L_{CM0}	$75\,\mu H$	$6 \times$ VAC *L2025-W380*, 1 Turn
CM-Filter Inductance	L_{CM1}	1.6 mH	VAC *L2045-V102*, 9 Turns
CM-Filter Inductance	L_{CM2}	1.0 mH	VAC *L2045-V102*, 7 Turns

The optimal chip area was selected for the inverter power semiconductors, all of which were implemented as next-generation $16\,m\Omega$ SiC MOSFETs (*C3M0016120K* [70]). A gate driver with an output clamp variant was selected [72] that drives the transistors at the maximum positive ($V_{G,on} = 15\,V$) and minimum negative ($V_{G,off} = -4\,V$) gate drive voltages for enhanced noise immunity. A $15\,\Omega$ gate resistor was added for turn-on and turn-off to stay below $dv/dt = 15\,V\,ns^{-1}$, as investigated in [61].

As previously mentioned, synchronous rectification was employed for the MOSFETs within the inverter [62], with the body diode therefore only conducting during the dead time t_D. Under the worst-case condition, where the body diode conducts the full-phase current within both dead time intervals of a switching period and with the diode forward voltage drop $V_F = 4.6\,V$ [70] and the selected inverter dead time of $t_D = 400\,ns$, the losses under nominal operation are $P_{VIdiode} = 3\,f_{Isw} 2 t_D\,V_F I_{PHavg} = 3.7\,W$ (where I_{PHavg} is from Equation (14)). These losses represent less then 5% of the calculated inverter losses $P_{VI} = 81.6\,W$ and can be safely neglected.

3.2.2. DC-Link Capacitor Selection

The minimum DC-link capacitance was determined by the high-frequency-voltage ripple caused by the PFC rectifier and the inverter [73]. Due to disturbances and the limited control bandwidth of the DC-link voltage control, though, there was a remaining low-frequency voltage ripple (see Figure 5). This ripple could be addressed with increased bandwidth; however, in the end, this would require an increase in switching frequency, and the corresponding increase in switching losses would eliminate this option. Instead, to keep the peak-to-peak voltage ripple below 40 V, an increased DC-link capacitance of $C_{DC} = 60\,\mu F$ was selected based on circuit simulations. This capacitance requirement was only $7.5\,\mu F\,kW^{-1}$.

The chosen capacitors must be rated for at least 800 V, eliminating both ceramic *X6S* capacitors (which are only available up to 400 V, and would therefore require hundreds of series-stacked capacitors) and *CeraLink* capacitors, where only small capacitance values are available. Three $20\,\mu F$ foil capacitors *B32776E9206K000* [74] were selected, resulting in a total volume of only 0.13 L (or $8\,in^3$)—equal to just 13% of the required electrolytic capacitor volume under conventional operation.

3.2.3. PFC Rectifier Design

Because the rectifier is not affected by the MPPB approach, a conventional PFC rectifier design was implemented (even in [75], the electrolytic capacitors comprised 25% of the overall converter volume). This rectifier must be designed to provide the maximum power across the entire input voltage range (see Figure 1b), with a maximum input current of 32 Arms (or 45 Apk).

The unfolder was implemented with the lowest-possible $R_{DS,on}$ device *C3M0016120K* [70], which resulted in a maximum of 19.6 W of conduction losses at the voltage minimum and 9.6 W at nominal operation. To limit the component stresses of the high-frequency bridge-leg, which is subject to high-frequency switching losses, an interleaved design with three branches was selected. This supports an increase in effective switching frequency for the same semiconductor losses [76], an improved loss distribution, and the reuse of the

design for future three-phase-supplied VSD systems. Each bridge-leg was operated with a switching frequency of 48 kHz to keep the frequency multiple below the stricter EMI considerations at 150 kHz. The high-frequency bridge-leg power semiconductors were again selected with the optimal chip area and implemented with 32 mΩ four-pin devices (*C3M0032120K* [71]) for bridge-leg losses of $P_{\mathrm{VRhb}} = 8.8$ W at nominal operation.

The PFC rectifier inductor design was selected from the optimal front of a Pareto optimization based on the guidelines of [77], and this selected inductor was implemented with four stacked *K4317E040* Kool-Mu cores with a relative permeability of forty and thirty turns of flat wire (7 mm × 0.5 mm) (note that the permeability of Kool-Mu is current-dependent, and the inductance varies between 428 µH and 342 µH [78]). The inductor has a boxed volume of 100 cm^3 (33.6 × 41.5 × 72 mm) and $P_{\mathrm{VRind}} = 9.5$ W of expected losses at the nominal operating point. The filter capacitor C_1 is subject to a current ripple at the interleaved frequency of 144 kHz, with the first and second harmonic canceled, and a 4 µF capacitance was selected with an implementation of four parallel X-rated 1 µF capacitors.

3.2.4. EMI filter

This high-frequency bridge-leg interleaving also eliminates the fourth and fifth harmonic components, and the Differential-Mode (DM) EMI filter therefore needs to be designed to meet CISPR 11/Class A [8] at the DM noise of the PFC rectifier at 288 kHz. With the design guidelines of [79], CISPR 11/Class A can be met with $C_2 = 1$ µF and $L_{\mathrm{DM}} = 4.7$ µH.

The common-mode noise is typically defined by the parasitic capacitance to the Earth, which is often dominated by the thermal interface material layer between the power semiconductors and the grounded heat sink. Here, the largest parasitic capacitance originates from the motor [80] at $C_{\mathrm{CM0}} = 1.9$ nF. The CM EMI filter, therefore, is designed for the inverter noise occurring at the 7th harmonic of 168 kHz. Again, following the design of [79], $C_{\mathrm{CM1}} = C_{\mathrm{CM2}} = 40$ nF, $L_{\mathrm{CM1}} = 1.2$ mH, and $L_{\mathrm{CM2}} = 0.8$ mH meets CISPR 11/Class A at 168 kHz. Both CM inductors were evaluated at 168 kHz, and they employ *L2045-V102* nanocrystalline cores [81] with seven and nine turns, respectively. An additional CM choke on the motor side L_{CM0}—to damp high-frequency CM currents inside the system and reduce the potential for radiated emissions [82]—was implemented with six *L2025-W380* [81] cores with one turn each and provided a series impedance of 75 µH inductance and a damping resistance of 100 Ω at 168 kHz.

3.3. Volume and Loss Distribution

These selected components are summarized in Table 3, resulting in the system loss breakdown at the nominal operating point (Table 2) of Figure 10a. The rectifier ($P_{\mathrm{VR}} = 74.9$ W) and inverter ($P_{\mathrm{VI}} = 81.6$ W) stages comprise a nearly equal contribution to the system losses, which are dominated by the motor ($P_{\mathrm{VM}} = 534$ W). Beyond the no-load and conduction losses characterized in Figure 8, the motor incurs an additional 17 W of capacitive switching losses, where the parasitic motor capacitance is charged and discharged with the PWM voltage impressed by the inverter bridge-legs. The total drive system losses are $P_{\mathrm{VDS}} = 703$ W, corresponding to a system efficiency at nominal operation of $\eta_{\mathrm{DS}} = 91.4\%$.

The volume distribution of the system is shown in Figure 10b, with a boxed volume of the complete drive system at 8.2 L (or 500 in^3) resulting in a power density of 0.91 kW L^{-1} (15 W in^{-3}). The outer motor dimensions are 205 mm × 105 mm × 105 mm, for a total boxed volume of 4.9 L (or 300 in^3), that is 60% of the system. The converter, at 3.3 L (or 200 in^3), accounts for the remaining 40% of the system volume (including the encoder). Without the MPPB concept, the electrolytic capacitor volume *alone* would account for 1 L (or 61 in^3), adding 30% to the converter and 12% to the total system—and preventing integration due to the lifetime considerations discussed previously.

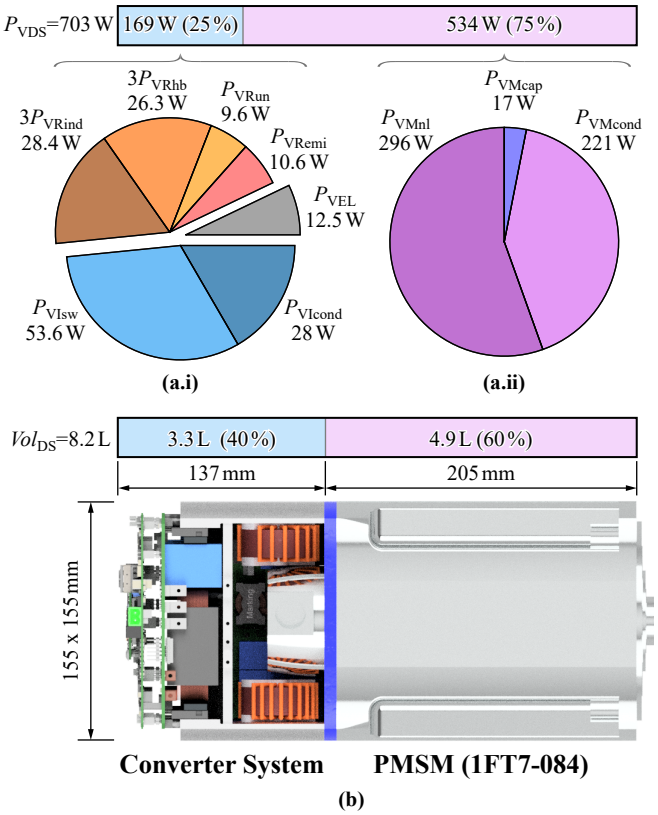

Figure 10. (**a**) Loss breakdown at the nominal operating point for the (**i**) inverter and (**ii**) motor. (**b**) Volume distribution for the realized demonstrator.

3.4. Detailed Motor Integration and Implementation

The motor integration must allow a retrofitting of an existing motor within the same flange dimension, mandating an axial stator mount of the power electronics system (options for motor integration were surveyed in [83]). The implementation is shown in Figure 11, with the three-level stack up and construction detailed side by side.

Firstly, the end plate was replaced to provide an interface for the converter system. The first level of the integrated drive system (Figure 11a) contains the EMI filter components, which were distributed around the encoder. Cables were mounted to the corresponding side walls to connect to the grid CM inductors, which were also connected to the filter Printed Circuit Board (PCB). The filter PCB contains all of the remaining DM and CM filter components and was connected to the Earth and the motor housing. An Earth- and housing-connected copper plate (not shown) was installed between the EMI filter and the motor-side CM inductor to provide shielding, and similarly, an aluminum plate was installed between the first and second levels to *(a)* shield the filter from the bridge-leg high-frequency noise and *(b)* provide mechanical stability.

The second converter level (Figure 11b) contains all power components, including the power semiconductor bridge-legs, the boost inductors, and the DC-link capacitors. The bridge-legs were connected to the DC-link capacitors through the power PCB and to the motor windings through the motor-side CM inductor. Critically, the vast majority of the converter losses were generated in this second level, resulting in the highest temperature, and this was where the electrolytic capacitors would need to be placed to connect to the DC-link—making a system with electrolytic capacitors infeasible.

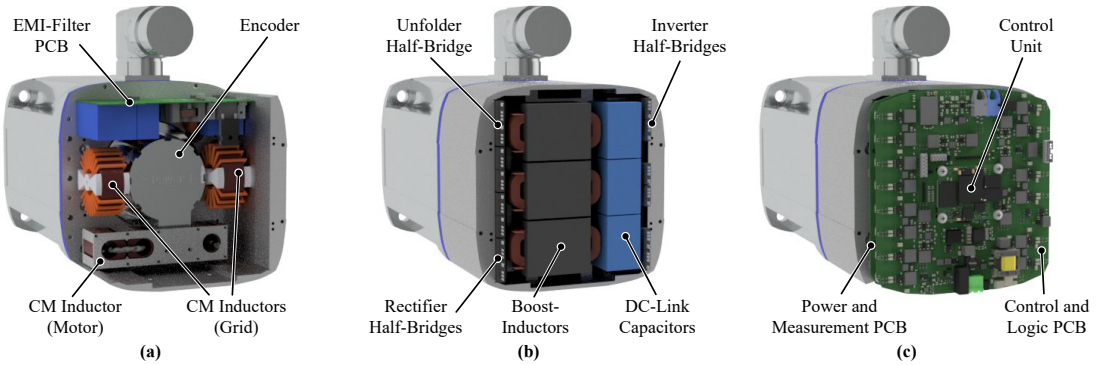

Figure 11. Motor integration of the VSD system, built up in three layers from left to right. (**a**) Encoder and filter components, (**b**) power components, and (**c**) circuitry and control unit.

The third level (Figure 11c) contains the gate drive, measurement, control, and logic circuitry on two separate PCBs, with the control unit on the top. Converter losses are cooled via the surface—and the thermal resistance (and insulation) can be improved through potting, if desired—with the large thermal capacitance improving the thermal characteristics significantly, since the system is not operated at full power for extended periods. The final motor-integrated drive is shown in Figure 12.

Figure 12. Photograph of the complete motor-integrated, MPPB-operated, single-phase-supplied, variable-speed-drive system of Figure 1.

4. Hardware Demonstration Verification

To evaluate the motor-integrated hardware demonstrator of Figure 12, the overall operation of the drive system across the continuously varying operating points, motor drive speeds, and torque fluctuation was evaluated. Full operation cannot be validated with a resistor–inductor (RL) load alone, and a complete motor test bench was employed here (instead of driving the compressor itself). This test bench comprises a motor bed, the Device-Under-Test (DUT), a speed and torque sensor (*TM310* with a maximum torque bandwidth of 5 kHz from Magtrol [84]), and a load motor operated with a commercially available drive system from Siemens with a constant load torque [50]. An identical setup was employed for the no-load measurements of Section 3. First, the concept was validated with time-domain measurements and waveforms. Then, the loss model was verified, and

EMI measurements were taken before validating the extended functionality (distorted grid voltage, ride-through operation, and battery supply operation) in Section 5.

Note that, due to the limited availability of the optimal 16 mΩ power semiconductors specified in Table 3, all transistors were implemented as the 32 mΩ device (*C3M0032120K* [71]) for the following measurements.

4.1. Time-Domain Waveforms and Operation

Firstly, the theoretical aspects of Section 2 were verified for the nominal operating point, as described in Table 2. The measured waveforms are shown in Figure 13, where the grid current (20.6 Arms) and voltage were in-phase for unity power factor operation (measured at 99.95%) at 8.2 kW input power, a steady DC-link voltage near the reference of 650 V, and a speed equal to the reference of 3700 rpm with a speed ripple so small that it is not visible on this oscilloscope capture. The low-frequency ripple of the DC-link voltage is investigated in depth in Appendix B and corresponds here to 35 Vpkpk, nearly identical to the simulation results of 34 Vpkpk shown in Figure 5. The measured motor currents are shown in Figure 14, corresponding to a phase current stress of 18.5 Arms and, again, matching the theoretical results in both behavior and predicted amplitude. Overall, the system behavior was correct and expected, validating the MPPB approach and the predicted operation.

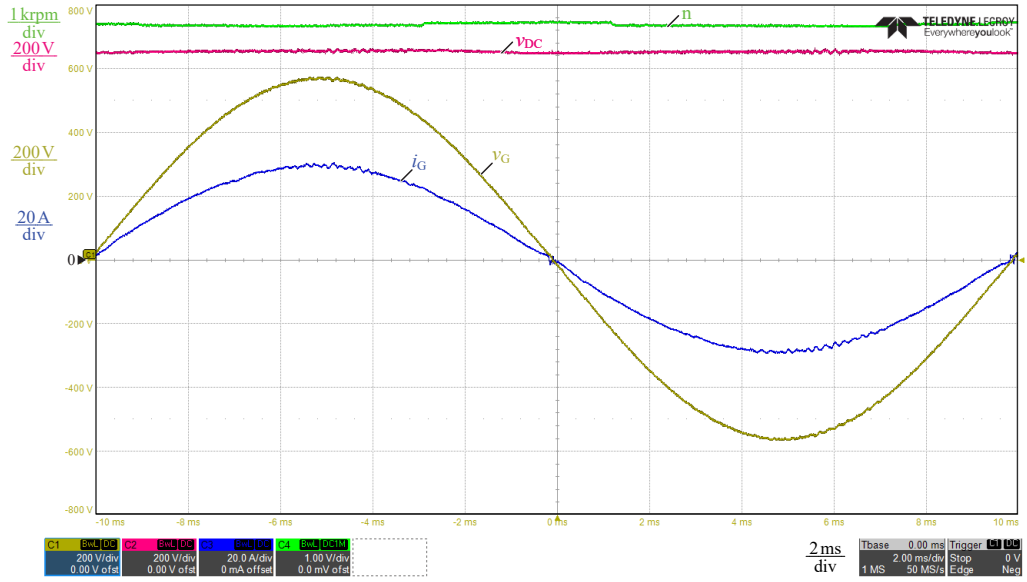

Figure 13. Measured waveforms under steady-state, nominal operation: grid voltage (yellow), DC-link voltage (red), grid current (blue), and speed (1000 rpm/div, green).

4.2. Efficiency

With the foundational operation of the MPPB approach verified, the introduced loss model was verified at nominal speed and DC-link voltage across the required mechanical output power range. Grid power input was measured with the *Yokogawa WT3000 precision power analyzer*, and the mechanical quantities were measured with a speed and torque sensor. For all calculations, the measured stator phase resistance of $R_s = 0.2\,\Omega$ was used, as the system was verified for the short-time operation needed for this particular application. With the MPPB approach encompassing the complete system, the difference in the measured input (grid) and mechanical output powers was the drive system losses P_{VDS}. These measured losses are shown across load torque—and, accordingly, mechanical output power—as the bullet points in Figure 15a. These measurements match the proposed loss model nearly precisely, validating both the proposed power converter and motor loss models under the proposed MPPB operation.

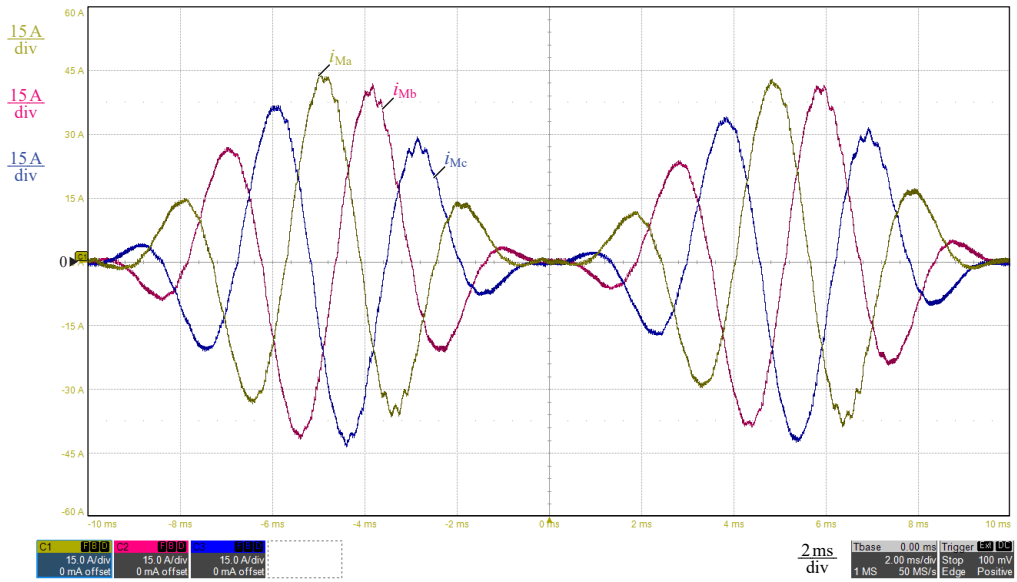

Figure 14. Measured three-phase motor current waveforms under steady-state, nominal operation.

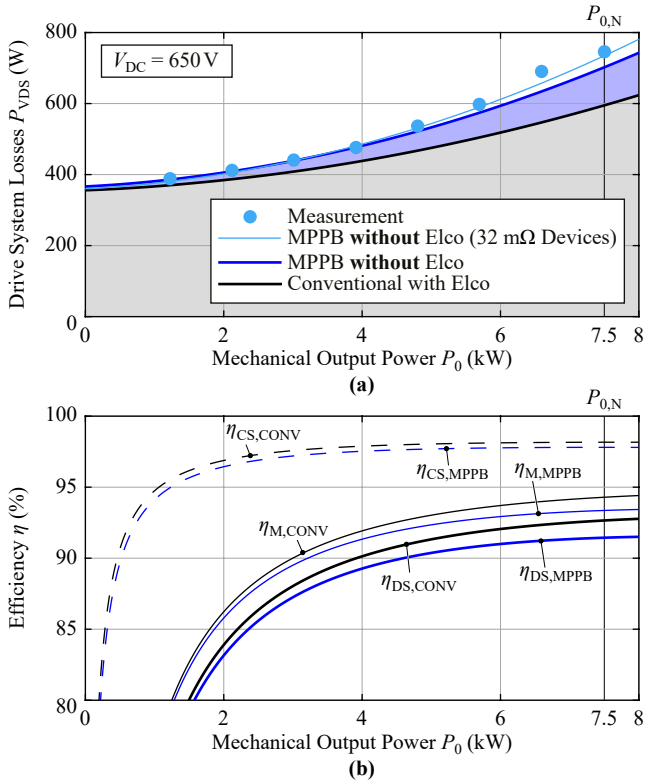

Figure 15. (**a**) Drive system losses across mechanical output power P_0 at nominal speed 3700 rpm with a DC-link voltage of 650 V. Measurements are indicated by bullets and match the introduced loss models. (**b**) Converter, motor, and drive system efficiencies for conventional operation (black) and MPPB operation (blue).

Next, the efficiency penalty associated with the significant power density increase of the MPPB concept was quantified, and the constructed MPPB system was compared to a conventional system with an electrolytic capacitor. The conventional system features lower phase current stresses, leading to lower currents and lower conduction losses in the motor and the inverter bridge-legs, but suffers from additional losses in the DC-link electrolytic capacitors. At the nominal output power, the system losses increase from 600 W for a grid-to-motor-shaft efficiency of 92.6% in the conventional system with an electrolytic

capacitor to 703 W (91.4%) with the MPPB approach, for a loss increase of 103 W, or 17%. This loss increase is the maximum across the operating load area, both in absolute and relative terms, with the load-dependent difference highlighted in blue in Figure 15a.

Figure 15b shows the motor, converter, and drive system efficiencies for conventional and MPPB operation over the output power range, where the converter efficiencies are nearly identical at around 98%. The overall efficiency is primarily limited by the motor itself, with the extra losses in MPPB operation contributed mostly by the additional phase current stresses. The MPPB system achieves a grid-to-motor-shaft efficiency above 90% for all loads above 5 kW (66% of the nominal load), a high and flat efficiency for the exceptional power density of the motor-integrated, electrolytic capacitor-less MPPB-operated system.

4.3. Conducted EMI

Because the drive system was tested in full operation on the motor bed, all measurements for EMI were conducted according to CISPR 16 for floor-standing equipment [85]. As discussed in the Introduction and highlighted in Table 1, the conducted EMI of the drive system in the frequency range of 150 kHz to 30 MHz must comply with the CISPR 11/Class A QP limit [8] (limits shown in Figure 16).

Both phases x and y of the drive system were scanned with a maximum peak detector with a step size of 1%, a bandwidth of 9 kHz, and a measurement time of 10 ms, and we report the results in Figure 16.

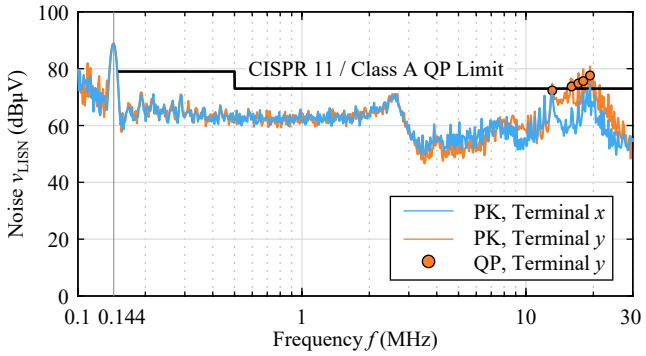

Figure 16. Measured conducted maximum peak (PK) EMI noise emissions of the prototype drive system (with the motor and converter mounted separately for safety and measurement), measured at a step size of 1%, a 10 ms measurement time, and with a bandwidth of 9 kHz for both phases x and y. Selected peaks (bullets) are measured with the quasi-peak (QP) detector with a 1 s measurement time [8].

Compliance with CISPR 11/Class A across the vast majority of the frequency space was verified, with only certain frequencies above 15 MHz exceeding the limit and the largest QP violation of 4.6 dB at 19.3 MHz in phase y. Selected measurement points in this regime were verified with a CISPR 11 quasi-peak detector ("QP") with a 1 s measurement time. These peaks, however, are only caused by the EMI test condition, where the converter and motor were separated and connected with a cable for safety and measurement, and the completed system would achieve CISPR 11/Class A compliance across the full considered frequency range.

4.4. Transient Response

To this point, steady-state operation was assumed. Next, the transient behavior of the system was analyzed to verify the controller performance of the MPPB approach. Figure 17 shows the system behavior for both a change in the reference speed and a step change in the instantaneous load torque.

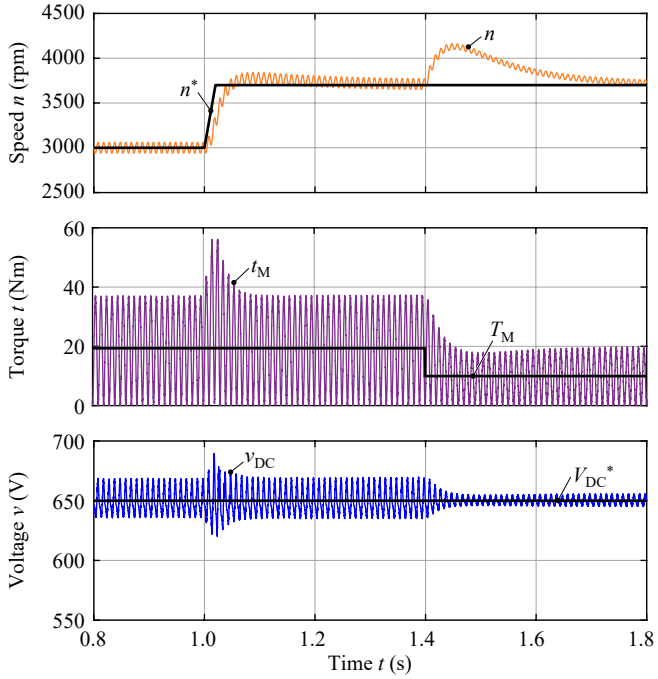

Figure 17. Dynamic response of the proposed control structure with a speed step at $t = 1$ s and a load torque step at $t = 1.4$ s. The reference speed n^*, the speed n, the load T_L, the motor torque t_M, the DC-link voltage v_{DC}, and the DC-link voltage reference V_{DC}^* are presented. For both steps, the system requires around 350 ms to return to steady-state. © 2018 IEEE. Adapted, with permission, from [28].

The system begins in steady-state operation at 3000 rpm and with a nominal load torque of $T_{L,N} = 19.4$ Nm, and there are steady-state speed, torque, and DC-link voltage ripples, as previously discussed. At $t = 1$ s, the reference speed was increased linearly to $n^* = 3700$ rpm over 20 ms, and the input power and average motor power increased to ramp the motor speed to match this reference. The maximum applied instantaneous torque reaches 56 Nm, and this transient causes a small disturbance in the DC-link voltage with a maximum deviation of 40 V. This voltage disturbance decays after around 100 ms, and the speed reaches steady-state after 350 ms.

At $t = 1.4$ s, the load torque decays instantaneously to 10 Nm, which is approximately half of the nominal torque. Again, the MPPB approach elegantly controls the system, with a short speed increase to 4169 rpm. The motor torque reaches steady-state after 100 ms, and the speed reaches steady-state after 350 ms. It should be noted that the DC-link voltage ripple will scale with the motor torque; cf. Figure 17.

5. Extended Functionality

To this point, the assumption was that the system operates with a purely sinusoidal grid input voltage, which is the nominal operating condition, but not sufficient to meet the complete set of application requirements. In this section, drive system functionality was validated under three abnormal conditions that were required for the application—with a distorted grid voltage, with a voltage sag on the grid, and with short- or long-term grid interruptions. These were analyzed and verified in turn.

5.1. Operation with a Distorted Grid Voltage

Industrial voltage supplies—and especially railway grids [86]—can be heavily distorted [87], with a grid voltage better described with the addition of a noise term v_{noise} as $v_G = \hat{V}_G \sin(2\pi f_G) + v_{noise}$. Under these conditions, a sinusoidal input current must still be drawn to minimize the grid stress [88]. While the noise components could be eliminated with a low-pass filter, this filter necessarily introduces an additional phase shift ($v_G^* = \hat{V}_G \sin(2\pi f_G + \varphi)$) that degrades the power factor away from unity. Therefore,

operation with a distorted grid voltage is addressed by reconstructing the fundamental of the grid voltage v_G^* around a Phase-Locked Loop (PLL) [89].

The PLL results in the input to the grid-current controller as $v_G^* = \hat{V}_G^* \sin(2\pi f_G)$, as shown in Figure 18. While PLLs based on a three-phase grid are simple to generate based on the orthogonal $\alpha\beta$-voltage system, the single-phase grid here requires an alternate approach. Instead, a Second-Order Generalized Integrator (SOGI) was used to derive v_{ff} and v_{fi} from the single-phase input voltage [90] based on the measured grid voltage v_G as the input. The SOGI outputs v_{ff}, v_{fi}, and v_{pk} to the PLL block, which is used to derive the grid frequency f_{PLL}—fed back as the second input of the SOGI in a coupled system.

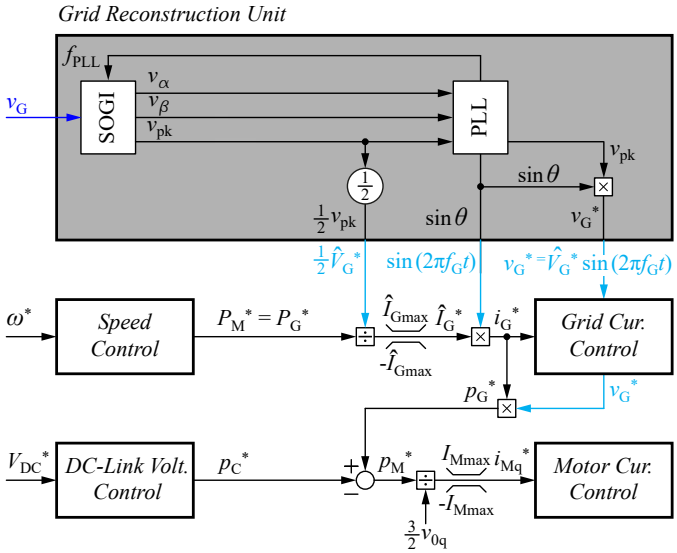

Figure 18. Details of the grid reconstruction unit control structure to achieve sinusoidal input current without a phase shift, even with heavily distorted grid input voltages.

The PLL derives the phase angle $\theta = 2\pi f_G t$, and following $\hat{V}_G^* = v_{pk}$, $v_G^*/\hat{V}_G^* = \sin\theta = \sin(2\pi f_G t)$, the grid voltage is reconstructed $v_G^* = \hat{V}_G^* \sin(2\pi f_G + \varphi)$. This v_G^* was used for the grid current controller input and was also used for the power feedforward term, as shown in Figure 18.

5.2. Operation under Grid Voltage Sag or Interruption

More specifically, the drive must operate correctly under two additional fault conditions: voltage sags, where the input voltage falls below the specified range, and grid interruption, where the grid provides no voltage for a period. The exact conditions for each of these faults were discussed comprehensively in [91].

Continued operation under fault conditions increases system reliability, uptime, safety, and financial payback, and grid-tied industrial applications often require ride-through operation to minimize downtime (e.g., in general converter systems [92] or for drives [93]). Under a fault, the system must both (*a*) not trip, keeping the system operational, and (*b*) apply the full requested torque, without significant delay, after the interruption or sag. This effect on the MPPB concept, where no significant electrical or electrochemical energy storage is included, must be analyzed.

5.2.1. Voltage Sag

The proposed MPPB system achieves the required operation under grid voltage sag by design, with:

- A large specified grid tolerance (of approximately ±30%; see Figure 1b) to cover the majority of sag cases with full-power operation;

- Even with the voltage outside of the specifications, the control structure detailed in Figure 18 will cover the voltage sag condition at reduced power, where the grid current limiter freezes speed control once the limit is reached. The control scheme guarantees rapid recovery, as shown later.

5.2.2. Grid Interruption

Railway systems regularly experience short-term grid interruptions in the range of several tens of milliseconds [94]. In conventional systems, these interruptions are easily covered by the DC-link capacitance energy storage—which is not present in the proposed MPPB approach, requiring a further investigation of the operation under grid interruption.

During grid interruption, there is no sinusoidal input voltage and no power can be extracted from the grid. When the phase lock of the PLL is lost, the PFC rectifier stops operating (all gates are turned off) and an idle power semiconductor state is entered, similar to the first state of startup. The PFC operation flag switches from $\mathrm{ON_{PFC}} = 1$ (normal operation) to $\mathrm{ON_{PFC}} = 0$, and the grid power request drops from the motor power $P_\mathrm{G}^* = P_\mathrm{M}^*$ to zero, $P_\mathrm{G}^* = 0\,\mathrm{W}$, as shown in Figure 19 for ride-through operation.

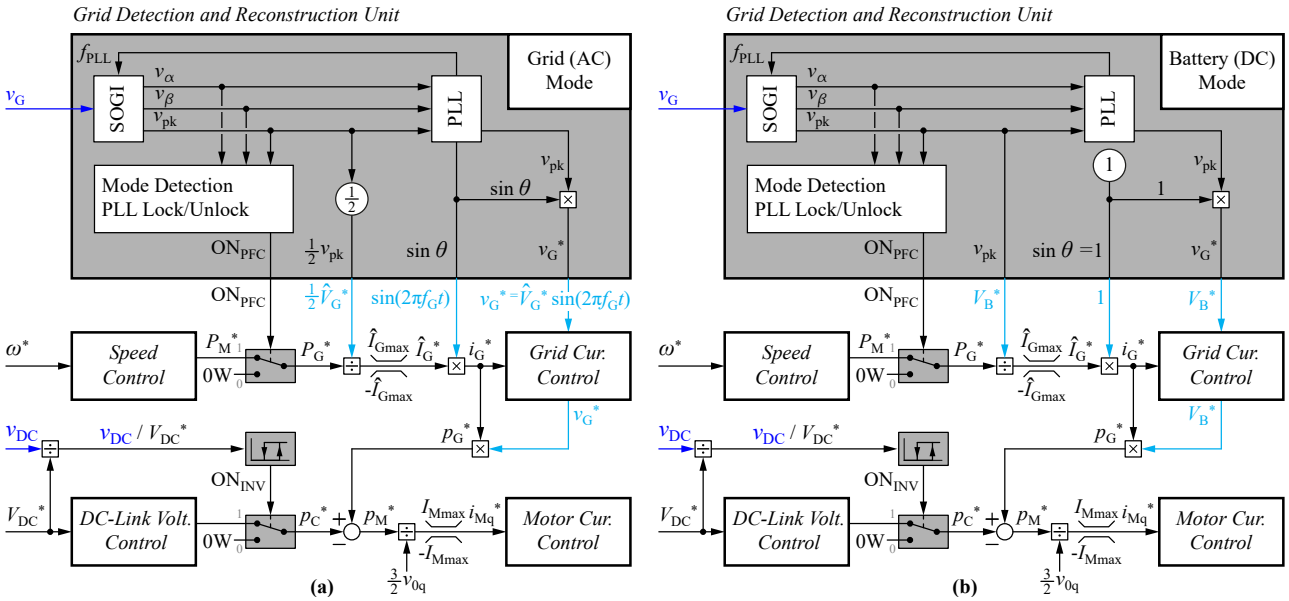

Figure 19. Details of the control structure—with PLL and SOGI blocks—to implement startup or ride-through operation for both (**a**) AC operation and (**b**) DC operation. Only the AC-referenced quantities change for DC-supplied operation, with no change in control structure or values.

Without electrical (or other) energy storage within the system, the compressor can no longer be driven, and the load torque of the compressor slows the rotational speed of the motor (the compressor is supplied from the kinetic energy storage of the motor inertia). During this period, the speed controller is frozen—all stored variables are continuously initialized with the instantaneous values to prevent triggered step responses—but the inverter remains turned on ($\mathrm{ON_{INV}} = 1$) to maintain the DC-link voltage control, which is now decoupled from the grid input (since the feedforward term is now $p_\mathrm{G}^* = 0\,\mathrm{W}$). The DC-link voltage control, then, continues to ensure that the DC-link voltage is driven to the reference voltage, which is supplied again by the motor inertia, and the rotating mass decelerates more quickly (and even more quickly if additional loads, such as discharge resistors or logic supply or fans, are connected to the DC-link).

At this point, with the decelerating motor supplying the DC-link to maintain the reference voltage, two cases—short-term and long-term interruptions—were analyzed separately.

Short-term interruption: If the grid returns while the system is still rotating (and supplying the DC-link), only the PFC rectifier needs to be re-synchronized, and the grid power can be ramped to stabilize the mechanical speed of the motor. Because the DC-link voltage is maintained above the voltage peak of the grid, no pre-charging state is required and the response time is fast.

This performance is verified in Figure 20, where a 100 ms interruption at a power level of 3.4 kW results in a fast and stable recovery to the mechanical speed request. When the grid is interrupted, PFC operation stops and the grid current goes to zero. The speed drops linearly with $d\omega/dt = T_L/J_M$ (under constant torque operation, which is the worst-case condition). When the grid returns after 100 ms, the PFC synchronizes and ramps up the motor power, and there is a reduction in the rate of the speed decay, which becomes zero at $\omega T_L = P_G$ (the speed minimum). From there, the control returns the motor to the desired steady-state speed, which occurs without significant DC-link voltage oscillations—even with the elimination of the DC-link energy storage capacitors provided by the MPPB approach. The recovery time could be even further shortened with the addition of a non-linear speed controller.

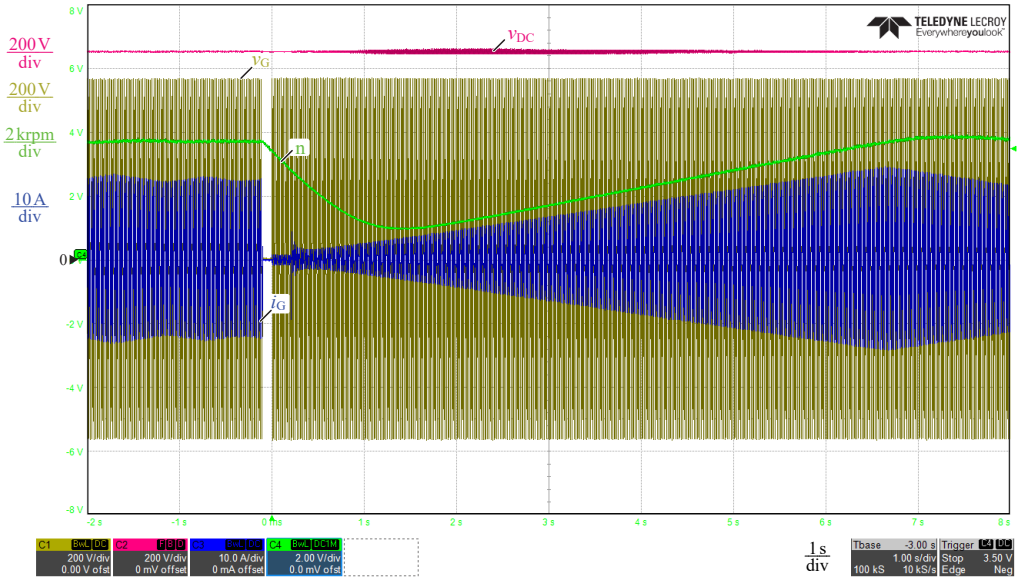

Figure 20. Measured system transient performance for ride-through of a 100 ms grid interruption at 3.4 kW mechanical output power: grid voltage (yellow), DC-link voltage (red), grid current (blue), and speed (2000 rpm/div, green).

The survivable ride-through time depends primarily on the speed before the interruption, the total kinetic energy, and the instantaneous load torque (or the pressure of the tank; see Figure 1). If the motor stops rotating, the battery supply starts, the final extended functionality case explored here.

Long-term interruption and battery supply operation: The system will enter standstill if the motor speed decays to zero and the DC-link voltage can no longer be maintained (with no remaining kinetic energy). At this point, the DC-link and inverter control are turned off and the systems returns to a state similar to before the initial startup.

The DC-link voltage controller was implemented with a hysteresis control based on the ratio of the instantaneous and reference DC-link voltages, and this supports the direct utilization of this concept for startup.

If the grid interruption is sustained, the switching network of Figure 1a connects the battery supply instead of the grid, and the "DC grid" is detected by the grid detection and reconstruction unit (see Figure 19b). The identical control structure, with identical controller gains, is reused for DC grid operation, with the grid-dependent variables in AC operation replaced by their DC equivalents (see the replacements between Figure 19a,b).

This implementation requires a single software code base for both operation modes, simplifying the implementation, testing, and maintenance. Of course, the traditional approach, similar to Figure 3a, could also be followed for DC operation, but this would increase the software effort for the design, validation, maintenance, and operation, where the two modes of operation would need to be actively switched during an extended grid voltage interruption. Because this introduces further complexity to the system, the approach of Figure 19 is preferred.

DC grid operation with a battery voltage of 100 V and a DC-link voltage of 150 V is validated in Figures 21 and 22, with sinusoidal motor currents as shown in Figure 6 at a mechanical power of 1.2 kW at 1000 rpm. DC grid operation and control was validated, and the MPPB system supports the required operation under fault conditions—even without DC-link energy storage.

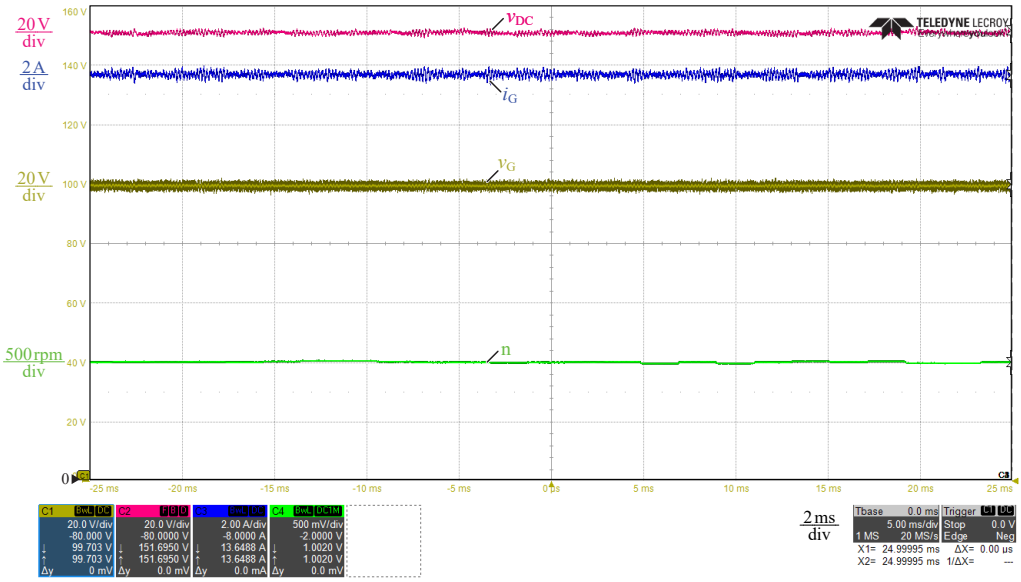

Figure 21. Measured waveforms under under steady-state DC-supplied operation at 1.2 kW mechanical output power: grid voltage (yellow), DC-link voltage (red), grid current (blue), and speed (500 rpm/div, green).

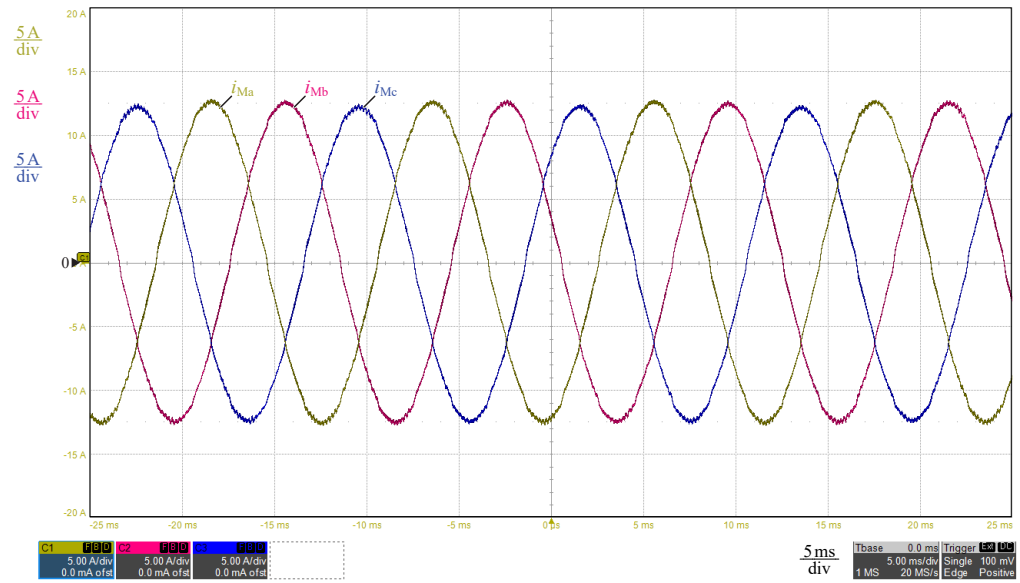

Figure 22. Measured three-phase motor current waveforms under steady-state DC-supplied operation at 1.2 kW mechanical output power.

6. Conclusions

Motor integration of Variable-Speed Drive (VSD) systems is desired for power density, integration, cost, and reliability—but for single-phase-supplied applications, is limited by the need to provide buffering energy storage on the DC-link, which is typically accomplished with electrolytic capacitors. These electrolytic capacitors occupy significant converter volume and cannot be operated across a wide temperature range with a high lifetime, preventing these VSDs from motor integration for the next-generation of electrified mobility.

This work proposed that the kinetic energy stored in the motor inertia itself be used to buffer the pulsating power from the single-phase grid, translating DC-link voltage and current ripple to motor speed and torque ripple. This concept is named the Motor-Integrated Power Pulsation Buffer (MPPB), and the control technique and structure required for nominal and grid fault condition operation were analyzed deeply. The control was realized by rearranging the connections between the same top-level controllers—without changing the core controllers themselves—supporting retrofitting and a simple software change.

A hardware demonstrator was constructed to verify the proposed MPPB concept for a single-phase-supplied railway application that drives a scroll compressor for air brakes (and other loads that require high reliability). The 7.5 kW demonstrator realized complete Permanent Magnet Synchronous Motor (PMSM) integration in a total volume of 8.2 L (or 500 in^3)—and without the DC-link capacitors that would occupy an additional 1 L (or 61 in^3) and prevent integration. The MPPB system achieved over 90% grid-to-motor-shaft efficiency for all loads over 5 kW or 66% of the nominal load, with a worst-case loss penalty over a conventional electrolytic-capacitor-based system of only 17%. The demonstrator will achieve CISPR 11/Class A compliance at full integration and operates across the required suite of extended functionality, including for ride-through and sustained grid faults.

The proposed MPPB concept shifts the required grid-buffering energy storage from an additional electrical element—large DC-link capacitors—to the motor, which is already required for the mechanical drive, achieving otherwise unobtainable power densities and integration levels for single-phase-supplied variable-speed electric drives.

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Abbreviations

The following abbreviations are used in this manuscript:

CM	Common-Mode
DM	Differential-Mode
DUT	Device-Under-Test
EMF	Electromotive Force
EMI	Electromagnetic Interference

IGBT	Insulated Gate Bipolar Transistor
MAF	Moving-Average Filter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPB	Motor-Integrated Power Pulsation Buffer
PCB	Printed Circuit Board
PFC	Power Factor Correction
PLL	Phase-Locked Loop
PMSM	Permanent Magnet Synchronous Motor
PPB	Power Pulsation Buffer
PWM	Pulse-Width-Modulation
RMS	Root Mean Square
SiC	Silicon Carbide
SOGI	Second-Order Generalized Integrator
VSD	Variable-Speed Drive
ZVS	Zero-Voltage Switching

List of Symbols

The following symbols are used in this manuscript:

α	Auxiliary variable
C_1, C_2	DM-filter capacitors/capacitances
C_{CM0}	CM-motor capacitance
C_{CM1}, C_{CM2}	CM-filter capacitors/capacitances
C_{DC}	DC-link capacitor/capacitance
CL, cl	Closed-loop transfer functions
d_a, d_b, d_c	Inverter duty-cycles
d_B	Boost duty-cycle
e_{KIN}	Kinetic energy of the drivetrain
e_{Lq}	Magnetic energy of the q-axis motor inductance
e_{sw}	Switching energy loss of a half-bridge
ε, ε_0	Mechanical rotor angles
$\eta_{CS,MPPB}$, $\eta_{CS,CONV}$	Converter system efficiency for MPPB/conventional operation
$\eta_{M,MPPB}$, $\eta_{M,CONV}$	Motor efficiency for MPPB/conventional operation
$\eta_{DS,MPPB}$, $\eta_{DS,CONV}$	Drive system efficiency for MPPB/conventional operation
f_{BW}	Bandwidth
f_{CO}	Crossover frequency
f_E	Electrical motor frequency
f_{Emin}	Minimum motor frequency in stationary operation with constant torque
f_{EQ}	Cutoff-frequency of a time-delay-equivalent low-pass filter
f_G	Grid frequency
f_i, f_{ii}, f_{iii}	Frequencies of harmonic motor current components
f_{Isw}	Inverter switching frequency
f_P	Power pulsation frequency
f_{PI}	Cutoff-frequency of a PI-controller
f_{PLL}	PLL frequency
G_D	Transfer function: time delay
G_{EQ}	Transfer function: time-delay-equivalent low-pass filter
G_F	Transfer function: filter
G_I	Transfer function: integrator
G_{PI}	Transfer function: PI-controller
I_B	Battery current
i_C	Instantaneous DC-link capacitor current
$\hat{I}_C$	DC-link capacitance capacitor amplitude
$I_{C,LFrms}$	Low-frequency rms DC-link capacitor current
i_G	Instantaneous grid current
$\hat{I}_G$	Grid current amplitude
$\hat{I}_{Gmax}$	Maximum grid current amplitude
i_I, I_I	Input current

i_{L}	Instantaneous boost inductor current
I_{M0}	Motor current space vector magnitude in conventional operation
$\hat{I}_{\mathrm{Ma,i}}$, $\hat{I}_{\mathrm{Ma,ii}}$, $\hat{I}_{\mathrm{Ma,iii}}$	Amplitudes of the motor current harmonics in MPPB operation
i_{Ma}, i_{Mb}, i_{Mc}	Instantaneous motor currents
$I_{\mathrm{Ma,avg}}$	Absolute global average current of phase *a*
i_{Md}	Instantaneous d-axis motor current
I_{Mmax}	Maximum motor current amplitude
i_{Mq}, I_{Mq}	Instantaneous/average q-axis motor current
$I_{\mathrm{PHa,rms}}$	RMS phase current in phase *a*
I_{PHavg}, I_{PH0avg}	Absolute average phase current for MPPB/conventional operation
I_{PHrms}, I_{PH0rms}	RMS phase current for MPPB/conventional operation
I_{PHpk}, I_{PH0pk}	Peak phase current for MPPB/conventional operation
J_{M}	Motor inertia
k	Load torque exponent
k_0, k_1, k_2	Switching loss coefficients
k_{P}	Proportional controller gain
k_{T}	Torque constant
k_{V}	Voltage constant
L_{B}	Boost inductor
L_{CM0}, L_{CM1}, L_{CM2}	CM-filter inductors/inductances
L_{d}	d-axis motor inductance
L_{DM}	DM-filter inductor/inductance
L_{EMI}	EMI-filter inductance
L_{q}	q-axis motor inductance
m	Index variable
n	Motor speed
Δn	Motor speed ripple amplitude
OL, ol	Open-loop transfer functions
$\mathrm{ON}_{\mathrm{INV}}$	Inverter operating state (on/off)
$\mathrm{ON}_{\mathrm{PFC}}$	PFC rectifier operating state (on/off)
p	Number of pole pairs
P_0	Mechanical power
P_{0DC}	Mechanical power in DC-operation
p_1, p_2	Air pressures
p_{C}, P_{C}	Instantaneous/average capacitor power
$\bar{p}_{\mathrm{C}}$	Averaged capacitor power
p_{G}, P_{G}	Instantaneous/average grid power
$\tilde{p}_{\mathrm{G}}$	AC component of the grid power
P_{I}	Average input power
p_{INV}	Instantaneous inverter power
p_{Lq}	Instantaneous q-axis magnetization power
$\bar{p}_{\mathrm{Lq}}$	Averaged q-axis magnetization power
p_{M}, P_{M}	Instantaneous/average motor power
p_{PFC}	Instantaneous PFC rectifier power
P_{V0}	Reference losses per phase
P_{VDS}	Drive system losses
P_{VEL}	Losses of the electronic circuitry
P_{VI}, P_{VI0}	Inverter losses for MPPB/conventional operation
P_{VIcond}	Inverter conduction losses
P_{VIdiode}	Inverter diode conduction losses
$P_{\mathrm{VIfet,i}}$, $P_{\mathrm{VI0fet,i}}$	Losses of MOSFET inverter with $\mathrm{d}v/\mathrm{d}t$ limitation of switching transitions
$P_{\mathrm{VIfet,ii}}$, $P_{\mathrm{VI0fet,ii}}$	Losses of MOSFET inverter with output filter
P_{VIigbt}, P_{VI0igbt}	Losses of IGBT inverter
P_{VIsw}	Inverter switching losses
P_{VM}, P_{VM0}	Motor losses for MPPB/conventional operation
p_{VMa}, p_{VMb}, p_{VMc}	Local average of the motor phase winding losses
P_{VMa}, P_{VMb}, P_{VMc}	Global average of the motor phase winding losses

P_{VMcap}	Capacitive motor losses
P_{VMcond}	Motor conduction losses
P_{VMnl}	No-load motor losses
P_{VPH}, P_{VPH0}	Average phase conduction losses for MPPB/conventional operation
P_{VPHmax}	Maximum phase losses
P_{VR}	Rectifier losses
P_{VRemi}	EMI filter losses
P_{VRhb}	Rectifier half-bridge losses
P_{VRind}	Rectifier inductor losses
P_{VRun}	Unfolder losses
PM	Phase margin
φ	Phase-shift
Ψ_{PM}	Permanent magnet flux linkage
R_{s}	Stator winding resistance
R_{on}	(Differential) on-resistance
$R_{\mathrm{DS,on}}$	Drain-source resistance of a MOSFET
s	Laplace variable
S_{UN}	Unfolder switching state
t	Time
ΔT,	Time-shift
T_{a}, T_{b}, T_{c}	Transistors of the inverter
T_{i}, T_{ii}, T_{iii}	Transistors of the PFC rectifier
T_{u}	Transistor of the unfolder
T_{A}	Acceleration torque
T_{C}	Control computation time
T_{D}	Time delay
T_{FFL}	Feedforward load torque
T_{G}	Grid period
T_{Isw}	Inverter switching period
T_{L}	Load torque
t_{M}, T_{M}	Instantaneous, average motor torque
T_{MAF}	MAF-filter averaging time
T_{Mnl}	No-load motor torque
T_{P}	Power pulsation period
T_{PWM}	PWM period
τ_{D}	Delay time constant
τ_{EQ}	Equivalent delay time constant
τ_{F}	Filter time constant
τ_{I}	Integrator time constant
τ_{i}, τ_{n}	Integral controller gain
τ_{PI}	PI-controller time constant
τ_{th}	Thermal time constant
θ	PLL-based grid angle
$\mathrm{d}v/\mathrm{d}t$	Motor terminal voltage slope
$\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$	Switch-node voltage slope
$v_{0\mathrm{q}}$	Approximated q-axis voltage
v_{ff}, v_{fi}	Components of the orthogonal $\alpha\beta-$voltage system
V_{B}	Battery voltage
Δv_{C}	Capacitor voltage ripple amplitude
v_{DC}, V_{DC}	Instantaneous / average DC-link voltage
$\bar{v}_{\mathrm{DC}}$	Averaged DC-link voltage
Δv_{DC}	DC-link voltage ripple amplitude
$v_{\mathrm{DC,AC}}$	AC-component of the DC-link voltage
v_{Dd}, v_{Dq}	dq-decoupling terms
v_{DS}	MOSFET drain-source voltage
V_{f}	Forward voltage drop
v_{G}	Instantaneous grid voltage
$\hat{V}_{\mathrm{G}}$	Grid voltage amplitude

$V_{G,on}$, $V_{G,off}$	Positive and negative gate driver voltage
v_I, V_I	Input voltage
v_{LB}	Instantaneous boost inductor voltage
v_{Ld}	Motor inductance d-axis voltage
v_{LISN}	Measured HF voltage noise
v_{Lq}	Motor inductance q-axis voltage
v_{Md}, v_{Mq}	Motor d-/q-axis voltage components
V_P	Voltage induced by the revolving rotor field
v_{pk}	Voltage peak derived by SOGI
v_{noise}	Noise voltage
$\dot{V}$	Air flow rate
Vol_{DS}	Drive system volume
ω	Instantaneous motor speed
$\Delta\omega$	Motor speed ripple amplitude
$\bar{\omega}$	Average motor speed
$\bar{\omega}_{min}$	Minimum average motor speed in stationary operation with constant torque
ω_{CO}	Angular crossover frequency
ω_i	Integral controller gain
ω_P	Angular power pulsation frequency

Appendix A. Low-Speed Operation with Constant Load Torque

In this Appendix, the low-speed limit of an MPPB-operated system with a constant load torque is investigated. This investigation is performed with an abstracted system, where the VSD is taken as lossless and forwards the complete grid power (see Equation (1)) to the motor. The motor power is therefore given, and the inner motor torque is $t_M = p_G/\omega$. The torque difference $t_M - T_L$ is then applied to the motor (and the load) inertia J_M and defines the speed change of the motor, which can be written as:

$$J_M \frac{\partial}{\partial t}\omega(t) = t_M(t) - T_L = \frac{p_G(t)}{\omega(t)} - T_L. \tag{A1}$$

The use case described here is analyzed, with a constant load torque T_L = cst., i.e., $k = 0$ (as discussed in Section 2). This dynamic system is shown as control-oriented block diagram in Figure A1a, and with the system described by a non-linear differential equation, the analysis must be conducted numerically to determine the minimal achievable average speed $\bar{\omega}_{min}$ for continuous MPPB operation.

Under the critical specifications for our application ($T_L = T_{L,N} = 19.4\,Nm$, $f_P = 100\,Hz$, $J_M = 4.5\,mkgm^2$), the behavior across speeds can be visualized. For large average speeds, the behavior is identical to that shown in Figure 2(e.ii), with an approximately symmetric speed ripple defined by Equation (5) as $2\Delta\omega = 13.7\,rad/s$. The first analyzed case in this section selects a grid power $P_0 = 388\,W$ to achieve $\bar{\omega} = 20\,rad/s$, recalling that in steady-state the average grid power P_0 must equal the average mechanical power $T_L\bar{\omega}$ (see Figure A1(c.i)). The corresponding time-domain waveform of the motor speed is shown in Figure A1(c.i), where even though the average speed is only 5% of the nominal speed, the system roughly behaves as expected. There is a slight asymmetry in the speed ripple amplitude (6.1 rad/s versus −7.2 rad/s) caused by the quadratic nature of the kinetic energy storage (see Figure A1b). The load power $T_L\omega$ contains a significant fluctuation as it scales proportionally with the instantaneous speed $\omega(t) \neq \bar{\omega}$, i.e., the small ripple assumption is no longer valid. This actually reduces the toque pulsation $t_M = p_G\omega^{-1}$ seen by the system and results in a slight phase shift of the speed variation and reduces the peak-to-peak speed ripple slightly from 13.7 rad/s to 13.3 rad/s.

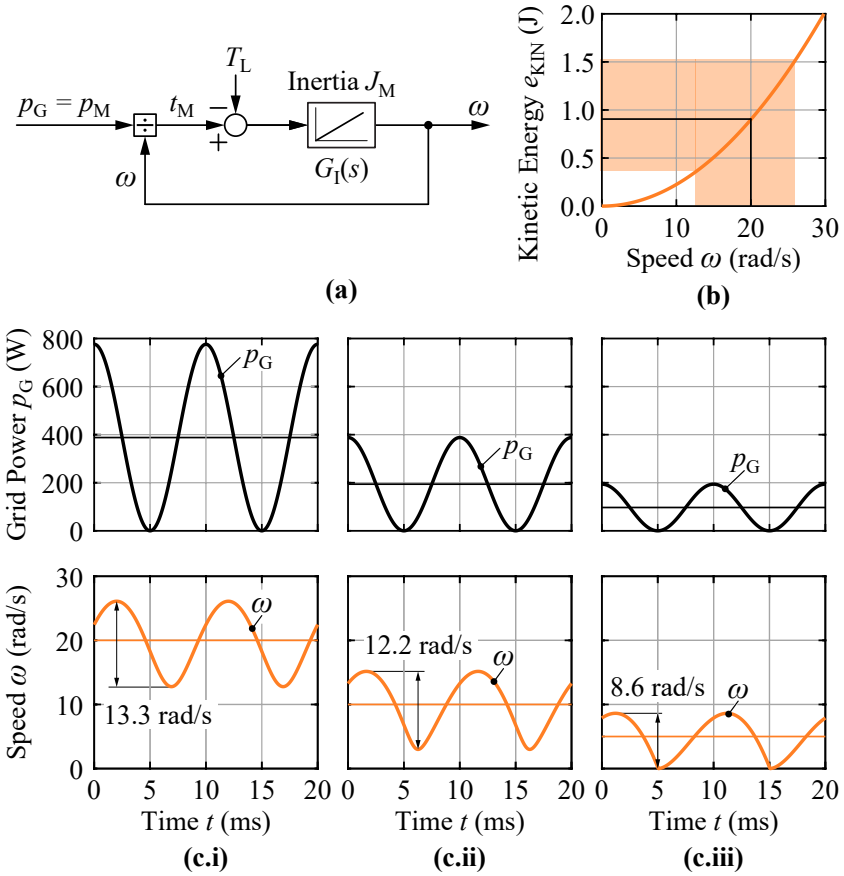

Figure A1. (**a**) Graphical representation of Equation (A1) for a constant load torque T_L. (**b**) Kinetically stored energy over speed with the indicated speed and energy range for operation at $\bar{\omega} = 20\,\mathrm{rad/s}$ and $T_L = T_{L,N} = 19.4\,\mathrm{Nm}$. (**c**) Grid power and instantaneous speed ω over one grid period for different average speeds (**c.i**) $\bar{\omega} = 20\,\mathrm{rad/s}$, (**c.ii**) $\bar{\omega} = 10\,\mathrm{rad/s}$, and (**c.iii**) $\bar{\omega} = 5\,\mathrm{rad/s}$. The average values are indicated by the thin lines and the peak-to-peak speed ripples are annotated.

As the input power is reduced to half in Figure A1(c.ii), the average speed is also halved to $\bar{\omega} = 10\,\mathrm{rad/s}$. A larger phase shift occurs, reducing the peak-to-peak ripple to 12.2 rad/s. The ripple amplitude asymmetry increases to 5.2 rad/s and $-7.0\,\mathrm{rad/s}$. With the ripple reduced, the instantaneous speed minimum also reduces.

Finally, through numerical methods, the minimum possible average speed for stationary MPPB operation (requiring $\omega(t) \geq 0\,\mathrm{rad/s}$) in the considered system is $\bar{\omega}_{\min} = 5\,\mathrm{rad/s} \approx 50\,\mathrm{rpm}$ (see Figure A1(c.iii) with $\omega(t)$ hitting zero).

Appendix B. Control Design and Enhancements

In this Appendix, the controller design is detailed to highlight enhancements to improve both steady-state and transient behavior in the MPPB system.

The analysis begins with the inner-most control loop, the motor current controller, which is shown in Figure A2a (similar to the corresponding control loop of Figure 4) and redrawn in Figure A2b in a more familiar model.

The control loop is investigated, the necessary controller is designed, and the bottlenecks and suggested improvements are highlighted. This procedure is then repeated for the outer control loops, with a special emphasis on the DC-link voltage control with a feedforward term to reduce the low-frequency voltage ripple.

Appendix B.1. Motor Current Control Loop

The control implementation is a conventional digital controller, where the control loop of Figure A2b is executed discretely when the sawtooth carrier of the PWM unit reaches

the top or bottom of the range. This execution occurs synchronously with the duty-cycle updates [95] twice per PWM (switching) period $T_{\mathrm{PWM}} = T_{\mathrm{Isw}} = 1/f_{\mathrm{Isw}}$ of the inverter.

At the updated time instants, the reference value i^*_{Mq} is compared to the measured value i'_{Mq}, and the error δi_{Mq} is input to the controller Riq, which is characterized by its transfer function (with $\omega_{\mathrm{i}} = 1/\tau_{\mathrm{i}} = k_{\mathrm{p}}/\tau_{\mathrm{n}}$):

$$G_{\mathrm{PI}}(s) = k_{\mathrm{p}} + \frac{\omega_{\mathrm{i}}}{s} = k_{\mathrm{p}} + \frac{1}{s\tau_{\mathrm{i}}} = k_{\mathrm{p}}\frac{1+s\tau_{\mathrm{n}}}{s\tau_{\mathrm{n}}}. \tag{A2}$$

The controller output v^*_{Lq} is converted to a duty-cycle and applied to the plant. In this process, a feedforward delay $\tau_{\mathrm{D,FF}}$ occurs, which comprises the delay between the controller execution and the duty-cycle update $\tau_{\mathrm{D,c}} = T_{\mathrm{Isw}}/2$ and the delay between the duty-cycle update and its influence to the plant $\tau_{\mathrm{D,pwm}}$, which is a result of the PWM operation itself. The average delay in the control loop can be approximated as a dead-time element of $\tau_{\mathrm{D,pwm}} = T_{\mathrm{Isw}}/4$ [96]. This feedforward term $\tau_{\mathrm{D,FF}} = \tau_{\mathrm{D,c}} + \tau_{\mathrm{D,pwm}}$ results in the transfer function of:

$$G_{\mathrm{D,FF}}(s) = G_{\mathrm{D,c}}(s) \cdot G_{\mathrm{D,pwm}}(s) = \exp(-s\tau_{\mathrm{D,FF}}). \tag{A3}$$

The plant itself corresponds to the energy storage of the controlled quantity as an integrator $G_{\mathrm{I}}(s) = 1/(s\tau_{\mathrm{I}})$, which, for the motor current controller, equals the q-inductance $\tau_{\mathrm{I}} = L_{\mathrm{q}} = 3\,\mathrm{mH}$.

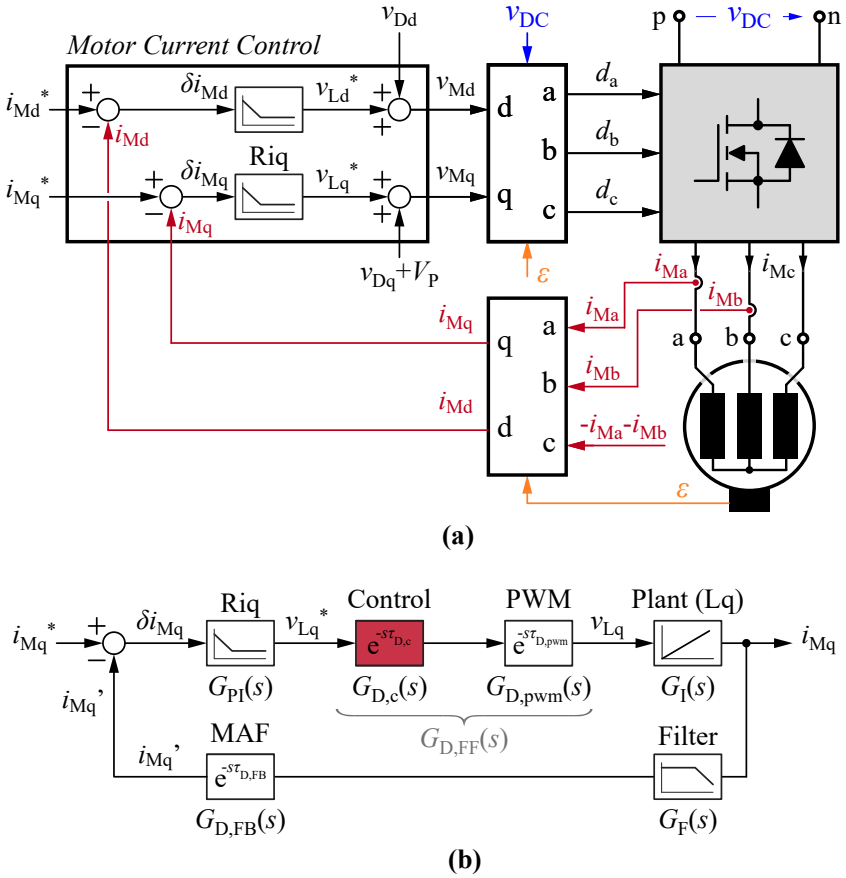

Figure A2. (**a**) Implementation of the motor current control (taken from Figure 4) and (**b**) corresponding control loop for the q-current.

For the feedback, the instantaneous current value i_{Mq} is measured and the feedback path comprises a low-pass filter $G_{\mathrm{F}}(s) = 1/(1+s\tau_{\mathrm{F}})$, with $\tau_{\mathrm{F}} = 1/\omega_{\mathrm{F}} = 1/(2\pi f_{\mathrm{F}})$ modeling the cut-off frequency of the sensor unit (here, $f_{\mathrm{F}} = 5\,\mathrm{MHz}$). A feedback delay is added to account for the time delay from the sensor to the controller execution,

$G_{D,FB}(s) = \exp(-s\tau_{D,FB})$, with the delay including $\tau_{D,FB} = T_{MAF}/2 + T_{D,vhdl}$ since a MAF filter [97] with $T_{MAF} = T_{Isw}$ is employed to eliminate all switching frequency components in the measured signal. $T_{D,vhdl} = 2.1\,\mu s$ accounts for the additional delay in the VHDL/C implementation.

The measured current is summed, with the appropriate sign, with the requested current, and the loop is closed.

Appendix B.2. Motor Current Controller Design

The current controller is designed around the phase margin criteria, where the phase margin PM defines the phase reverse (referenced to 180°) at the crossover frequency f_{CO} of the open loop transfer function $OL(s)$, which is

$$OL(s) = G_{PI}(s) \cdot G_{D,FF}(s) \cdot G_I(s) \cdot G_F(s) \cdot G_{D,FB}(s) \tag{A4}$$

The delay is replaced with an equivalent low-pass filter (Pade approximation) with the time constant $\tau_D = (\tau_{D,FF} + \tau_{D,FB})\, 2\sqrt{3}/\pi$, arriving at

$$G_{D,FF}(s) \cdot G_{D,FB}(s) \approx G_D(s) = \frac{1}{1 + s\tau_D}, \tag{A5}$$

and define the equivalent time constant $\tau_{EQ} = \max(\tau_F, \tau_D)$ (assuming $\tau_F >> \tau_D$ or $\tau_F << \tau_D$, which is typically valid), arriving at the simplified equivalent delay term:

$$G_{D,FF}(s) \cdot G_{D,FB}(s) \cdot G_F(s) \approx G_{EQ}(s) = \frac{1}{1 + s\tau_{EQ}} \tag{A6}$$

and the simplified open loop transfer function $ol(s)$:

$$ol(s) = G_{PI}(s) \cdot G_I(s) \cdot G_{EQ}(s) = \frac{k_p + sk_p\tau_n}{s^2\tau_I\tau_n + s^3\tau_I\tau_n\tau_{EQ}}. \tag{A7}$$

The phase margin criteria for $ol(j\omega)$ are:

$$|ol(j\omega_{CO})| = 1 \tag{A8}$$

$$\arg[ol(j\omega_{CO})] = PM - 180^\circ, \tag{A9}$$

with the phase margin PM achieved at the angular cross-over frequency $\omega_{CO} = 2\pi f_{CO}$. Solving for the controller gains results in the fully analytical expressions:

$$k_p = \frac{\tau_I}{\tau_{EQ}} \cdot \sqrt{\frac{1 + 1/\alpha}{1 + \alpha}} \quad \text{and} \quad \tau_n = \alpha\tau_{EQ} \tag{A10}$$

with $\alpha = \left(2\tan^2 PM + 1\right) + \sqrt{\left(2\tan^2 PM + 1\right)^2 - 1}$, and the crossover frequency result of:

$$f_{CO} = \frac{1}{2\pi}\frac{1}{\tau_{EQ}}\frac{1}{\sqrt{\alpha}}. \tag{A11}$$

The proposed control loop, with $f_{Isw} = 24\,kHz$ and a phase margin of $PM = 40°$, results in the controller gains of $k_p = 23.4$ and $\omega_i = 85.2\,rad/ms$. With these controller gains, the full (OL) and simplified (ol) open-loop transfer functions are shown in Figure A3, with the indicated phase margin $PM = 40°$ at the cross-over frequency $f_{CO} = 1.2\,kHz$, verifying the introduced approach.

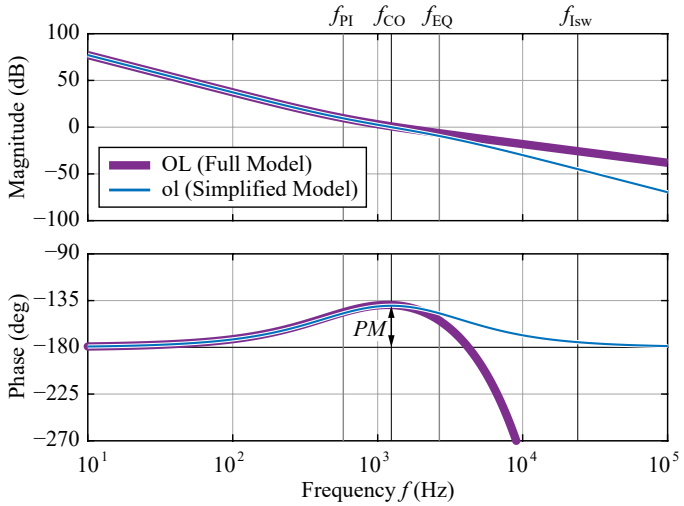

Figure A3. Bode plot of the full-model OL and simplified-model ol for loop and controller parameters. The phase margin PM is indicated at the crossover frequency f_{CO}, with the inverter switching frequency f_{Isw}, the cut-off frequency of the equivalent low-pass filter f_{EQ}, and the PI-controller cut-off frequency $f_{PI} = 1/(2\pi\tau_i)$ also highlighted.

The closed-loop transfer function can be calculated as:

$$CL(s) = \frac{i_{Mq}}{i^*_{Mq}} = \frac{G_{PI}(s) \cdot G_{D,FF}(s) \cdot G_I(s)}{1 + OL(s)} \tag{A12}$$

and simplified by $cl(s) = \frac{G_{PI}(s) \cdot G_I(s)}{1 + ol(s)}$, resulting in the simplified closed-loop transfer function:

$$cl(s) = \frac{k_P + sk_P(\tau_n + \tau_{EQ}) + s^2 k_P \tau_n \tau_{EQ}}{k_P + sk_P\tau_n + s^2\tau_I\tau_n + s^3\tau_I\tau_n\tau_{EQ}} \approx \frac{k_P}{k_P + s\tau_I}, \tag{A13}$$

where the approximation $cl(s) \approx 1/(1 + s\tau_I/k_P)$ can be used as an equivalent time constant for the design of an outer control loop (including for the DC-link voltage controller).

In case, the described system would employ a pure proportional controller, the analytical calculation results in:

$$f_{CO} = \frac{1}{2\pi} \frac{1}{\tau_{EQ} \tan PM} \tag{A14}$$

$$k_P = \frac{\tau_I}{\tau_{EQ}} \frac{\sqrt{1 + 1/\tan^2 PM}}{\tan PM} \tag{A15}$$

$$ol(s) = \frac{k_p}{s\tau_I + s^2\tau_I\tau_{EQ}} \tag{A16}$$

$$cl(s) = \frac{k_p + sk_p\tau_{EQ}}{k_P + s\tau_I + s^2\tau_I\tau_{EQ}} \approx \frac{k_P}{k_P + s\tau_I} \tag{A17}$$

Appendix B.3. Improvements to the Motor Current Controller: Feedforward Delay Reduction

The inner current controller is primarily limited by the sum of the delays, or the equivalent time constant of the controller. Next, the timing constraints of the structure are investigated to find options for improvement.

As mentioned previously, the duty-cycle of the PWM unit is only updated once the carrier reaches top or bottom, for an update rate of twice per switching period T_{PWM}. This behavior is shown in Figure A4a.

The ADC, however, operates in free run and gives new samples asynchronously. These samples are summed by an accumulator, which implements the first part of the

MAF. The second part of the MAF—the division by the sample length—is performed within the controller itself. To ensure that averaging occurs over the full switching period with the double-update rate of the duty-cycle, two 180°-phase-shifted accumulators are implemented, one for the top update and one for bottom update of the PWM (Accu. I and Accu. II in Figure A4b). The data read-out and reset is synchronized with the duty-cycle update, similar to a synchronous sampling structure [98].

After the read-out of the MAF, the controller derives the new duty-cycles, the calculation of which requires the control computation time T_C. Although T_C may be significantly smaller than $T_{PWM}/2$, its result (the new duty-cycle) can only be used at the next duty-cycle update, which is defined by the sawtooth carrier. In the end, then, the time difference $\Delta T = T_{PWM}/2 - T_C$ is wasted by waiting every half-cycle, as highlighted in Figure A4b.

To improve this time delay, the accumulator read-out can be shifted forward by ΔT (minus some margin) rather than synchronized with the duty-cycle, and the accumulator read-out now occurs shortly before the duty-cycle update. A forward shift of T_C plus some margin (Figure A4c) is introduced, and $\tau_{D,c}$ is reduced from half the switching period to T_C alone. Here, $T_C = 260$ ns to account for the VHDL implementation of the current controller.

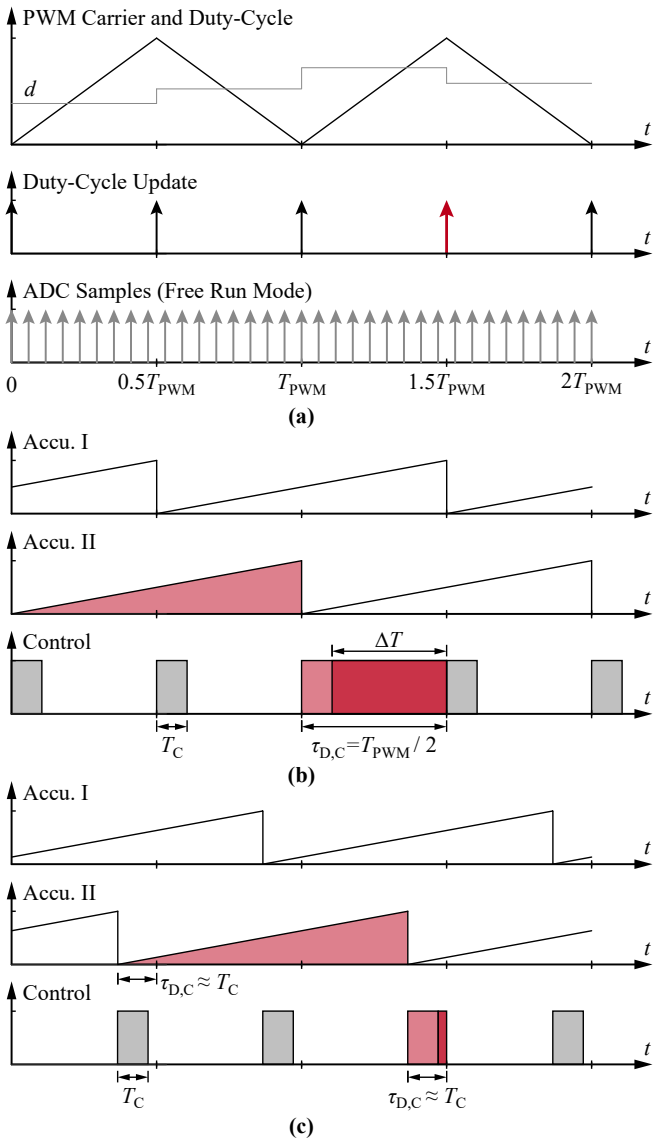

Figure A4. (**a**) PWM waveforms with indicated duty-cycle update and ADC sample timing. The timing considerations of the accumulators and the controller execution are highlighted for the (**b**) conventional and (**c**) improved implementation of the duty-cycle update timing.

The PI controller gains are again calculated based on the phase-margin criteria of 40°, leading to a controller with $k_\mathrm{p} = 37.7$, $\omega_\mathrm{i} = 221.5\,\mathrm{rad/ms}$ and $f_\mathrm{CO} = 2.0\,\mathrm{kHz}$. The crossover frequency of the open-loop transfer function, then, is increased by nearly 60% with this proposed delay reduction.

Finally, the closed-loop transfer function is compared and evaluated:

$$CL'(s) = \frac{i'_\mathrm{Mq}}{i^*_\mathrm{Mq}} = \frac{OL(s)}{1 + OL(s)}. \tag{A18}$$

(Note that i_Mq cannot be evaluated directly in the selected implementation with the MAF filter before the dq-transform block). The original and improved closed-loop transfer function is shown in Figure A5, with the indicated $-3\,\mathrm{dB}$ bandwidth for each implementation highlighted.

The model and the measurements match well, with the small deviation around the resonances due to the neglected motor phase resistance. The improvement in timing improves the bandwidth from $f_\mathrm{BW} = 2.9\,\mathrm{kHz}$ to $f_\mathrm{BW} = 4.7\,\mathrm{kHz}$, an improvement of 60%.

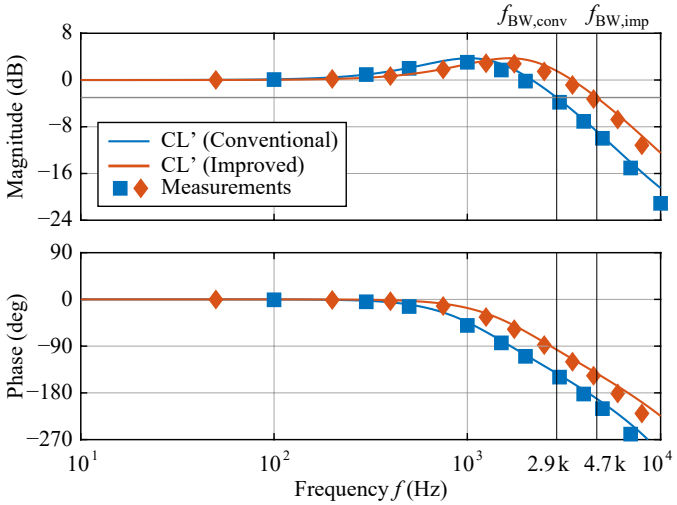

Figure A5. Model and verification measurement of the closed-loop transfer function $CL'(s) = i'_\mathrm{Mq}/i^*_\mathrm{Mq}$ for the conventional and improved implementation.

Appendix B.4. Improvements to the DC-Link Voltage Controller

The same procedure can be applied to the DC-link voltage controller, where a particular improvement to the low-voltage ripple is sought. The equivalent time constant is now defined by the inner current controller $\tau_\mathrm{EQ,V} = \tau_\mathrm{I}/k_\mathrm{P}$, which would, in this case, be located in the feedforward path.

To achieve a bandwidth separation of around $4\times$ from the inner current control, the phase margin target is $PM_\mathrm{VDC} = 62°$. The conventional controller gain is $k_\mathrm{p,V} = 0.117$, $\omega_\mathrm{i,V} = 56.7\,\mathrm{rad/s}$ and $f_\mathrm{CO,V} = 309\,\mathrm{Hz}$ and the improved controller gain is $k_\mathrm{p,V} = 0.188$, $\omega_\mathrm{i,V} = 147\,\mathrm{rad/s}$ and $f_\mathrm{CO,V} = 500\,\mathrm{Hz}$.

For each controller and timing implementation, the measured AC component of the DC-link voltage (measured with a high-pass) is shown in Figure A6a for the conventional controller and (b) for the improved controller operation. In the conventional case, the voltage ripple is $2\Delta v_\mathrm{DC} = 35\,\mathrm{Vpkpk}$, which is almost identical to the simulation results of Figure 5 (the simulation employs the same controller configuration). With the improved controller setting, the DC-link voltage ripple is reduced to $2\Delta v_\mathrm{DC} = 23\,\mathrm{Vpkpk}$.

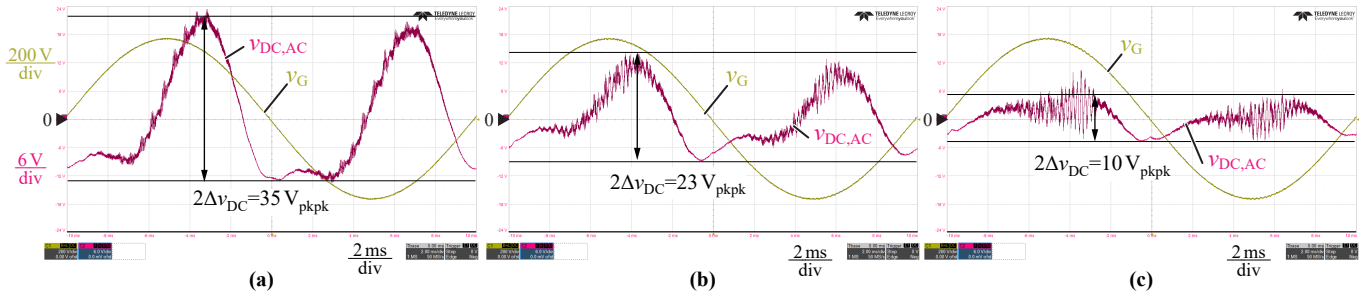

Figure A6. Measured grid voltage v_G and AC-component of the DC-link voltage $v_{DC,AC}$ at nominal operation for (**a**) conventional current control, (**b**) improved current control, and (**c**) improved current control with inductor voltage feedforward (see Figure 4).

Interestingly, the voltage ripple reduces by a 60% factor, which can be explained straightforwardly. The timing structure allows higher controller gains while maintaining stability, which increases the gain of the open-loop transfer function and enables a higher crossover frequency. Because the open-loop transfer function appears in the denominator of the disturbance transfer function, the impact of any disturbances below the crossover frequency are reduced by the improved open-loop transfer function.

Even with this improvement, though, these results imply a significant amount of disturbance power at low frequencies (multiples of 100 Hz) that is resulting in a large DC-link voltage fluctuation. The motor itself, and particularly at the waveforms surrounding the motor inductance (Figure A7), are therefore investigated next.

Starting with the q-current (from Equation (12)), and considering the motor inductance $L_q = 3\,\text{mH}$, the magnetically stored energy within the motor over several grid periods is $e_{Lq}(t) = i_{Mq}^2(t)L_q/2$. The magnetization power is found as $p_{Lq}(t) = de_{Lq}(t)/dt$, shown in Figure A7, which is the disturbance quantity. The inductive power demand of the motor, with a zero average ($\bar{p}_{Lq}(t) = 0\,\text{W}$), is acting as the low-frequency disturbance. The peak power is almost 1 kW, which is about 13% of the average output power.

To address this disturbance in the control architecture, the inductor voltage that results from the q-current change is calculated as $v_{Lq}(t) = p_{Lq}(t)/i_{Mq}(t) = L_q di_{Mq}(t)/dt$. The resulting voltage can be used as a feedforward term, along with the induced voltage V_P. The derivation of this voltage requires a differentiation, with the associated concerns of robustness, but because the instantaneous grid phase angle is known from the PLL the inductor voltage can be calculated open-loop.

For a sinusoidal input, then, the inductor voltage can be calculated as $v_{Lq}(\theta) = I_{M0}L_q f(\theta)$, with the function $f(\theta)$ as:

$$f(2\pi f_G t) = 4 \cdot 2\pi f_G \cdot \cos(2\pi f_G t) \cdot \sin(2\pi f_G t). \tag{A19}$$

The feedforward term is implemented as shown in Figure 4, and, with this improvement, the corresponding DC-link voltage measurement is shown in Figure A6c. The voltage ripple is reduced another 55%—beyond the timing improvement—to a much-improved ripple of $2\Delta v_{DC} = 10\,\text{Vpkpk}$.

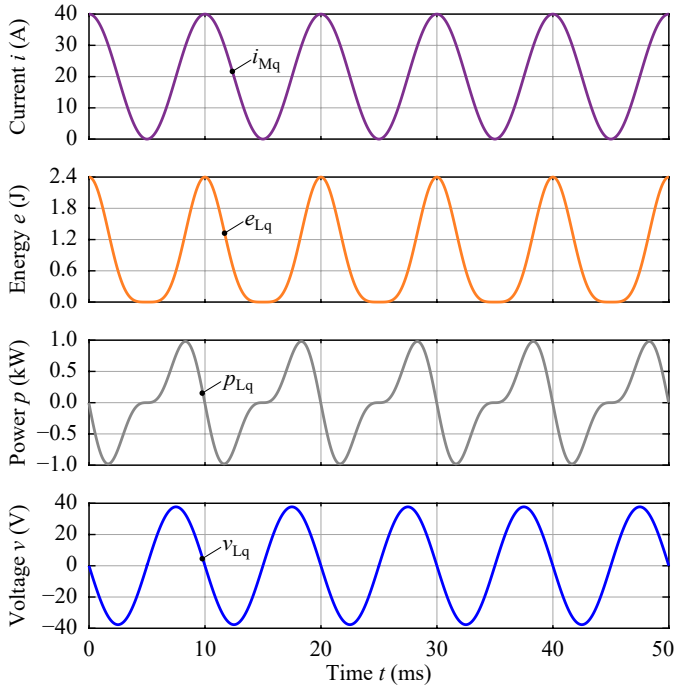

Figure A7. Motor inductance waveforms: q-current i_{Mq}, stored magnetic energy e_{Lq}, corresponding magnetization power p_{Lq}, and q-inductor voltage v_{Lq}, which can be used as a feedforward term to reduce the DC-link voltage ripple.

Appendix C. Phase Current Analysis

In this section, the phase currents in the inverter and motor under MPPB operation are detailed, including an investigation of the loss-characteristic currents and different frequency ratios between the electrical motor frequency $f_E = p\bar{\omega}/(2\pi)$ and the power pulsation frequency f_P.

First, the phase stress is analyzed for the rms currents under a variety of frequency ratio cases before moving to an average current analysis. For completeness, the analytical equations for all three phase currents are given below in Equations (A20)–(A22).

$$\begin{aligned} i_{Ma}(t) &= -I_{M0}\sin(p\bar{\omega}t+\varepsilon_0) \\ &\quad -\frac{I_{M0}}{2}\sin(p\bar{\omega}t+2\pi f_P t+\varepsilon_0) \\ &\quad -\frac{I_{M0}}{2}\sin(p\bar{\omega}t-2\pi f_P t+\varepsilon_0) \end{aligned} \tag{A20}$$

$$\begin{aligned} i_{Mb}(t) &= -I_{M0}\sin\left(p\bar{\omega}t+\varepsilon_0+\frac{2\pi}{3}\right) \\ &\quad -\frac{I_{M0}}{2}\sin\left(p\bar{\omega}t+2\pi f_P t+\varepsilon_0+\frac{2\pi}{3}\right) \\ &\quad -\frac{I_{M0}}{2}\sin\left(p\bar{\omega}t-2\pi f_P t+\varepsilon_0+\frac{2\pi}{3}\right) \end{aligned} \tag{A21}$$

$$\begin{aligned} i_{Mc}(t) &= -I_{M0}\sin\left(p\bar{\omega}t+\varepsilon_0-\frac{2\pi}{3}\right) \\ &\quad -\frac{I_{M0}}{2}\sin\left(p\bar{\omega}t+2\pi f_P t+\varepsilon_0-\frac{2\pi}{3}\right) \\ &\quad -\frac{I_{M0}}{2}\sin\left(p\bar{\omega}t-2\pi f_P t+\varepsilon_0-\frac{2\pi}{3}\right) \end{aligned} \tag{A22}$$

Appendix C.1. RMS Current Stress

The phase currents are the superposition of three sinusoidal waveforms: $f_{\mathrm{i}} = f_{\mathrm{E}}$ with amplitude I_{M0} and $f_{\mathrm{ii}} = f_{\mathrm{E}} + f_{\mathrm{P}}$ and $f_{\mathrm{iii}} = f_{\mathrm{E}} - f_{\mathrm{P}}$, each with amplitude $I_{\mathrm{M0}}/2$. Depending on the ratio of f_{E} and f_{P}, though the coincidence of sines will vary, potentially leading to asymmetric phase current stresses.

The current amplitudes, maximum phase losses $P_{\mathrm{VPHmax}} = \max\left(P_{\mathrm{VMa}}, P_{\mathrm{VMb}}, P_{\mathrm{VMc}}\right)$, and total losses $P_{\mathrm{VMcond}} = P_{\mathrm{VMa}} + P_{\mathrm{VMb}} + P_{\mathrm{VMc}}$ with $P_{\mathrm{VMa}} = \bar{p}_{\mathrm{VMa}}(t)$ are analyzed for a variety of motor speeds (and resulting frequencies), with the results summarized in Table A1 for the speed ratio cases. The phase losses are benchmarked to $P_{\mathrm{VPH0}} = R_{\mathrm{s}} I_{\mathrm{M0}}^2/2$, which are the phase losses under conventional operation. For the first four cases in Table A1, the corresponding phase currents (i_{Ma}, i_{Mb}, and i_{Mc}) and local conduction losses $p_{\mathrm{VMa}}(t) = R_{\mathrm{s}} i_{\mathrm{Ma}}^2(t)$ are shown in Figure A8a–d for phase a with $f_{\mathrm{P}} = 100\,\mathrm{Hz}$ and worst-case conditions. While the analysis is conducted for $f_{\mathrm{E}} \geq f_{\mathrm{Emin}} = p\bar{\omega}_{\mathrm{min}}/(2\pi) = 4\,\mathrm{Hz}$, with f_{Emin} derived as in Appendix A, the results are also, of course, valid for $f_{\mathrm{E}} \leq -f_{\mathrm{Emin}}$ (the opposite direction of rotation).

Each case is separated below to detail the calculations behind the results of Figure A8 and Table A1.

Appendix C.1.1. Case A, $f_{\mathrm{E}} > f_{\mathrm{P}}$

In this case, the superposition maintains three distinct frequencies with the amplitudes given in Table A1. The RMS stress is the superposition of the three sines, as:

$$I_{\mathrm{PHrms}}^2 = \frac{1}{2} I_{\mathrm{M0}}^2 + \frac{1}{2}\frac{I_{\mathrm{M0}}^2}{4} + \frac{1}{2}\frac{I_{\mathrm{M0}}^2}{4} = \frac{3}{2}\frac{I_{\mathrm{M0}}^2}{2}. \tag{A23}$$

The conduction losses are $P_{\mathrm{VPH}} = 3/2\, P_{\mathrm{VPH0}}$ for a single phase and $P_{\mathrm{VMcond}} = 9/2\, P_{\mathrm{VPH0}}$ for the three-phase system. The waveforms are shown in Figure A8a at $f_{\mathrm{E}} = 120\,\mathrm{Hz}$, with symmetrical stresses across the three phases verified.

Appendix C.1.2. Case B, $f_{\mathrm{E}} = f_{\mathrm{P}}$

With the frequencies equal, the result is two distinct frequency components with a DC-offset, since $f_{\mathrm{iii}} = 0\,\mathrm{Hz}$. The DC magnitude in phase a is $I_{\mathrm{M0}}/2\, \sin\varepsilon_0$, and, since both sines are multiples of the power pulsation frequency, there is a standing wave, as shown in Figure A8b. Because the phase currents are locked with the power pulsation frequency, the conduction losses of the phases are asymmetric.

The RMS stress in phase a is $I_{\mathrm{PHa,rms}}^2 = \left(5 + 2\sin^2\varepsilon_0\right)/4\; I_{\mathrm{M0}}^2/2$, which now depends on ε_0, or the position at which the frequencies lock. For $\varepsilon_0 = 0$, which is the minimum stress for phase a, the RMS current is $I_{\mathrm{PHa,rms}}^2 = 5/4\; I_{\mathrm{M0}}^2/2$ and for $\varepsilon_0 = \pi/2$, the maximum stress for phase a, the RMS current is $I_{\mathrm{PHa,rms}}^2 = 7/4\; I_{\mathrm{M0}}^2/2$. The maximum conduction loss for a phase, then, is $P_{\mathrm{VPHmax}} = 7/4\; P_{\mathrm{VPH0}}$, an increase of 16% for losses in a particular phase. Because the two remaining phases are 120°-phase-shifted, though, the total losses remain the same at $P_{\mathrm{VMcond}} = 9/2\; P_{\mathrm{VPH0}}$.

Table A1. Overview of phase current stress, with a special emphasis on asymmetry, at different motor speeds and frequency ratios with I_{M0} equal to the q-current magnitude in conventional operation.

Condition	$f_{\mathrm{i}} = f_{\mathrm{E}}$	$f_{\mathrm{ii}} = f_{\mathrm{E}} + f_{\mathrm{P}}$	$f_{\mathrm{iii}} = f_{\mathrm{E}} - f_{\mathrm{P}}$	$\hat{I}_{\mathrm{Ma,i}}/I_{\mathrm{M0}}$	$\hat{I}_{\mathrm{Ma,ii}}/I_{\mathrm{M0}}$	$\hat{I}_{\mathrm{Ma,iii}}/I_{\mathrm{M0}}$	$P_{\mathrm{VPHmax}}/P_{\mathrm{VPH0}}$	$P_{\mathrm{VMcond}}/P_{\mathrm{VPH0}}$
(a) $f_{\mathrm{E}} > f_{\mathrm{P}}$	$f_{\mathrm{E}} > 0\,\mathrm{Hz}$	$>0\,\mathrm{Hz}$	$>0\,\mathrm{Hz}$	1	1/2	1/2	3/2	9/2
(b) $f_{\mathrm{E}} = f_{\mathrm{P}}$	$f_{\mathrm{E}} > 0\,\mathrm{Hz}$	$2f_{\mathrm{E}} > 0\,\mathrm{Hz}$	$=0\,\mathrm{Hz}$	1	1/2	$\frac{1}{2}\sin(\varepsilon_0)$	7/4	9/2
(c) $f_{\mathrm{P}}/2 < f_{\mathrm{E}} < f_{\mathrm{P}}$	$f_{\mathrm{E}} > 0\,\mathrm{Hz}$	$>0\,\mathrm{Hz}$	$<0\,\mathrm{Hz}$	1	1/2	1/2	3/2	9/2
(d) $f_{\mathrm{P}}/2 = f_{\mathrm{E}}$	$f_{\mathrm{E}} > 0\,\mathrm{Hz}$	$3f_{\mathrm{E}} > 0\,\mathrm{Hz}$	$-f_{\mathrm{E}} < 0\,\mathrm{Hz}$	$\sqrt{\frac{5}{4} - \cos(2\varepsilon_0)}$	1/2	–	5/2	9/2
(e) $f_{\mathrm{Emin}} < f_{\mathrm{E}} < f_{\mathrm{P}}/2$	$f_{\mathrm{E}} > 0\,\mathrm{Hz}$	$>0\,\mathrm{Hz}$	$<0\,\mathrm{Hz}$	1	1/2	1/2	3/2	9/2

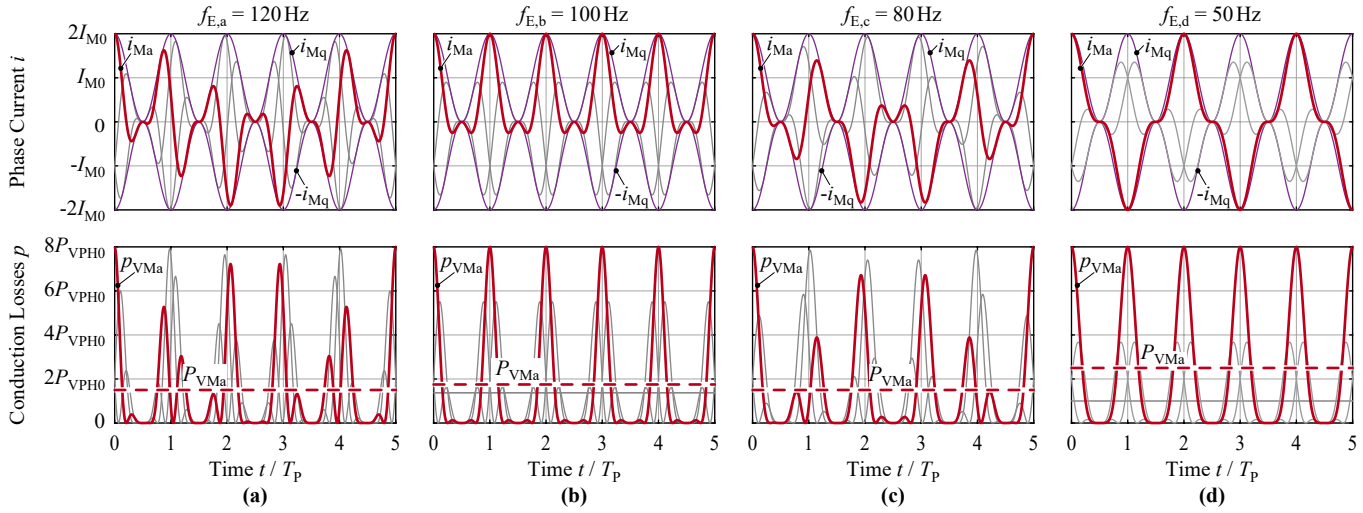

Figure A8. (**a**–**d**) Motor phase currents and corresponding local conduction losses for different electrical frequencies f_E and $f_P = 100$ Hz, indicating asymmetrical phase stress for particular cases of frequency ratios.

Appendix C.1.3. Case C, $f_P/2 < f_E < f_P$

This case again results in three distinct frequencies, as in *Case a*, with the waveforms shown in Figure A8c for $f_E = 80$ Hz.

Appendix C.1.4. Case D, $f_P/2 = f_E$

Here, two sine functions collapse into one, with $f_i = -f_{iii} = f_E$, so for $f_P = 100$ Hz, the result is $f_i = -f_{iii} = f_E = 50$ Hz with an amplitude of $I_{M0}\sqrt{5/4 - \cos(2\varepsilon_0)}$. f_{ii} oscillates at $3f_E$ with an amplitude of $I_{M0}/2$.

These conditions result with $i_{Ma}(t)$ equal to nearly $i_{Mq}(t)$, as shown in Figure A8d for $f_E = 50$ Hz. The asymmetry between the phases is increased further, with the RMS current stress for phase *a* of $I^2_{PHa,rms} = [6 - 4\cos(2\varepsilon_0)]/4\ I^2_{M0}/2$ for $\varepsilon_0 = 0$ (minimum stress for phase *a*) and $I^2_{PHa,rms} = 1/2\ I^2_{M0}/2$ and for $\varepsilon_0 = \pi/2$ (maximum stress for phase *a*) at $I^2_{PHa,rms} = 5/2\ I^2_{M0}/2$. The maximum conduction losses for a particular phase are $P_{VPHmax} = 5/2\ P_{VPH0}$, an increase in 66% over the symmetric case. Again, the total losses remain the same due to the phase shift between the phases.

Appendix C.1.5. Case E, $f_{Emin} < f_E < f_P/2$

This case is identical to *Case c*.

The total losses for this condition, even at the maximum phase stress, remain the same as for every other frequency ratio. With total losses identical, the primary remaining consideration is the thermal time constant of the key components—the motor and the inverter power semiconductors—in the vicinity of these key corner cases to verify safe operation.

The motor winding time constant is approximated as $\tau_{th} = 50$ s and a faster time constant of $\tau_{th} = 0.1$ s is used for the MOSFET power semiconductors [99]. With these time constants, the system can be designed to operate outside restricted frequency ranges as $|p\bar{\omega}| = 2\pi f_P$ (see *Case b*), $|p\bar{\omega}| = \pi f_P$ (see *Case d*), and $|\bar{\omega}| > |\bar{\omega}_{min}|$, with a 0.01 Hz width for the slow motor time constant and a 5 Hz width for the faster power semiconductor time constant. These results are illustrated in Figure A9, where the maximum losses and the restricted frequency ranges are highlighted. Note that the motor frequencies corresponding to these restricted frequency ranges can be influenced via the number of pole pairs in the selected motor.

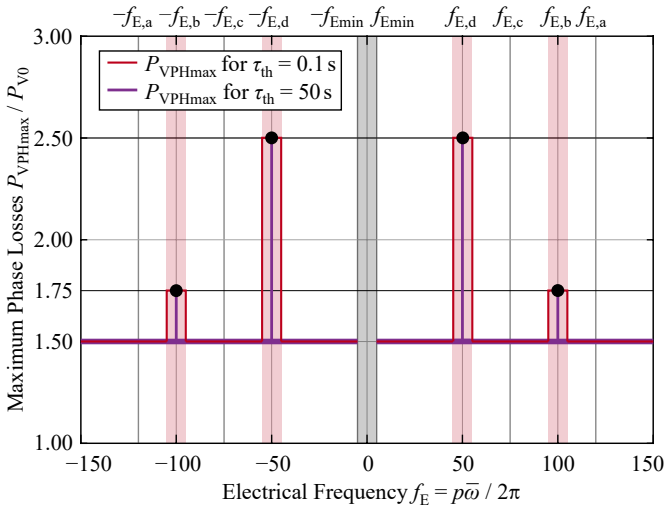

Figure A9. Maximum phase conduction losses P_{VPHmax} over the electrical frequency f_E with the illustration of the restricted operating areas for different thermal time constants τ_{th}. The prevented speed operating range according to Appendix A is indicated by the grey area. The • indicates the analytical calculations of Table A1.

Appendix C.2. Absolute Average Current

With the RMS current analyzed for each case, next the average current stress of phase *a*, $I_{Ma,avg}$, for each frequency ratio assuming a non-zero speed, i.e., $|\bar{\omega}| > 0$ rad/s, is analyzed.

By definition, $I_{Ma,avg} = \frac{1}{T}\int_0^T |i_{Ma}(\tau)|d\tau$. Starting from $|i_{Ma}(t)| = i_{Mq}(t)|\sin(p\bar{\omega}t + \varepsilon_0)|$ with $i_{Mq}(t) \geq 0$ A, $i_{Mq}(t) = I_{M0} + I_{M0}\cos(2\pi f_P t)$ is substituted and splitting the equation as $I_{Ma,avg} = I^i_{Ma,avg} + I^{ii}_{Ma,avg}$, the results for each part are:

$$I^i_{Ma,avg} = \frac{I_{M0}}{T}\int_0^T |\sin(p\bar{\omega}\tau + \varepsilon_0)|d\tau = \frac{2}{\pi}I_{M0} \quad \text{(A24)}$$

$$I^{ii}_{Ma,avg} = \frac{I_{M0}}{T}\int_0^T [|\sin(p\bar{\omega}\tau + \varepsilon_0)|\cos(2\pi f_P \tau)]d\tau. \quad \text{(A25)}$$

Applying the Fourier transform reveals that $I^{ii}_{Ma,avg} \equiv 0$ A if $p\bar{\omega}/(2\pi) = f_E \neq f_P/(2m)$ with $m = 1, 2, 3, ...$, so these cases have a symmetrical current stress of $I_{Ma,avg} = 2/\pi\, I_{M0}$.

For $f_E = f_P/(2m)$ with $m = 1, 2, 3, ...$, the average current stress is asymmetrical across phases, with numerical calculations showing a worst-case increase of 33.3% for $m = 1$, 6.7 % for $m = 2$, and <3% for $m \geq 3$.

The sum $I_{Ma,avg} + I_{Mb,avg} + I_{Mc,avg} = 6/\pi\, I_{M0}$, though, remains constant, similar to the constant total losses in the RMS analysis. There are, therefore, no further restrictions on the frequency ratio for the MPPB operation from the average current stress.

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