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Next Generation Measurement Systems with High Common-Mode Rejection

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***Abstract*—There is an increasing importance for floating measurements with high bandwidth in the field of power electronics, driven by the need to characterize power converters utilizing latest wide bandgap devices which offer very fast voltage transitions. In this paper, the required Common-Mode Rejection Ratio (CMRR) as the most important performance metric of a floating or isolated measurement system is analyzed and quantified for different converter realizations with the aim to limit the resulting time-domain error voltage. Afterwards, state of the art isolated single-ended probes are investigated and analyzed in terms of practical applicability and sensitivity regarding variations of the measurement setup, specifically looking at non-ideal connections between probe and converter, often inevitable in power electronic applications. It is found that the performance of isolated single-ended probes quickly degrades when additional connecting wires are used between the circuit under test and probe input. To overcome this inherent limitation of any single-ended approach, an isolated differential structure is presented that combines the advantages of conventional high-voltage differential probes and isolated single-ended probes. Finally, challenges involved when designing a matched differential system are discussed, in particular the influence of amplitude and phase imbalance on the maximum achievable CMRR. Especially the required phase accuracy which needs to be around six times higher than the amplitude accuracy is very hard to realize over the whole frequency range of interest. It turns out, however, that thanks to the passive common-mode filtering already present in state of the art single-ended approaches, CMRR values of around $30-40\,\mathrm{dB}$ in the difference-stage enable significant performance improvement for the differential structure.**

***Index Terms*—Advanced Measurement Systems, Common-Mode Rejection, Common-Mode Robustness, Power Electronic Measurements, Floating Measurements, High-Side Gate-Source Voltage Measurement, Single-Ended Probe, Differential Probe**

I. Introduction

Today's research in power electronics is driven more and more towards maximum power density accompanied with the demand for highest efficiencies, where possible applications are for example ultra-compact photovoltaic inverters [1], high-efficient automotive solutions [2] and highly integrated medium-voltage systems [3]. Apart from the very limited space making it almost impossible to access all signals of interest, the high packaging density and switching frequencies in the multi-megahertz range impose several challenges regarding the measurements required for characterization and performance verification. A very common situation often faced during the commissioning process is the measurement of floating voltages, e.g. the gate-source voltage $v_{\mathrm{gs,1}}$ of the high-side switch in a half-bridge, being a part of a complex converter system. **Fig. 1** shows the measurement of $v_{\mathrm{gs,1}}$ using a state of the art isolated single-ended probe. The floating nature arises from the absence of a steady measurement reference potential. The high-side gate-source voltage $v_{\mathrm{gs,1}}$ is referred to the switch-node potential v_{sw}, fluctuating between ground and the full dc link voltage V_{dc} with the switching frequency f_{sw}. The respective transitions can be very fast, depending on V_{dc} and the corresponding $\mathrm{d}v/\mathrm{d}t$. Acting equally on both inputs, v_{sw} is therefore denoted as a *common-mode* (CM) disturbance, whereas the gate-source voltage $v_{\mathrm{gs,1}}$ to be measured is hereinafter denoted as *differential-mode* (DM) voltage.

In general, measurement systems suited for floating measurements in power electronics should provide superior CM robustness, i.e. to attenuate or reject the CM disturbance by a high factor (high common-mode rejection ratio as defined in **Section II**) while keeping the DM signal unaffected. Since the probe is connected directly between gate and source of the high-side switch and thanks to the galvanic isolation, it is implicitly immune against such CM disturbances in the ideal case. Another advantage is certainly the comparably small required DM voltage rating, i.e. low input divider attenuation, and the thereby resulting high measurement accuracy.

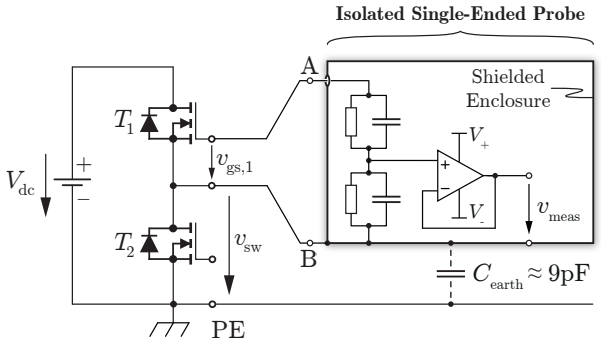

Fig. 1. Half-bridge comprising an upper side switch T_1 and a lower side switch T_2 where the floating high-side gate-source voltage $v_{\mathrm{gs,1}}$ is measured using an isolated single-ended probe.

In **Section II**, key performance parameters for such measurement systems are defined and quantified, while in **Section III** state of the art measurement techniques with their advantages and disadvantages are presented. Finally, a concept based on a differential measurement for improved performance is proposed and analyzed in **Section IV**.

II. Performance Requirements

As shown in **Fig. 1**, between an isolated measurement system and the surrounding environment on steady potential (usually PE), a parasitic capacitance C_{earth} is formed, which has to be charged and discharged through the connecting lines during each voltage transition of v_{sw}. In a half-bridge configuration as given in **Fig. 1**, the measurement system is typically excited with a quasi trapezoidal CM voltage (cf. **Fig. 2 (a)**). Due to the finite rise and fall times T_{slope} during the voltage transitions, a certain $\mathrm{d}v/\mathrm{d}t$ is present, which charges C_{earth} with a current i_{earth} given as

$$i_{\mathrm{earth}} = C_{\mathrm{earth}} \cdot \frac{\mathrm{d}v}{\mathrm{d}t}. \tag{1}$$

The earth capacitance solely depends on the geometry of the measurement system and the corresponding test setup. Typical values range between $5-20\,\mathrm{pF}$.

The charging current has to flow through the connecting lines of the floating measurement and since they always have a certain impedance $\underline{Z}_{\mathrm{line}}$, a voltage builds up across them, eventually acting as disturbance

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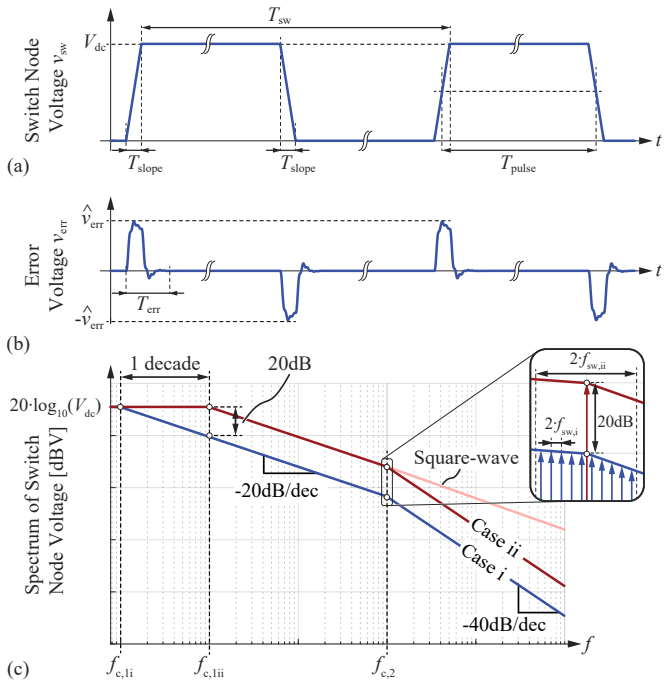


Fig. 2. (a) Trapezoidal signal waveform of a typical switch-node voltage v_{sw} acting as CM input voltage on floating measurement systems used for measuring the high-side gate-source voltage in power electronic converters and **(b)** schematic waveform of the error signal v_{err} appearing at the output as a result of the CM distortion. **(c)** Spectral envelopes of two trapezoidal signals $v_{sw,i}$ (Case i) and $v_{sw,ii}$ (Case ii) with equal amplitudes V_{dc} and equal rise and fall times T_{slope} but different switching frequencies $f_{sw,i}$ and $f_{sw,ii}$.

for the measurement system, which then outputs an erroneous output voltage $v_{err} = v_{meas}$ at the terminals of the measurement system even for pure common-mode excitation, as schematically shown in **Fig. 2 (b)**. It can be seen that the error signal v_{err} is decreasing quite rapidly after the transitions of the CM input voltage v_{sw}, i.e. after T_{slope} when the capacitor C_{earth} is fully charged or discharged, which means that mainly the high frequency content of the CM input voltage v_{sw} is responsible for the disturbances.

The ability of a measurement system, hereinafter synonymously called probe, to attenuate or reject common-mode disturbances is described with the Common-Mode Rejection Ratio (CMRR), defined as the ratio between differential-mode gain (or attenuation) A_{dm} and common-mode gain A_{cm}

$$\text{CMRR} = \frac{A_{dm}}{A_{cm}}. \tag{2}$$

The concept of the CMRR is widely known as a performance metric of operational amplifiers but can also be used in other systems such as probes. A_{dm} as well as A_{cm} are frequency-dependent, hence the CMRR is not a constant number over a given frequency range.

The amplitude of v_{err} is therefore directly dependent on the CMRR of the probe and the question arises how large the CMRR of the measurement system over frequency needs to be in order to limit v_{err} below a certain maximum error voltage $\hat{v}_{err}$ for a known input CM voltage v_{sw}. To answer this question, the spectrum of the trapezoidal CM voltage v_{sw} is analyzed. In **Fig. 2 (c)** two spectral envelopes for two input CM voltages $v_{sw,i}$ and $v_{sw,ii}$ are plotted, both with the same transition time T_{slope} but with different switching cycles $T_{sw,i}$ and $T_{sw,ii}$, separated by a factor of 10 ($f_{sw,i} = 1/T_{sw,i} = 10\,\text{kHz}$ and $f_{sw,ii} = 1/T_{sw,ii} = 100\,\text{kHz}$). It can be seen that each envelope features two cut-off frequencies $f_{c,1}$ and $f_{c,2}$, each contributing a $-20\,\text{dB/dec}$ amplitude roll-off. For a given duty-cycle $D = T_{pulse}/T_{sw}$ the cut-off frequencies are found as

$$f_{c,1} = \frac{1}{\pi \cdot T_{pulse}} = \frac{1}{\pi \cdot D \cdot T_{sw}} \overset{D=0.5}{=} \frac{2}{\pi \cdot T_{sw}} = \frac{2}{\pi} \cdot f_{sw} \tag{3}$$

and

$$f_{c,2} = \frac{1}{\pi \cdot T_{slope}} = \frac{1}{\pi} \cdot \frac{|\mathrm{d}v/\mathrm{d}t|}{V_{dc}} \tag{4}$$

as shown in [4] and [5].

Consequently, the spectrum of a trapezoidal waveform can roughly be divided into three sections:

- $f < f_{c,1}$: The value is constant at $20 \cdot \log_{10}(V_{dc})$.
- $f_{c,1} < f < f_{c,2}$: The amplitude rolls off with $-20\,\text{dB/dec}$ as it is the case in the spectrum of a perfect square-wave signal.
- $f > f_{c,2}$: Additional roll-off by $-20\,\text{dB/dec}$ due to the finite rise and fall times, resulting in a total decay of $-40\,\text{dB/dec}$.

The dc amplitude $20 \cdot \log_{10}(V_{dc})$ is chosen such that the envelope matches the exact amplitude $\frac{4}{\pi} \cdot \frac{V_{dc}}{2}$ of the fundamental component of v_{sw} at f_{sw} (which is not equal to $f_{c,1}$), assuming a linear decay of $-20\,\text{dB/dec}$ after $f_{c,1}$.

For an ideal square-wave signal the rise and fall times are zero and therefore $f_{c,2}$ moves to infinity. Hence, there will solely be an amplitude roll-off with $-20\,\text{dB/dec}$ after $f_{c,1}$, which is also depicted in **Fig. 2 (c)**.

As can be noted, the spectrum of the signal with lower switching frequency $f_{sw,i}$ starts to decay already at $f_{c,1i}$, whereas the one with the higher switching frequency decays at $f_{c,1ii} = 10 \cdot f_{c,1i}$, thus resulting in stronger attenuation of the high-frequency content (20 dB more attenuation for the separation of $f_{sw,i}$ and $f_{sw,ii}$ by a factor of 10). As already mentioned, mainly the high-frequency content is responsible for the output error v_{err} and therefore one could assume that v_{err} is also decreased by a factor of 10 when the system is excited with $v_{sw,i}$, i.e. the CM input voltage with the lower switching frequency $f_{sw,i}$. It is true that in the spectrum of $v_{sw,i}$ each spectral component is ten times stronger attenuated (i.e. 20 dB lower) for higher frequencies, however, due to the lower switching frequency the spectral components are also appearing with a ten times higher density, meaning that in a given frequency interval, there will be ten times more spectral components compared to the spectrum of $v_{sw,ii}$ (cf. **Fig. 2 (c)**). In other words, the spectral density, which is related to the signal energy, is the same in both cases and therefore, for a given probe CMRR characteristic, in a first step approximation the resulting time-domain error v_{err} will be the same even for different switching frequencies. An alternative way of looking at this, is to consider the time-domain waveform in **Fig. 2 (a)** and **(b)** and notice that v_{err} quickly decays back to zero and consequently is independent of the switching frequency, as long as $T_{err} < T_{pulse}$. Therefore, v_{err} can be considered as the step response of the measurement system after a CM step and it does not matter how often the step is being applied, provided that the response has decayed back to zero prior to applying the next step.

Typically, the user defines a desired time-domain accuracy ε_{meas} relative to the DM full-scale range $v_{dm,FS}$, meaning that the peak value of the error voltage v_{err} must not exceed $\hat{v}_{err} = \varepsilon_{meas} \cdot v_{dm,FS}$. The accuracy may be related to the oscilloscope resolution, e.g lower than one least significant bit (LSB) which for a 8 bit system corresponds to $\varepsilon_{meas} \approx 0.4\,\%$. Note that today's 12 bit oscilloscopes also feature only around 8 bits of effective resolution but offer much higher bandwidths than older 8 bit oscilloscopes. For $v_{dm,FS} = 25\,\text{V}$ this gives a maximum allowed time-domain error voltage of 100 mV (or $-20\,\text{dBV}$ in a logarithmic scale).

Given the voltage $\hat{v}_{err}$, the worst-case shape fulfilling the requirement $|v_{err}(t)| \leq \hat{v}_{err}$ is a rectangular signal, because at each time instant it has either its maximum or minimum signal value $\pm\hat{v}_{err}$. Assuming a rectangular signal v_{err} with amplitude $\hat{v}_{err}$ as the worst-case output, the spectral components decay with $-20\,\text{dB/dec}$ and therefore the signal spectrum of the maximum allowed output error

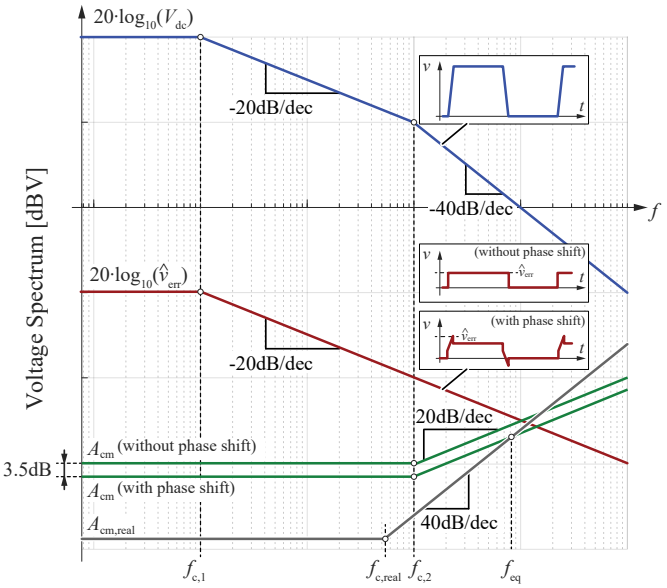


Fig. 3. Magnitude of the spectral envelopes of the trapezoidal CM input voltage v_{sw} (blue), the resulting output error v_{err} (red), which depending on the phase-shift has a purely rectangular shape or some additional over- and undershoot caused by the equivalent line inductance L_{line}. Additionally depicted is the maximum allowed A_{cm} (green) derived from the difference of the two other envelopes, in order to achieve a certain maximum time-domain error $\hat{v}_{\text{err}}$ for the cases without and with phase-shift. Furthermore, an example of a real probe characteristic with a 40 dB/dec increase of $A_{\text{cm,real}}$ (gray) is shown, where the DC value and $f_{\text{c,real}}$ are adjusted to achieve the same $\hat{v}_{\text{err}}$ as with A_{cm}.

voltage is known (cf. red curve in **Fig. 3**). Together with the given spectrum of the CM input voltage v_{sw} (cf. blue curve in **Fig. 3**), the minimum required CMRR characteristic is immediately derived (cf. green curve in **Fig. 3**). The required value (green) can be determined graphically by taking the difference between the input (blue) and the error spectra (red). Please note that in contrast to the CMRR definition in (2) the plotted values are negative on a logarithmic scale, i.e. smaller than one. The reason is, that actually only the CM gain A_{cm} is plotted but since the probe's DM gain A_{dm} is known, the CMRR is directly derived. Within this paper, A_{dm} is always assumed to be unity, hence the inverse value of A_{cm} (i.e. the negated value in a logarithmic scale) directly corresponds to the CMRR.

Concerning the CMRR requirements of the measurement system, it is found that up to the cut-off frequency $f_{\text{c,2}}$, determined by the transition time T_{slope} (cf. (4)), the A_{cm} (or CMRR) characteristic must be flat and only for $f > f_{\text{c,2}}$ an increase of 20 dB/dec (-20 dB/dec decrease of the CMRR) is allowed, since the CM input voltage rolls off with -40 dB/dec, whereas the spectrum of the worst-case error signal only has to roll-off with -20 dB/dec. In this case, the resulting error signal v_{err} is a square-wave voltage with the same switching period T_{sw} as the trapezoidal CM input voltage v_{sw}. This simplification, however, assumes that solely the amplitude but not the phase response is affected by the measurement system.

In real measurement systems, the impedance $\underline{Z}_{\text{line}}$ of the connecting wires between the circuit under test (CUT) and the probe can be modeled as a series connection of a resistance R_{line} and an inductance L_{line}. Hence, the relation between the current i_{earth} flowing through the probe connections to charge the parasitic earth capacitance C_{earth} and the resulting voltage v_{line} across the impedance $\underline{Z}_{\text{line}}$, which actually results in the error voltage v_{err} measured by the probe, can be written

TABLE I. Operation parameters for converters using different types of semiconductor devices.

Device	f_{sw}	V_{dc}	$\mathrm{d}v/\mathrm{d}t$	T_{slope}	$f_{\text{c,2}}$
GaN 200V	400 kHz	150 V	100 kV/µs	1.5 ns	213 MHz
GaN 650V	200 kHz	400 V	200 kV/µs	2 ns	160 MHz
SiC 1200V	200 kHz	800 V	50 kV/µs	16 ns	20 MHz
SiC 10kV	50 kHz	7 kV	80 kV/µs	87.5 ns	3.6 MHz
IGBT 1200V	1 kHz	800 V	2 kV/µs	400 ns	0.8 MHz

as

$$\underline{v}_{\text{line}} = (R_{\text{line}} + j\omega \cdot L_{\text{line}}) \cdot \underline{i}_{\text{earth}}. \tag{5}$$

As can be noticed, when choosing the elements R_{line} and L_{line} accordingly, the same amplitude response as obtained for the maximum allowed A_{cm} (or the minimum required CMRR) characteristic shown in **Fig. 3** (green curve) can be achieved, where apart from the amplitude response the inductance also adds a phase-shift from 0° to 90° for frequencies around $f_{\text{c,2}}$, which even if the amplitude response is the same, also affects the signal in time-domain as

$$v_{\text{line}} = R_{\text{line}} \cdot i_{\text{earth}} + L_{\text{line}} \cdot \frac{\mathrm{d}v_{\text{line}}}{\mathrm{d}t}. \tag{6}$$

If for the minimum required CMRR the same relation between v_{sw} and v_{err} as in (5) is used, whereas now according to real systems also a phase-shift for higher frequencies is considered, R_{line} and L_{line} can be substituted and written as

$$\underline{v}_{\text{err}} = A_{\text{cm}} \cdot \underline{v}_{\text{sw}} = (G_{\text{dc}} + j \cdot \omega \cdot G_{\text{ac}}) \cdot \underline{v}_{\text{sw}}. \tag{7}$$

The time-domain output error response can be analytically expressed in terms of the CM input v_{sw} as

$$v_{\text{err}}(t) = G_{\text{dc}} \cdot v_{\text{sw}}(t) + G_{\text{ac}} \cdot \frac{\mathrm{d}v_{\text{sw}}(t)}{\mathrm{d}t}, \tag{8}$$

where G_{dc} is defined by the maximum CM input voltage V_{sw} (usually V_{dc}) and the maximum allowed output error $v_{\text{err,max}}$ as $G_{\text{DC}} = v_{\text{err,max}}/V_{\text{dc}}$. G_{ac} follows from the given transition time T_{slope} and G_{dc} as $G_{\text{ac}} = G_{\text{dc}} \cdot \frac{T_{\text{slope}}}{2} = G_{\text{dc}} \cdot \frac{1}{2\pi \cdot f_{\text{c,2}}}$.

For a trapezoidal signal v_{sw}, (8) can be further simplified by using $\frac{\mathrm{d}v_{\text{sw}}(t)}{\mathrm{d}t} = \frac{V_{\text{dc}}}{T_{\text{slope}}}$ such that the resulting error voltage becomes

$$\begin{aligned} v_{\text{err}}(t) &= G_{\text{dc}} \cdot v_{\text{sw}}(t) + G_{\text{ac}} \cdot \frac{V_{\text{dc}}}{T_{\text{slope}}} \\ &= G_{\text{dc}} \cdot \left(v_{\text{sw}}(t) + \frac{T_{\text{slope}}}{2} \cdot \frac{V_{\text{dc}}}{T_{\text{slope}}} \right) \end{aligned} \tag{9}$$

with a resulting peak value of

$$\hat{v}_{\text{err}} = G_{\text{dc}} \cdot V_{\text{dc}} + G_{\text{dc}} \cdot \frac{V_{\text{dc}}}{2} = \frac{3}{2} \cdot G_{\text{dc}} \cdot V_{\text{dc}}. \tag{10}$$

It is found that the peak value $\hat{v}_{\text{err}}$ is increased by just a factor of 1.5 compared to the case where the phase-shift was not considered. Hence, to account this, the maximum allowed A_{cm} found by only considering the amplitude response must be decreased by approximately 3.5 dB or equivalent, the minimum required CMRR must be increased by 3.5 dB (cf. the two green curves in **Fig. 3**). Accordingly, having defined the maximum allowed $\hat{v}_{\text{err}}$, the shape of $A_{\text{cm,max}}$ can be found for different circuit realizations with different operating voltages V_{dc} and voltage slopes $\mathrm{d}v/\mathrm{d}t$ as shown in **Fig. 4**, whereas a maximum allowed error voltage $\hat{v}_{\text{err}} = 100$ mV and a probe bandwidth of 1 GHz are assumed. Furthermore, different maximum A_{cm} characteristics for some practice-relevant implementations found in literature [6]–[9] with the respective parameters summarized in **Table I** are highlighted.

It turns out that for realizations with lower operating voltages, typically employing GaN switches, the DC CMRR must not be extremely high (i.e. G_{dc} must not be extremely low) but due to the fast voltage slope and the thereby achievable fast transition times, the

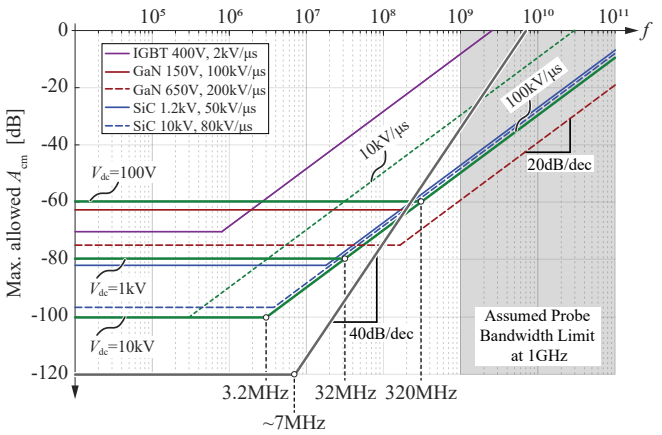


Fig. 4. Maximum allowed A_{cm} to measure converter realizations with different operating voltages V_{dc} and different voltage slopes $\mathrm{d}v/\mathrm{d}t$. The green curves show the cases for a constant $\mathrm{d}v/\mathrm{d}t$ of 100 kV/µs and operating voltages 100 V, 1 kV and 10 kV. Notable is that the curves coincide for frequencies above $f_{\text{c,2}}$. The gray curve shows a possible realization with 40 dB/dec and a DC value of −120 dB giving the same $\hat{v}_{\text{err}}$ for the case of a $\mathrm{d}v/\mathrm{d}t = 100\,\text{kV/µs}$. Additionally depicted are the realizations from **Table I**. In all cases, a probe bandwidth limit of 1 GHz was assumed.

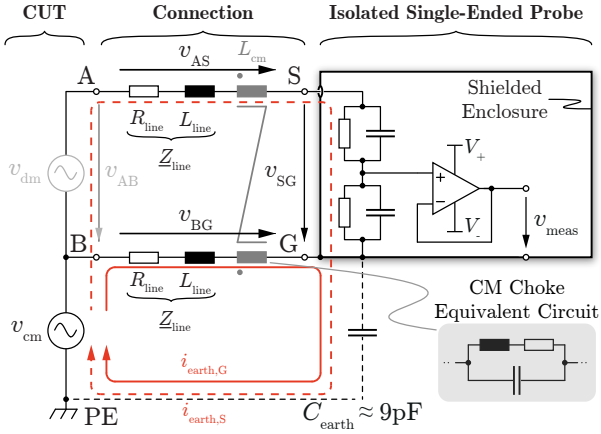


Fig. 5. Simplified circuit of an isolated single-ended probe excited with a differential-mode voltage v_{dm} (gray) and a common-mode voltage v_{cm}, together with the impedances coming from the connections of the probe with a circuit under test. Additional damping by means of a common-mode choke L_{cm} is illustrated as well.

DC value must be maintained up to high frequencies, which is quite demanding for any measurement system.

Furthermore, CMRR measurements with state of the art isolated measurement systems showed that with increasing frequency the CMRR is typically not only decreasing with −20 dB/dec but even with −40 dB/dec. The reason for this is that the CM input voltage v_{sw} is not only directly applied to the line impedance $\underline{Z}_{\text{line}}$ but to the series connection of $\underline{Z}_{\text{line}}$ and the parasitic earth capacitance C_{earth}, which together with the parasitic line inductance L_{line} forms a second order system and therefore the error voltage increases with 40 dB/dec. Consequently, in order to achieve the same small error voltage as with the derived minimum CMRR characteristic which only decreases with −20 dB/dec, for a real system where the CMRR decreases with −40 dB/dec (or equivalent, A_{cm} increases with 40 dB/dec), the cut-off frequency $f_{\text{c,real}}$ and/or the DC CMRR must be increased to higher values (i.e. G_{dc} must be decreased) as it is shown with the gray curve in **Fig. 4** for a $\mathrm{d}v/\mathrm{d}t = 100\,\text{kV/µs}$. Assuming $G_{\text{dc}} = -120\,\text{dB}$, which is a typical value achieved by state of the art isolated measurement systems, all low-frequency components of the CM input signal (where $A_{\text{cm,real}} < A_{\text{cm}}$) are attenuated much stronger than defined by the minimum required CMRR, which would then result in a smaller peak error voltage $\hat{v}_{\text{err}} < 100\,\text{mV}$. Consequently, in order to obtain the same $\hat{v}_{\text{err}}$ for the real transfer function $A_{\text{cm,real}}$, the higher frequency components (where $A_{\text{cm,real}} > A_{\text{cm}}$) are allowed to be less attenuated. It turned out, when assuming a constant voltage slope $\mathrm{d}v/\mathrm{d}t$, the cut-off frequency $f_{\text{c,real}}$ is always the same, even for different operating voltages V_{dc}. Specifically for the case with $\mathrm{d}v/\mathrm{d}t = 100\,\text{kV/µs}$ and the 120 dB DC CMRR, the −40 dB/dec decrease must start no earlier than at 7 MHz. Hence, in order to keep the cut-off frequency $f_{\text{c,real}}$ at this high frequency, the line inductance L_{line} must be kept at a minimum, since in combination with C_{earth} it mainly defines $f_{\text{c,real}}$.

III. State of the Art Measurement Techniques

A. Isolated Single-Ended Probes

As seen in the previous section, the challenge for a good measurement system is to provide a low-impedance path for i_{earth} such that the desired DM measurement is not distorted.

Fig. 5 shows a simplified circuit of an input stage found in an isolated single-ended probe. It consists of a single, frequency compensated voltage divider and a wideband buffer amplifier (also referred to as input buffer) enclosed within a shielded box to provide the necessary immunity against EMI. The enclosure is connected to the probe circuit's reference potential G which itself is equal to the measurement reference and therefore connected e.g. directly to the switch-node. The voltage divider and buffer amplifier are only exposed to the DM voltage v_{dm} and thus for the targeted application do not need to be designed to withstand high voltages. Ideally, for pure CM excitation (i.e. $v_{\text{dm}} = 0$), i_{earth} flows entirely over the ground line and no voltage appears across the voltage divider and input buffer, resulting in an undistorted measurement. As already mentioned, in reality the ground line features a certain impedance, thus during the CM voltage transitions when the earth capacitance has to be charged, a voltage $v_{\text{line}} = v_{\text{BG}}$ appears across the line impedance $\underline{Z}_{\text{line}}$. Even though $\underline{Z}_{\text{line}}$ is also present in the signal connecting line, due to the probe's input impedance, the two impedances seen from the CM input B to the enclosure potential G are not the same, thus the voltages v_{AS} and v_{BG} are unbalanced and yield a voltage v_{SG}, which is measured by the probe and appears at the output terminals as error voltage $v_{\text{meas}} = v_{\text{err}}$ indistinguishable from a desired DM measurement. The decreasing impedance of C_{earth} at elevated frequencies and the simultaneously increasing $\underline{Z}_{\text{line}}$ lead to a decreasing CMRR (as already mentioned typically with −40 dB/dec) at higher frequencies.

B. Verification of Practical Applicability

To reach the specified performance of commercial probes it is usually required to have a nearly ideal setup where the influence of parasitic effects such as the previously mentioned earth capacitance C_{earth} or the CUT-probe connection impedance $\underline{Z}_{\text{line}}$ is reduced as much as possible. Therefore, some probe manufacturers recommend to already consider during the design phase of power electronic converters to include connectors in the layout, such that during the commissioning phase the floating probe can be optimally connected to the measurement point in order to achieve the highest measurement quality. However, especially in power electronic converters employing latest wide bandgap devices, the commutation or gate loop inductances are very critical, hence the used space of the power stage in the layout should be as small as possible and is in many cases even smaller than the footprint of the connectors proposed by the probe manufacturers. Consequently, these connectors cannot be included in the design in order to not degrade the electrical performance of the converter systems. Furthermore, the connectors might not be

suitable in many applications, especially when there are strict space constraints in order to achieve maximum power density or when creepage distance requirements between the measurement points have to be met. The usage of additional wires attached to the connecting lines of the probe, which on the other side are soldered to the PCB or measurement point are often unavoidable.

Typically, measurement systems are internally compensated for the parasitics up to their connecting lines and any additional wires lead to a decrease of the CMRR. In order to be applicable in practice, an isolated measurement system needs to achieve a performance in accordance with the minimum required CMRR vs. frequency also with real measurement setups. Hence, a test setup was built to capture the frequency response of the probe's CMRR where twisted-pair connecting wires of different lengths (0 cm, 1.5 cm, 3 cm and 6 cm) were inserted between common-mode excitation and probe. The probe was elevated by 12 cm and placed on a metal plate connected to PE, resulting in a measured earth capacitance of roughly 9 pF, as also indicated in **Fig. 5**. The PE-referred CM input signal was supplied by a standard arbitrary function generator with an amplitude of $10\,\mathrm{V_{pp}}$ into a $50\,\Omega$ terminated transmission line. The influence of twisted-pair connecting wires of different lengths was investigated and also compared to simulation results where $\underline{Z}_{\mathrm{line}}$ was approximated using a lumped RL-circuit consisting of R_{line} and L_{line}. The two parameters were obtained by measuring the impedance of the twisted-pair cables that were used for the probe measurements. The two current loops (signal and ground line with corresponding return paths over C_{earth} and PE back to the CM input) forming the inductance L_{line} are indicated in **Fig. 5**. Assuming symmetric connections due to the twisted-pair wires with equal length, L_{line} is identical for both the ground and the signal line.

Fig. 6 shows the measurement results of A_{cm} (i.e. 1/CMRR, since $A_{\mathrm{dm}} = 1$) for the connection wires with the lengths as specified above. It can be clearly seen that there is a drastic performance degradation, even for very short connection wires. When doubling the wire length, the inductance roughly increases by a factor of two and the CMRR is expected to drop by 6 dB which is verified by the measurements and visible in the frequency range up to 100 MHz before secondary effects such as resonances start to dominate. Apart from the cases with additional connection wires, **Fig. 6** also shows the case where the CM source is directly connected to the probe without additional leads (blue curve). Nevertheless, a small inductance of 200 pH due to the interconnection is assumed. The dotted lines in **Fig. 6** show the simulated CMRR with the RL-approximation for $\underline{Z}_{\mathrm{line}}$. Adding an additional impedance in series with the probe inputs, which is only appearing for CM signals, i.e. a CM choke (CMC), the CMRR can be improved, since the CM impedance limits the charging current i_{earth} and consequently the voltage v_{line} causing the error voltage v_{err} is lowered. The simulation was carried out for the cases without (dotted lines) and with CMC (solid lines) and for the latter case, the measurements fit the calculations and simulations very well.

At lower frequencies, the mismatch between simulated and measured values is due to the finite resolution of the measurement. The measured values were obtained using the oscilloscope's FFT function where the captured spectra were averaged to achieve a better signal-to-noise ratio. For a CMRR of 120 dB, a common-mode excitation of $10\,\mathrm{V_{pp}}$ yields an error output voltage v_{err} of only $10\,\mu\mathrm{V_{pp}}$, which is hardly measurable in the noise floor despite the averaging. Consequently, values are likely to be even better for frequencies around 1 MHz and below.

From the additionally depicted maximum allowed A_{cm} as obtained from the gray curve in **Fig. 4**, it becomes clear that even for the case with a CMC, already very short wires of $1-2$ cm length lead to a performance degradation of almost 40 dB at higher frequencies. Increasing the wire length up to 6 cm reduces the rejection by a factor of 1000 (i.e. 60 dB) such that at 100 MHz only 20 dB are achieved, hence the usability of single-ended isolated probes under non-ideal

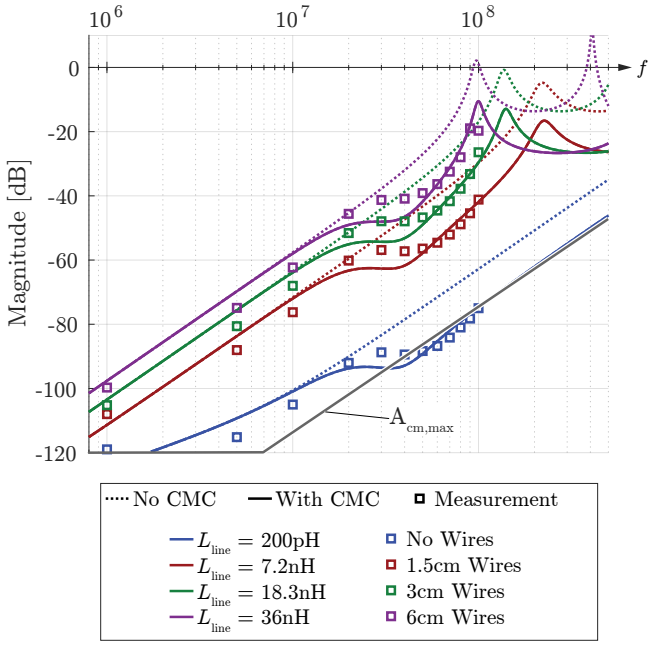


Fig. 6. CMRR measurements with an isolated single-ended probe together with the comparison to simulation outputs with an approximated connection line impedance using a lumped RL-circuit for the cases with and without an input CM choke. Furthermore, the minimum required CMRR for a voltage slope $\mathrm{d}v/\mathrm{d}t = 100\,\mathrm{kV/\mu s}$ as defined in **Fig. 3** is shown (values below $\mathrm{CMRR_{min}}$ indicate sufficient performance).

conditions is highly limited. Furthermore, it needs to be noted that the performance degradation is not due to unequal lengths of the twisted-pair connecting wires because the reduction is also visible in the simulation where perfectly symmetric impedances $\underline{Z}_{\mathrm{line}}$ were assumed for both, the signal and the ground line. To conclude, it can be said that the usage of a CMC to attenuate distortions before they are applied to the probe does help to improve the performance but isolated single-ended probes are inherently very sensitive regarding parasitics from the actual measurement setup.

C. High-Voltage Differential Probe

An alternative method to carry out floating measurements is the usage of standard non-isolated high-voltage differential probes. The principal structure of such a system is shown in **Fig. 7** and contains basically two frequency-compensated voltage dividers referred to PE forming a Wheatstone bridge [10], followed by a difference amplifier subtracting the two divided input signals. To have a high input impedance, two matched signal buffers, responsible to transform the high input divider impedance to a low output impedance suitable for the difference amplifier, are included between the divider and the subtraction stage. As opposed to an isolated solution, the two input dividers need to be designed not only to withstand the full DM voltage but also the full CM voltage. Since the latter can be as high as several kilovolts, a division ratio in the range of 1:100 to 1:1000 or even higher is required. However, as an advantage, due to the high input voltage capability, those probes are insensitive to erroneous connection because the DM input voltage rating is equal to the CM voltage rating. The disadvantage is that the large division ratio also attenuates the typically already small v_{dm}. Eventually, taking the difference of two heavily attenuated signals is much more prone to errors such as circuit noise or matching inaccuracies compared to measuring directly the difference signal, thus resulting in a reduced measurement resolution.

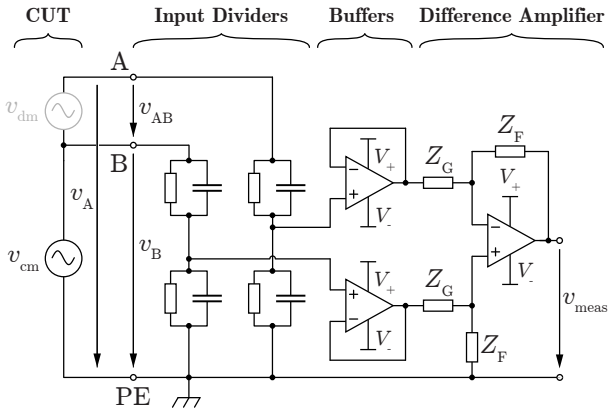


Fig. 7. Standard non-isolated high-voltage differential probe with all the circuitry referred to PE.

IV. Improved Approach

A. Circuit Structures

With the aim to combine the advantages of both, the isolated single-ended and the non-isolated differential approach, in this paper a floating differential measurement is introduced with the basic structure given in **Fig. 8 (a)** and **(b)**. Due to the isolation, the complete circuit is referred to the floating potential G and the input stage is exposed solely to v_{dm}, allowing a smaller division ratio and therefore higher measurement resolution as it is the case for isolated single-ended probes. Special care needs to be taken of the low capacitive impedance of C_{earth} at higher frequencies (e.g. less than $180\,\Omega$ at 100 MHz for $C_{\text{earth}} = 9\,\text{pF}$) because in contrast to a single-ended probe, there is no low impedance ground line present to carry the majority of the CM charging current i_{earth}. Without additional measures, a capacitive voltage divider is formed with the compensation capacitors of the input dividers and C_{earth}. Since their values are in a similar range as or slightly smaller than C_{earth}, inadmissibly high voltages appear at the buffer inputs potentially destroying the measurement-device.

The introduction of a third connection between CUT and probe, a so-called charging line, which can be directly connected between one of the differential inputs and the enclosure prevents the occurrence of high voltages at the buffer inputs as it has the same purpose as the ground line for single-ended probes (cf. **Fig. 5**). A certain parasitic impedance $\underline{Z}_{\text{line}}$, actually the same as for single-ended probes, is again present as soon as a physical connection is made, leading to a splitting of i_{earth} into the main part $i_{\text{earth,G}}$ flowing over the charging line and two symmetric parts $i_{\text{earth,A}}$ and $i_{\text{earth,B}}$ flowing through the input dividers. The exact ratio between the three currents depends on $\underline{Z}_{\text{line}}$ as well as the input impedance of the two voltage dividers.

Apart from the charging line it is again advisable to use a CMC L_{cm} at the probe inputs to additionally damp the disturbance. By doing so, there exist two possible configurations:

i) The charging line is fed through the CMC together with the two signal lines, hence a large part of v_{cm} appears over L_{cm} and only a very small remainder is present at the probe inputs (cf. Configuration A in **Fig. 8 (a)**)
ii) The charging line bypasses the CMC, i.e. a low-impedance path for i_{earth} is provided. A part of the voltage v_{CG} across the charging line is appearing across the CMC in the signal lines such that again only a very small remainder results at the probe inputs A and B with respect to G (cf. Configuration B in **Fig. 8 (b)**)

Fig. 8 (c) shows the simulated common-mode rejection A_{cm} from the input v_{cm} to one of the probe inputs A or B with respect to G, i.e. the transfer function $v_{\text{AG}}/v_{\text{cm}}$ or $v_{\text{BG}}/v_{\text{cm}}$ respectively, assuming the worst-case connection with $L_{\text{line}} = 36\,\text{nH}$. The rejection for the two previously described configurations A and B as well as for the case without charging line is plotted, each with (solid lines) and without CMC (dotted lines) at the inputs. Obviously, configurations A and B behave identical in case of a missing CMC. As a comparison, also the rejection obtained with the single-ended probe with the same line inductance is shown (purple line).

The big advantage of the differential structure is that the remaining error voltage can be further reduced by taking the difference between the input voltages v_{AG} and v_{BG}. Compared to the single-ended approach, the proposed structure therefore allows further reduction of the CM error voltage v_{err}. Provided perfectly symmetric connection wires, i.e. equal $\underline{Z}_{\text{line}}$ at inputs A and B, the voltage difference v_{AB} between the inputs is zero and together with well matched input dividers, no voltage appears between the two divider bridge legs and the CM voltage is not leading to an error voltage v_{err}.

For the cases with charging line it becomes evident that an input CMC helps to improve the rejection. Configuration A performs almost identical to the single-ended case, while Configuration B performs even better at high frequencies, improving the rejection up to 20 dB compared to the single-ended case without even taking the difference, making it the favorite solution. A further advantage of Configuration B is the small voltage drop across the CMC (not larger than v_{CG}, which is already small due to the low charging line impedance), which prevents accidental saturation of the CMC core.

Comparing the plots with the maximum allowed A_{cm}, none of the approaches seem to be suited for the target $\hat{v}_{\text{err}} = 100\,\text{mV}$ with the given $L_{\text{line}} = 36\,\text{nH}$ and $\text{d}v/\text{d}t = 100\,\text{kV/µs}$. In addition, looking at the dependence of the rejection of Configuration B on the value of L_{line} (cf. **Fig. 8 (d)**), the same performance drawback as in the single-ended case is visible. However, the subsequent difference amplifier rejects the error being common to v_{AG} and v_{BG} and since the two voltages are identical when assuming a symmetric connection and pure CM excitation, the performance is improved further and the exact amount is only dependent on the matching of the two channels and only a relative mismatch of $\underline{Z}_{\text{line}}$ between the connections to terminals A and B develops an additional error voltage. In contrast, for the single-ended case, any presence of $\underline{Z}_{\text{line}}$, regardless whether matched or unmatched lead to an increased error voltage.

B. Limitations

The previously presented structure improves the performance compared to an isolated single-ended one, thanks to the subtraction of the two voltages v_{AG} and v_{BG}, which are equivalent for pure CM excitation, in a subsequent stage, as it is the case in a conventional differential probe. There are two key limitations inherent to any form of a differential probe (non-isolated and isolated), that need to be taken into account:

i) Asymmetries in the input divider stage and between the two input buffers.
ii) Limited CMRR of the difference amplifier.

Referring back to **Fig. 8 (a)** and **(b)**, one could also think of this as an arrangement of two matched isolated single-ended probes, each of them represented by one voltage divider and one buffer amplifier. One of them is measuring the actual DM signal referred to the fluctuating CM voltage and the other one solely the CM excitation. To cancel the effect of the limited CMRR of the two probes, the respective output voltages are subtracted by the difference amplifier. This analogy, however, is only valid when the charging line is present and connected to one of the inputs. For conventional differential probes this is usually not the case.

Assuming the two single-ended probes are connected to the same source, i.e. for pure CM excitation, any asymmetry or mismatch between them leads to outputs being not perfectly equal in magnitude and/or phase. When taking the difference afterwards, an error voltage v_{err} results. **Fig. 9 (a)** shows the influence of a relative amplitude and

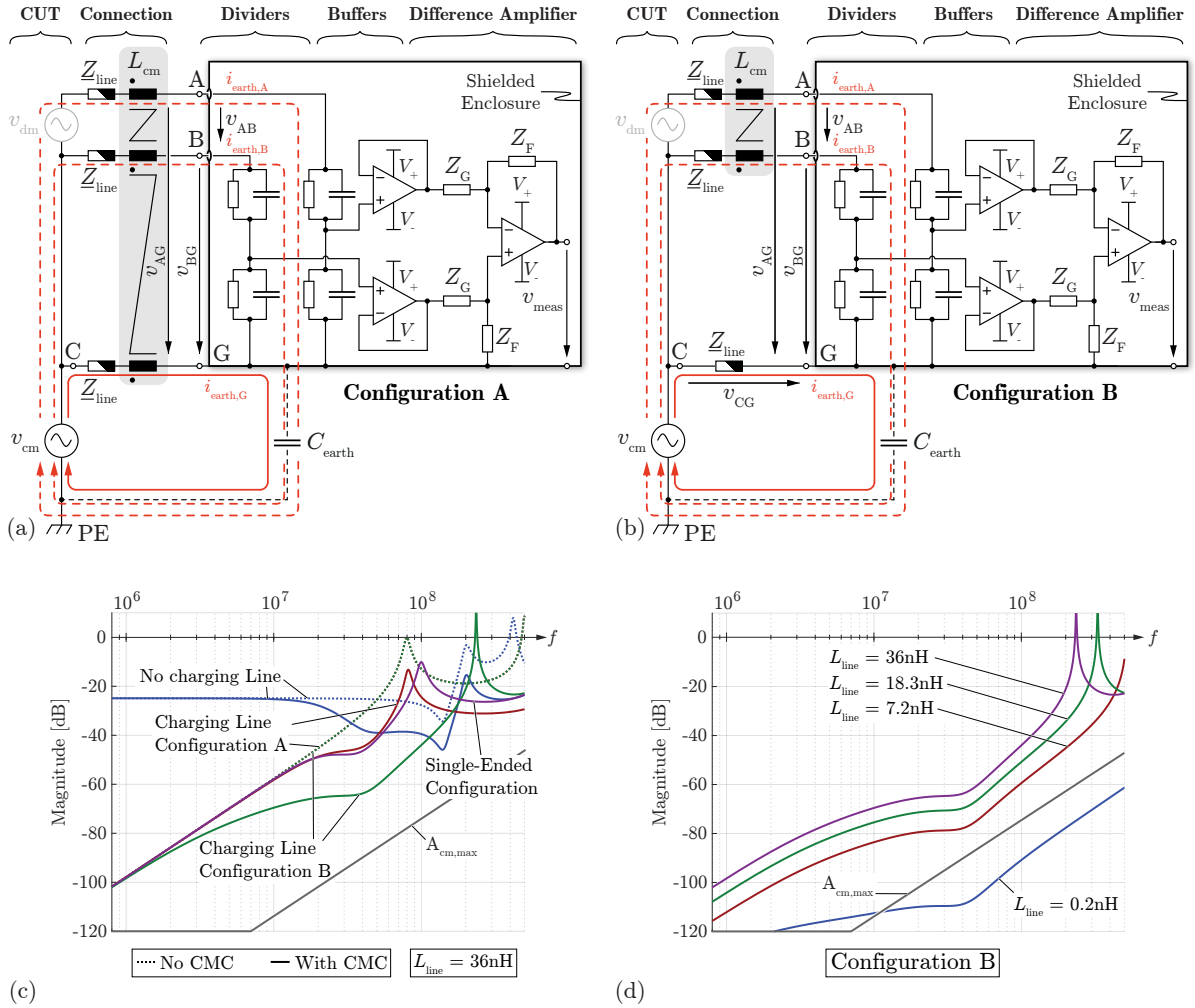


Fig. 8. Two isolated differential probe structures where the charging line between C and G is **(a)** also fed through the CMC (Configuration A) and **(b)** bypassing the CMC (Configuration B). **(c)** Simulation of the CMRR for the two configurations with and without the input CMC L_{cm} assuming $L_{line} = 36\,nH$. Included is also the measurement from the single-ended structure with the same L_{par} as well as the minimum required CMRR as found in **Fig. 4**. In addition, the case for a missing charging line is plotted. **(d)** Sensitivity of Configuration B with respect to various line inductances, including again the minimum required CMRR.

phase error between two nominally identical signals on the maximum achievable CMRR, assuming an ideal difference amplifier. Please note that when looking at **Fig. 8 (a)** and **(b)**, the term CMRR now relates only to the ratio between the input v_{AG} or v_{BG} and the output error voltage v_{err} at the v_{meas} terminal. Therefore, this stage further improves the performance already obtained from the passive filtering (cf. **Fig. 8 (c)** and **(d)**).

Assuming solely an amplitude mismatch, the maximum allowed relative amplitude error $\varepsilon_{ampl,max}$ for a desired CMRR in dB can be calculated as

$$\varepsilon_{ampl,max} = 10^{-CMRR/20}. \tag{11}$$

In a similar way, assuming perfect amplitude matching but mismatched phases, the maximum allowed relative phase error $\varepsilon_{phase,max}$ is found as

$$\varepsilon_{phase,max} = \frac{1}{\pi} \cdot \arcsin\left(\frac{1}{2} \cdot 10^{-CMRR/20}\right). \tag{12}$$

Evaluating (11) and (12) for different CMRR values, it can be seen that the phase accuracy must be more than six times higher than the amplitude accuracy, in order to get the same CMRR.

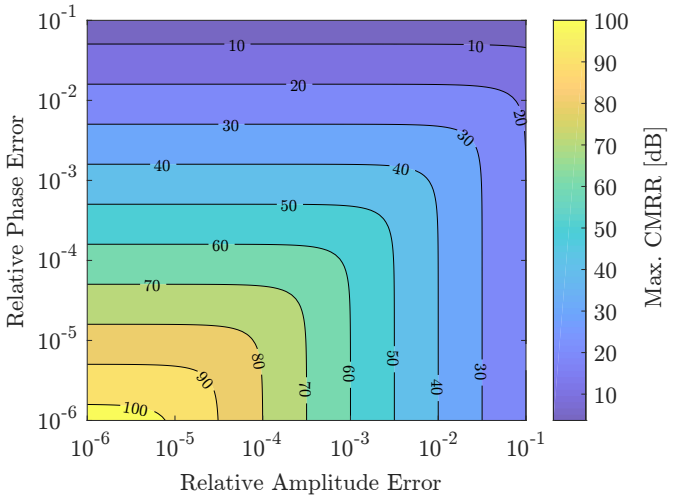
While the amplitude can be matched very precisely using potentiometers, the phase must be adjusted with tunable capacitors. Matching of the phase response over the whole frequency range is particularly difficult because there are always parasitic impedances present e.g. from the circuit layout and component placement. In addition, second-order effects such as non-linearities from the buffer amplifiers e.g. due to slightly unequal bandwidths, slew rates etc. are influencing the behavior as well. These issues could be addressed by integrating the complete analog front-end on an integrated circuit.

When also considering the second limiting factor, namely the finite CMRR of the difference amplifier $CMRR_{OPA}$, the maximum achievable CMRR is limited to this value as shown in **Fig. 9 (b)** where $CMRR_{OPA} = 60\,dB$ was assumed throughout the desired frequency range [11] (worst-case approximation). When using linear terms (i.e. not the values in dB), the total CMRR can be calculated analytically as described in [12] as

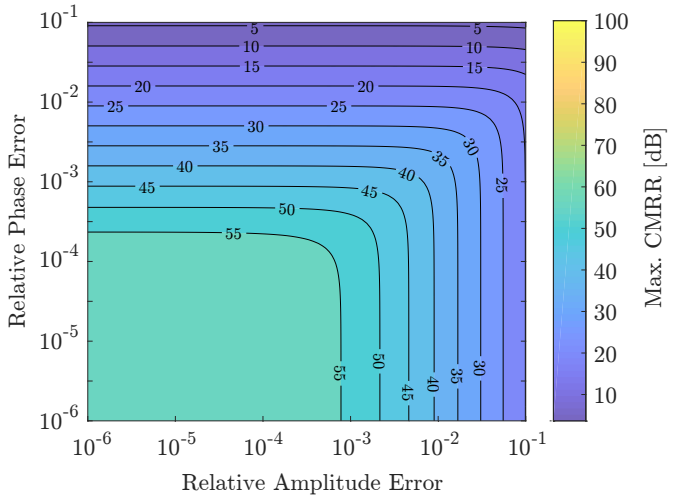
$$\frac{1}{CMRR_{tot}} = \frac{1}{CMRR_{Matching}} + \frac{1}{CMRR_{OPA}}. \tag{13}$$

The upper limit

$$CMRR_{tot,max} = \min\{CMRR_{Matching}, CMRR_{OPA}\} \tag{14}$$



(a)



(b)

Fig. 9. Maximum achievable CMRR with a differential probe versus relative amplitude and phase error between the two nominally identical input signals **(a)** assuming an ideal difference amplifier and **(b)** assuming a finite CMRR of 60dB from the difference amplifier itself.

is then immediately visible. To achieve values below CMRR_{OPA}, according to **Fig. 9**, the required matching accuracy is almost identical for both, ideal and non-ideal OPA CMRR.

C. Applicability for Isolated Differential Probes

Despite the aforementioned limitations, even an imperfect difference stage helps to improve the performance given in **Fig. 8 (c)** and **(d)** because any CMRR larger than one (i.e. A_{cm} smaller than one) in the difference stage further attenuates the remaining error visible at the probe input terminals. Comparing the results in **Fig. 8 (d)** with the maximum allowed A_{cm}, an additional rejection by around $30-40\,\text{dB}$ is needed to achieve sufficient performance, given a line inductance L_{line} of $36\,\text{nH}$, voltage slopes $\text{d}v/\text{d}t = 100\,\text{kV/µs}$ and $\hat{v}_{\text{err}} = 100\,\text{mV}$. Referring to **Fig. 9 (b)**, this corresponds to a phase accuracy of around $0.15\,\%$, i.e. an absolute error of $0.54\,\text{deg}$, which is still achievable with tunable capacitors, adequate operational amplifiers and careful trimming.

V. Conclusion

This paper shows the importance of isolated measurement systems in today's and next generation power electronic applications. The presented method to estimate the required performance of a measurement system based on the operating parameters of a given converter realization helps to select an appropriate solution. It is shown that the single-ended structure, on which state of the art solutions rely, is very sensitive with respect to imperfections faced in real measurement setups. Any connection wires between the probe and the circuit under test lead to a significant performance degradation, making it very hard to reach a sufficient Common-Mode Rejection Ratio (CMRR) over the whole frequency range of interest. To improve the performance and reduce the sensitivity, a differential structure is proposed. It uses two isolated measurement channels, each of them already featuring good common-mode rejection, which are then subtracted from each other to reduce the residual error signal even more. However, two perfectly matched symmetric signal chains are very difficult to realize, especially at high frequencies. Based on the corresponding amplitude and phase mismatch, an upper value for the CMRR of the difference stage alone is found. It is shown that compared to a conventional differential probe, the performance does not solely rely on the matching accuracy but is rather determined by the combination of isolation and passive CM filtering already present on single-ended structures as well as the additional CMRR of the subsequent difference stage, thus offering improved overall rejection. Thanks to the differential configuration, any error caused by symmetric connection wires is canceled and does therefore not degrade the measurement performance.

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