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Closed-Loop IGBT Gate Drive Featuring Highly Dynamic dI/dt and dv/dt Control

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Closed-Loop IGBT Gate Drive Featuring Highly Dynamic $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ Control

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***Abstract*—In this paper, a closed-loop active IGBT gate drive providing highly dynamic $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control is proposed. By means of using only simple passive measurement circuits for the generation of the feedback signals and a single operational amplifier as PI-controller, high analog control bandwidth is achieved enabling the application even for switching times in the sub-microsecond range.**

Therewith, contrary to state of the art gate drives, the parameter dependencies and nonlinearities of the IGBT are compensated enabling accurately specified and constant $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ values of the IGBT for the entire load and temperature range. This ensures the operation of an IGBT in the safe operating area (SOA), i.e. with limited turn-on peak reverse recovery current and turn-off overvoltage, and permits the restriction of electromagnetic interference (EMI).

A hardware prototype is built to experimentally verify the proposed closed-loop active gate drive concept.

I. Introduction

IGBT modules are widely used in inductive load switching voltage source power electronic converters such as drives, switched-mode power supplies or solid state transformers. Driving the IGBT and thereby minimizing its switching losses, limiting the current and voltage conditions to the SOA and restricting EMI for the entire load and temperature range is the challenging task of an IGBT's gate drive. Low switching losses can be achieved by means of fast switching transients [1]. To operate the IGBT in the SOA mainly the turn-off overvoltage $v_\mathrm{CE,ov}$ and the diode's peak reverse recovery current i_rr during turn-on have to be limited. In doing so, the (negative) collector current slope $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ at turn-off causes an overvoltage,

$$v_\mathrm{CE,ov} = -L_\mathrm{s}\frac{\mathrm{d}i_\mathrm{C}}{\mathrm{d}t}, \tag{1}$$

where L_s denominates the commutation loop inductance (cf. Fig. 1). At turn-on, the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ affects the peak reverse recovery current,

$$i_\mathrm{rr} \approx \sqrt{Q_\mathrm{rr}\frac{\mathrm{d}i_\mathrm{C}}{\mathrm{d}t}}, \tag{2}$$

assuming a symmetrical triangular-shaped reverse recovery current where Q_rr corresponds to the diode's reverse recovery charge.

To provide electromagnetic compatibility (EMC), the collector-emitter voltage slope $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ and the collector current slope $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$, i.e. the rate of change of the current in the commutation loop, have to be restricted [2, 3].

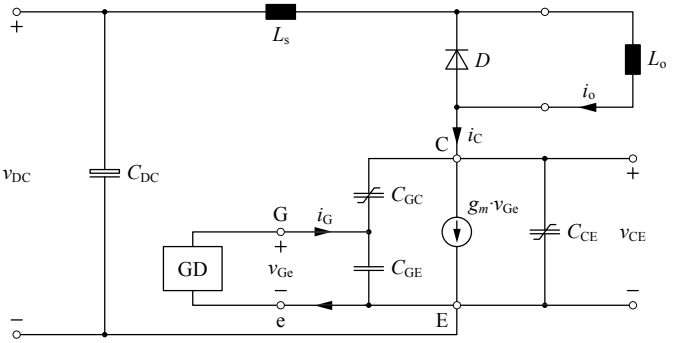

Fig. 1: Equivalent circuit for the inductive load switching including a simple IGBT model. L_s corresponds the sum of the DC-link, busbar and IGBT module internal inductance, i.e. the commutation loop inductance.

As will be shown in the following, the current and voltage slopes depend on various internal parameters and effects of the IGBT. Accordingly, for conventional gate drives a considerable variation of the switching trajectories could occur. To identify the main dependencies of an IGBT's switching behavior, the equivalent circuit of Fig. 1 including a simple IGBT model as used in [4] and also similar to a MOSFET model [5] is considered for the analysis of the inductive load switching in the following.

A. Nonlinearities and temperature dependency

During the current slope, assuming a gate capacitance C_GE significantly larger than the Miller capacitance C_GC as shown in Fig. 3 for $v_\mathrm{CE} \gg 0\,\mathrm{V}$, the gate current i_G mainly charges C_GE,

$$\frac{\mathrm{d}v_\mathrm{Ge}}{\mathrm{d}t} = \frac{i_\mathrm{G}}{C_\mathrm{ies}} \approx \frac{i_\mathrm{G}}{C_\mathrm{GE}}. \tag{3}$$

Considering a transconductance g_m of an IGBT module and using (3), the collector current and its time derivative can be calculated,

$$i_\mathrm{C} = g_m \cdot v_\mathrm{Ge}, \tag{4}$$

$$\frac{\mathrm{d}i_\mathrm{C}}{\mathrm{d}t} \approx \frac{i_\mathrm{G}}{C_\mathrm{GE}}\left(g_m + v_\mathrm{Ge}\frac{\mathrm{d}g_m}{\mathrm{d}v_\mathrm{Ge}}\right). \tag{5}$$

As a result, according to (5) and due to the nonlinearity and junction temperature (T_j) dependency of the transconductance g_m (cf. Fig. 2), for a given gate current i_G a higher junction

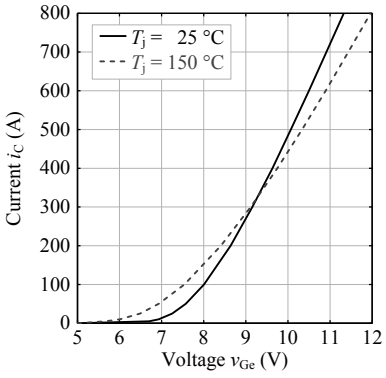

Fig. 2: Typical nonlinear IGBT transconductance g_m (Infineon FF450R12KE4) in dependency of the junction temperature T_j.

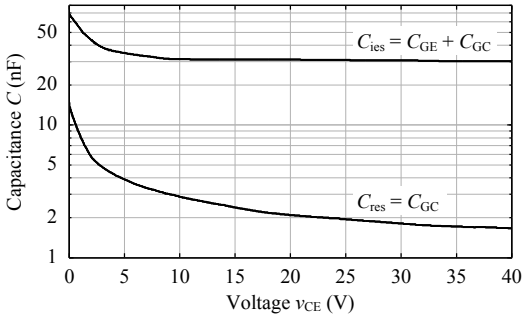

Fig. 3: Typical voltage v_CE dependency of C_res and C_ies (Semikron SKM 500 GA 123 D) valid in the small-signal domain at $v_\mathrm{Ge} = 0\,\mathrm{V}$ and $f = 1\,\mathrm{MHz}$.

temperature T_j leads to a slower current slope and $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ increases with increasing v_Ge and i_C.

During the voltage slope, the gate voltage stays constant at $v_{\mathrm{Ge},i_\mathrm{o}}$ while the gate current i_G charges the Miller capacitance C_GC,

$$\frac{\mathrm{d}v_\mathrm{CE}}{\mathrm{d}t} = -\frac{\mathrm{d}v_\mathrm{GC}}{\mathrm{d}t} = -\frac{i_\mathrm{G}}{C_\mathrm{GC}}. \tag{6}$$

Since the Miller capacitance C_GC strongly depends on the voltage v_CE (cf. Fig. 3), i.e. C_GC is comparably large for low values of v_CE, for a given gate current i_G, $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ varies with the actual collector-emitter voltage v_CE.

B. Operating point / load current dependencies

A voltage source ($v_{+/-}$) gate drive with gate resistor R_G is typically applied to drive an IGBT. Therewith, the gate current i_G during the voltage slope can be expressed as

$$i_\mathrm{G} = \frac{v_{+/-} - v_{\mathrm{Ge},i_\mathrm{o}}}{R_\mathrm{G}}. \tag{7}$$

According to an IGBT's transconductance g_m (cf. Fig. 2) an increase in the load current i_o and / or i_C leads to a higher gate voltage $v_{\mathrm{Ge},i_\mathrm{o}}$ and as per (7) reduces the turn-on gate current i_G at the voltage slope but increases the negative gate current at turn-off. Taking (6) into account, it can be declared for this case that a higher load current i_o increases the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ at turn-off but decreases the voltage slope at turn-on. This behavior is enhanced at turn-off due to the influence of the

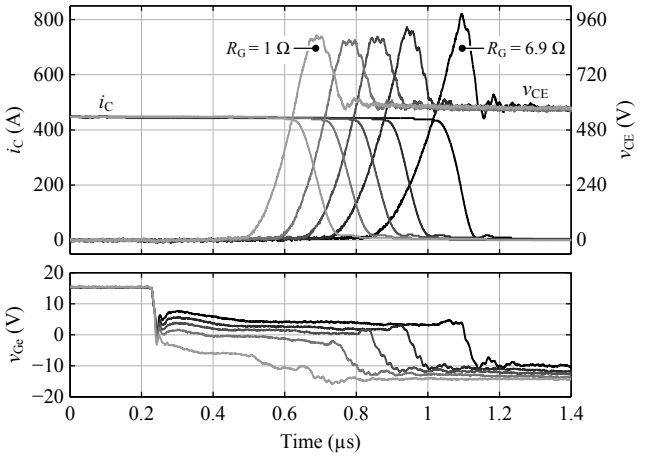

Fig. 4: Measured inductive load turn-off waveforms of a Trench IGBT module (Infineon FF450R12KE4) for different gate resistor values $R_\mathrm{G} = \{1\,\Omega, 2.7\,\Omega, 3.9\,\Omega, 5\,\Omega, 6.9\,\Omega\}$.

charge carrier density in the IGBT [6, 7].

C. Intrinsic switching behavior of Trench IGBT modules

According to (7) and (6) a slight increase of the gate resistor R_G during turn-off leads to a lower $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$. Thereby, more stored charge is extracted, i.e. a desaturation of the device occurs, resulting for Trench IGBTs in an unexpected and typically unwanted faster current slope causing higher overvoltage (cf. (1)) [6–8]. In Fig. 4 the measured turn-off transients for a Trench IGBT module are depicted for different gate resistors to verify this phenomena.

In summary, the mentioned parameter dependencies and effects, that influence the IGBT's switching transients, make it challenging for the gate drive to optimally switch the IGBT at the desired current and voltage slopes for all load current and temperature conditions and are calling for advanced, i.e. active gate drive concepts.

In this paper, first, state of the art gate drive concepts for adjusting the switching transients are illustrated in section II. Thereafter, in section III an active IGBT gate drive providing highly dynamic closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$- and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$-control is proposed. Key components for the hardware implementation of the system are subsequently investigated in section IV. Finally, the performance of the proposed gate drive is experimentally verified in section V by measurements with a developed hardware prototype.

II. State of the art concepts for adjusting the current and voltage slopes

In this section state of the art feed-forward (II-A) and closed-loop (II-B) control concepts for adjusting the current and voltage slopes at turn-on and turn-off are discussed.

A. Feed-forward control concepts

A simple and common way of adjusting the switching speed of IGBTs is to extend the basic gate drive circuit by additional passive components. Additional gate resistance R_G reduces the gate current for a voltage source gate driver as per (7)

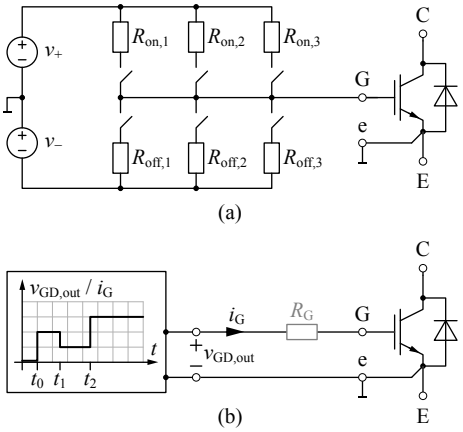

Fig. 5: Adjustable gate drive by means of (a) switchable gate resistors or (b) switchable gate voltage or gate current source featuring discrete resistances or voltage or current levels.

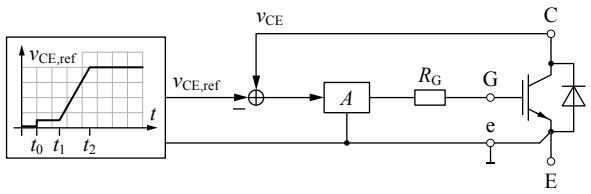

Fig. 6: Simplified closed-loop v_{CE} control concept with a reference voltage v_{CE} profile.

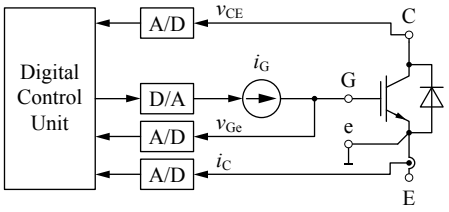

Fig. 7: Digital gate driver unit comprising a microcontroller (e.g. FPGA), A/D converters for measuring the IGBT's state variables and a D/A converter providing the reference signal for the controlled gate current source [27].

and therefore also both current and voltage slopes according to (5) and (6). The insertion of extra Miller capacitance C_{GC} mainly lowers $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ considering (6) and added gate-emitter capacitance C_{GE} slows down $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$, cf. (5), [9]. This approach typically causes either increased switching losses or increased switching delays and gate driving losses due to the larger capacitances.

For avoiding additional switching and gate drive losses, a feed-forward gate-voltage shape generator [10] can be used to adjust the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ at turn-on, tough with this approach the controllability of the voltage slope is limited.

Switchable or adjustable gate resistor(s) [9, 11–13], current sources / sinks [3, 4, 11, 14–20] or gate voltages [21] are further possibilities to influence the gate current and therewith the current and voltage slopes during the switching transients. A schematic overview of such gate drive concepts is depicted in Fig. 5. Independent of the applied concept, the selection of the driver output stage's value can either be based on a fixed profile [11, 19], an operating point dependent action [12, 13, 20] or an event feedback of the switching transients [4, 12, 14–17, 21]. As the implementation has to ensure an operation of the IGBT in the SOA, i.e. finally limited $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$, for all operating conditions (varying T_{j}, i_{C}, v_{DC}), for most of the operating points the desired optimal current and voltage slopes are not achieved leading to increased switching losses. In addition, if an event feedback is employed, the actual state of the semiconductor, e.g. the transition from the current to the voltage transient and vice versa, must be detected with minimum delay in an additional complex circuit, in order to be able to independently adjust $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$.

Missing compensation of the IGBT's nonlinearities and / or typically remaining dependencies on the load and temperature conditions is a further and main drawback of all these open-loop control concepts. With an open-loop approach, accurately defined and constant current and voltage slopes in all operating points can therefore hardly be obtained. For that reason, closed-loop concepts with negative feedback are applied to achieve more precise control.

B. Closed-loop control concepts

Compensation of the IGBT's nonlinearities and operating point and temperature dependencies is achieved by feedback of information on i_{C} and / or v_{CE}.

A closed-loop analog v_{CE} control topology as shown in Fig. 6 was proposed and investigated in [22–26]. A similar approach could also be followed for an i_{C} control. If a combination of voltage and current control is needed, the generation of both reference signals by analog circuits will be involved and hardly feasible due to their mutual dependency and the dependency on the operating point, e.g. the temporal variation of the state transition (current- / voltage slope) or the value of the load current.

By means of a digital approach for controlling i_{C} and v_{CE} as developed in [27–30] and schematically pictured in Fig. 7, the handling of a combined current and voltage control becomes feasible. In doing so, all main state variables (i_{C}, v_{CE} and v_{Ge}) are sampled and processed in a digital control unit that controls the gate current in accordance to the desired switching operation. Due to the large delay times of the D/A- and A/D-conversion of 100 to 200 nanoseconds [27] in the signal paths, a real-time approach is not promising for IGBT switching transients faster than a few microseconds. Iterative, adaptive and system parameter dependent approaches are therefore typically applied to overcome this problem [27–30]. Their main downside is the lack of accurate control for a significant change in the system state of subsequent switching operations.

In addition, the limited bandwidth of current sensors and the highly dynamic reference and feedback signals are limiting the performance and accuracy of any i_{C} and v_{CE} control concept.

Best performance with regard to analog control bandwidth is achieved by means of closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control concepts [31, 32] as shown in Fig. 8 due to constant reference value(s), simple control amplifier stages and passive

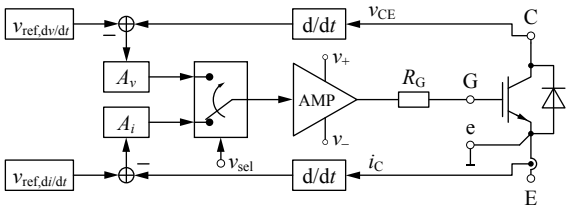

Fig. 8: Schematic closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control topology [39] where the transition between $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control has to be actively triggered via v_{sel}.

measurement circuits providing high analog bandwidth as will be explained in section IV-A. Different implementations of only $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control [33–35], $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control at turn-on and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control at turn-off [36], or individual solutions for current or voltage slope control during turn-on or turn-off [37, 38] have been presented. A complete solution of turn-on and turn-off $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control was presented in [39, 40]. Therewith, due to the implementation with a large number of bipolar transistors and the need for detection and selection of the active control loop (cf. Fig. 8), the performance was limited to $200\,\mathrm{A}/\mu\mathrm{s}$ and $1\,\mathrm{kV}/\mu\mathrm{s}$ respectively.

In the following section, a highly dynamic closed-loop combined $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control individually for turn-on and turn-off without a need of active control loop selection is proposed and presented.

III. Proposed Closed-Loop Active Gate Drive

A. Conceptual description and operating principle

To explain the basic idea of the proposed solution, first, the inductive current switching of an IGBT is reviewed. Based on typical waveforms, cf. Fig. 9, further described in Table I, it can be seen that the intervals with current and voltage changes always appear in direct sequence and / or without overlap at both turn-on and turn-off. Furthermore, ideally, $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ is zero during the collector current change and $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ is zero during the collector-emitter voltage change. This fact permits the utilization of a combined $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ closed-loop control, i.e. both control loops are closed simultaneously via a single PI-controller and / or in contrast to [39, 40] no active selection of a control loop is required. In so doing, a natural transition from the current to the voltage slope control and vice versa occurs due to the just highlighted characteristic of the inductive current switching of the IGBT.

However, a single exception has to be considered and handled. In the phase where i_{C} is reduced after the diode's peak reverse recovery current at turn-on, $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ is not zero during the voltage slope, different to the original assumption, cf. Fig. 9 (a). For that reason, a clipping circuit preventing this unwanted negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback during the turn-on voltage slope will be presented in section IV-C.

The block diagram for the proposed combined closed-loop current and voltage slope control is depicted in Fig. 10. There, the input reference signal $v_{\mathrm{ref,d}/\mathrm{d}t}$, that is set once at the beginning of every switching operation, is kept at a constant value for the whole switching process and defines in

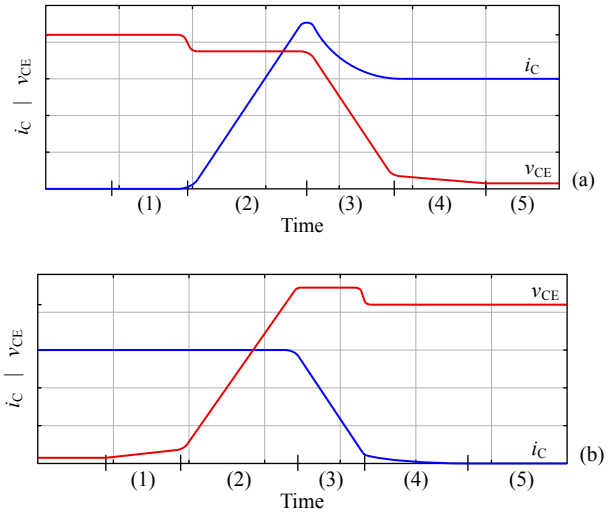

Fig. 9: Schematic current and voltage waveforms of the inductive load switching transients at (a) turn-on and (b) turn-off. Each labeled interval (i) is specified and described in Table I.

TABLE I: Description of the intervals of the inductive load switching transients according to Fig. 9.

interval	(a) turn-on	(b) turn-off
(1)	turn-on delay ($v_{\mathrm{Ge}} < v_{\mathrm{Ge,th}}$)	charge large C_{GC}
(2)	$\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$	$\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$
(3)	$\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$	$\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$
(4)	discharge large C_{GC}	tail current
(5)	on-state	off-state

combination with the feedback gains k_i and k_v, cf. Fig. 10, the set-points for both control variables,

$$\left(\frac{\mathrm{d}i_{\mathrm{C}}}{\mathrm{d}t}\right)_{\mathrm{ref}} = \frac{v_{\mathrm{ref,d}/\mathrm{d}t}}{k_i \cdot L_{\mathrm{E}}}, \tag{8}$$

$$\left(\frac{\mathrm{d}v_{\mathrm{CE}}}{\mathrm{d}t}\right)_{\mathrm{ref}} = -\frac{v_{\mathrm{ref,d}/\mathrm{d}t}}{k_v}. \tag{9}$$

Accordingly, a turn-on, at which $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ is positive and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ negative, is initiated by setting $v_{\mathrm{ref,d}/\mathrm{d}t}$ to a constant positive value which is amplified and integrated by the PI-controller to charge the IGBT's gate. Applying a negative value at $v_{\mathrm{ref,d}/\mathrm{d}t}$ initiates a turn-off. To be able to adjust the current and voltage slopes individually for turn-on and turn-off, the amplitude of the reference voltage $v_{\mathrm{ref,d}/\mathrm{d}t}$ and also the feedback gains k_i and k_v may be selected differently for turn-on and turn-off.

As the dynamic feedbacks of $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ only provide information of the system during the current and voltage slopes, the PI-controller is not able to control the IGBT during the turn-on and turn-off delay intervals, cf. Fig 9, what typically results in an overshoot of $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ at turn-on and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ at turn-off. A solution acting prior to a current or voltage slope feedback is presented in the following section.

B. Extension by gate current control

Missing feedback during the delay intervals of the switching transients typically leads to excessive gate current values caus-

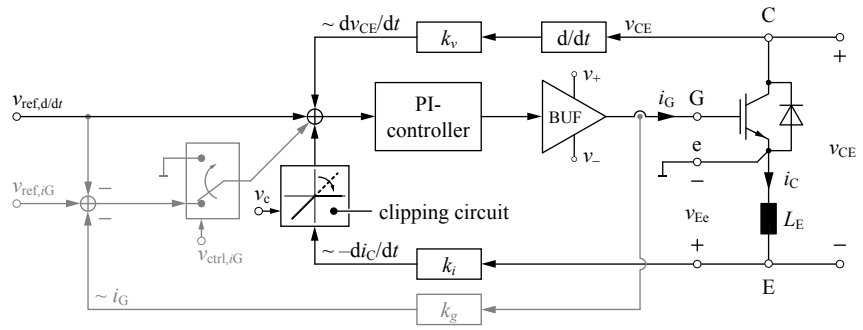

Fig. 10: Block diagram of the proposed combined closed-loop current slope and voltage slope control (dark-colored) extended by an additional gate current control (light-colored) that is used to define the gate current during the turn-on and turn-off delay intervals as described in section III-B.

ing overshoots in $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ at turn-on and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ at turn-off. If the gate current, that mainly defines the current and voltage slopes according to (5) and (6), is actively controlled, the overshoots can be prevented. Such a gate current control can be implemented into the proposed active gate drive concept without changing the current and voltage slope control part as depicted in Fig. 10.

To initiate the switching operation, both control loops are activated simultaneously by setting the individual reference signals $v_{\mathrm{ref,d}/\mathrm{d}t}$, $v_{\mathrm{ref},i\mathrm{G}}$ and the multiplexer via v_c to the desired values. Subsequently, the gate current control must be deactivated by means of toggling the multiplexer not later than the beginning of the current rise at turn-on or the voltage rise at turn-off. This point in time can be assumed to occur with a defined time delay after the initiation of the switching operation, or derived from reaching a predefined gate-emitter voltage level or the point of active current or voltage slope feedback at the latest.

IV. Hardware implementation of the proposed active gate drive

According to Fig. 10, the realization of the proposed active gate drive relies on $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ feedback signals, the determination of the control error, the implementation of the PI-controller and a highly dynamic and powerful gate drive output stage. A schematic of the proposed active gate drive is presented in Fig. 11 and will be discussed in the following subsections.

A. Measurement circuits

The measurement of the current i_C and voltage v_CE time derivative feedback signals features a duality. Feedback proportional to $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ is provided as voltage drop across an inductance in the load current path, e.g. via the emitter's parasitic bonding wire inductance L_E. The current of a capacitor in the voltage path is used as feedback signal proportional to $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$. Neglecting any parasitic inductance in the auxiliary emitter connection and assuming a (+)-input voltage of the operational amplifier being comparably small with regard to v_CE, the two feedback signals can be expressed as

$$v_\mathrm{Ee} \approx -L_\mathrm{E} \cdot \mathrm{d}i_\mathrm{C}/\mathrm{d}t, \tag{10}$$

$$i_{Cv} \approx C_v \cdot \mathrm{d}v_\mathrm{CE}/\mathrm{d}t. \tag{11}$$

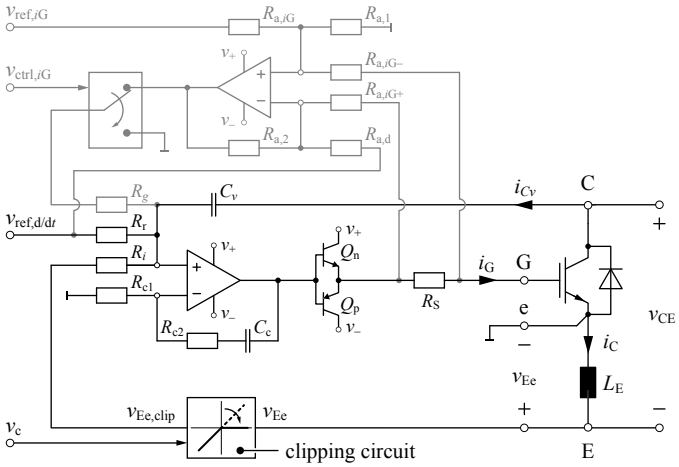

Fig. 11: Schematic of the proposed active gate drive (dark-colored) including extension by gate current control (light-colored) and clipping circuit to block negative $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ feedback at turn-on as explained in section IV-C.

For the generation of the control error, i.e. summing up the reference and feedback signals, a passive network can be employed as depicted in Fig. 11. Due to the capacitor C_v in the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ feedback path, a low-pass characteristic of all remaining signals occurs. This capacitor's value is typically several picofarads and the resistors's values are about few hundred Ohms. For that reason, a low-pass time constant in the low nanosecond range results. If this low-pass characteristic, depending on all resistor and capacitor values of the reference signal generation, would cause a problem, a buffer amplifier could be inserted to decouple the voltage slope feedback.

B. Control amplifier and buffer stage

The PI-controller can be implemented with a fast operational amplifier as shown in Fig. 11, where the P- and the I-part result in accordance with

$$P = 1 + R_\mathrm{c2}/R_\mathrm{c1}, \tag{12}$$

$$I = 1/(R_\mathrm{c1} \cdot C_\mathrm{c}). \tag{13}$$

As output buffer, a push-pull emitter-follower can be used to provide the high analog bandwidth and needed current gain. In doing so, the parallel connection of lower current rated bipolar transistors is beneficial compared to single devices in

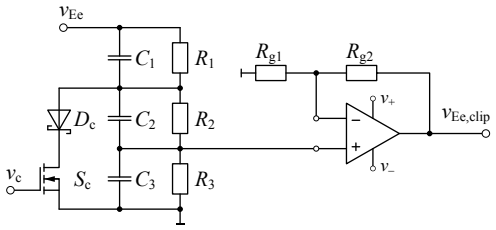

Fig. 12: Schematic of the clipping circuit to restrict negative $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ feedback during turn-on, at which S_c has to be closed permanently.

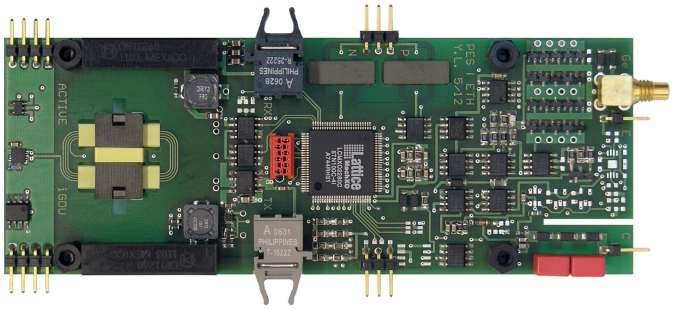

Fig. 13: Developed prototype of the proposed active gate driver; dimensions of the PCB: 50 mm x 133.3 mm and/or 1.97 in x 5.25 in.

terms of current gain (typ. $h_\mathrm{FE} > 100$) and analog bandwidth ($f_\mathrm{T} > 100\,\mathrm{MHz}$).

C. Clipping of negative $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ feedback at turn-on

Ideally, the time intervals with current and voltage slopes of the inductive current switching are not overlapping as illustrated in section III-A enabling the proposed combined $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control. However, at turn-on the collector current i_C is reduced after the diode's peak reverse recovery current i_rr leading to unwanted additional current feedback during the voltage slope. To achieve an optimal control of $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$, this negative feedback of $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ must be prevented or at least strongly limited at turn-on. This can be achieved by means of inserting the proposed clipping circuit shown in Fig. 12 into the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ feedback path. In doing so, the switch S_c must be closed during the entire turn-on transients. This limits the feedback of negative current time derivatives to the forward voltage of diode D_c multiplied by the ratio of the voltage divider ($R_2||C_2$, $R_3||C_3$).

V. Experimental Results

A prototype of the proposed active gate drive was developed, cf. Fig. 13, that contains all described measurement and control circuits. The setting and activation of the needed reference signals is triggered by a CPLD.

Double-pulse tests have been performed to obtain the following experimental measurement results. The test setup consisted of a DC link (up to 1 kV, 320 μF), one Infineon FF450R12KE4 IGBT half-bridge module (1.2 kV, 450 A), an air-core inductor (53 μH) and a busbar interconnecting all components.

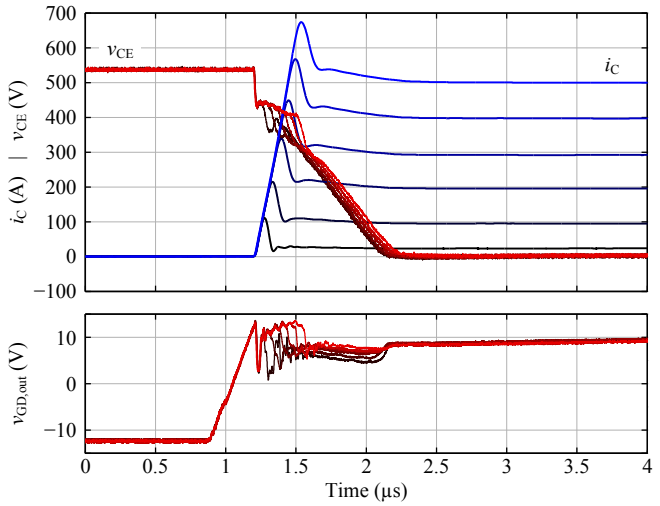

Fig. 14: Measured turn-on waveforms of i_C, v_CE and gate driver output voltage $v_\mathrm{GD,out}$ (high-side) for different load currents i_o at $\mathrm{d}i_\mathrm{C}/\mathrm{d}t = 2\,\mathrm{kA}/\mu\mathrm{s}$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t = 0.5\,\mathrm{kV}/\mu\mathrm{s}$.

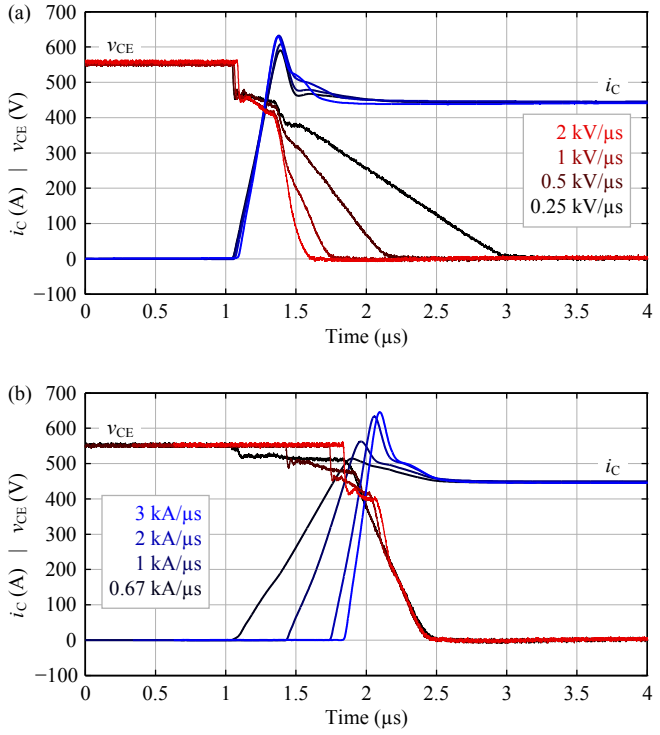

Fig. 15: Measured turn-on waveforms of i_C and v_CE (high-side) for (a) varied voltage slopes at $\mathrm{d}i_\mathrm{C}/\mathrm{d}t = 2\,\mathrm{kA}/\mu\mathrm{s}$ and (b) varied current slopes at $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t = 1\,\mathrm{kV}/\mu\mathrm{s}$.

A. Turn-on transients

To verify the proposed natural transition from current to voltage slope control, the turn-on waveforms of the IGBT have been measured for a variation of the load current i_o as depicted in Fig. 14. There, the active gate drive controls its output voltage $v_\mathrm{GD,out}$ as expected to first achieve the desired $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ until the point of peak reverse recovery current and then to attain the requested value for of $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$.

Individual control of the current and voltage slopes has

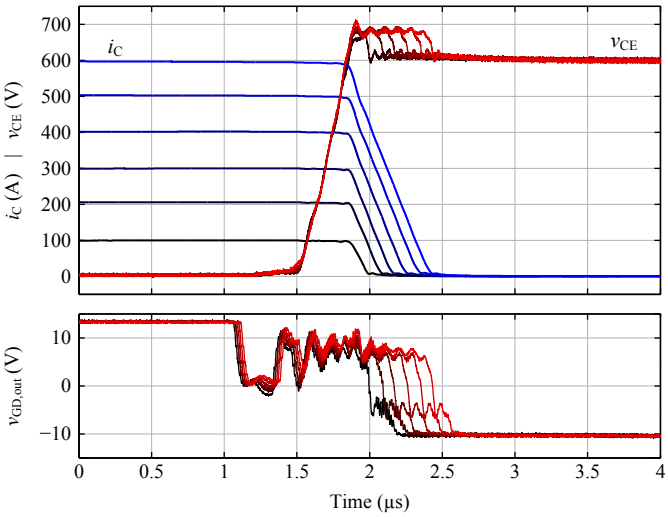

Fig. 16: Measured turn-off waveforms of i_C, v_{CE} and gate driver output voltage $v_{GD,out}$ (high-side) for different load currents i_o at $\mathrm{d}i_C/\mathrm{d}t = 1\,\mathrm{kA}/\mu\mathrm{s}$ and $\mathrm{d}v_{CE}/\mathrm{d}t = 2\,\mathrm{kV}/\mu\mathrm{s}$.

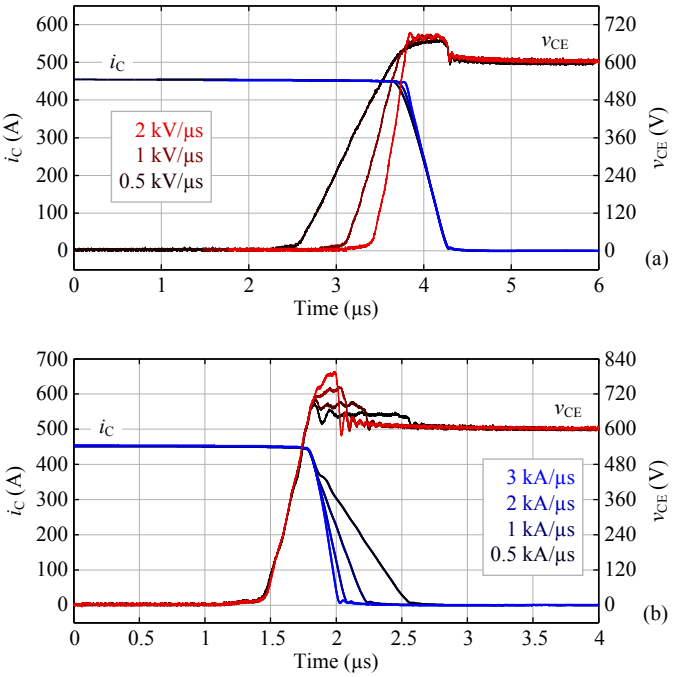

Fig. 17: Measured turn-off waveforms of i_C and v_{CE} (high-side) for (a) varied voltage slopes at $\mathrm{d}i_C/\mathrm{d}t = 1\,\mathrm{kA}/\mu\mathrm{s}$ and (b) varied current slopes at $\mathrm{d}v_{CE}/\mathrm{d}t = 2\,\mathrm{kV}/\mu\mathrm{s}$.

also been verified experimentally. On the one hand, at a constant reference of $\mathrm{d}i_C/\mathrm{d}t_{ref} = 2\,\mathrm{kA}/\mu\mathrm{s}$, the measurements for $\mathrm{d}v_{CE}/\mathrm{d}t_{ref} = 0.25\,\mathrm{kV}/\mu\mathrm{s} \ldots 2\,\mathrm{kV}/\mu\mathrm{s}$ are shown in Fig. 15 (a). On the other hand, the waveforms for $\mathrm{d}i_C/\mathrm{d}t_{ref} = 0.67\,\mathrm{kA}/\mu\mathrm{s} \ldots 3\,\mathrm{kA}/\mu\mathrm{s}$ at constant $\mathrm{d}v_{CE}/\mathrm{d}t_{ref} = 1\,\mathrm{kV}/\mu\mathrm{s}$ are shown in Fig. 15 (b). In both cases, the current and voltage waveforms are accurately controlled to their reference values, i.e. it is possible at turn-on to individually control the current and voltage slopes to their set-point values.

B. Turn-off transients

Similar as for the turn-on case, first, the waveforms for a variation of the load current at turn-off are presented in Fig. 16. To achieve the same voltage slope for all values of the load current, the active gate drive increases its output voltage $v_{GD,out}$ according to the increase in the load current, to compensate the dependency of v_{GE,i_o} on the load current as described in section I-B. Due to the fact that $\mathrm{d}i_C/\mathrm{d}t$ is controlled to a constant value, the magnitude of the overvoltage doesn't change with the load current amplitude.

Individual control of the current and voltage slopes has also been verified experimentally for the turn-off case. On the one hand, at a constant reference of $\mathrm{d}i_C/\mathrm{d}t_{ref} = 1\,\mathrm{kA}/\mu\mathrm{s}$, the measurements for $\mathrm{d}v_{CE}/\mathrm{d}t_{ref} = 0.5\,\mathrm{kV}/\mu\mathrm{s} \ldots 2\,\mathrm{kV}/\mu\mathrm{s}$ are shown in Fig. 17 (a). On the other hand, the waveforms for $\mathrm{d}i_C/\mathrm{d}t_{ref} = 0.5\,\mathrm{kA}/\mu\mathrm{s} \ldots 3\,\mathrm{kA}/\mu\mathrm{s}$ at constant $\mathrm{d}v_{CE}/\mathrm{d}t_{ref} = 2\,\mathrm{kV}/\mu\mathrm{s}$ are shown in Fig. 17 (b). In both cases, again the current and voltage waveforms are largely controlled to their reference values, i.e. it is possible at turn-off to individually control the current and voltage slopes to their set-point values. Therewith, the gate drive is able to compensate for the mentioned intrinsic switching characteristic of the IGBT as discussed in section I-C.

VI. Conclusion

In this paper, an active IGBT gate drive providing independent $\mathrm{d}i_C/\mathrm{d}t$ and $\mathrm{d}v_{CE}/\mathrm{d}t$ control with a single PI-controller has been proposed. It permits to adjust the current and voltage slopes according to their set-point values by compensating the nonlinearities and eliminating parameter dependencies of the IGBT with the closed-loop approach. As has been verified experimentally, this enables an IGBT operation within the SOA and a restriction of EMI while minimizing the switching losses within the entire operating range.

By means of using only simple passive measurements for the generation of the feedback signals and a single operational amplifier as PI-controller, high analog control bandwidth is achieved enabling the application of a closed-loop gate drive even for switching times in the sub-microsecond range.

A natural transition from the $\mathrm{d}i_C/\mathrm{d}t$ to the $\mathrm{d}v_{CE}/\mathrm{d}t$ control loop and vice versa takes place for inductive current switching, i.e. no active switchover of the control loops is required.

Constant reference signals that are set prior to the switching transients allow to avoid the elaborate generation of any collector current and / or collector-emitter voltage profiles. An additional gate current control prevents an overshoot in the collector current slope at turn-on and an overshoot in the collector-emitter voltage slope at turn-off which otherwise would result due to the turn-on and turn-off delays.

In the course of further research the proposed active gate drive will be tested with different IGBT modules of various manufacturers and stability considerations will be made on the basis of a control oriented IGBT model. Short circuit switching and active voltage clamping will also be a part of further work.

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