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***Abstract*—In the public low voltage mains the stress caused by harmonic currents is strongly increased due to the higher demand of electronic equipment in everyday use. Therefore, standards were created in order to limit the harmonic currents injected into the network, thus maintaining a high voltage quality of these networks. Hence, converter systems with active PFC are indispensable, where in general the compliance of the created directives for lower harmonics can be easily fulfilled. Typically, in single-phase systems, boost PFC converter topologies are used, which offer a wide input voltage range and a controlled output voltage. Depending on the underlying applications, a subsequent reduction and/or isolation of the output voltage based on a DC/DC-converter is needed. The major disadvantages of this converter cascading are the reduction of the overall efficiency, the large component count and the increasing control complexity. In comparison to the conventional two-stage PFC converter system, the true bridgeless Cuk PFC rectifier system can perform the PFC functionality and the galvanic isolation in a single-stage, thus eliminating the mentioned disadvantages. In this paper a comprehensive analysis of the operation, design and limits of the recently proposed single-stage Cuk concept is investigated. In addition, a comparative evaluation concerning efficiency and power density against a conventional two-stage approach based on bridgeless PFC rectifier and a subsequent LLC-resonant DC/DC-converter is presented.**

I. Introduction

Due to the higher demand of electronic equipment in everyday use, like PC's and consumer electronics, the stress caused by harmonic currents in public low voltage mains is strongly increased. Especially for uninterrupted services - e.g. servers and telecom applications - the generated losses due to the harmonic currents could be considerable. In addition, single-phase (1-Φ) systems connected to the three-phase mains, can lead to an overload in the neutral conductor due to the superposition of odd harmonic currents with ordinal numbers dividable by three.

Therefore, to maintain a high voltage quality of these networks, standards were created in order to limit the harmonic currents which are injected into the network [1]. For example, for all systems connected to the public mains which have a power rating higher than 75 W and a maximum phase current of 16 A, the permissible content of harmonics is defined in the directive IEC/EN 61000-3-2.

Typically, with passive input filters, which are simple, robust and cost-effective, the harmonic content in the line current can be reduced. However, for the suppression of low frequencies the employed inductors are usually large and heavy. In addition, the inserted series-inductance leads to a voltage drop, thus is not applicable for higher power ratings and for a wide input voltage range. Furthermore, the input current is not sinusoidal, thus the system also has to be designed for higher rms-currents.

However, in industry a trend towards green energy emerged, which is becoming a more and more important sales argument besides costs. Labels like "Energy Star" gained considerable attention in recent years, where e.g. in addition to the harmonics content limitation also a minimum power factor ($\lambda > 0.9$) and a minimum efficiency are demand. Therefore, high efficiency converter systems with active PFC are becoming indispensable, where in general the compliance of the mentioned directives for lower harmonics can be easily ensured. On the other hand, standards concerning conducted EMI for higher order harmonics ($> 150\,\mathrm{kHz}$) are getting crucial, which typically limit the switching frequency of active PFC rectifier systems below $150\,\mathrm{kHz}$, in order to keep the input filter effort as low as possible.

In the literature [5]–[9] different topologies featuring active PFC are proposed, where the wide-range input voltage (cf. **Table I**) is stepped up to around 400 V. The most common and simplest solution for single-phase applications is the conventional boost PFC rectifier. However, this topology suffers from high conduction losses caused in the input diode full-bridge rectifier especially for low input voltages. Therefore, in industry the bridgeless PFC rectifier is gaining more and more acceptance, since the system efficiency can be improved with the drawback of higher component effort.

TABLE I: Given specifications for the comparative evaluation of the two PFC converter systems.

Input voltage range $V_{\mathrm{in,rms}}$	$90\,\mathrm{V} - 270\,\mathrm{V}$
Output voltage V_{out}	$12\,\mathrm{V}$
Output power P_{out}	$100\,\mathrm{W}$
Output voltage ripple ΔV_{out}	$1\,\%$

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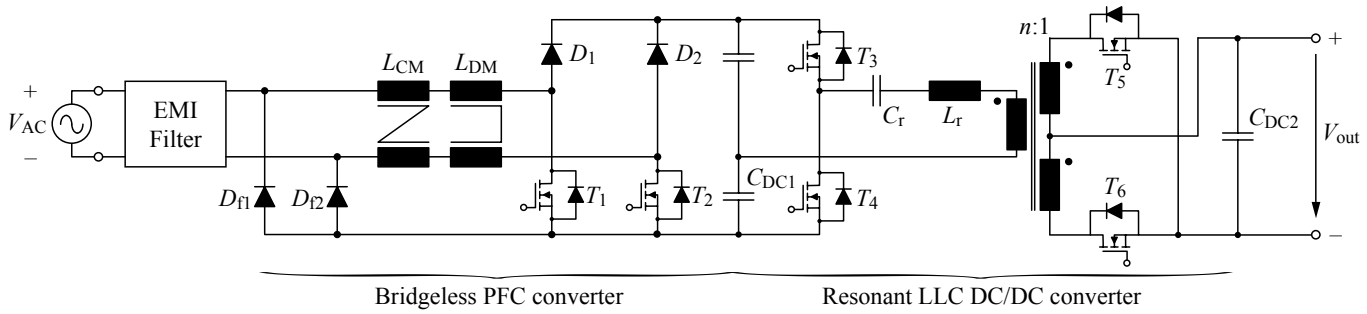

Fig. 1: Today's widely used conventional single-phase AC/DC-converter system consisting of a front-end PFC boost rectifier stage and a subsequent isolated DC/DC-converter.

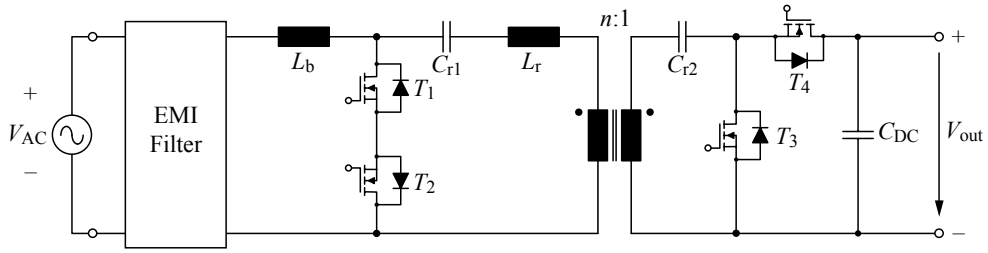

Fig. 2: Isolated True Bridgeless Cuk Single-Phase PFC Rectifier System proposed in [2], where PFC functionality and isolation can be achieved with a single stage.

Depending on the underlying applications a subsequent reduction and/or isolation of the output voltage based on a DC/DC-converter is needed, where especially for low voltages (e.g. 12 V output, cf. **Table I**) an isolation is required due to the high conversion ratio (cf. **Fig. 1**). The major disadvantages of this converter cascading are the reduction of the overall efficiency, the large component count and the increasing control complexity.

In [2] a new isolated 1-Φ single-stage PFC AC/DC converter topology was proposed (cf. **Fig. 2**), where PFC functionality and isolation can be implemented with a single stage ("true bridgeless PFC") and thus an outstanding efficiency of 98 % is achieved. This clearly gives the motivation for this paper to analyze the proposed concept in more detail in order to clarify the operation and design, identify the limits of the concept, and to provide a comparative evaluation against a conventional two-stage approach (cf. **Fig. 1**) in terms of efficiency and power density.

In Section II the basic operation of single-stage converter is explained. Based on this analysis and the given specifications of **Table I**, in Section III the design of the converter is performed. In Section IV, suitable converter topologies are selected for the conventional two-stage system, whose performance is finally compared with the proposed true bridgeless Cuk PFC rectifier system.

II. Operation Principle of the True Bridgeless Cuk PFC Rectifier

The operation principle of the true bridgeless Cuk PFC rectifier system is explained separately for positive and negative DC-voltages, where first the galvanic isolation is omitted (cf. **Fig. 3 a)**). In addition, the switches T_3 and T_4, used as synchronous rectifiers, in order to reduce the conduction losses, are substituted with the diodes D_1 and D_2. Thus, the single stage PFC rectifier shows the same circuit structure like the conventional boost converter, however, with an additional resonant circuit consisting of C_{r1}, L_r and D_1.

Assuming a positive input voltage V_{in} and a turn-on state of switch T_1, V_{in} is applied to the boost inductor L_b resulting in a linearly increasing input current $i_{Lb,Ton}$ as shown in **Fig. 3 b)**. In addition, if the resonant capacitor C_{r1} is charged to a positive voltage $\hat{V}_{Cr1}$, a sinusoidal resonant current $i_{r,Ton}$ through D_1 and L_r is initiated (cf. **Fig. 3 b)**). Due to the diode D_1 the oscillation will be stopped as soon as the resonant current $i_{r,Ton}$ returns to zero and, with a lossless resonant circuit, the capacitor is discharged to $-\hat{V}_{Cr1}$. Actually, the oscillation period defines the on-time T_{on} of the switch T_1, which is set to half of a resonant period, resulting in highest efficiency and best performance of the single-stage PFC converter as described in [2]. Thus, the output voltage is controlled with a variable turn-off time T_{off}, hence switch T_1 is operated with a variable switching frequency.

At $t = T_r/2$, the switch T_1 is turned-off and the input current i_{Lb} has to commutate from T_1 to the resonant circuit.

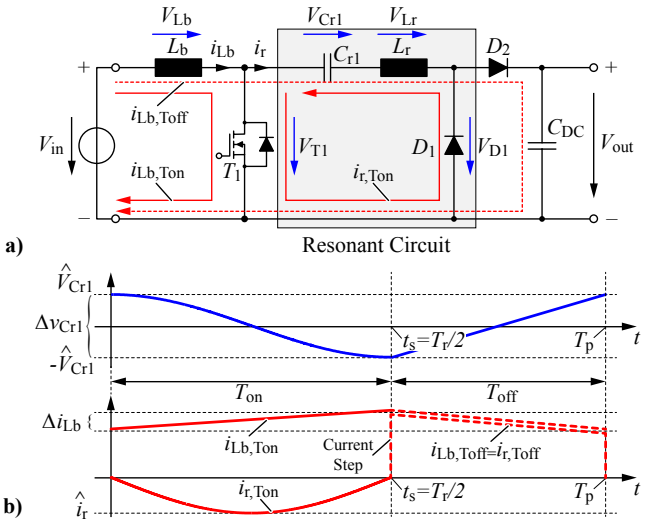

Fig. 3: a) Simplified schematic of the single-stage PFC converter proposed by [2] without galvanic isolation showing the current paths during T_{on} and T_{off}, **b)** current and voltage waveforms in the resonant circuit (V_{Cr1} and i_{Lr}) and in the input inductor (i_{Lb}) for positive input voltage V_{in}.

Since at this time instant $i_{\text{r,Ton}}$ is zero, during the switching operation the current i_{r} has to be quickly increased to the same value as i_{Lb}, which results in a high over-voltage across T_1. As described in [2], with a snubber circuit based on Zener diodes (cf. **Fig. 5 b)**) the over-voltage can be limited to a defined value which is only slightly increasing the overall converter losses since the resonant inductor value L_r is small. However, as will be shown in this paper, the value of the resonant inductor L_{r} is limited to a minimum value. In addition, the generated snubber losses also depend on the output voltage V_{out} and the clamping voltage V_{ZD} of the Zener diode snubber.

After the commutation ($i_{\text{r}} = i_{\text{Lb}}$), the current is flowing from the input through the diode D_2 to the output as long as T_1 is kept off. Thus, with a large boost inductance L_{b}, the resonant capacitor C_{r1} is quasi linearly charged to its initial value $\hat{V}_{\text{Cr1}}$.

For negative input voltages, with a switch T_1 that also features a negative voltage blocking capability, the same functionality can be achieved. A bidirectional switch with positive and negative blocking capability can be realized e.g. with two MOSFETs connected in anti-series with common source and gate connection. Of course, with this configuration the conduction losses are doubled, however the switching performance is not influenced.

The corresponding current paths for negative input voltages are shown in **Fig. 4 a)**. During the on-state interval T_{on} the resonant current is now flowing in the other direction through D_2 and the output capacitor C_{DC}. Since in general C_{DC} is much larger than C_{r1}, the resonant frequency is not changed. The current path of i_{Lb} is also changed for T_{off}, which is now flowing through D_1, thus no current is flowing directly from the input to the output (cf. **Fig. 4 b)**).

The voltage transfer ratio of the single-stage PFC converter for steady state can be deduced from the average voltages applied to the different components. Based on the fact that in steady state the net voltage-time product across L_{b} and L_{r} over one switching period is equal to zero, i.e. $\overline{V}_{\text{Lb}} = \overline{V}_{\text{Lr}} = 0\,\text{V}$, the average switch voltage $\overline{V}_{\text{T1}}$ has to be equal to the input voltage V_{in}.

For positive voltages, during T_{on} the switch voltage V_{T1} is zero and, based on Kirchhoff's voltage law, during T_{off} it is $V_{\text{Cr1}} + V_{\text{D1}}$, since $\overline{V}_{\text{Lr}} = 0\,\text{V}$. Accordingly, during T_{on} the diode D_1 conducts the resonant current, thus $V_{\text{D1}} = 0\,\text{V}$, and during T_{off} it blocks the output voltage V_{out}. This leads to

$$\overline{V}_{\text{T1}} = V_{\text{in}} = (V_{\text{out}} + V_{\text{Cr1}}) \cdot (1 - D) T_{\text{s}}. \tag{1}$$

For L_{r}, the net voltage-time product is also zero after the on-state interval T_{on} ($i_{\text{r}}(0) = i_{\text{r}}(T_{\text{on}}) = 0\,\text{A}$). Therefore, since during the on-state interval T_{on} only the voltage V_{Cr1} is applied to the inductor L_{r}, the average voltage $\overline{V}_{\text{Cr1}}$ has to be zero and the same duty-cycle as for the conventional boost converter is found,

$$D = 1 - \frac{V_{\text{in}}}{V_{\text{out}}}. \tag{2}$$

As shown in [2], for negative input voltages the same voltage transfer ratio is achieved. Due to the asymmetric circuit behavior, however, the average voltage of the resonant capacitor $\overline{V}_{\text{Cr1}}$ is changing from $0\,\text{V}$ to $-V_{\text{out}}$. For negative input voltages, during the on-state interval T_{on}, the resonant current is additionally flowing through the output capacitor C_{DC} and thus, the voltage applied to the inductor L_{r} is $V_{\text{Cr1}} + V_{\text{out}}$. However, since the net voltage-time product applied to L_{r} also has to disappear after T_{on}, the average resonant capacitor voltage $\overline{V}_{\text{Cr1}}$ has to be equal to $-V_{\text{out}}$. Otherwise, during T_{on} the diode D_2 would be reverse biased and the resonant current couldn't flow through C_{DC} (cf. **Fig. 4 a)**).

Since the average voltage $\overline{V}_{\text{Cr1}}$ for positive and negative input voltages is different, for an AC-input voltage the resonant capacitor C_{r1} has to be charged and discharged after each zero voltage transition of the input voltage. According to **Fig. 5 a)**, during the transition from positive to negative input voltage this leads to a discontinuous power transfer to the output. This is due to the fact that the resonant capacitor C_{r1} first has to be charged to the output voltage level $-V_{\text{out}}$ before any current can flow to the output. Thus, during this interval no resonant current is flowing. On the other hand, during the transition from negative to positive input voltage, the resonant capacitor C_{r1} has to be discharged, which is only possible through the output diode D_2 and the output capacitor C_{DC}, since the diode D_1 is reverse biased until the resonant capacitor C_{r1} is discharged. In summary, during the charging interval (transition from positive to negative input voltage), the energy drawn from the mains is stored in the resonant capacitor C_{r1} - resulting in discontinuous output power transfer - and during the discharging interval (transition from negative to positive

input voltage) this energy is released to the output again (cf. **Fig. 5 a**)).

It has to be mentioned, however, that outside these dis-/charging intervals the waveform of the resonant current, i.e. the shape and the peak value, is not changed. In order to limit the time needed to charge and discharge C_{r1} - during this time the steady state duty cycle found in (2) is no more valid - a reasonable small resonant capacitance C_{r1} has to be selected. Consequently, for a certain resonant frequency a larger resonant inductor L_r has to be designed, resulting in higher over-voltages during the switching transient.

According to **Fig. 2**, a transformer can be introduced without changing the system behavior, which enables the generation of isolated output voltages with arbitrary voltage levels. In this case, to prevent the transformer from saturation, the resulting average voltage on the transformer's primary side has to be blocked by the resonant capacitor C_{r1}. This voltage is equal to the input voltage ($\overline{V}_{Cr1} = V_{in}$) based on the fact that in steady state for any inductor or transformer the net voltage-time product during one switching cycle has to be zero. For the same reason an additional resonant capacitor C_{r2} has to be inserted on the transformer's secondary side.

In order to not change the resonant frequency of the rectifier system, the values of both resonant capacitors have to be adapted in such a way that the series connection of C_{r1} and C_{r2} (the transformer's turns ratio has to be considered) for the isolated rectifier is equal to the resonant capacitor C_{r1} of the non-isolated rectifier. In addition, also the total average voltage across the resonant capacitors C_{r1} and C_{r2} for the isolated rectifier has to be equal to the average voltage across the resonant capacitor C_{r1} of the non-isolated rectifier. Thus, the average voltage of the resonant capacitor $\overline{V}_{Cr2}$ can be easily deduced, which is $-V_{in}$ for positive and $-V_{out}+V_{in}$ for negative input voltages, assuming a transformer's turns ratio of one.

In addition, to keep the component count as low as possible, the resonant inductance L_r for the isolated true bridgeless Cuk PFC rectifier system can be magnetically integrated into the transformer, which means that L_r is realized by the transformer's leakage inductance. As already mentioned, in order to reduce the conduction losses of the output rectifiers, the diodes D_1 and D_2 can be substituted by MOSFETs, used as synchronous rectifiers, which especially will lead to a higher converter efficiency for low output voltages (cf. **Fig. 2**). As can be noticed, based on the currents paths shown for positive and negative input voltages, the synchronous rectifiers T_3 and T_4 can be controlled with the same gate signal as T_1 and T_2. Depending on the input voltage's sign, however, either the gate signal for T_3 or T_4 has to be inverted.

III. Detailed Analysis and Design

The range of the switching frequency, which occurs during one quarter of the mains period, is mainly defined by the selected resonant frequency f_r (i.e. defined by L_r and C_{r1}), since the on-time T_{on} is equal to half of the resonant period. Based on (2), for low input voltages the highest duty cycles

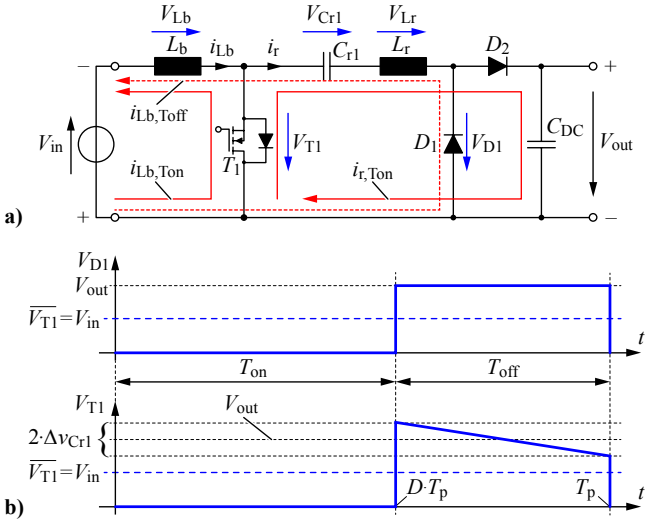

Fig. 4: a) Resulting current paths during T_{on} and T_{off} for negative input voltage V_{in} and **b)** applied voltage to the switch V_{T1} and the diode V_{D1} in order to calculate the voltage transfer ratio of the converter.

- in practice usually limited slightly below one (~ 0.95) - are achieved. Thus, the highest resulting switching frequency equals $f_{s,max} \approx 1/T_{on}$. The voltage dependent switching frequency is given as follows

$$T_{on} = \frac{1}{2 \cdot f_r} \tag{3}$$

$$f_s(t) = \frac{D(t)}{T_{on}} = 2 \cdot f_r \cdot (1 - \frac{v_{in}(t)}{V_{out}}). \tag{4}$$

In order to keep the input filter effort as low as possible, typically the switching frequency $f_{s,max}$ is selected below 150 kHz, which is the starting frequency of the CISPR directive. Therefore, the resonant frequency f_r is limited to 75 kHz, which is a reasonable choice as will be shown in the following. In addition, the switching frequency should be kept above the audible frequency range, thus the minimum switching frequency $f_{s,min}$ is around 20 kHz. For a given (non-isolated) output voltage V_{out} - for the isolated converter it is the secondary voltage transformed to the primary - the lowest switching frequency is obtained at the peak of the input voltage, which is defined by the local mains voltage level. Consequently, in order to ensure that the switching frequency doesn't fall below the defined minimum switching frequency, the output voltage V_{out} has to be higher than a certain minimum voltage level (cf. (2)).

For the given specifications in **Table I**, the lowest duty cycle occurs at $V_{in} = 270\,V_{rms}$, thus with a selected resonant frequency of $f_r = 75$ kHz a minimum output voltage (transformed to the primary) of $V_{out} = 440$ V is obtained. Based on (2), for lower resonant frequencies f_r the output voltage would even increase and larger resonant components would be needed. In this case, switches with higher voltage blocking capability would have to be employed, which typically show

a worse switching behavior and higher on-state resistances. In addition, also the passive components would have to be designed for a higher isolation strength.

On the other hand, with higher resonant frequencies and thus lower output voltages, the amplitude of the resonant current $\hat{i}_\mathrm{r}$ is drastically increased, which for the non-isolated system can be easily deduced from the voltage ripple Δv_{Cr1} across the resonant capacitor C_{r1}. As shown in **Fig. 3 b)**, during the off-state interval T_{off} - assuming a constant input current i_{Lb} during T_{off} - the resonant capacitor C_{r1} is linearly charged from its minimum to its maximum voltage. Thus, the highest voltage ripple $\Delta\hat{v}_{\mathrm{Cr1}}$ across the C_{r1} is achieved with the highest input current $\hat{i}_{\mathrm{Lb}}$, which can be expressed by the output power P_{out} and the peak input voltage $\hat{V}_{\mathrm{in}}$, given by

$$\Delta\hat{v}_{\mathrm{Cr1}} = \frac{\pi \cdot P_{\mathrm{out}}}{(V_{\mathrm{out}} - \hat{V}_{\mathrm{in}})} \cdot \sqrt{\frac{L_\mathrm{r}}{C_{\mathrm{r1}}}}. \tag{5}$$

Based on the characteristic impedance Z_r of the resonant circuit, the resonant current $\hat{i}_\mathrm{r}$ can be calculated as

$$\hat{i}_\mathrm{r} = \frac{\Delta\hat{v}_{\mathrm{Cr1}}}{Z_\mathrm{r}} = \Delta\hat{v}_{\mathrm{Cr1}} \cdot \sqrt{\frac{C_{\mathrm{r1}}}{L_\mathrm{r}}} = \frac{\pi \cdot P_{\mathrm{out}}}{(V_{\mathrm{out}} - \hat{V}_{\mathrm{in}})}. \tag{6}$$

As can be noticed, for a given output power P_{out} the peak current value $\hat{i}_\mathrm{r}$ only depends on the voltage difference between the output voltage V_{out} and the peak input voltage $\hat{V}_{\mathrm{in}}$. For smaller voltage differences, i.e. higher input voltages or lower output voltages, the current ripple strongly increases. Therefore, even if the resonant frequency would be increased above 75 kHz (neglecting any EMI distortions), which would result in lower minimum output voltage. A further output voltage reduction is not reasonable, since the high resonant current would lead to higher conduction losses and to higher current stresses in almost all circuit components.

For the sake of completeness, it has to be mentioned that the resonant frequency could also be increased above 75 kHz without decreasing the output voltage. In this case, the resonant component values could be further decreased (since $\omega_\mathrm{r} = 1/\sqrt{L_\mathrm{r}C_{\mathrm{r1}}}$) and the resonant current could be still kept at a reasonable level. However, the EMI-noise emissions and thus the input filter effort would strongly increase.

With the given resonant frequency the resonant elements C_{r1} and L_r can be dimensioned. Since the L_r and C_{r1} don't influence the resonant current amplitude (cf. (6)), the ratio of L_r and C_{r1} has to be selected properly, in order to achieve an optimal system behavior where the stresses in the components and the overall system losses can be kept low.

As was already explained for the operation with an AC-input voltage, the resonant capacitance C_{r1} is either charged or discharged during each zero voltage transition of the input voltage. Consequently, during these charging and discharging intervals the steady state duty cycle based on (2) is no more valid - the duty cycle D has to be modified, resulting in a more complex control scheme, in order to keep the input current sinusoidal - since in these intervals no resonant current is flowing (both rectifier diodes are blocking). Thus, the resonant

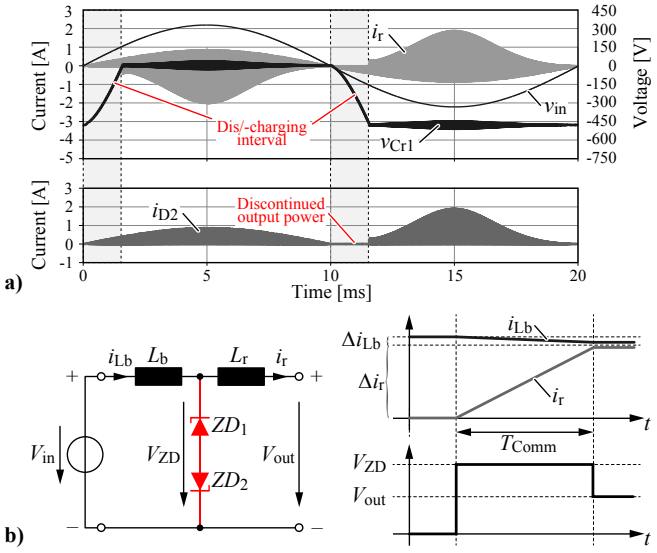

Fig. 5: a) Simulated waveforms of the resonant capacitor voltage V_{Cr1} showing the charging and discharging interval and the currents i_r and i_{D2} illustrating the discontinuous power flow to the output and **b)** simplified circuit diagram and corresponding currents and voltages during the commutation interval T_{comm} to calculate the snubber losses.

capacitor is only charged and discharged during the off-state interval T_{off}. In addition, due to the PFC functionality of the converter, after the zero crossing of the mains voltage the input current is small, thus the charging/discharging time can be considerably high. Therefore, in order to not significantly change the rectifier's behavior, the charging and discharging intervals have to be kept short (cf. **Fig. 5 a)**), which means that the resonant capacitor is limited to a certain maximum value.

However, decreasing the resonant capacitance C_{r1} or the charging time respectively, leads to a higher voltage ripple Δv_{Cr1}, which causes higher voltage stress at the main switch T_1 (cf. (1)), but also at the resonant capacitor itself. In practice, the maximum allowed voltage ripple depends on the selected capacitor type and is limited e.g. by the losses caused in the dielectric material or the expected capacitor's lifetime. Consequently, also a lower limit is encountered for the resonant capacitance, which is defined by the maximum allowed voltage ripple $\Delta\hat{v}_{\mathrm{Cr1}}$ of the selected capacitor type. However, it has to be mentioned that larger voltage ripples can be tolerated if multiple capacitors are connected in series. For the isolated true bridgeless Cuk PFC rectifier, for example, the voltage ripple v_{Cr1} is shared by the two resonant capacitors C_{r1} and C_{r2}.

Nevertheless, for the design of the rectifier a small voltage ripple resulting in a reasonable charging and discharging time is pursued in this paper. On the one hand, with a small voltage ripple or a large resonant capacitance respectively, the EMI-behavior of the converter might be improved and the voltage stress at the main switch can be reduced.

On the other hand, a low resonant capacitance would

result in a large resonant inductance L_r, in order to keep the resonance frequency constant. The resonant inductance L_r, however, strongly influences the resulting semiconductor losses and over-voltage at the switch T_1. Thus, for lower losses and lower over-voltages a small resonant inductance is desirable.

As already mentioned, the over-voltage during the turn-off transient can be limited e.g. with a Zener diode based snubber circuit (cf. **Fig. 5 b)**), thus the maximum blocking voltage capability of the main switch $V_{\mathrm{T1,max}}$ is defined by the Zener diode voltage V_ZD. The resulting snubber losses depend on the selected snubber voltage V_ZD and the selected output voltage V_out. This voltage in combination with V_ZD, defines the current slope or the duration of the commutation process T_comm respectively. The resulting losses are calculated based on the linear model shown in **Fig. 5 b)**. During the commutation interval T_comm, a constant input, output and Zener diode voltage are assumed, which results in a linear slope of the input current i_Lb and the resonant current i_r

$$\Delta i_\mathrm{Lb} + \Delta i_\mathrm{r} = I_{Lb} \tag{7}$$

$$\Delta i_\mathrm{Lb} = \frac{T_\mathrm{Comm}}{L_\mathrm{b}} \cdot (V_\mathrm{ZD} - V_\mathrm{in}) \tag{8}$$

$$\Delta i_\mathrm{r} = \frac{T_\mathrm{Comm}}{L_\mathrm{b}} \cdot (V_\mathrm{ZD} - V_\mathrm{out}). \tag{9}$$

Thus, the losses in the snubber circuit can be calculated for different input current ratings $i_\mathrm{Lb}(t)$, inductance values L_b and L_r1 and Zener diode voltages V_ZD as

$$P_\mathrm{ZD} = U_\mathrm{ZD} \cdot \int_0^{T_\mathrm{Comm}} (i_\mathrm{Lb}(t) - i_\mathrm{r}(t))dt. \tag{10}$$

Typically, the losses in the snubber circuit are reduced if a high Zener breakdown voltage and a low output voltage are selected. However, with a high Zener voltage V_ZD, semiconductors with higher voltage ratings, worse switching behavior and higher on-state resistance are needed. In addition, the low output voltage leads to higher amplitudes of the resonant current and higher conduction losses. Consequently, a multi-dimensional optimization has to be performed, where also the gate, conduction and switching losses of the semiconductors as well as the losses and volumes of the passive components and input filter have to be considered.

IV. Two-Stage PFC Converter System

In order to quantify the achievable performance of the single-stage converter, i.e. power density and efficiency, the converter is compared with a commonly used two-stage approach consisting of a boost PFC rectifier and an isolated DC/DC-converter.

Among other topologies, for the AC-DC input stage a conventional boost PFC converter with input diode rectifier or a bridgeless PFC boost converter [5]–[9] could be employed (cf. **Fig. 6**). The conventional boost PFC converter offers a compact, simple and cheap solution, thus is widely used in industry. However, it suffers from high conduction losses - especially for low input voltages - caused in the input diode rectifier.

The bridgeless PFC converter, on the other hand, shows an increasd efficiency since the input rectifier is partly removed. Compared to the conventional PFC converter, where the current has to flow through three semiconductor devices, this number is reduce to two with the bridgeless PFC converter . The major disadvantage of the bridgeless PFC rectifier is the higher component effort, where two boost inductors, switches and SiC diodes are needed (cf. **Fig. 6 b)**). In addition, to significantly reduce the conducted CM-noise emissions, two feedback diodes D_f1 and D_f2 are needed. Depending on the input voltage's sign, one of these feedback diodes clamps the negative output rail to one connection of the input voltage. As can be noticed, this bridgeless topology consists of two conventional boost converters which are alternately operated, (L_b1, D_1, T_1, D_f2) for positive and (L_b2, D_2, T_2, D_f1) for negative input voltages. Depending on the switching state of the inactive switch, i.e. permanently on or off, the return current only flows through one of the feedback diodes (inactive switch is permanently off) or partially flows through the MOSFET and the corresponding boost inductance (inactive switch is permanently on). As can be noticed, a drawback of this topology is the poor utilization of the semiconductors and the magnetic components; each component is only used during one half of the mains period. Thus, despite of the high efficiency, a lower power density is achieved.

Therefore, as presented in the literature [7], [8], the overall rectifier volume and losses can be decreased, if the two boost inductances are magnetically coupled, by which an improved utilization of the magnetic component can be achieved (cf. **Fig. 1**). Due to the mutual coupling and the induced voltages, the coupled boost inductance has to be realized with a series connection of a differential mode (DM) inductance and a common mode (CM) inductance. Typically two cores are used, but both inductances can also be realized with just one core and two windings [8]. There, depending on the dimensioning of the CM-inductance, the current can be forced to fully return through the inactive switch, which advantageously is turned-on in order to reduce the conduction losses in the body diode, or the current is forced to only return through the corresponding feedback diode.

In the first case, the CM-inductance has to be much larger than the DM-inductance [8], thus the input diode is only clamping the negative output rail to the input voltage, and almost no current is flowing through the feedback diode. Thus, the feedback diode can also be substituted by a feedback capacitor [5]. In the other case, where the CM- and DM-inductances are equal [7], the diode is conducting the full input current, which is due to the worse forward characteristic of diodes compared to MOSFETs and can lead to higher losses, especially at high output power ratings. However, for the underlying specifications with relatively low power ratings (cf. **Table I**) the bridgeless PFC rectifier based on the later

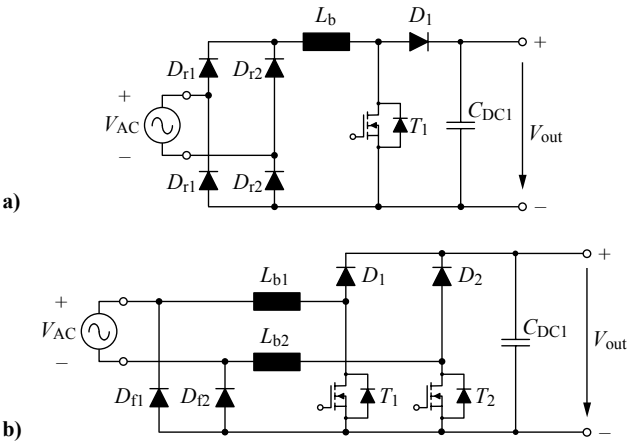

Fig. 6: Circuit diagram of the **a)** conventional boost PFC converter with input diode rectifier and **b)** bridgeless PFC boost converter consisting of two conventional boost converters which are alternately operated, (L_{b1}, D_1, T_1, D_{f2}) for positive and (L_{b2}, D_2, T_2, D_{f1}) for negative input voltages.

concept is pursued for the AC-DC stage of the two-stage converter (cf. **Fig. 1**). With the improved utilization of the magnetic components, the bridgeless converter is only slightly bigger than the conventional PFC converter, but the efficiency is appreciable increased.

In contrast to the single-stage true bridgeless Cuk PFC rectifier, the bridgeless PFC rectifier is operated with a constant switching frequency. In order to minimize the conducted emissions into the mains, the switching frequency is again set below the EMI spectrum of the CISPR directive. Considering a certain frequency margin, a constant switching frequency of 130 kHz and an output voltage of 400 V are selected.

For the subsequent isolated DC/DC converter a resonant LLC-converter with a center-tapped secondary winding is used [3] (cf. **Fig. 1**). On the primary side, the half-bridge, consisting of the two switches T_3 and T_4, is operated with a 50%-50% duty cycle. If the LLC-converter's switching frequency is selected equal to the resonant frequency f_{r1} of the LLC-tank, which consists of the resonant capacitor C_{r}, the leakage inductance L_{r} and the magnetizing inductance L_{m}, a load independent input to output voltage ratio given by the transformer's turns ratio is achieved [4]. The resonant frequency f_{r1} is given as

$$f_{\mathrm{r1}} = \frac{1}{2\pi \cdot \sqrt{L_{\mathrm{r}} C_{\mathrm{r}}}}. \tag{11}$$

Thus, a square wave voltage excitation of the LLC resonant tank at the resonant frequency f_{r1} results in a sinusoidal resonant current i_{Cr} and in a triangular magnetizing current i_{Lm} on the primary side, whereas only the sinusoidal resonant current (considering the transformer's turns ratio) is flowing on the secondary side of the DC/DC-converter [4]. It should be mentioned that the sinusoidal currents lead to lower losses in the transformer due to the missing higher frequency components and especially has a positive impact on the conducted emissions. In addition, a split DC-link capacitor is used, in order to not apply any DC-voltage to the resonant capacitor C_{r}. Thus, a resonant capacitor with lower voltage rating can be used.

As well as for the resonant circuit of single-stage converter, with a proper design of the leakage and magnetizing inductance, the resonant inductor can be magnetically integrated into the isolation transformer. In order to further downsize the overall volume of the conventional two-stage rectifier system, a smaller DC-link capacitor C_{DC1} can be employed on the primary side, even if the output voltage ripple is limited to 1% (cf. **Table I**). Of course, this leads to a larger voltage ripple $\Delta v_{\mathrm{C_{DC}}}$ at twice the mains frequency (100/120 Hz). However, this can be compensated with the subsequent LLC-converter since the input to output voltage ratio can be controlled by slightly varying the switching frequency around the resonant frequency f_{r1}. As shown in [4], the sensitivity of the input to output voltage ratio depending on the frequency variation, i.e. the quality factor Q of the LLC-resonant circuit, strongly depends on the selected value of the magnetizing inductance L_{m}. Lower values of L_{m} lead to a higher quality factor Q, thus to a second dominant resonant frequency f_{r2}

$$f_{\mathrm{r2}} = \frac{1}{2\pi \cdot \sqrt{(L_{\mathrm{r}} + L_{\mathrm{m}}) C_{\mathrm{r}}}}. \tag{12}$$

Thus, the output voltage V_{out} can be properly regulated even if, compared to the output capacitor C_{DC} of the single-stage concept, a much smaller dc-link capacitance C_{DC1} is used. In addition, also the dc-link capacitance C_{DC2} can be decreased, since at the output of the DC/DC-converter no 100/120 Hz voltage ripple has to be filtered.

V. Performance Comparison of both Concepts

A comparative evaluation of the two presented PFC rectifier systems concerning efficiency and power density is performed based on the specifications given in **Table I**. In order to have a fair comparison of the overall volume of both concepts,

TABLE II: Resulting volume and share of losses of the designed single and two-stage rectifier systems for an input voltage of 230 V and an output power of 100 W.

	Single-stage		**Two-stage**	
	Volume [cm^3]	Losses [W]	Volume [cm^3]	Losses [W]
EMI Input filter	24.7	0.04	24.7	0.04
Input diodes	-	-	2.8	0.25
Boost inductor	21.8	0.39	22.8	0.19
Switches	1.6	2.15	2.4	1.82
SiC diodes	-	-	0.8	0.49
Resonant capacitor	9.8	-	1.3	-
Transformer	21.8	1.01	30.5	1.35
Output Capacitor (1%)	112.0	0.26	54.1	0.4
Output Capacitor (2%)	56.0	0.26	27.1	0.4
Control	-	0.5	-	0.5
Total (1%)	**191.7**	**4.37**	**139.4**	**4.68**
Total (2%)	**135.7**	**4.37**	**112.4**	**4.68**
Efficiency		**95.6%**		**95.3%**

also an EMI input filter was designed, such that the EMC directive (CISPR, class B) are fulfilled. As a consequence, for the true bridgeless Cuk PFC rectifier, the variable switching frequency was limited to the range of $20 - 150\,\mathrm{kHz}$ and for the conventional two-stage system a constant switching frequency of $130\,\mathrm{kHz}$ was selected for both stages. Thus, the spectral component at the switching frequency doesn't have to be considered for the input filter design. However, other requirements have to be met, like the ground currents for the common mode filter design, which have to be limited below $3.5\,\mathrm{mA}$ or the minimum power factor of $\lambda > 0.9$ for the differential mode filter design, which is desired over the full input voltage range and a wide output power range.

In the design of the boost inductor, for the single and two-stage concept, a compromise between volume, losses and EMI-noise emissions has to be made. Typically, in a wide design range the volume and losses are reduced with decreasing inductances, since less turns and less core material are needed, which however results in a higher input filter effort. Moreover, due to the higher current ripple, the converter is partially operated in the discontinuous conduction mode (DCM) where the parasitic output capacitances of the semiconductors lead to current and voltage oscillations as soon as the boost inductor current returns to zero. Thus, the current control can be quite challenging. On the other hand, for a given core type, the maximum feasible inductance is given by the maximum allowed losses or the given thermal limits respectively.

Similar aspects concerning volume and losses have to be considered for the design of the isolation transformer. In addition, for the magnetic integration of the resonant inductance, a proper mechanical design of the winding arrangement is needed.

For the designed single and two-stage rectifier systems in **Table II** the resulting volumes and losses for an input voltage of $230\,\mathrm{V}$ and an output power of $100\,\mathrm{W}$ are shown. For the specifications given in **Table I**, the two-stage converter results in a smaller volume. As can be noticed, almost $60\,\%$ of the single-stage rectifier's overall volume is due to the large output capacitor, which is needed to keep the 100/120 Hz-voltage ripple within the specifications. In comparison, the total capacitor volume of the two-stage converter is only half the size, since on the primary's DC-voltage a larger voltage ripple can be allowed, which is then compensated by the subsequent DC/DC-converter. However, if the specification of the allowable voltage ripple is increased to $2\,\%$, the output capacitor volume is halved, thus resulting in similar overall volumes for both concepts. It has to be mentioned that with the true bridgeless Cuk PFC rectifier the high resonant current leads to high current stresses in the output capacitor. Hence, for this design the output voltage can't be further increased than $2\,\%$.

According to **Table II**, for the single-stage rectifier system a slightly higher efficiency is achieved for an input voltage of $230\,\mathrm{V}$ and an output power of $100\,\mathrm{W}$. In addition to the listed share of losses a constant power of $0.5\,\mathrm{W}$ was considered for the control electronics.

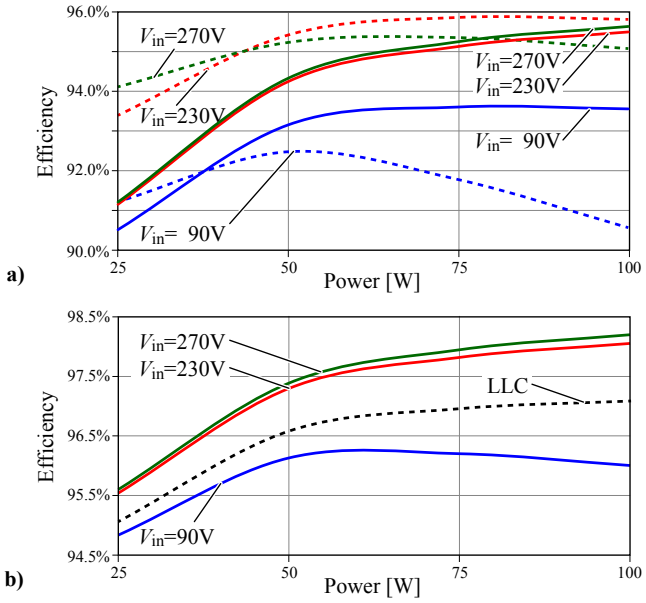

Fig. 7: a) Calculated efficiency of the true bridgeless Cuk (dashed lines) and the conventional PFC AC/DC converter system (solid lines) for different input voltages and **b)** separated efficiencies of both stages used for the conventional concept.

In **Fig. 7 a)** the efficiency of the true bridgeless Cuk PFC (dashed lines) and the two-stage rectifier system (solid lines) are compared for different input voltages and loads. There, especially with high input voltages in the part-load range the single-stage rectifier achieves considerably higher efficiencies. In contrast, by the fact that both stages of the conventional rectifier concept show a low efficiency in the part-load range (cf. **Fig. 7 b)**), the cascading of the two stages results in an even lower overall efficiency. There, the overall efficiency is found by multiplying the two individual efficiencies.

At high input voltages, the losses in the single-stage rectifier are mainly dominated by the conduction losses in the semiconductors and the transformer, due to the large resonant current which only depends on the input to output voltage difference. At $V_{\mathrm{in}} = 270\,\mathrm{V}$ and nominal output power, for example, the total semiconductor losses are $1.9\,\mathrm{W}$ and the transformer losses $1.7\,\mathrm{W}$. For low input voltages the efficiency of the single-stage concept is drastically reduced, since with the high input current the losses in the switch and the snubber circuit are dominant.

At $V_{\mathrm{in}} = 90\,\mathrm{V}$ and nominal output power, the semiconductor losses are calculated to $7.1\,\mathrm{W}$, whereas almost $4\,\mathrm{W}$ - which is $4\,\%$ of the efficiency - are dissipated in the snubber circuit. Therefore, if these snubber losses could be reduced by active snubber circuits, much higher efficiencies would be achievable with the true bridgeless Cuk PFC rectifier system also for low input voltage. A further loss contribution at low input voltages is found in the boost inductor ($2.5\,\mathrm{W}$) due to the high input current ratings. For the single-stage converter the highest efficiency of $95.8\,\%$ is found at input voltages around $V_{\mathrm{in}} = 230\,\mathrm{V}$, since there the input current as well as the resonant current show similar moderate values.

VI. Conclusion

In this paper a new isolated 1-Φ single-stage PFC AC/DC converter topology is analyzed in detail and and general design considerations are done. In addition, the limits of the concept are identified and comparative evaluation against a conventional two-stage approach in terms of efficiency and power density is provided. For high input voltages the true bridgeless Cuk PFC converter offers a notably high efficiency in the part-load range. For low input voltages, however, the efficiency is drastically reduced due to losses in the snubber circuit. Consequently, the design of the snubber circuit and especially the resonant circuit is very crucial.

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