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***Abstract*—High power EV chargers connected to AC power distribution architectures employ a three-phase (3-Φ) PFC rectifier front-end and a series-connected isolated DC/DC converter to cover a wide range of traction battery voltages and efficiently supply the required charging current. In this paper, the operating principle of a two-stage 3-Φ buck-boost current DC-link PFC rectifier system is first introduced. Its optimal operating modes, minimizing conduction losses, switching losses, and CM noise emissions for every DC output voltage level, are identified. Adequate modulation strategies are proposed and explained through detailed switching patterns. Importantly, the two stages of the PFC rectifier system, i.e. the 3-Φ buck-type current source rectifier input stage and the subsequent three-level boost DC/DC stage, are controlled synergetically which ensures an automatic selection and seamless transition between the optimal combinations of operating modes of both stages. Simulation results verify the operation of the described power converter for different output voltage and output power levels. Furthermore, a new common-mode (CM) filtering method, requiring a CM DC-link inductor and a capacitive connection between an artificial 3-Φ neutral point and the DC output mid-point, is analyzed with the support of a derived CM equivalent circuit. Finally, a complete guideline for the design of the CM filter, based on analytical calculations of the CM voltage-time area, is presented.**

***Index Terms*—Three-Phase Buck-Boost Current DC-Link PFC rectifier system, Three-Phase Buck-Type Current Source Rectifier, CM Equivalent Circuit, CM Filter Design.**

I. Introduction

HIGH power and high efficiency on- and off-board battery chargers, which facilitate a significant reduction of the charging times of electric vehicles (EVs), are of crucial importance for the implementation of sustainable mobility concepts. Today, two types of fast (or Level 3) EV charging architectures, i.e. systems supplied from a local three-phase (3-Φ) power distribution AC-bus and, alternatively, DC-bus based systems, are discussed in literature [1]. 3-Φ AC-bus based charging stations are benefiting from standard and mature AC protection and metering technologies, and are realized as cascaded converter structures, comprising an AC/DC front-end and a series-connected isolated DC/DC converter [2]. Besides ensuring 3-Φ sinusoidal input currents and galvanic isolation between the AC-bus and the EV, the employed converter system must cover a wide output voltage range to adapt to different vehicle battery voltages, e.g. to 360 V [3] and 800 V [4]. The required voltage regulation can be performed by the AC/DC front-end, or the isolated DC/DC converter, or shared between both converters. However, if the isolated DC/DC converter is realized as series resonant converter, which offers high efficiency but limited output voltage controllability [5], the AC/DC front-end must provide the complete voltage adaption. Moreover, according to the developing vehicle-to-grid (V2G) trend [6], EVs are planned to serve as distributed energy storage elements to support the grid operation. Therefore, future EV chargers must allow bidirectional power conversion, resulting in an according requirement for the AC/DC front-end.

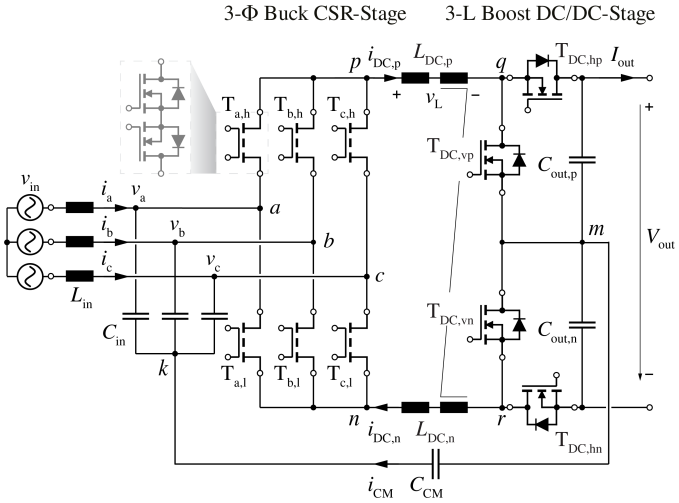

Fig. 1: Power circuit schematic of the proposed three-phase (3-Φ) buck-boost (bB) current DC-link PFC rectifier system (EV charger AC/DC front-end) employing a three-level (3-L) boost DC/DC stage. The system specifications and circuit parameters are indicated in **Tab. I**. To filter the common-mode (CM) noise at the DC output port, the artificial 3-Φ neutral point k and the DC mid-point m are connected through a CM filter capacitor C_{CM}, and a CM filter inductor is employed in the current DC-link.

In this context, the 3-Φ buck-boost (bB) current DC-link PFC rectifier system shown in **Fig. 1**, formed by a 3-Φ buck-type current source rectifier (CSR)-stage [7] and a subsequent three-level (3-L) boost DC/DC-stage, offers several advantages compared to a conventional boost-type PFC rectifier approach, i.e. a reduced number of magnetic components, direct start-up capability, and a sinusoidally varying switched voltage which potentially reduces the occurring switching losses [8]. Moreover, a 3-Φ bB current DC-link PFC rectifier system can also be applied in non-isolated on-board chargers protected by an on-board ground fault circuit interrupter [9]. There, the

TABLE I: System specifications and simulation parameters.

	Description	Value		
V_{in}	AC-bus RMS phase voltage	230 V		
$\cos(\phi)$	power factor	1.0		
f_{in}	AC-bus frequency	50 Hz		
f_{sw}	switching frequency	100 kHz (both stages)		
C_{in}	input capacitance	3 × 10 µF		
$L_{\text{DC,DM}}$	DM DC-link inductance	270 µH		
$L_{\text{DC,CM}}$	CM DC-link inductance	1 mH		
C_{CM}	CM filter capacitance	1.1 µF		
C_{out}	output capacitance	2 × 50 µF		
V_{out}	DC output voltage	200 V	400 V	1000 V
I_{out}	output current	25 A	25 A	10 A
P_{out}	output power	5 kW	10 kW	10 kW

switches of the traction inverter and the stator coils of the motor, which are already present on-board the EV, can be used as DC/DC-stage and DC-link inductor, resulting in a compact and low-cost solution [10].

Different operating modes of the proposed 3-Φ bB current DC-link PFC rectifier system can be employed depending on the instantaneous output voltage level. In particular, in order to fully exploit the potential of this topology, i.e. to minimize conduction losses, switching losses, and CM noise emissions,

- the number of switching instants can be reduced by de-activating the DC/DC-stage when only buck functionality is required, and by applying a variable DC-link current control strategy [11], [12];
- the DC-link current can be kept at the minimum value, such that the CSR-stage is always modulated with the maximum possible modulation index;
- the CM noise can be reduced by appropriately selecting (different from conventional PWM schemes [13], [14]) the zero state of the CSR-stage.

Additionally, a new CM filtering concept, i.e. a CM DC-link inductor in combination with a capacitive connection between an artificial 3-Φ neutral point and the DC output mid-point, can be used for suppressing high-frequency CM noise at the DC output port.

These considerations motivate a comprehensive analysis of the 3-Φ bB current DC-link PFC rectifier system illustrated in **Fig. 1**, which is the subject of this paper. First, the different operating modes and the CM/DM voltage generation of the proposed converter are analyzed in **Section II** with the help of simulations and a CM/DM equivalent circuit, assuming operation in a 3-Φ 400 V RMS (line-to-line) grid, a wide DC output voltage range of 200 V - 1000 V, and a rated power of 10 kW (cf. **Tab. I**). Next, **Section III** provides a guideline for the design of the main high-frequency magnetic component of the converter, i.e. the CM/DM DC-link inductor, and of the proposed CM filter. Finally, **Section IV** concludes this paper.

II. Operating Behavior

The operating principle of the proposed 3-Φ bB current DC-link AC/DC PFC rectifier system is described in this section.

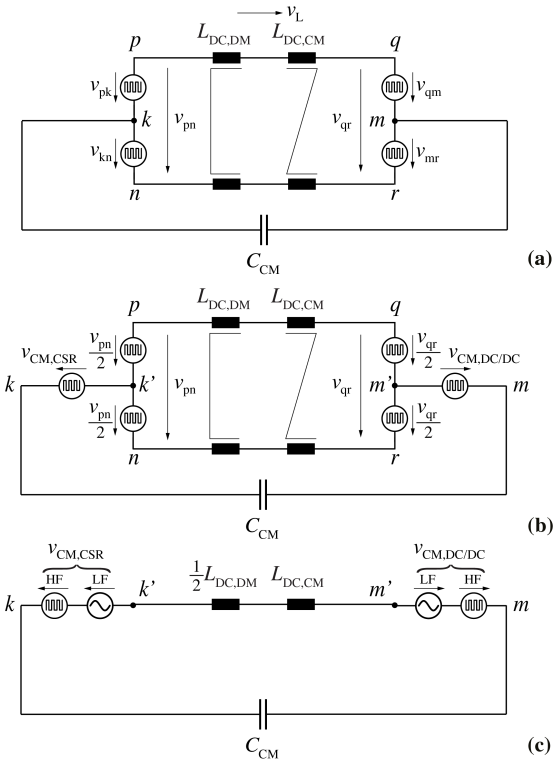

Fig. 2: CM/DM equivalent circuit of the proposed 3-Φ bB current DC-link PFC rectifier system (cf. **Fig. 1**). In particular, the CSR-stage and the DC/DC-stage are replaced by **(a)** switched voltage sources and **(b)** equivalent CM/DM voltage sources. In **(c)**, only high-frequency (HF) and low-frequency (LF) CM voltage sources are shown together with the new CM filter structure under the assumption that the two windings of the CM inductor are perfectly coupled.

In particular, the different operating modes, selected depending on the output voltage level (see **Tab. II**), which minimize the occurring conduction losses, switching losses, and CM noise emissions, are analyzed with the support of simulation results.

A. CM/DM Equivalent Circuit

In order to provide a basis for the understanding and analysis of the CM/DM behavior of the proposed converter system, a CM/DM equivalent circuit is derived in the following. First, mixed CM/DM voltage sources are introduced, i.e. the CSR-stage is replaced with two switched voltage sources v_{pk} and v_{kn}, and the DC/DC-stage is replaced with two switched voltage sources v_{qm} and v_{mr}, as shown in **Fig. 2(a)**. Hence, the fictitious CM voltage v_{CM0} of the overall converter, i.e. the potential difference between the DC mid-point *m* and the artificial 3-Φ neutral point *k* in case no capacitive connection via C_{CM} is present (open-circuit/inner CM voltage source), is calculated as

$$\begin{aligned} v_{\text{CM0}} &= v_{\text{pk}} - v_{\text{L}} - v_{\text{qm}} \\ &= v_{\text{pk}} - \tfrac{1}{2}(v_{\text{pn}} - v_{\text{qr}}) - v_{\text{qm}} \\ &= v_{\text{pk}} - \tfrac{1}{2}(v_{\text{pk}} - v_{\text{nk}} - v_{\text{qm}} + v_{\text{rm}}) - v_{\text{qm}} \\ &= \tfrac{1}{2}(v_{\text{pk}} + v_{\text{nk}}) - \tfrac{1}{2}(v_{\text{qm}} + v_{\text{rm}}) \\ &= v_{\text{CM,CSR}} - v_{\text{CM,DC/DC}}, \end{aligned} \tag{1}$$

where the CM voltage of the CSR-stage, $v_{\text{CM,CSR}} = \frac{1}{2}(v_{\text{pk}} + v_{\text{nk}})$, and the CM voltage of the DC/DC-stage, $v_{\text{CM,DC/DC}} =$

TABLE II: Operating regions and corresponding operating modes of the proposed 3-Φ bB current DC-link PFC rectifier system. In particular, the modulation scheme of the CSR-stage and the input voltage of DC/DC-stage, v_{qr}, are indicated. Due to the operating range of the considered application (see **Tab. I**), ***Boost-Mode #3*** is not analyzed in this paper.

$g_{\mathrm{v}} = V_{\mathrm{out}} / \hat{V}_{\mathrm{in}}$	Operating Mode	CSR-stage	DC/DC-stage v_{qr}
$g_{\mathrm{v}} < \frac{3}{2}$	***Buck***	3/3-PWM	V_{out}
$\frac{3}{2} < g_{\mathrm{v}} < \sqrt{3}$	***Transition***	3/3-PWM 2/3-PWM	V_{out} $\frac{1}{2}V_{\mathrm{out}}$ - V_{out} - $\frac{1}{2}V_{\mathrm{out}}$
$\sqrt{3} < g_{\mathrm{v}} < 3$	***Boost #1***	2/3-PWM	$\frac{1}{2}V_{\mathrm{out}}$ - V_{out} - $\frac{1}{2}V_{\mathrm{out}}$
$3 < g_{\mathrm{v}} < 2\sqrt{3}$	***Boost #2***	2/3-PWM	$\frac{1}{2}V_{\mathrm{out}}$ - V_{out} - $\frac{1}{2}V_{\mathrm{out}}$ 0 V - $\frac{1}{2}V_{\mathrm{out}}$ - 0 V
$g_{\mathrm{v}} > 2\sqrt{3}$	***Boost #3***	2/3-PWM	0 V - $\frac{1}{2}V_{\mathrm{out}}$ - 0 V

$\frac{1}{2}(v_{\mathrm{qm}} + v_{\mathrm{rm}})$, are introduced. Eq. (1) highlights how v_{CM0} results from the superposition of the CM voltages of the two stages.

Next, an equivalent circuit explicitly showing the CM/DM voltage sources is obtained separating the CM voltages from the generic switched voltage sources (cf. **Fig. 2(a)** and **(b)**). Thus, the DM voltages are calculated as

$$v_{\mathrm{pk'}} = v_{\mathrm{pk}} - v_{\mathrm{CM,CSR}} = \tfrac{1}{2}v_{\mathrm{pn}} = v_{\mathrm{k'n}}, \tag{2}$$

$$v_{\mathrm{qm'}} = v_{\mathrm{qm}} - v_{\mathrm{CM,DC/DC}} = \tfrac{1}{2}v_{\mathrm{qr}} = v_{\mathrm{m'r}}. \tag{3}$$

This analysis facilitates the understanding of the CM behavior, hence, the implementation of a new CM filtering concept, comprising a capacitive connection (through C_{CM}) between m and k, and a CM DC-link filter inductor $L_{\mathrm{DC,CM}}$. The introduced CM filter (see **Fig. 2(c)**), in series with the equivalent CM voltage source v_{CM0}, basically acts as a frequency dependent voltage divider, i.e. the HF components $v_{\mathrm{CM,L}}$ are largely applied across $L_{\mathrm{DC,CM}}$, while the remaining LF components v_{mk} largely appear across C_{CM}, significantly minimizing the HF CM noise emissions at the DC output port, under the assumption that C_{in} and C_{out}, with relatively large capacitance values, are ignored compared to C_{CM}. Furthermore, since the DC-link current i_{DC} is mainly driven by the difference between the CSR-stage output voltage v_{pn} and the DC/DC-stage input voltage v_{qr}, i_{CM} has almost no influence on i_{DC}, given the comparatively large impedance of $L_{\mathrm{DC,CM}}$.

B. System Simulation

Simulated waveforms of the proposed converter are shown in **Fig. 3**, highlighting the 3-Φ mains voltages $v_{\{\mathrm{a,b,c}\}}$, the output voltage V_{out}, the 3-Φ mains currents $i_{\{\mathrm{a,b,c}\}}$, and the DC-link current i_{DC}, as well as the voltages v_{pn} and v_{qr}. Characteristic waveforms describing the formation of $v_{\mathrm{CM,CSR}}$ and $v_{\mathrm{CM,DC/DC}}$, i.e. the CM behavior, are presented, subsequently, in **Fig. 4**. The CM voltage v_{CM0}, obtained as in (1), is indicated in **Fig. 5(a)**. Finally, the voltage v_{mk} across the CM filter capacitor C_{CM} and the voltage $v_{\mathrm{CM,L}}$ across the CM inductor $L_{\mathrm{DC,CM}}$ are illustrated in **Figs. 5(b)** and **(c)** to explain the functionality of the proposed CM filter structure.

TABLE III: Switching states of the CSR-stage and associated DM voltages v_{pn} and CM voltages $v_{\mathrm{CM,CSR}}$.

S_{CSR}	on-state		v_{pk}	v_{kn}	v_{pn}	$v_{\mathrm{CM,CSR}}$
[aa]	$\mathrm{T_{a,h}}$	$\mathrm{T_{a,l}}$	v_{a}	$-v_{\mathrm{a}}$	0 V	$\frac{v_{\mathrm{a}}+v_{\mathrm{a}}}{2} = v_{\mathrm{a}}$
[bb]	$\mathrm{T_{b,h}}$	$\mathrm{T_{b,l}}$	v_{b}	$-v_{\mathrm{b}}$	0 V	$\frac{v_{\mathrm{b}}+v_{\mathrm{b}}}{2} = v_{\mathrm{b}}$
[cc]	$\mathrm{T_{c,h}}$	$\mathrm{T_{c,l}}$	v_{c}	$-v_{\mathrm{c}}$	0 V	$\frac{v_{\mathrm{c}}+v_{\mathrm{c}}}{2} = v_{\mathrm{c}}$
[ab]	$\mathrm{T_{a,h}}$	$\mathrm{T_{b,l}}$	v_{a}	$-v_{\mathrm{b}}$	v_{ab}	$\frac{v_{\mathrm{a}}+v_{\mathrm{b}}}{2}$
[ba]	$\mathrm{T_{b,h}}$	$\mathrm{T_{a,l}}$	v_{b}	$-v_{\mathrm{a}}$	$-v_{\mathrm{ab}}$	$\frac{v_{\mathrm{b}}+v_{\mathrm{a}}}{2}$ $\Big\}$ $= v_{\mathrm{CM,ab}}$
[bc]	$\mathrm{T_{b,h}}$	$\mathrm{T_{c,l}}$	v_{b}	$-v_{\mathrm{c}}$	v_{bc}	$\frac{v_{\mathrm{b}}+v_{\mathrm{c}}}{2}$
[cb]	$\mathrm{T_{c,h}}$	$\mathrm{T_{b,l}}$	v_{c}	$-v_{\mathrm{b}}$	$-v_{\mathrm{bc}}$	$\frac{v_{\mathrm{c}}+v_{\mathrm{b}}}{2}$ $\Big\}$ $= v_{\mathrm{CM,bc}}$
[ca]	$\mathrm{T_{c,h}}$	$\mathrm{T_{a,l}}$	v_{c}	$-v_{\mathrm{a}}$	v_{ca}	$\frac{v_{\mathrm{c}}+v_{\mathrm{a}}}{2}$
[ac]	$\mathrm{T_{a,h}}$	$\mathrm{T_{c,l}}$	v_{a}	$-v_{\mathrm{c}}$	$-v_{\mathrm{ca}}$	$\frac{v_{\mathrm{a}}+v_{\mathrm{c}}}{2}$ $\Big\}$ $= v_{\mathrm{CM,ca}}$

TABLE IV: Switching states of the DC/DC-stage and associated DM voltages v_{qr} and CM voltages $v_{\mathrm{CM,DC/DC}}$.

$S_{\mathrm{DC/DC}}$	$\mathrm{T_{DC,hp}}$	$\mathrm{T_{DC,vp}}$	$\mathrm{T_{DC,vn}}$	$\mathrm{T_{DC,hn}}$	v_{qr}	$v_{\mathrm{CM,DC/DC}}$
[00]	0	1	1	0	0 V	0 V
[10]	1	0	1	0	$\frac{1}{2}V_{\mathrm{out}}$	$\frac{1}{4}V_{\mathrm{out}}$
[01]	0	1	0	1	$\frac{1}{2}V_{\mathrm{out}}$	$-\frac{1}{4}V_{\mathrm{out}}$
[11]	0	1	0	1	V_{out}	0 V

All the zoomed plots in **Figs. 3-5** offer a detailed view of the switched voltage waveforms and of the corresponding switching patterns of the CSR-stage (S_{CSR}, see **Tab. III**), and of the DC/DC-stage ($S_{\mathrm{DC/DC}}$, see **Tab. IV**). The system specifications and the considered simulation parameters are summarized in **Tab. I**.

C. Buck-Mode Operation ($V_{\mathrm{out}} < \frac{3}{2}\hat{V}_{\mathrm{in}}$)

In ***Buck-Mode*** operation, only the CSR-stage operates with 3/3-PWM (switching operation of all three bridge legs within a pulse period, [11]) to step down the 3-Φ mains voltages to a DC output voltage lower than $\frac{3}{2}\hat{V}_{\mathrm{in}}$, and the two switches $\mathrm{T_{DC,hp}}$ and $\mathrm{T_{DC,hn}}$ of the DC/DC-stage are permanently on. This minimizes the overall conduction losses and avoids any switching losses in the DC/DC-stage.

Two types of 3/3-PWM, different with respect to the zero state utilized in the CSR-stage, are considered in ***Buck-Mode*** operation, i.e. the conventional 3/3-PWM [7] and the reduced CM (RCM) 3/3-PWM [13]. In the conventional 3/3-PWM, the phase with the maximum current is shorted during the zero state (see **Fig. 3(i)**); differently, with RCM 3/3-PWM, the phase with the minimum absolute current value is used (see **Fig. 3(ii)**). Both types of 3/3-PWM have identical DM performance, but the associated waveforms of $v_{\mathrm{CM,CSR}}$ are different, as shown in **Fig. 4(a)**. In fact, during the zero states, $v_{\mathrm{CM,CSR}}$ coincides with the phase voltage associated to the shorted bridge-legs, which differs in these two variants of 3/3-PWM (see **Tab. III**).

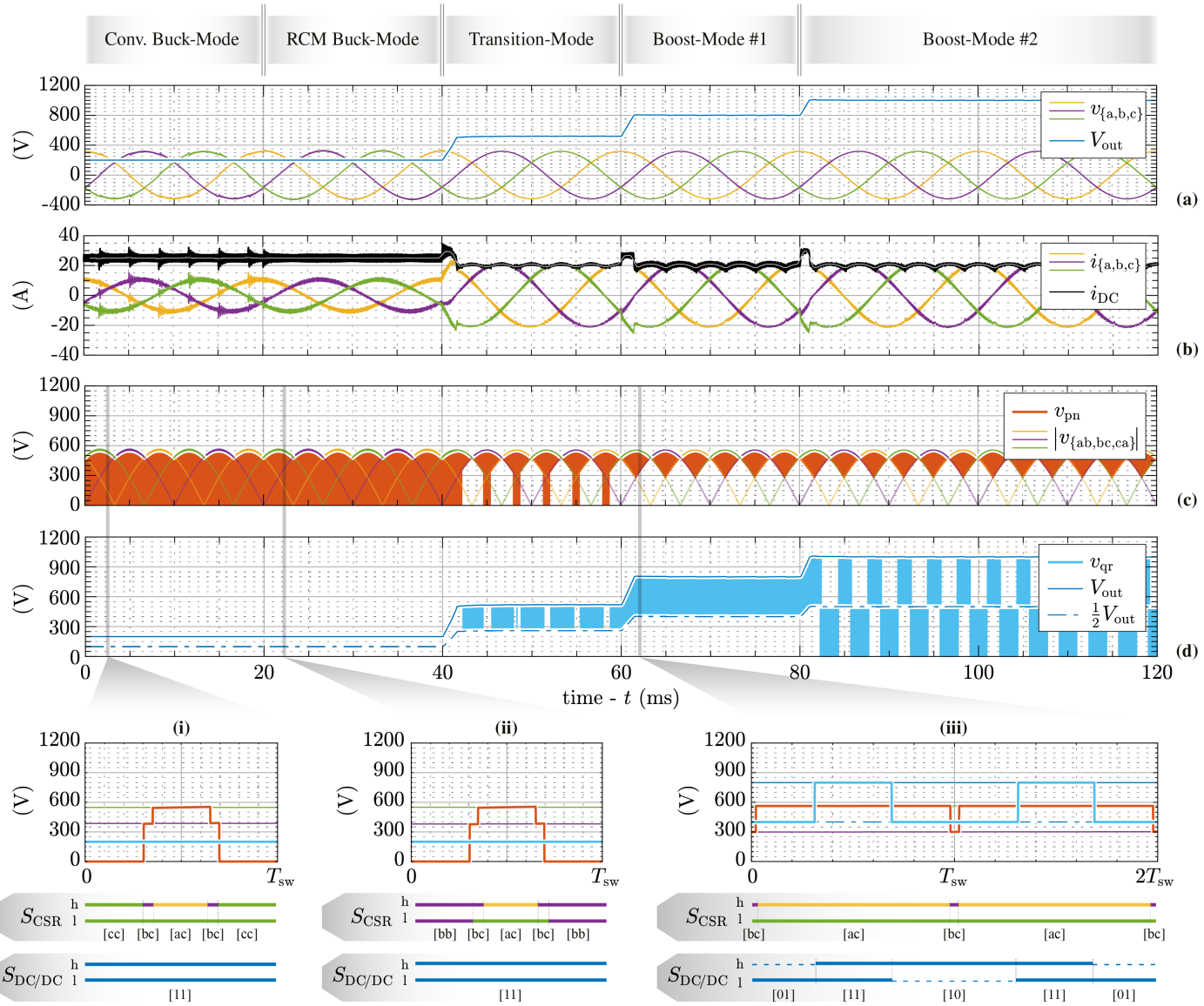

Fig. 3: Simulated DM waveforms of the proposed converter for different output voltage levels and operating modes. Corresponding CM waveforms are shown in **Fig. 4**. **(a)** 3-Φ mains voltages $v_{\{a,b,c\}}$ and output voltage V_{out}; **(b)** 3-Φ mains currents $i_{\{a,b,c\}}$ and DC-link current i_{DC}; **(c)** output voltage of the CSR-stage v_{pn} alternately assuming the absolute values of the line-to-line voltages $v_{\{ab,bc,ca\}}$ during the active states and 0 V during the zero state; **(d)** input voltage of the DC/DC-stage v_{qr} switching between 0 V and $\frac{1}{2}V_{out}$ or $\frac{1}{2}V_{out}$ and V_{out}. This simulation covers a wide output voltage range forcing the converter to operate in all the modes indicated on top of **(a)**. The graphs at the bottom offer a zoomed view of the switched voltage waveforms and indicate the corresponding switching patterns of the CSR-stage (S_{CSR}) and of the DC/DC-stage ($S_{DC/DC}$).

The implementation of the mentioned CM filtering method requires the continuity of the local average value (average value over one switching period) of v_{CM0}, especially at the boundary between different sectors, i.e. 60°-wide intervals of a mains period. In fact, a step change of v_{CM0} excites the resonance of the CM filter and distorts the DC-link current and the 3-Φ mains currents. This phenomenon is visible in **Fig. 3(b)** for $0 < t < 20\,\text{ms}$, and is attributed to the CSR-stage, which employs conventional 3/3-PWM, since $v_{CM0} = v_{CM,CSR}$ in ***Buck-Mode*** operation. RCM 3/3-PWM, instead, meets the continuity requirement, and reduces the CM noise generated by the CSR-stage (see **Fig. 5**), hence, it is preferred in the following.

D. Boost-Mode Operation ($V_{out} > \sqrt{3}\hat{V}_{in}$)

The boost functionality of the analyzed converter, which is achieved by operating both the CSR-stage and the DC/DC-stage simultaneously, is required when $V_{out} > \sqrt{3}\hat{V}_{in}$. Here, the CSR-stage operates with 2/3-PWM (only two out of three phases are switched in a switching period, as shown in **Fig. 3(iii)**) to reduce the switching losses, and with the maximum modulation index to reduce i_{DC}, and thus, the conduction losses of the whole converter [11] and [12]. Accordingly, i_{DC} is controlled to a specific profile with six times mains frequency variation (see **Fig. 3(b)** for $60\,\text{ms} < t < 120\,\text{ms}$).

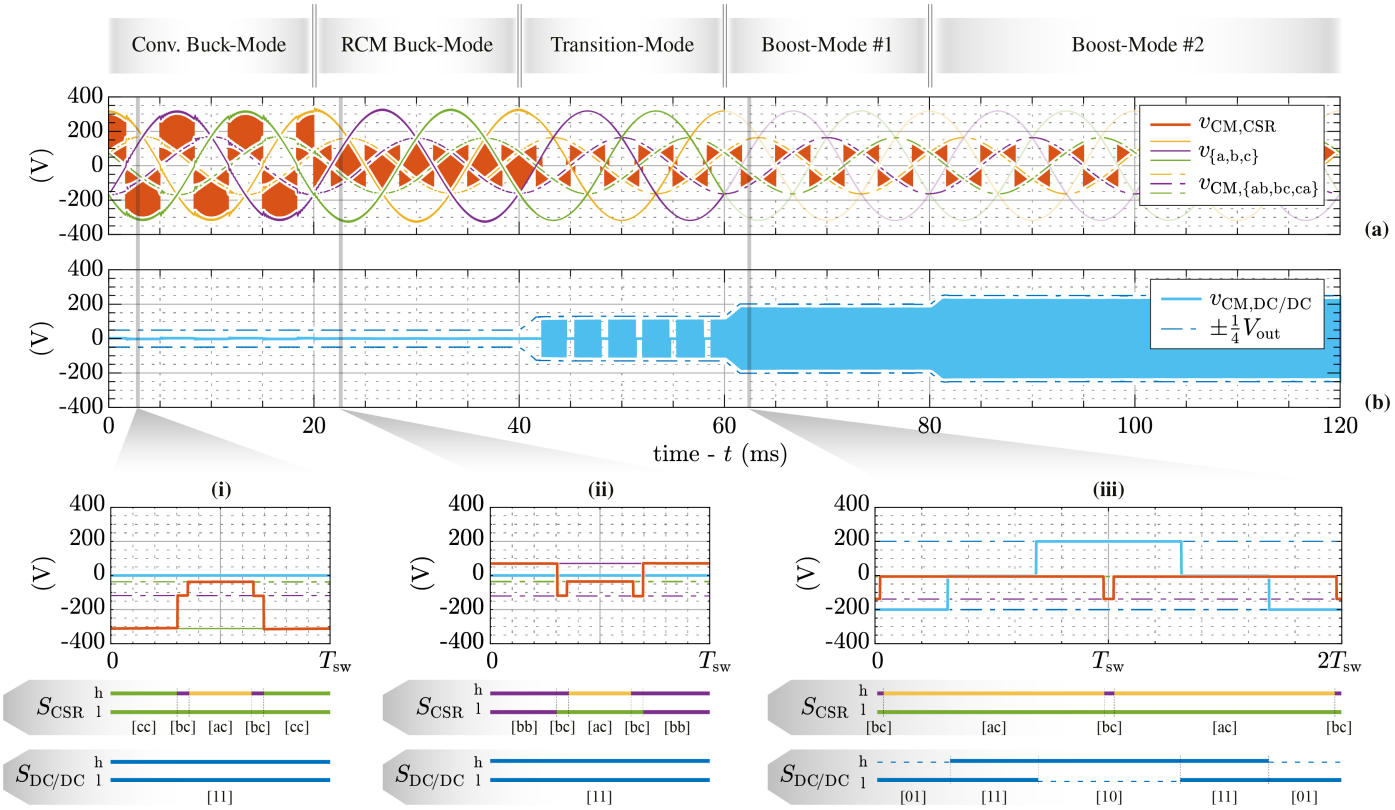

Fig. 4: Simulated CM waveforms highlighting the formation of the CM voltages of the two stages for different output voltage levels and operating modes. Corresponding DM waveforms are shown in **Fig. 3**. **(a)** CM voltage generated by the CSR-stage $v_{CM,CSR}$ alternately assuming the values of the CM voltage associated to the active states $v_{CM,\{ab,bc,ca\}}$ and to the zero state $v_{\{a,b,c\}}$ (see **Tab. III**); **(b)** CM voltage generated by the DC/DC-stage $v_{CM,DC/DC}$ alternately assuming the values of 0 V and $\pm\frac{1}{4}V_{out}$ (see **Tab. IV**). This simulation covers a wide output voltage range forcing the converter to operate in all the modes indicated on top of **(a)**. The graphs at the bottom offer a zoomed view of the switched voltage waveforms and indicate the corresponding switching patterns of the CSR-stage (S_{CSR}) and of the DC/DC-stage ($S_{DC/DC}$).

In ***Boost-Mode*** operation, the waveforms of the CSR-stage (see, e.g., v_{pn} in **Fig. 3(c)** and $v_{CM,CSR}$ in **Fig. 4(a)**) are independent of the output voltage level, since the DC/DC-stage adjusts v_{qr} to balance the voltage-time area generated by the CSR-stage and provides the required voltage gain. The 3-L behavior of the DC/DC-stage is visible on v_{qr}, alternatively assuming the values of 0 V, $\frac{1}{2}V_{out}$, and V_{out}, as shown in **Tab. IV**. Depending on this, three sub-modes exist, i.e. ***Boost-Mode #1***, ***#2***, and ***#3*** (see **Tab. II**):

1) Boost-Mode #1 Operation ($\sqrt{3}\hat{V}_{in} < V_{out} < 3\hat{V}_{in}$)
$\bar{v}_{pn}$ (the local average value of v_{pn}) is always larger than $\frac{1}{2}V_{out}$, and v_{qr} switches between $\frac{1}{2}V_{out}$ and V_{out}, as shown in **Fig. 3(d)** for $60\,\text{ms} < t < 80\,\text{ms}$.

2) Boost-Mode #2 Operation ($3\hat{V}_{in} < V_{out} < 2\sqrt{3}\hat{V}_{in}$)
Due to the increased V_{out}, $\bar{v}_{pn}$ is alternatively larger or smaller (in each 60°-wide sector of a mains period) than $\frac{1}{2}V_{out}$. Hence, when $\bar{v}_{pn} < \frac{1}{2}V_{out}$, v_{qr} additionally switches between 0 V and $\frac{1}{2}V_{out}$, as shown in **Fig. 3(d)** for $80\,\text{ms} < t < 120\,\text{ms}$.

3) Boost-Mode #3 Operation ($2\sqrt{3}\hat{V}_{in} < V_{out}$)
$\bar{v}_{pn}$ is always smaller than $\frac{1}{2}V_{out}$, thus v_{qr} always switches between 0 V and $\frac{1}{2}V_{out}$.

Importantly, when $v_{qr} = \frac{1}{2}V_{out}$, either $C_{out,p}$ or $C_{out,n}$ can be connected at the input port of the DC/DC-stage. This degree of freedom is used to balance the output mid-point m, by alternating between $C_{out,p}$ and $C_{out,n}$, as shown in **Fig. 3(iii)**. In this mode, v_{CM0} (see **Fig. 5(a)**) is obtained with the superposition of $v_{CM,CSR}$ and $v_{CM,DC/DC}$, as described by (1). $v_{CM,CSR}$ alternately assumes the values of the CM voltage associated to the active states $v_{CM,\{ab,bc,ca\}}$, as shown in **Fig. 4(a)**. $v_{CM,DC/DC}$, instead, depends on the actual switching pattern of the DC/DC-stage (see **Fig. 4(iii)**), and features only HF components, with the main component at $\frac{1}{2}f_{sw}$. Hence, with an appropriate filter design, the LF components of v_{CM0} (see **Fig. 5(b)**), correspond to the LF components of $v_{CM,CSR}$.

For completeness, to conclude the analysis of the ***Boost-Mode*** operation, the effect of the phase shift between the PWM carriers of the CSR-stage and of the DC/DC-stage is analyzed. Two scenarios, with or without phase shift, are compared in **Fig. 6**, under the assumption that one switching period starts with a switching state featuring a smaller DM voltage and the one with a larger DM voltage is centered with the carrier peak (see v_{qr} in **Fig. 6 (a)**). The configuration without phase shift is preferred due to the relatively small voltage-time area $Vt_{DM,L}$ applied across the DM DC-link inductor, which leads to a

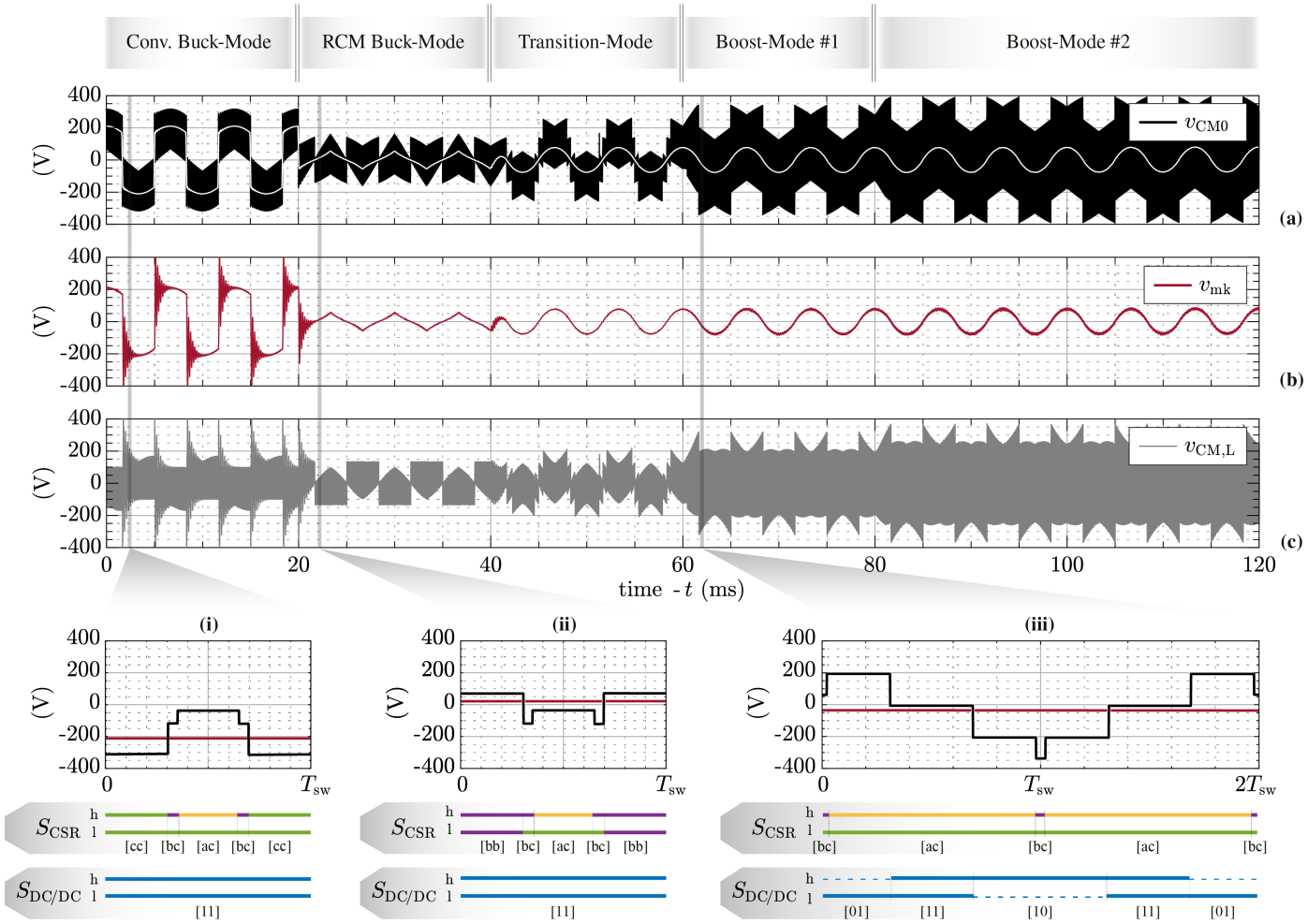

Fig. 5: Simulated CM waveforms highlighting the formation and filtering of the CM voltage of the proposed converter for different output voltage levels and operating modes. **(a)** Fictitious CM voltage v_{CM0} where the white line indicates the local average value of the switched voltage waveform; **(b)** voltage v_{mk} across the CM capacitor C_{CM}; **(c)** voltage $v_{CM,L}$ across the CM inductor $L_{DC,CM}$. This simulation covers a wide output voltage range forcing the converter to operate in different modes indicated on top of **(a)**. The graphs at the bottom offer a zoomed view of the switched voltage waveforms and indicate the corresponding switching patterns of the CSR-stage (S_{CSR}) and of the DC/DC-stage ($S_{DC/DC}$).

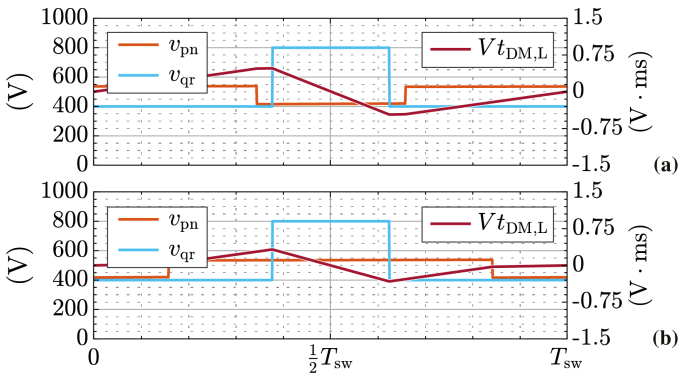

Fig. 6: Waveforms of the output voltage of the CSR-stage v_{pn} and the input voltage of the DC/DC-stage v_{qr}, and corresponding DM voltage-time area $Vt_{DM,L}$ applied across the DM DC-link inductor **(a)** with and **(b)** without phase shift between the carriers of the CSR-stage and of the DC/DC-stage.

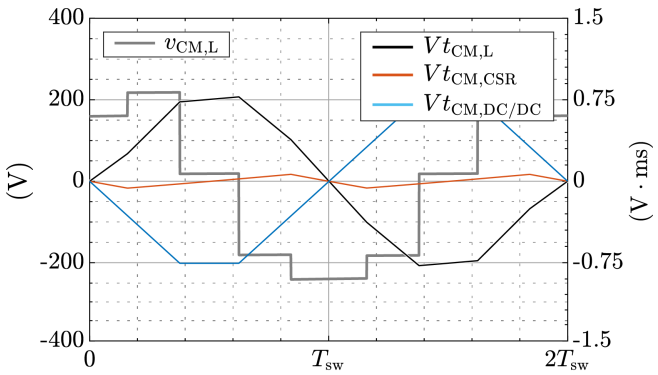

Fig. 7: Waveform of the voltage $v_{CM,L}$ across the CM inductor $L_{DC,CM}$ and corresponding CM voltage-time area $Vt_{CM,L}$ obtained with the superposition of the voltage-time areas generated by the CSR-stage $Vt_{CM,CSR}$ and by the DC/DC-stage $Vt_{CM,DC/DC}$.

smaller inductor design. The carrier arrangement has a negligible influence on the CM DC-link inductor design, because, *(i)* the CM voltage-time area generated by the DC/DC-stage $Vt_{CM,DC/DC}$ is much larger than the HF CM voltage-time area generated by the CSR-stage $Vt_{CM,CSR}$, and *(ii)* a trapezoidal shape of $Vt_{CM,DCDC}$ at $\frac{1}{2}f_{sw}$ is hardly influenced by $Vt_{CM,CSR}$,

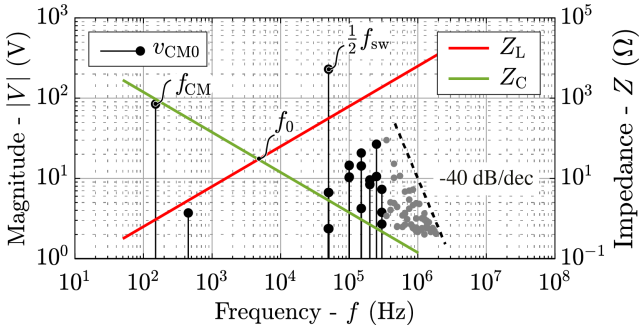

Fig. 8: Frequency spectrum of the fictitious CM voltage v_{CM0} when the converter operates in ***Boost-Mode #1*** ($V_{out} = 800\,V$). In particular, LF components mainly exist at f_{CM} and its odd multiples, while HF components are at $\frac{1}{2}f_{sw}$ and its multiples. The amplitudes of the components decreasing with $-40\,dB/dec$ are neglected. The CM filter, formed by $L_{DC,CM}$ and C_{CM}, is designed based on the selected natural frequency f_0.

i.e. a triangular shape at f_{sw}, as shown in **Fig. 7**.

E. Transition-Mode Operation ($\frac{3}{2}\hat{V}_{in} < V_{out} < \sqrt{3}\hat{V}_{in}$)

In ***Transition-Mode*** operation ($40\,ms < t < 60\,ms$), the converter alternatively operates in ***Buck-Mode*** and ***Boost-Mode***, depending on the instantaneous value of $\bar{v}_{pn}$, i.e. if $\bar{v}_{pn} > V_{out}$, 3/3-PWM is applied in the CSR-stage and the DC/DC-stage is deactivated, whereas, if $\bar{v}_{pn} < V_{out}$, 2/3-PWM is applied in the CSR-stage and the DC/DC-stage steps up the mains voltage to the required output level. The seamless transition between the operating modes is realized by the synergetic control structure described in [15], which simultaneously ensures minimum switching losses and conduction losses.

III. CM/DM DC-Link Inductors Design

In this section, first, a design guideline for the proposed CM filtering method is presented based on the analysis of the frequency spectrum of v_{CM0}. Furthermore, analytical formulas of the voltage-time areas applied to the CM/DM DC-link inductors are derived.

To effectively filter the HF components of the fictitious CM voltage v_{CM0}, the natural frequency f_0 of the CM filter should be selected between the third harmonic of the CM fundamental frequency $3f_{CM}$ ($= 3 \times 150\,Hz$, ensuring a sufficient attenuation of the LF odd harmonics of f_{CM}, e.g. 3rd, 5th, 7th, etc, visible in **Fig. 5(a)** in ***Buck-Mode***), and half of the switching frequency $\frac{1}{2}f_{sw}$ ($= \frac{1}{2} \times 100\,kHz$, see **Fig. 5(iii)**), as shown in **Fig. 8**. Therefore,

$$f_0 = \frac{1}{2\pi}\frac{1}{\sqrt{L_{DC,CM}C_{CM}}} = \sqrt{3f_{CM}\cdot\frac{1}{2}f_{sw}}, \tag{4}$$

where f_{CM} is three times the mains frequency f_{in}, is selected. Furthermore, the CM inductance $L_{DC,CM}$ is designed to limit the current ripple Δi_{CM} flowing through C_{CM}, which is determined by

$$\Delta i_{CM} = \frac{Vt_{CM,L}}{L_{DC,CM}}, \tag{5}$$

where $Vt_{CM,L}$ is the voltage-time area applied to the CM DC-link inductor. In case a CM/DM integrated DC-link inductor structure would be employed, the interactions between the

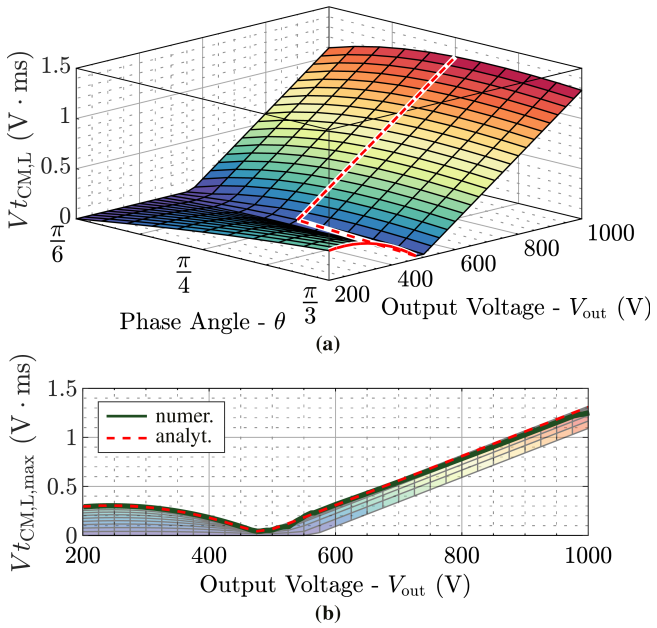

Fig. 9: **(a)** CM voltage-time area $Vt_{CM,L}$ over half of one 60°-wide sector (angle θ) defined by the 3-Φ mains currents and in dependency of the output voltage V_{out}. In the considered sector phase c shows the minimum current value. The dotted line specifies the maximum voltage-time area $Vt_{CM,L,max}$ for a given V_{out}. **(b)** Comparison of $Vt_{CM,L,max}$ calculated numerically and obtained with the derived formulas.

CM/DM inductors, e.g. the limited winding window and the shared magnetic path, should be considered [16]. A separate CM/DM DC-link inductor design could be advantageous to fully utilize the magnetic material characteristics, as e.g. nanocrystalline materials, which features higher permeability and saturation flux density compared to ferrites, allow a downsizing of the CM inductor.

To derive analytical expressions for $Vt_{CM,L}$, different $v_{CM,L}$ waveforms are first grouped depending on their shape. Hence, analytical expressions of $Vt_{CM,L}$ are obtained as function of the phase angle θ within one mains period and of V_{out}, as shown in **Fig. 9(a)**. Afterwards, the value of θ corresponding to the maximum voltage-time area for a given V_{out} is identified, and considered to calculate $Vt_{CM,L,max}$. In 3/3-PWM,

$$Vt_{CM,L,max,3/3} = \frac{T_{sw}V_{out}}{12\hat{V}_{in}}\cdot(3\hat{V}_{in} - 2V_{out}) \tag{6}$$

occurs at $\theta = \pi/3$, while in 2/3-PWM,

$$Vt_{CM,L,max,2/3} = \frac{T_{sw}}{8}\cdot(2V_{out} - 9\sqrt{2}\hat{V}_{in} + 4\sqrt{6}\hat{V}_{in}) \tag{7}$$

occurs at $\theta = \pi/4$.

Also analytical expressions for $Vt_{DM,L}$, i.e. the counterpart of $Vt_{CM,L}$ in DM (see **Fig. 10(a)**), are derived as function of θ and V_{out} in the same manner, to evaluate the DC-link current ripple. Thus, in 3/3-PWM,

$$Vt_{DM,L,max,3/3} = \frac{T_{sw}V_{out}}{6\hat{V}_{in}}\cdot(3\hat{V}_{in} - \sqrt{3}V_{out}) \tag{8}$$

occurs at $\theta = \pi/6$, while in 2/3-PWM,

$$Vt_{DM,L,max,2/3} = \frac{T_{sw}}{4V_{out}}\cdot(3\hat{V}_{in} - 2V_{out})\cdot(V_{out} - 3\hat{V}_{in}) \tag{9}$$

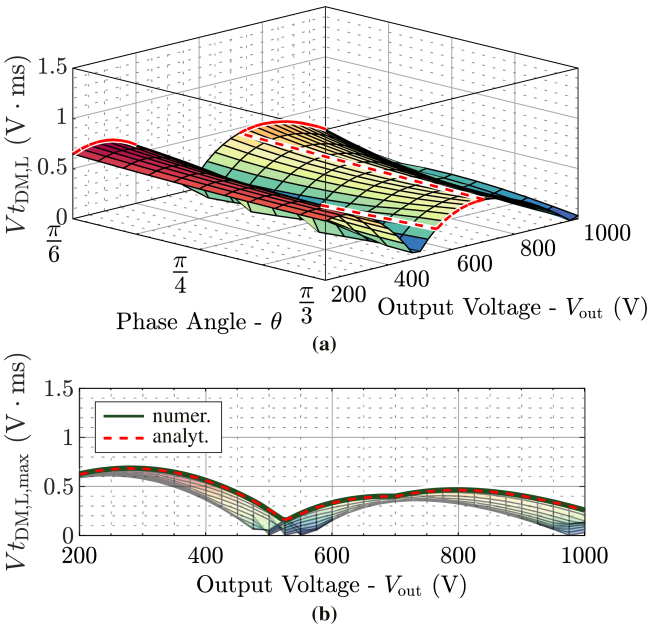

Fig. 10: **(a)** DM voltage-time area $Vt_{\mathrm{DM,L}}$ over half of one 60°-wide sector (angle θ) defined by the 3-Φ mains currents and in dependency of the output voltage V_{out}. In the considered sector, phase c shows the minimum current value. The dotted line specifies the maximum voltage-time area $Vt_{\mathrm{DM,L,max}}$ for a given V_{out}. **(b)** Comparison of $Vt_{\mathrm{DM,L,max}}$ calculated numerically and obtained with the derived formulas.

is valid for $\theta = \pi/3$ if $V_{\mathrm{out}} < \frac{3}{\sqrt{2}}\hat{V}_{\mathrm{in}}$, and

$$Vt_{\mathrm{DM,L,max,2/3}} = \frac{T_{\mathrm{sw}}}{2V_{\mathrm{out}}} \cdot (2\sqrt{3}\hat{V}_{\mathrm{in}} - V_{\mathrm{out}}) \cdot (V_{\mathrm{out}} - \sqrt{3}\hat{V}_{\mathrm{in}}) \quad (10)$$

occurs for $\theta = \pi/6$ if $V_{\mathrm{out}} > \frac{3}{\sqrt{2}}\hat{V}_{\mathrm{in}}$. Only the HF voltage-time area is considered here, but the DC components of the DC-link current should be included when designing the DM DC-link inductor.

For both CM and DM, the obtained analytical formulas are compared with the results of the numerical method, and their excellent accuracy is verified in **Fig. 9(b)** and **Fig. 10(b)**.

Finally, a CM DC-link inductor $L_{\mathrm{DC,CM}}$ of 1 mH (see **Tab. I**) is selected to limit the maximum peak CM current ripple (the maximum CM voltage-time area is identified in **Fig. 9**) to 1.5 A according to (7). The natural frequency of the CM filter is selected according to (4) as $f_0 = 4.7\,\mathrm{kHz}$, thus, $C_{\mathrm{CM}} = 1.1\,\mu\mathrm{F}$, resulting in a HF (at $\frac{1}{2}f_{\mathrm{sw}}$) CM voltage at the DC output mid-point of $5\,\mathrm{V_{pk}}$. The DM DC-link inductor $L_{\mathrm{DC,DM}}$ is designed to limit the maximum peak-to-peak DC-link current ripple (see **Fig. 10**) to 25%. Considering a 20% margin, $L_{\mathrm{DC,CM}} = 270\,\mu\mathrm{H}$ is selected based on (8). The above mentioned component values are listed in **Tab. I** and have already been used for the simulations throughout the papers.

IV. Conclusion

The widespread adoption of EVs requires a high efficiency, reliable, and distributed battery charging infrastructure. Hence, a three-phase (3-Φ) buck-boost current DC-link AC/DC PFC rectifier system, suitable to perform AC/DC energy conversion in fast EV charging architectures connected to a local AC power distribution system, is introduced in this paper. The proposed topology ensures low conduction and switching losses as well as reduced CM noise emissions free of high-frequency components, while operating as AC/DC front-end in a wide DC output voltage range. First, the CM voltage generation is analyzed with the support of CM/DM equivalent circuits. Furthermore, optimal operating modes are proposed to reduce the required DC-link current, to avoid unnecessary switching actions, and to minimize the CM noise emissions at different output voltage levels. All the mentioned functionalities are verified by circuit simulations, focusing on the effectiveness of the presented CM filtering concept, which consists of a CM DC-link inductor in combination with a capacitive connection between the artificial 3-Φ neutral point and the DC output mid-point, and limits the CM voltage of the DC output port to a low-frequency variation. Finally, the selection of the natural frequency of the CM filter and the analytical equations of the voltage-time area applied across the CM/DM DC-link inductor are provided in order to support the filter design.

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