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***Abstract*— The unprecedented performance potential of Gallium-Nitride-on-Silicon (GaN-on-Si) High Electron Mobility Transistors (HEMTs) is seen as the key enabler for the design of power converters featuring extreme power-density figures, as demanded in next generation power electronics applications. However, unexpected loss mechanisms, i.e. dynamic $R_{ds,on}$ phenomena and C_{oss}-losses, are appearing in currently available GaN transistors and are compromising their operation. In this paper, measurements of C_{oss}-losses are performed in a dedicated calorimetric measurement setup and, through a systematic approach, the root cause of the loss mechanism is potentially identified. Afterwards, with the essential support of a manufacturer of power semiconductors, a novel transistor, featuring an enhanced multi-layer III-N buffer, is developed according to the acquired knowledge. A significant reduction in terms of C_{oss}-losses, i.e. of soft-switching losses, and the absence of dynamic $R_{ds,on}$ phenomena are verified experimentally on the new device. These achievements enable a significant performance improvement for future soft-switching power converters featuring GaN-on-Si HEMTs.**

***Index Terms*— Soft-Switching Losses, C_{oss}-Losses, GaN-on-Si HEMTs, Calorimetric Loss Measurements.**

I. Introduction

The remarkable electron mobility and breakdown electric field figures of Gallium-Nitride (GaN), together with a revolutionary semiconductor structure based on a two-dimensional electron gas (2DEG) [1], enable the realization of Gallium-Nitride-on-Silicon (GaN-on-Si) High Electron Mobility Transistors (HEMTs) with outstanding switching and conduction performance [2]. Nowadays, normally-off GaN transistors are widely adopted in power-density optimized converters featuring voltages up to $500\,\mathrm{V}$ [3] and are foreseen as promising semiconductor solutions for power converters on-board of electric vehicles and *More Electric Aircraft* (MEA) [2]. The above mentioned features guarantee high efficiencies, e.g. $99\,\%$, even at high switching frequencies when soft-switching modulation schemes and/or converter concepts are considered [3]. The excellent switching and conduction performance result in lowered cooling and filtering requirements [2], hence in unbeatable power-density figures, since magnetic components and heat-sink elements often dominate the volume and weight breakdowns of power converters [3].

GaN power transistors have been commercially available for only about five years, but, because of their promising performance, they soon became a trending research topic among the power electronics community. Accordingly, GaN devices have been thoroughly investigated in the last years and several unexpected, and not yet completely understood, loss mechanisms have been observed. Among them, dynamic $R_{ds,on}$ phenomena and C_{oss}-losses are of main importance, since they can significantly limit the potential of these devices.

Dynamic $R_{ds,on}$ phenomena can be explained by stored and/or trapped charges in the channel of GaN devices, which lead to a temporary increase of the drain-source resistance $R_{ds,on}$, i.e. of the occurring conduction losses, after the transistors are turned on. Although this issue is still not completely solved by most of the manufacturers [4], [5], it is at least well characterized in literature [6].

The expression C_{oss}-*losses*, instead, defines a loss mechanism relative to the charging/discharging process of the output capacitance C_{oss} of power transistors, particularly affecting the performance of soft-switching power converters. Soft-switching operation is ideally considered loss-less from the point of view of the power semiconductors, however, evidences of C_{oss}-losses, i.e. of soft-switching losses, are recently documented in literature, also in GaN devices [7]–[10]. Accordingly, soft-switching operation of GaN power transistors is shown to be lossy and to even compromise the operation and the efficiency of soft-switching power converters switching in the MHz range. As an example, the measured efficiency of the soft-switching Class-Φ_2 inverter presented in [9] resulted $5\,\%$ lower than what originally estimated. The main responsible for this discrepancy was identified in the unexpected C_{oss}-losses. However, despite this substantial influence and in contrast to the case of dynamic $R_{ds,on}$ phenomena, currently only few evidences of C_{oss}-losses in GaN-on-Si HEMTs are available in literature and only unconfirmed hypotheses on their origin are speculated. This provides a solid motivation to this work, essentially aiming to identify the cause of C_{oss}-losses in GaN-on-Si HEMTs.

Loss mechanisms in capacitors, e.g. C_{oss}-losses, are typi-

cally quantified evaluating the hysteresis curve originating from charging/discharging a sample with large signal voltage waveforms. This method, based on the Sawyer-Tower (ST) circuit, has first been used in 1929 [11] to measure the ferro-electric hysteresis loop of Rochelle Salt, but recently gained new attention after being applied to super-junction (SJ) Silicon (Si) MOSFETs [12], where the first evidences of C_{oss}-losses were observed. In this ST experiment, the MOSFET is kept permanently off and a sinusoidal voltage waveform is applied across its drain and source terminals, i.e. to C_{oss}. The hysteresis in the voltage-charge plane, observed during the charging and discharging processes of C_{oss}, is then providing a direct measure of the energy lost in a full charging/discharging cycle.

The underlying loss mechanism can be understood by analyzing the dynamics of charge transport within the p- and n-columns characterizing the SJ structure highlighted in **Fig. 1 (a)** [13]. During the charging process of C_{oss}, i.e. the turn-off transition of a SJ device, the space charge region expands around the surface of the blocking pn-junction formed by the deep p-columns, hence reaching far into the active area of the device. If stranded charges are left within the p-columns during the depletion, they can no longer flow as majority carriers, thus creating losses.

Since this loss mechanism is largely associated with stranded charges [13], losses can only occur during the depletion process of the p-columns. The sharp variation of C_{oss} at around $50\,\mathrm{V}$, typical for SJ devices, indicates that the depletion process is fully completed around this voltage. Later technology nodes (with lower area-specific on-state resistance) often achieve an even earlier, i.e. at lower voltages, depletion of the p- and n-column structure. Generally, the design of the SJ structure, e.g. in terms of doping concentration, and the technology considered for its realization have a significant influence on the formation of stranded charges [13]. **Fig. 1 (b)** shows, as an example, a cross-section of a SJ structure created by multiple epitaxy steps and subsequent implantation of p-dopants. As this type of technology creates locally strongly varying doping concentrations in both p- and n-regions, special care is taken to ensure a seamless depletion of the p-columns. It can be concluded that the results obtained applying the ST method to SJ devices [12] provided a physical understanding and a solid basis for the reduction of the C_{oss}-losses and/or of the soft-switching losses observed in SJ Si MOSFETs [7].

Differently from SJ devices, GaN-on-Si HEMTs feature symmetric C_{oss} charging and discharging processes and have an entirely distinct device structure, i.e. dopant charges are practically not present. Hence, a different loss mechanism, investigated in this work, must be at the origin of the observed $\mathrm{d}v/\mathrm{d}t$ dependent C_{oss}-losses [10].

Conventional ST measurement setups can achieve values of $\mathrm{d}v/\mathrm{d}t$ typical for the operation of GaN devices only when high frequencies, in the range of tens of MHz, are considered. Moreover, sinusoidal voltage waveforms, common in the ST method, are generally not representative of the operating conditions of a device in a switching circuit. Additionally, several motivations discussed in [14] discourage the usage of any electric measurement method to characterize soft-switching losses, especially when high switching speeds, i.e. $\mathrm{d}v/\mathrm{d}t$, are involved, mainly because of their limited accuracy. Given the similarity between soft-switching losses and C_{oss}-losses, for the above mentioned reasons, calorimetric measurement methods [7], [14], [15] should be preferred to electric measurement methods [16] and to the ST method.

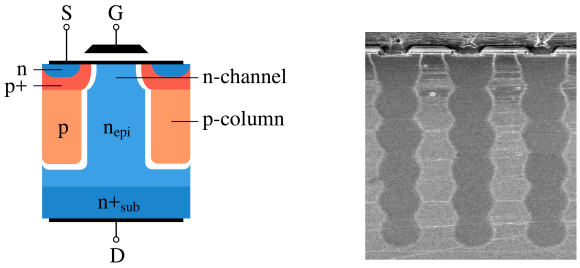


Fig. 1: Cross-section of a SJ Si MOSFET highlighting (a) the different doping concentrations and the characteristic 3D structure of p- and n-columns and (b) the inhomogeneity of the doping profiles as a results of the multi-epitaxy technology and subsequent implantation of p-dopants.

In [9], a calorimetric measurement method is proposed to characterize C_{oss}-losses in GaN transistors. In particular, in order to isolate C_{oss}-losses from other sources of loss, high $\mathrm{d}v/\mathrm{d}t$ voltage waveforms are generated across the C_{oss} of several permanently turned off transistors. Hence, the steady-state temperature of each Device-Under-Test (DUT) is measured and the occurring losses are estimated by means of the known thermal resistances of the system. The mentioned voltage waveform is generated by a switching circuit placed physically very close to the DUT, i.e. avoiding that parasitic elements, as otherwise introduced by an electrically long connection, could distort the signal and compromise the measurements. However, this inevitably leads to a measurement setup where self and mutual (between the DUT and the exciting circuit) thermal resistances are in the same order of magnitude. Since the losses occurring in the DUT are only a small share of the total losses occurring in the overall setup, it can be shown that a small error in the temperature measurement, and/or in the estimation of the thermal resistances, can cause a significant error in the measurement result [10].

At the contrary, in the setup presented in [14], the DUT is thermally well isolated from the exciting half-bridge, but a significant parasitic inductance is introduced by their connection. However, the voltages at stake (around $7\,\mathrm{kV}$) are significantly higher than the ones characterizing GaN transistors (up to $600\,\mathrm{V}$) and allow to neglect voltage distortions, e.g. oscillations, with amplitudes up to several hundreds of volts. A novel approach, ideally combining the advantages of both [14] and [10], is developed along this paper to accurately measure C_{oss}-losses occurring in GaN-on-Si HEMTs.

Finally, as stated in [10], it was impossible, up to now, to

address the root cause of the observed C_{oss}-losses in GaN devices mainly because the "detailed device constructions are proprietary to the device manufacturers", which prevents a clear understanding of the loss mechanism. For this reason, with the aim to remedy the C_{oss}-losses observed in GaN-on-Si HEMTs, the insight of the semiconductors manufacturers is considered fundamental. Accordingly, it is preferred to focus on a single transistor, of which a variety of different prototypes and detailed information are available through the manufacturer itself, rather than characterizing many. Because of an on-going research collaboration, the choice is guided towards the IGT60R070D1 [17] *CoolGaN*™ enhancement-mode GaN power transistor from *Infineon Technologies*.

In Section II of this manuscript, the setup initially considered to characterize the soft-switching losses of the analyzed GaN-on-Si HEMT is described from the electrical and thermal point of view, whereas in Section III the results of the soft-switching loss measurements are presented. In Section IV, a novel measurement setup, enabling the isolation of the C_{oss}-losses, is illustrated and the results of the relative measurements are discussed. Section V offers a detailed description of the internal structure of the considered transistor, allowing to speculate on the cause of the measured losses. Afterwards, in Section VI, a novel measurement procedure, aiming to identify the region of the transistor where the losses are originated, is described. The acquired knowledge facilitates the design of an enhanced GaN-on-Si HEMT which, as expected and confirmed in Section VII, does not exhibit any C_{oss}-losses nor dynamic $R_{ds,on}$ phenomena. Section VIII concludes the work summarizing the achievements.

II. Calorimetric Soft-Switching Loss Measurements

The results of the soft-switching loss measurements relative to a GaN-on-Si HEMT presented in [7] are significantly higher than expected according to the device simulations performed by the semiconductors manufacturer itself. With the aim of investigating the possible reasons causing this discrepancy, e.g. an unexpected loss mechanism like the C_{oss}-losses, a novel calorimetric measurement setup is designed and new experimental measurements are performed in this work. The DUT is a commercial *CoolGaN*™ enhancement-mode GaN power transistor IGT60R070D1 from *Infineon Technologies* [17] with the characteristics listed in **Table I**.
In this section, the measurement setup, the modified measurement procedure and the improvements to enhance the measurement accuracy (with respect to [7]) are first described; afterwards, the obtained measurement results are presented and discussed.

A. Description of the Measurement Circuit

From the electrical point of view, the considered measurement setup essentially consists of the DC-source V_{dc}, the input filter L_{dc}-C_{dc}, the switching half-bridge T_1-T_2 (T_1 and T_2 are, herein, the DUT) and the output inductor L_{load} connected from the switching-node of the half-bridge to the mid-point of the split DC-link, as shown in **Fig. 2**. $L_{dc,h\text{-}l}$ have the only purpose of protecting the DC-source from high frequency current harmonics. As also visible in **Fig. 3**, C_{dc} is formed by the parallel connection of $C_{dc,h}$ and $C_{dc,l}$ with $C_{dc,hf}$: $C_{dc,h\text{-}l}$ are energy storage film-capacitors [18] designed to maintain a constant DC-link voltage during operation of the half-bridge, whereas $C_{dc,hf}$ are low-parasitics multi-layer ceramic capacitors (MLCCs) [19] installed to improve the switching performance of the half-bridge (i.e. to minimize the commutation loop inductance, thus preventing over-voltage and voltage oscillations after high speed switching transitions [4]). The combination of L_{load} with $C_{dc,h\text{-}l}$ serves as well as output filter for the output voltage and output current, denominated v_{ds} and i_{load} respectively. Silicon-Carbide (SiC) Schottky diodes [20] D_1 and D_2, featuring a much lower threshold voltage compared to the reverse voltage of the DUT [17], are connected in parallel to T_1 and T_2 to reduce the conduction losses occurring during the dead-times t_{dt} of the half-bridge. C_{ext} are MLCCs

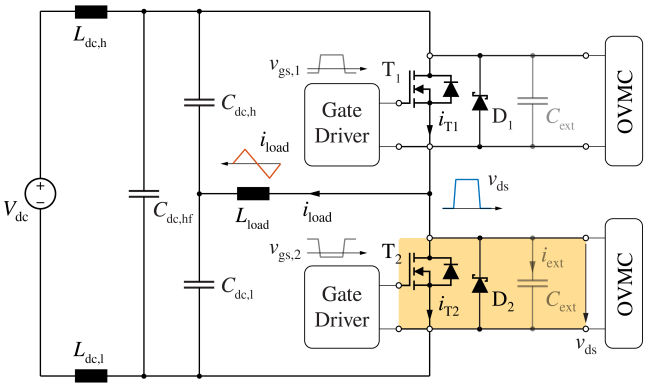


Fig. 2: Schematic of the realized soft-switching loss measurement setup consisting of the half-bridge formed by the two DUT T_1 and T_2. With the considered modulation scheme ($v_{gs,1}$ and $v_{gs,2}$), the illustrated waveforms of v_{ds} and i_{load} are obtained.

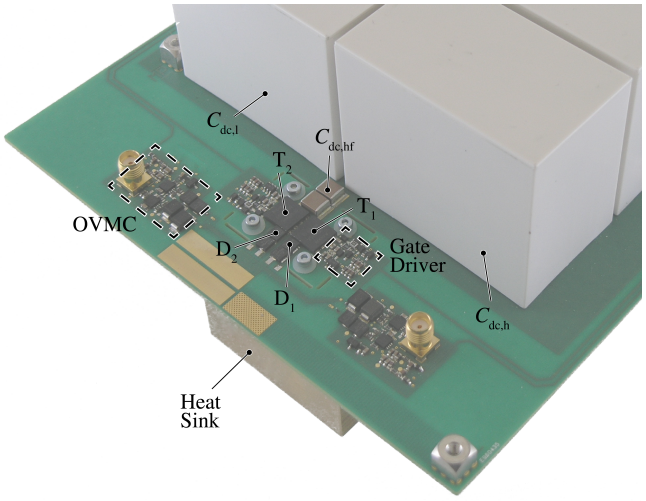


Fig. 3: Picture of the realized soft-switching loss measurement setup. The switching half-bridge formed by the two DUT T_1 and T_2, the anti-parallel diodes D_1 and D_2, the gate drivers, the OVMCs and the capacitors $C_{dc,h}$, $C_{dc,l}$ and $C_{dc,hf}$ are highlighted.

TABLE I: Main characteristics of the IGT60R070D1 [17] *CoolGaN™* enhancement-mode GaN power transistor from *Infineon Technologies*. Subscript Q and E in C_{oss} differentiate charge equivalent and energy equivalent capacitances.

$V_{ds,MAX}$	$I_{dc,MAX}$ @ 25 °C	$R_{ds,on}$ @ 25 °C	$R_{g,int}$	$C_{oss,Q} - C_{oss,E}$ (pF) @ 100 V	@ 200 V	@ 300 V	@ 400 V
600 V	31 A	55 mΩ	0.63 Ω	170 − 146	131 − 104	111 − 85	101 − 79

TABLE II: Circuit parameters and value of the components of the realized soft-switching loss measurement setup of **Fig. 2**.

	Description	Value	Note
V_{dc}	DC-source voltage	100 V... 400 V	
$L_{dc,h\text{-}l}$	DC-input inductor	1 mH	
$C_{dc,h\text{-}l}$	split DC-link capacitor	60 µF	[18]
$C_{dc,hf}$	DC-snubber capacitor	4.4 µF	[19]
L_{out}	output inductor	0.6 µH... 10 µH	
$T_{1\text{-}2}$	DUT		**Table I**
$D_{1\text{-}2}$	anti-parallel diodes		[20]
C_{ext}	external capacitor	0... 100 pF	[21]
f_{sw}	switching frequency	1 MHz	
I_{sw}	switched current	5 A... 20 A	

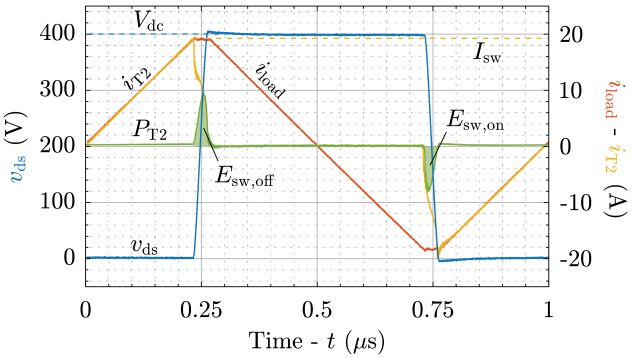


Fig. 4: Main waveforms characterizing the half-bridge of **Fig. 2** in soft-switching operation, i.e. v_{ds}, i_{load}, i_{T2} and P_{T2} for one switching period ($f_{sw} = 1$ MHz) in case $V_{dc} = 400$ V and $I_{sw} \approx 20$ A.

[21] necessary for measurement purposes, as described in Section III. The selected gate drivers and the On-State Voltage Measurement Circuits (the latter labeled OVMC in **Fig. 2** and **Fig. 3**) are thoroughly described in [3] and [22] respectively, and just adapted for the needs of the setup presented herein.

The modulation scheme adopted for the half-bridge simply consists of a 50 % duty-cycle PWM signal with a switching frequency of $f_{sw} = 1$ MHz (see $v_{gs,1}$ and $v_{gs,2}$ in **Fig. 2**). Thus, the switching-node voltage v_{ds} resembles a symmetric square-wave shaped waveform of amplitude V_{dc} and, accordingly, a symmetric (with respect to 0 A) triangular current waveform i_{load} of peak value I_{sw}

$$\frac{V_{dc}}{2} = L_{load}\frac{2I_{sw}}{1/2f_{sw}} \quad \longrightarrow \quad I_{sw} = \frac{V_{dc}}{8L_{load}f_{sw}} \tag{1}$$

appears at the output of the half-bridge. Hence, V_{dc} and $\pm I_{sw}$ correspond to the switched voltage and switched current, respectively. Further details of all circuit parameters and components are provided in **Table II**.

In order to vary the operating point of the half-bridge, V_{dc} is adjusted through the DC-source, f_{sw} is maintained constant and L_{load} is modified according to (1) to obtain the desired I_{sw}. **Fig. 4** shows the waveforms of v_{ds} and i_{load} for one switching period in case $V_{dc} = 400$ V and $I_{sw} \approx 20$ A. The current flowing in T_2 is additionally included in **Fig. 4** to highlight the conduction time of T_2 (corresponding to $v_{ds} \approx 0$ V).

When I_{sw} and the energy stored in L_{load} during the switching transitions of the half-bridge (i.e. $\approx L_{load}{I_{sw}^2}/2$) are sufficient to charge and/or discharge the equivalent capacitance of the switching-node ($\approx 2C_{oss}$) during t_{dt}, complete soft-switching operation is guaranteed and sensible soft-switching loss measurements can be carried out.

The fundamental principle of soft-switching operation can be visualized focusing on the waveform of the calculated instantaneous power P_{T2} at the terminals of T_2, also shown in **Fig. 4**. Depending on the direction of the slope of v_{ds}, C_{oss} of T_2 is charged (positive slope of v_{ds}, turn-off transition of T_2) or discharged (negative slope, turn-on) by i_{load}. Generally, i_{load} acts as a current source charging or discharging the parallel connection of C_{oss} of the two DUT. Consequently, a certain amount of energy (calculated as the area underlying P_{T2}) is stored $E_{sw,off}$ or released $E_{sw,on}$ e.g. in, or from, C_{oss} of T_2. As suggested by preceding measurements, this process causes losses and, in particular, the soft-switching losses E_{sw} can be defined as the difference between $E_{sw,off}$ and $|E_{sw,on}|$.

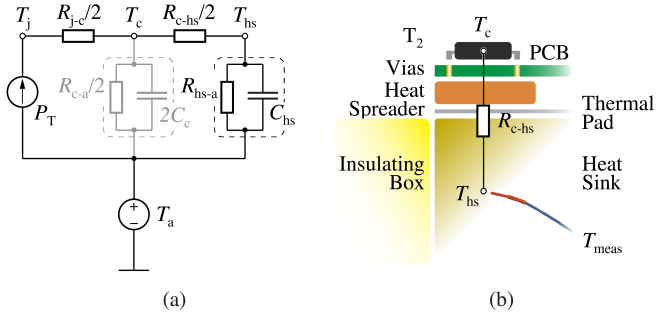
It is worth mentioning that the considered setup (see **Fig. 2**) features the advantage of emulating, for the DUT, the very same switching conditions occurring in a power converter operating in soft-switching. Hence, the results of these measurements are expected to be representative of the real switching performance, i.e. to provide accurate soft-switching loss data, useful for the multi-objective optimization of soft-switching power converters [3].

B. Description of the Calorimetric Loss Measurement Setup

In order to calorimetrically measure the losses occurring in the DUT forming the soft-switching half-bridge, i.e. $P_{T1} + P_{T2} \coloneqq P_T$, the Printed Circuit Board (PCB) where the DUT are installed is thermally coupled with a solid brass heat-sink whose temperature T_{hs} is recorded by means of a fiber optic thermometer [23]. If symmetry, both in terms of losses, i.e. $P_{T1} = P_{T2} = {P_T}/2$, and physical parameters, e.g. dimensions of the PCB, is assumed between T_1 and T_2, the thermal equivalent circuit of **Fig. 5 (a)**, with the parameters described in **Table III**, can be derived to model the measurement setup [7].

TABLE III: Value of the parameters of the thermal equivalent circuit of **Fig. 5 (a)**.

	Description	Value	Note
P_T	losses in the DUT	0 W... 30 W	
T_a	ambient temperature	20 °C... 25 °C	
$R_{j\text{-}c}$	junction-to-case	1.0 K/W	[17]
$R_{c\text{-}a}$	case-to-ambient	-	negligible [7]
$R_{c\text{-}hs}$	case-to-heat-sink	4.8 K/W	
$R_{hs\text{-}a}$	heat-sink-to-ambient	13 K/W	
C_c	case	-	negligible [7]
C_{hs}	heat-sink	269 J/K	



(a) (b)

Fig. 5: (a) Thermal equivalent circuit of the calorimetric loss measurement setup and (b) vertical stack of the elements forming $R_{c\text{-}hs}$.

Particular attention must be paid to $R_{j\text{-}c}+R_{c\text{-}hs} := R_{j\text{-}hs}$, i.e. the thermal resistance from the junction of a DUT, through its case and to the heat-sink, since, neglecting the contribution of the case, it defines the junction temperature $T_j = P_T R_{j\text{-}hs}/2 + T_{hs}$ reached in steady-state. Thus, once T_{hs} is fixed, $R_{j\text{-}hs}$ limits the maximum value of losses allowed in the setup $P_{T,MAX}$ not to exceed the maximum tolerable junction temperature $T_{j,MAX} = 150\,°C$ indicated in the datasheet [17]. $R_{j\text{-}c}$ is fixed by the internal structure of the DUT, hence $R_{c\text{-}hs}$ represents the only design variable and must be minimized.

In addition to a good thermal coupling between the DUT and the heat-sink, i.e. a minimized $R_{j\text{-}c}$, also electric insulation is necessary between them and a trade-off must be found. In fact, the DUT are bottom-cooled and their lead-frames are connected externally to the common heat-sink through PCB vias and internally to the respective source terminals, i.e. they are at different potentials during switching operation. Since the heat-sink is conductive, an insulating material must be inserted between the PCB and the heat-sink to prevent a short-circuit. This feature is intrinsic in the Insulated Metal Substrate (IMS) board considered in [7], but for the reasons discussed in Section II-C, a conventional PCB is preferred in this study. A layer of the best-in-class thermal-pad [24] introduces an excessive $R_{c\text{-}hs}$ if the vertical heat-flow from the DUT to the heat-sink is constrained in the area defined by the lead-frame of the DUT. For this reason, two copper heat-spreaders, i.e. one per DUT, are introduced in the vertical stack between the PCB and the thermal-pad, as illustrated in **Fig. 5 (b)** for the case of T_2. The high thermal conductivity of copper allows the spreading of the heat-flow in the horizontal plane and the bottleneck introduced by the pad is alleviated due to the wider surface. An overall $R_{c\text{-}hs} = 4.8\,K/W$ is finally obtained, successfully limiting $T_j - T_{hs}$ to, e.g., approximately 85 °C when $P_T = 30\,W = P_{T,MAX}$.

The derived thermal equivalent circuit of **Fig. 5 (a)** is characterized by two time constants: a fast one, associated with the cases of the DUT, and a slow one, associated with the common heat-sink. If in a first approximation only the latter is considered, the differential equation

$$P_T = C_{hs}\frac{dT_{hs}(t)}{dt} + \frac{T_{hs}(t) - T_a}{R_{hs\text{-}a}}, \tag{2}$$

yields to

$$T_{hs}(t) = (T_0 - P_T R_{hs\text{-}a} - T_a)e^{-\frac{t}{R_{hs\text{-}a}C_{hs}}} + P_T R_{hs\text{-}a} + T_a, \tag{3}$$

which describes the evolution of T_{hs} ($T_{hs}(0) := T_0$) after a power step P_T is applied to the system (at $t = 0$). Equation (3) is of the type $y = 1 - e^{-|x|}$, with initial value T_0, steady-state value $P_T R_{hs\text{-}a} + T_a$ and several independent parameters. In particular, the ambient temperature T_a, which can be easily measured, $R_{hs\text{-}a}$ and C_{hs}, dependent on the geometry of the setup, i.e. mainly associated with the insulating box ($R_{hs\text{-}a}$) and the heat-sink (C_{hs}) shown in **Fig. 6**, and P_T, relative to the operating point.

In a first calibration phase, both DUT are turned on and operated as resistors. Thus, a known constant power P_T is injected via the DUT into the thermal system at known T_a while T_{hs} is recorded from 30 °C to 40 °C. For consistency among measurements, $T_{hs} = 30\,°C$ is always considered as measurement starting point. Repeating this procedure for several values of P_T yields to the set of curves T_{meas} illustrated in **Fig. 6**. Hence, the values of $R_{hs\text{-}a}$ and C_{hs}, best fitting T_{meas} according to a least-mean-square (LMS) regression performed on the model represented by (3), are extracted (see **Table III**). The satisfactory matching of the proposed model with the experimental data (also justifying the made assumptions) can be visualized in **Fig. 6** comparing T_{meas} (solid) with the set of curves T_{fit} (dashed) calculated inserting in (3) the measured P_T and T_a, and the identified LMS optima $R_{hs\text{-}a}$ and C_{hs}.

In a subsequent measurement phase, i.e. when the half-bridge formed by the DUT is operated in soft-switching, P_T is unknown but $R_{hs\text{-}a}$ and C_{hs} remain unchanged. Consequently, the LMS regression can now be applied to estimate P_T from a new set of curves T_{meas}.

It is worth noticing that T_{meas} associated with the highest P_T, e.g. 20 W, are practically linear (i.e. the influence of $R_{hs\text{-}a}$ is not yet visible), which allows to simplify (2) to

$$P_T = C_{hs}\frac{dT_{hs}(t)}{dt}. \tag{4}$$

In this case, once C_{hs} is known, P_T is determined with good approximation by the ratio $\Delta T_{hs}/\Delta t$, where ΔT_{hs} indicates the temperature excursion within one measurement and Δt its time duration. Since typical resolution of the temperature and time

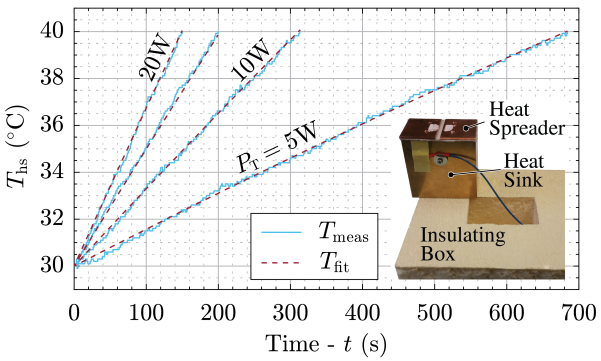


Fig. 6: T_{meas} (solid) and T_{fit} (dashed) for different P_T. The agreement of the model (see **Fig. 5 (a)** and **Table III**) with the experimental data is satisfactory.

measurements are 0.1 °C and 1 s respectively, $\Delta T_{hs} = 10\,°C$ and $\Delta t_{min} = 100\,s$ are imposed, limiting the quantization error to 1 % in both cases. To ensure $\Delta t \geq \Delta t_{min}$ when $P_T = P_{T,MAX}$, equation (4) is rearranged and an expression for the minimum feasible C_{hs} is obtained. This parameter also defines the minimum difference in terms of Δt between measurements of similar P_T, e.g. $\bar{P}_T$ and $\bar{P}_T + 10\,\%$.
In case P_T is significantly lower, the dynamic of T_{hs} is influenced also by $R_{hs\text{-}a}$. Hence, $R_{hs\text{-}a}$ should be maximized (e.g through an insulating box) to increase the sensitivity of T_{hs} with respect to P_T. It can still occur that T_{hs} does not reach 40 °C (never or not in reasonable time) for very low values of P_T; in this case, an alternative measurement target (different from $T_{hs} = 40\,°C$) can be defined. E.g. a measurement can be interrupted once, according to the derived model, a sufficient difference in terms of T_{hs} is guaranteed between two measurements of similar P_T, e.g. $\bar{P}_T$ and $\bar{P}_T + 10\,\%$.

C. Description of the Measurement Procedure

The subtractive calorimetric measurement method introduced in [7] is applied as well in this work. Accordingly, to isolate the switching losses P_{sw}, all other loss contributions, combined in P_{ext}, are identified, estimated (measured or calculated) and subtracted from the power P_{tot} resulting from the calorimetric measurement, i.e.

$$P_{sw} = P_{tot} - P_{ext}. \tag{5}$$

As discussed in [22], the accuracy of P_{sw} (σ_{Psw} is e.g. the worst-case uncertainty of P_{sw}) is influenced from the accuracy of both the calorimetric measurement itself and of the estimations defining P_{ext} (σ_{Pext}). However, intuitively (or as formally derived in [22]) the impact of σ_{Pext} on σ_{Psw} is reduced proportionally to P_{sw}/P_{ext}. To increase this ratio, P_{sw} is maximized keeping $f_{sw} = 1\,MHz$ and attention is paid to accurately estimate all the identified contributions to P_{ext}, minimizing σ_{Pext}. In particular:

- The OVMC developed in [22] is connected to each DUT to measure the real-time value of their on-state resistance $R_{ds,on}$ and accurately calculate the occurring conduction losses P_{cond}, major contributors to P_{ext}. The results of these measurements are summarized in **Fig. 7**, where the measured $R_{ds,on}$ in soft-switching operation (solid) are compared with the values measured during calibration (dashed) and with the nominal values reported in the datasheet of the DUT [17] (dotted) as function of the measured (or estimated from T_j in the case of the datasheet) P_{tot} and at $T_{hs} = 30\,°C$. It is worth mentioning that, differently from other GaN devices analyzed in [22], these DUT do not feature any dynamic $R_{ds,on}$ phenomena [6] and there is a very good agreement between the measured and nominal $R_{ds,on}$.
- Conduction losses occur in D_1 and D_2 during t_{dt} and are calculated and subtracted. In each operating point, t_{dt} is adjusted to ensure the completion of the switching transition while minimizing the diode conduction time with the maximum resolution allowed by the digital control circuit. It should be noticed that, since the time resolution on setting t_{dt} is limited, and the safety margin with respect to the completion of the switching transition can be assumed constant, further increasing f_{sw} to increase P_{sw} inevitably leads to a higher impact of this loss contribution to the final measurement accuracy, because the product $t_{dt} f_{sw}$ increases.
- The equivalent series resistances (ESRs) of $C_{dc,h\text{-}l}$ and $C_{dc,hf}$ cause additional conduction losses during switching operation. It is challenging to measure the current flowing, e.g. in $C_{dc,hf}$, denominated $i_{Cdc,hf}$, without affecting the commutation loop inductance of the half-bridge formed by the DUT [4]. Therefore, the parasitic elements of the circuit are measured and/or estimated and comprehensive simulations are performed to determine $i_{Cdc,hf}$. **Fig. 8** shows, as an example, the Fourier transform of the simulated $i_{Cdc,hf}$ (solid) in combination with the value of ESR of $C_{dc,hf}$ specified in its datasheet [19] (dashed). This information allows to calculate the occurring losses in $C_{dc,hf}$ and a similar procedure is followed also for $C_{dc,h\text{-}l}$ and C_{ext}.
  The losses in the PCB dielectric are calculated not to have any significant impact on P_{tot} and are therefore neglected. This is achieved minimizing the parasitic capacitance of the PCB in the design phase, as well of importance to maximize the achievable dv/dt for a given I_{sw}. Similarly, the losses in any other parasitic capacitor are neglected too.
- In a soft turn-off switching transition of T_2, it could happen that v_{ds} rises before the channel of T_2 is completely opened (the opposite holds for T_1). The time overlap of non-zero voltage and current creates V-I overlap losses. It is impossible to separate the current flowing in the channel of T_2 from the one flowing in its C_{oss} by means of measurements. However, the existence of V-I overlap losses is excluded in this case, since $v_{gs,2}$ is measured to reach the specified threshold, i.e. $i_{T2} = 0\,A$, before v_{ds} rises (given the presence of C_{oss}). To support this thesis, a circuit model is developed and simulations based on the measured waveforms are performed; finally, the V-I overlap losses are quantitatively evaluated and, although negligible, subtracted.
- The losses occurring in the auxiliary circuits, e.g. the gate drivers and the OVMCs, are estimated operating them individually and measuring their influence on T_{hs}.

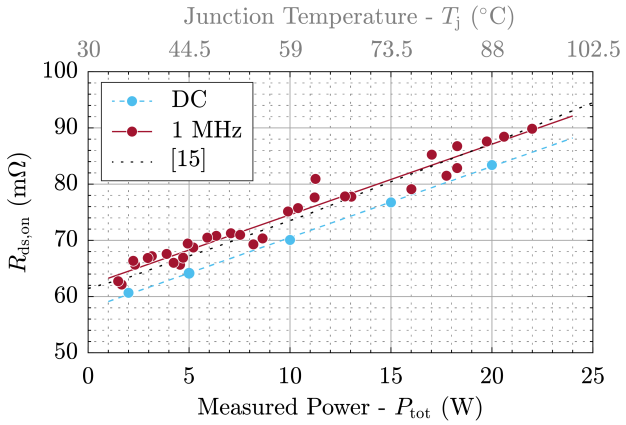


Fig. 7: Measured $R_{ds,on}$ in soft-switching operation (solid) compared with the values measured during calibration (dashed) and with the nominal values reported in the datasheet of the DUT [17] (dotted) as function of P_{tot} and at $T_{hs} = 30\,°C$. T_j, obtained in first approximation as $T_{hs} + P_{tot}(R_{j\text{-}c}+R_{c\text{-}hs})/2$, is additionally indicated to facilitate the comparison with the corresponding plot reported in [17].

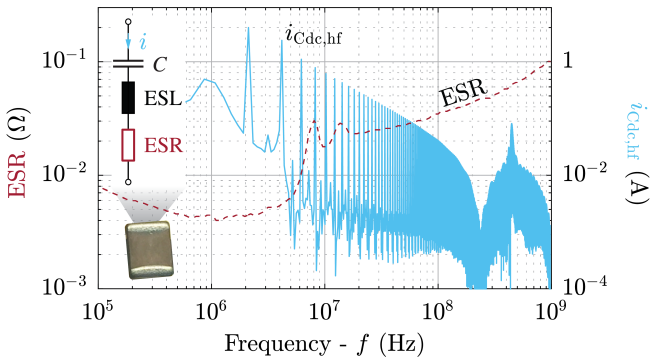


Fig. 8: Fourier transform of the simulated $i_{Cdc,hf}$ (solid) and nominal ESR of $C_{dc,hf}$ [19] (dashed) considered to calculate the losses occurring in $C_{dc,hf}$ during switching operation.

All the listed contributions to P_{ext} (except for P_{cond}) are generally below 20 % of P_{sw}, i.e. even a significant error on their estimation is ideally attenuated up to five times once P_{sw} is calculated [22]. However, to improve the measurement accuracy it is important to estimate them carefully, especially benefiting of the implemented OVMCs for the calculation of P_{cond} [22], since $P_{sw}/P_{cond} \approx 0.5$ for the highest values of I_{sw}.

III. Soft-Switching Loss Measurement Results

Considering the measurement setup and procedure described in the previous section, P_{sw} is measured in different operating conditions of the DUT, i.e. with V_{dc} ranging from 100 V to 400 V (in 100 V steps) and I_{sw} from 5 A to 20 A (in 5 A steps). Assuming symmetry, the resulting P_{sw} of the half-bridge are halved to obtain the losses of a single DUT and divided by f_{sw} to provide data independent of frequency. The obtained $E_{sw} = P_{sw}/2f_{sw}$ are plotted as function of I_{sw} in **Fig. 9** (dots) for different V_{dc}. The dependency of E_{sw} on V_{dc} and I_{sw} is evident. Moreover, since the data relative to a single V_{dc} are aligned, linear interpolations are performed and shown (solid). The linear model fits the measurement results except for the

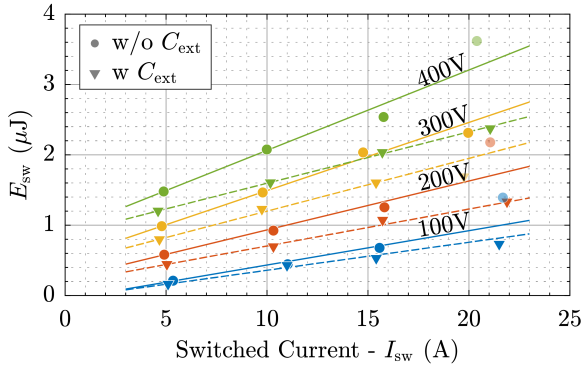


Fig. 9: E_{sw} as function of I_{sw} (5 A… 20 A) for different V_{dc} (100 V… 400 V). E_{sw} without (dots) and with (triangles) C_{ext} are compared.

case of $I_{sw} = 20\,A$ where, mainly because of P_{cond}, σ_{Psw} is more significantly affected from σ_{Pext}.

Overall, E_{sw} summarized in **Fig. 9** are lower than their counterpart reported in [7], potentially because of the following reasons:

- The DUT belong to a new generation of *CoolGaN*™ which features 30 % reduced C_{oss} and improved switching performance compared to the prototype samples considered in [7].
- The enhancements brought to the measurement procedure, as described in Section II-C, significantly improve σ_{Pext} and therefore σ_{Psw}. Moreover, carefully characterizing (and subtracting) all the contributions to P_{ext}, finally ends up reducing P_{sw} according to (5).
- The measurement setup considered in [7] is based on an IMS board which guarantees good thermal coupling and electric isolation between the DUT and the heat-sink without additional effort. However, only a single layer is available on an IMS board to route the interconnections and place the components, thus, only sub-optimal designs in terms of parasitic capacitances, commutation loop and gate loop inductances can be realized, inevitably worsening the switching performance of the half-bridge formed by the DUT. To overcome this, a PCB is preferred to an IMS board in this setup, since only by introducing the thermal-pad described in Section II-B, similar thermal performance are achieved (e.g. in terms of $R_{c\text{-}hs}$) and the same simplified (and convenient) thermal model remains valid.

To further investigate the linear dependency of E_{sw} with respect to I_{sw}, the same measurements are repeated after connecting $C_{ext} = 100\,pF$ in parallel to each DUT (see **Fig. 2**). The resulting E_{sw} are also indicated in **Fig. 9** (triangles), accompanied by linear interpolating curves (dashed).

For the same V_{dc} and I_{sw}, E_{sw} in case of $C_{ext} = 100\,pF$ (triangles) is consistently lower than E_{sw} measured without C_{ext} (dots). Since the presence of C_{ext} reduces the fraction of I_{sw} flowing through C_{oss}, i.e. it reduces the switched voltage slope dv_{ds}/dt for the same I_{sw}, it is interesting to compare these results as function of dv_{ds}/dt as in **Fig. 10**. dv_{ds}/dt defining the x-axis is calculated measuring the time taken from v_{ds} to rise (or fall) from $0.1V_{dc}$ to $0.9V_{dc}$ (or vice versa). Depending

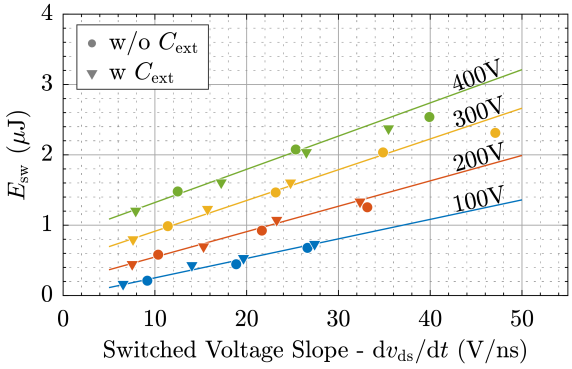


Fig. 10: E_{sw} as function of $^{dv_{ds}}/_{dt}$ obtained with different I_{sw} (5 A... 20 A) for different V_{dc} (100 V... 400 V). E_{sw} without (dots) and with (triangles) C_{ext} follow the same interpolation lines (solid).

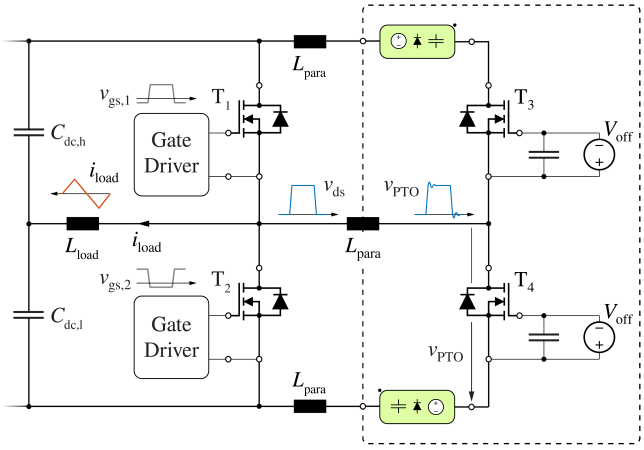


Fig. 11: Schematic of the realized measurement setup consisting of the half-bridge formed by the PTO DUT T_3 and T_4 (dashed box) connected in parallel to the switching half-bridge T_1-T_2. T_1 and T_2 generate high $^{dv}/_{dt}$ square-wave voltage waveforms across the drain and source terminals of T_3 and T_4.

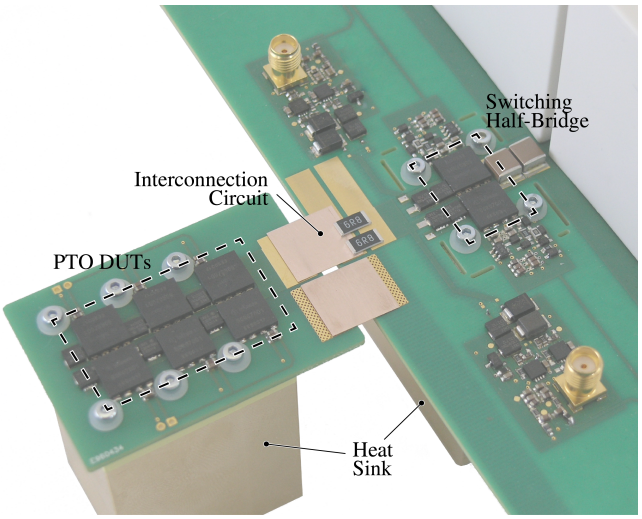


Fig. 12: Picture of the realized measurement setup for the PTO DUT. On the right hand-side PCB, the switching half-bridge is highlighted. On the left hand-side PCB, the half-bridge formed by the PTO DUT separated by the interconnection circuit from the switching half-bridge is visible (see **Fig. 13**).

on the presence of C_{ext}, different $^{dv_{ds}}/_{dt}$ are measured for the same I_{sw}, however, all the measured points (dots and triangles) surprisingly align, for each V_{dc}, along the same linear interpolating curve (solid) for all the considered range of $^{dv_{ds}}/_{dt}$, i.e. from $6\,^{V}/_{ns}$ to $47\,^{V}/_{ns}$. It can be concluded that E_{sw} is not only proportional to I_{sw}, but, more precisely, to the current flowing in C_{oss} (or to $^{dv_{ds}}/_{dt}$ [10]), exactly as if its charging/discharging process would be lossy.

IV. Measurements of Permanently Turned Off DUT

To confirm the evidence of a lossy C_{oss} charging/discharging process resulting from Section III, the setup described in Section II-A is now modified introducing a second half-bridge T_3-T_4 connected in parallel to the switching half-bridge T_1-T_2, as shown in **Fig. 11** (dashed box). T_3 and T_4 (i.e. the DUT) are Permanently Turned Off (PTO) applying a negative DC-voltage $-V_{off}$ between their gate and source terminals, while the switching half-bridge is operated as described in Section II-A. Hence, high $^{dv}/_{dt}$ square-wave voltage waveforms are generated across the drain and source terminals of the PTO DUT, isolating the loss mechanism associated with C_{oss} from all the other sources of loss contributing to P_{ext} (see Section II-C). This measurement setup for the PTO DUT, featuring voltage waveforms representative of real operating conditions (see Section II-A), is preferred over others where sinusoidal voltage excitations are considered (see Section I).

A. Description of the Measurement Setup and Procedure

In order to calorimetrically measure the occurring losses in the PTO DUT $P_{tot,PTO}$ following the procedure described in Section II-B, the half-bridge formed by the PTO DUT is mounted on a separate heat-sink constituting a second thermal system, as shown in **Fig. 12**. This heat-sink is optimized for the new range of lower losses, since e.g. $P_{cond,PTO} = 0\,W$ for definition of PTO, and the whole thermal system is calibrated accordingly (see Section II-B).

To maximize the measurement accuracy, the influence of P_{tot} on $P_{tot,PTO}$ should be minimized, i.e. ideally no thermal coupling between the two half-bridges is desired. For this reason, the possibility of attaching the half-bridge formed by the PTO DUT on the same heat-sink of the switching half-bridge is discarded. Nevertheless, the electrical connection between the half-bridges is necessary for the correct operation of the setup, i.e. their thermal coupling can, in reality, only be minimized. Long and narrow interconnections between the half-bridges would surely limit their thermal coupling, but as well introduce significant parasitic inductances L_{para}. The resonant network formed by L_{para} in combination with C_{oss} of the PTO DUT (characteristic impedance $Z_{rn} \propto \sqrt{L_{para}/C_{oss}}$) is excited by v_{ds}. Hence, the voltage measured across T_4, labeled v_{PTO}, does not coincide with v_{ds} as desired, but is partially distorted by a super-imposed voltage oscillation, as visible in **Fig. 11**. Since C_{oss} is fixed from the PTO DUT, L_{para} defines a trade-off between distortion of v_{ds} and thermal coupling, and a compromise must be achieved.

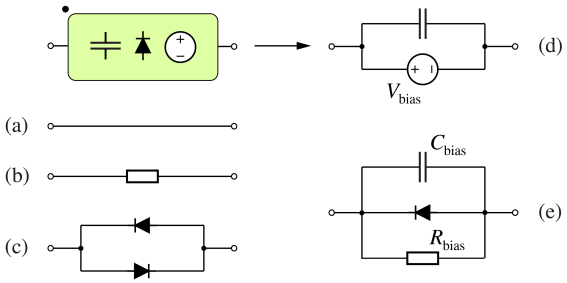


Fig. 13: Different solutions to interconnect the half-bridges; (d) is preferred since properly adjusting V_{bias}, the reverse conduction of both PTO DUT is prevented.

Several solutions tested to overcome the above-mentioned issue, essentially consisting of different circuits suitable for the interconnection of the two half-bridges, are proposed in **Fig. 13**. If no precaution would be taken (i.e. solution (a) would be adopted) the voltage oscillation present on v_{PTO} would be clamped by the PTO DUT in reverse conduction, not only violating the assumption of PTO, but as well introducing additional losses which would need to be estimated and subtracted. If a resistor (b) of sufficient value, e.g. $2Z_{rn}$, or diodes (c) would be connected as shown in **Fig. 12**, the effects of the voltage oscillation could be significantly reduced, but new sources of loss would be again introduced. An alternative solution, similar to (c), is therefore proposed herein.

Properly adjusting the voltage V_{bias} of the voltage source (d), each PTO DUT can be biased as highlighted in **Fig. 14** and summarized in **Table IV** for the case of T_2 and T_4. If V_{bias} is selected at least equal to the amplitude of the voltage ringing characterizing v_{PTO} after a turn-on transition of T_2 (dashed), $v_{PTO} \geq 0\,V$, i.e. the reverse conduction of T_4 is prevented. Moreover, since no passive element is present in the circuit, (d) is ideally loss-less.

Although (d) is effective, two potentially negative aspects associated with its implementation have to be mentioned:

- During a turn-off transition of T_2, while v_{ds} changes from $0\,V$ to V_{dc}, v_{PTO} changes from V_{bias} to $V_{dc}+V_{bias}$, i.e. v_{PTO} is unnecessarily shifted of V_{bias} also during a turn-off transition of T_2. This can be solved replacing V_{bias} with an opportunely modulated switched voltage source v_{bias} ($v_{bias} = 0\,V$ before T_2 turns off and $v_{bias} = V_{bias}$ before T_2 turns on) or with the passive network (e). In (e), C_{bias} is adjusted to build up the desired V_{bias} through the capacitive current originated by a turn-on transition of T_2 and R_{bias} to discharge C_{bias} before the subsequent turn-off transition.
- Since (d) itself does neither limit nor attenuate the voltage oscillation present on v_{PTO}, a combination of (d) with (b) or (c) can be additionally considered.

B. Discussion on the Measurement Results

$P_{tot,PTO}$ is measured with the described setup featuring (d) and for the same operating points considered in Section III. Afterwards, E_{PTO} is calculated from $P_{tot,PTO}$ and the obtained results are provided in **Fig. 15** (squares) as function of $^{dv_{PTO}}/_{dt}$. Only

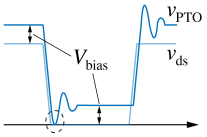


Fig. 14: Simplified v_{ds} and v_{PTO} waveforms highlighting the effect of V_{bias} in (d).

TABLE IV: Nominal v_{ds} and v_{PTO} in (d).

T_2 state	on	off
v_{ds} (V)	0	V_{dc}
v_{PTO} (V)	V_{bias}	$V_{dc}+V_{bias}$

two measurement points are recorded for $V_{dc} = 100\,V$, since, for higher $^{dv_{PTO}}/_{dt}$, the required V_{bias} (proportional to $^{dv_{PTO}}/_{dt}$ exciting the resonant circuit) becomes an excessive fraction of V_{dc}. Additionally, linear interpolating curves (dashed) are reported. The range of $^{dv_{PTO}}/_{dt}$ (x-axis) roughly corresponds to the one of $^{dv_{ds}}/_{dt}$ in the measurements performed with $C_{ext} = 100\,pF$, since each PTO DUT has the same impact as C_{ext} on the transistors forming the switching half-bridge (and $C_{ext} \approx C_{oss}$). In fact, in order to avoid an excessive reduction of $^{dv_{PTO}}/_{dt}$, only a single PTO DUT per side forms the half-bridge T_3-T_4, as visible in the thermal snippet of **Fig. 15**. More than one PTO DUT connected in parallel would increase the sensitivity of the measurements, but also further reduce the occurring $^{dv_{PTO}}/_{dt}$, unless I_{sw} is not increased. The result of the linear interpolation of E_{sw} for $V_{dc} = 400\,V$ (see Section III) is additionally reported in **Fig. 15** (solid) as function of $^{dv_{ds}}/_{dt}$ to compare the two experiments.

Although E_{PTO} is lower than E_{sw} in the same operating conditions (this is consistent for all V_{dc}, cf. **Fig. 10**), a significant fraction of E_{sw}, generally from 50 % (from 70 % in the case of $V_{dc} = 400\,V$) to 90 %, is still observed in the PTO DUT. It can be concluded that the C_{oss} charging/discharging process itself has a major impact on the losses occurring in soft-switching operation. These results are in good agreement with the findings presented in [10], where comparable E_{PTO} (especially if normalized with respect to C_{oss}) are measured for the same V_{dc} and $^{dv_{PTO}}/_{dt}$ on a similar PTO DUT.

The following causes can explain the discrepancy between E_{sw} and E_{PTO}:

- Additional loss mechanisms related to the conduction of i_{load}

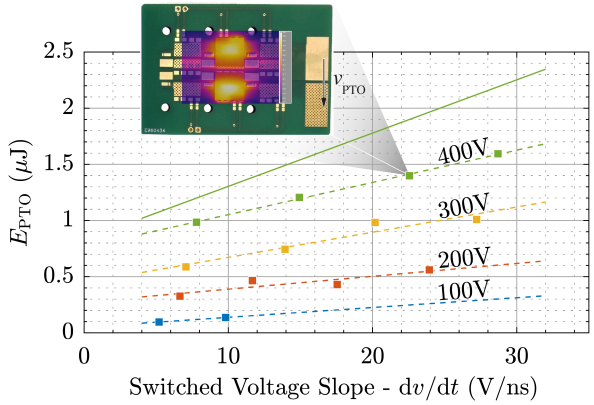


Fig. 15: E_{PTO} as function of $^{dv_{PTO}}/_{dt}$ obtained with different I_{sw} (5 A... 20 A) for different V_{dc} (100 V... 400 V). E_{PTO} (dashed) constitutes from 70 % to 90 % of E_{sw} (solid) in the case of $V_{dc} = 400\,V$.

may occur in switching operation, whereas not being present in the PTO DUT.

- σ_{Pext} associated with the switching half-bridge, e.g. in the case of the V-I overlap losses, is limited. In fact, it relies on circuit simulations which potentially underestimate their impact, finally resulting in overestimating E_{sw} according to (5).
- As a consequence of the selected interconnection circuit (d), $v_{\text{PTO}} \approx v_{\text{ds}} + V_{\text{bias}}$ during a turn-off transition of T_2. Even if the amplitude of both v_{PTO} and v_{ds} square-wave shaped waveforms is V_{dc} (excluding the voltage oscillation), the non-linearity of C_{oss}, in combination with the voltage offset V_{bias}, might be to a large extent responsible for the loss mismatch. In fact, C_{oss} is significantly larger at low voltage, e.g. $C_{\text{oss}}(0\,\text{V}) \approx 3C_{\text{oss}}(30\,\text{V})$ [17], i.e. in the voltage range not covered by v_{PTO}. Thus, since the investigated loss mechanism involves the charging/discharging process of C_{oss}, it is legit to expect that the voltage range characterized by the highest amount of charge has the highest impact on E_{PTO}.
  The previous assumption is confirmed with two experiments. First, repeating the measurements for different V_{bias} (higher than the limit defined by the voltage ringing), it results that E_{PTO} decreases inversely proportional to V_{bias} for the same V_{dc}. Second, considering the interconnection circuit (e), E_{PTO} approaches E_{sw}. However, (e) requires to adjust C_{bias} in each operating point and the overall effort of the measurement procedure significantly increases. Employing (d), this issue is only partially mitigated in the turn-on transitions of T_2, adjusting V_{bias} such that v_{PTO} reaches 0 V (including the voltage oscillation). Nevertheless, (d) is still considered the best solution among the ones shown in **Fig. 13**.
  At the expense of a modified $\mathrm{d}v_{\text{PTO}}/\mathrm{d}t$, a switching half-bridge generating a sinusoidal, rather than a square-wave, v_{ds} voltage waveform could as well alleviate the issue.
- The voltage oscillation visible in v_{PTO} is well damped after every switching transition from the resistance of the connections between the half-bridges (e.g. PCB copper tracks and interconnection circuit), i.e. a second source of loss contributes to E_{PTO}. To compensate for this, the energy stored in the resonant network L_{para}-C_{oss} is estimated from C_{oss} and from the amplitude of the first peak of the voltage oscillation present on v_{PTO}, and subtracted from $P_{\text{tot,PTO}}$. This implicitly considers the worst-case assumption that all the energy stored in L_{para}-C_{oss} is dissipated in the PTO thermal system, which ultimately leads to a slight reduction of E_{PTO}.

To better understand the origin of E_{PTO}, a simplified loss model can be derived. As anticipated in Section II-A, each soft-switching transition can be described with an equivalent circuit formed by a current source I_{sw} charging/discharging the parallel connection of the C_{oss} from 0 V to V_{dc} in a time $\bar{t} = V_{\text{dc}}(\mathrm{d}v/\mathrm{d}t)^{-1}$. If a certain R_{oss} is assumed to justify the evidence of losses, the occurring E_{PTO} would result as

$$E_{\text{PTO,R}} \approx R_{\text{oss}} \left(\frac{I_{\text{sw}}}{2}\right)^2 \bar{t} = R_{\text{oss}} C_{\text{oss,Q}} V_{\text{dc}} \frac{I_{\text{sw}}}{2} \tag{6}$$

(neglecting any other capacitance present in the circuit). Equation (6) is calculated computing the energy dissipated by a resistor R_{oss} when a lossy capacitor $C_{\text{oss,Q}}$ (calculated at V_{dc}) is charged from 0 V to V_{dc} by a current source $I_{\text{sw}}/2$. This model can explain the linear trend of E_{PTO} with respect to I_{sw} (or $\mathrm{d}v_{\text{PTO}}/\mathrm{d}t$) and the increasing slope of the interpolating curves with increasing V_{dc}. It must be noticed that $C_{\text{oss,Q}}$ decreases non-linearly with increasing V_{dc} as described in **Table I**, thus partially compensating the increase of the slopes. Additionally, with a properly adjusted value of R_{oss}, this model can as well reproduce the hysteresis curves of C_{oss} measured in [10].
On the other hand, unfortunately, this model is too simplistic to give any insight on the non-zero intercepts of the interpolating curves (dashed), which can be visualized extrapolating them towards $\mathrm{d}v_{\text{PTO}}/\mathrm{d}t = 0\,\text{V/ns}$. It is obvious that E_{PTO} should be 0 J at this point, but this is even not of any practical interest, since outside the range of typical $\mathrm{d}v/\mathrm{d}t$ of soft-switching converters. Moreover, it is interesting to notice that, if E_{PTO} is normalized with respect to the energy stored in C_{oss} (i.e. $C_{\text{oss,E}} V_{\text{dc}}^2/2$), the dependency of E_{PTO} on V_{dc} practically disappears.
Nevertheless, the proof of a lossy C_{oss} charging/discharging process is once more confirmed and an in depth analysis of the DUT structure is conducted in the next section to investigate the physical reasons, possibly explaining the highlighted phenomena.

V. Hypotheses on the Origin of the C_{oss}-Losses

Each terminal of the DUT excited by a high $\mathrm{d}v/\mathrm{d}t$ voltage waveform during every switching transition, namely source, drain and substrate, must be analyzed separately to identify potential loss mechanisms in the device structure, causing the observed C_{oss}-losses.
An equivalent circuit of the DUT, including the parasitic capacitors connecting the three mentioned terminals, is shown in **Fig. 16 (a)**. Additionally, comparing **Fig. 16 (a)** with the cross-section of the internal structure of the DUT illustrated in **Fig. 16 (b)**, the main structural components determining these capacitors can be visualized. The drain-source capacitor $C_{\text{d-s}}$ is mainly defined by the inter-metal capacitances between

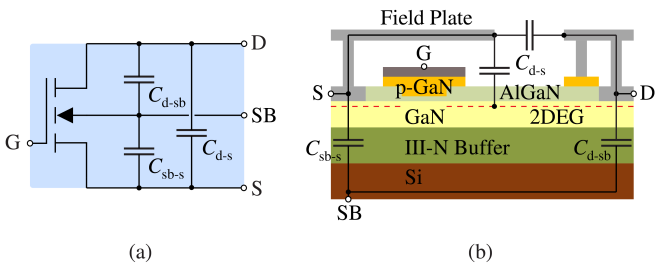


Fig. 16: (a) Equivalent circuit and (b) cross-section of the DUT illustrating the main structural components determining the parasitics capacitors $C_{\text{d-s}}$, $C_{\text{sb-s}}$ and $C_{\text{d-sb}}$.

source and drain metals, including the field plate and the two-dimensional electron gas (2DEG). $C_{\text{d-s}}$ also includes the drain-gate capacitor $C_{\text{g-d}}$, considered in parallel to $C_{\text{d-s}}$ in a first approximation. These elements are typically considered loss-less, as long as the inter-level dielectrics can be assumed nearly ideal. As well the drain p-GaN region, under the assumption of PTO, is considered loss-less, since there is no potential drop applied across it that could cause the injection of holes. Differently, in the two capacitors from the drain and source metals to the conductive Si substrate, denominated $C_{\text{sb-s}}$ and $C_{\text{d-sb}}$ respectively, the relevant dielectric is the III-N buffer, which could in principle show intrinsic loss mechanisms in contrast to traditional dielectrics, as discussed in the following.

The basic role of the epitaxial layers forming the III-N buffer, is to provide electrical insulation between the substrate (on the bottom-side) and the lateral GaN channel (on the top-side), when a non-zero v_{ds} is applied to the DUT. Therefore, the III-N buffer should ideally form a capacitor with no vertical leakage current I_{leak}. In reality, I_{leak} increases with v_{ds} but is limited well below $1\,\text{nA}/\text{mm}^2$ for typical static conditions below $125\,^\circ\text{C}$ and with $v_{\text{ds}} < 480\,\text{V}$. Consequently, given a die area in the range of a few mm^2, the contribution of I_{leak} to the overall losses in static conditions can be neglected. Nevertheless, losses occurring in dynamic conditions could be more significant, depending on the technology selected to create the III-N buffer.

The complete structure of typical III-N buffers consists of several layers. At the bottom, an Aluminum-Nitride (AlN) buffer layer is typically used to nucleate on the Si substrate. On top of this, several layers are required to compensate for the thermal expansion mismatch between Si and the remaining III-N buffer (between growth temperature of around $1000\,^\circ\text{C}$ and room temperature), thus providing a base of sufficiently good quality for the GaN channel [25]. Since the layers typically used are not intrinsically insulating, deep traps are introduced through foreign dopants during growth of the III-N buffer.

The most commonly used dopant is Carbon (C), which is already available from the metal-organic precursor used to grow III-N layers and, moreover, is fully compatible with the contamination requirements of the standard fabrication process of Si CMOS. Even though it is empirically shown that layers with increased concentrations of C exhibit significantly lower I_{leak}, the responsible mechanism is still under discussion. Additionally, the nature of C-doped GaN (GaN:C) layers is best described by a lossy (rather than a leakage suppressing) dielectric, i.e. I_{leak} is not completely suppressed [26]–[29]. However, this feature seems to offer an advantage in terms of dynamic conduction performance, by allowing a fast discharge of the GaN channel and of the III-N buffer from trapped and/or stored charges, hence alleviating dynamic $R_{\text{ds,on}}$ phenomena [26], [27]. Recently, it has been suggested that C atoms might also segregate to the structural defects, e.g. threading dislocations or low-angular grain boundaries, which are an inevitable part of III-N buffers grown on Si. The distance between these atoms could become sufficiently small to enable direct defect-to-defect interactions. The results of several electrical measurements [28]–[30] suggest the existence of such a defect band related transport mechanism.

Interestingly, when comparing a single GaN:C-layer, revealing the isolated leakage behavior of the defect band, with actual multi-layer III-N buffers, the same exponential dependency of I_{leak} with respect to temperature can be recognized, as illustrated in **Fig. 17 (a)** where the measured leakage current densities J_{leak}, obtained dividing I_{leak} by the dies area, are plotted as function of temperature for both cases. This result suggests that the same physical transport mechanism might not only act in single GaN:C-layers, but that it could also play a significant role in the real full multi-layer III-N buffer.

Moreover, comparing J_{leak} in these two cases as function of the applied electric fields as in **Fig. 17 (b)**, an exponential field dependency with different pre-factors and offsets is visible. The presence of an offset clearly indicates that the defect band transport induced by C doping is actually not the sole mechanism causing the insulating behavior of the multi-layer III-N buffer. The offset can be best described as an additional potential drop, whose origin is assumed to be related to the different combination of layers within the buffer, comparable to a depletion region characteristic of p-n junctions. Moreover, it is verified that in reverse bias condition, a simple GaN:C/GaN:Si-layer can guarantee a voltage blocking behavior with very low I_{leak} [29].

It can be concluded that a single GaN:C-layer is not sufficient to provide the desired insulating behavior, but an optimized sequence of different layers forming the full III-N buffer is required. As a consequence, the resistive behavior of the C-related defect band, visible in **Fig. 17 (b)**, could be responsible for a significant fraction of the losses measured in Section IV, in particular during the formation of the buffer depletion region. This hypothesis could be relevant in contrast to the trapping phenomena seen in C-doped buffers. Interestingly, both the presence of traps and of resistive layers within the buffer could cause a similar hysteresis of C_{oss}, hence justifying the losses.

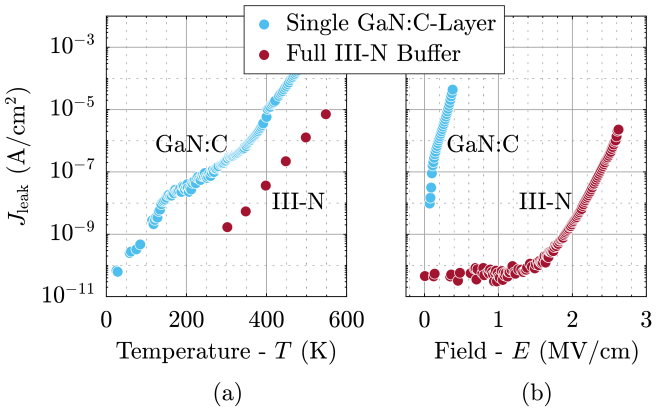


Fig. 17: Measured J_{leak} of a single GaN:C-layer compared to a complete multi-layer III-N buffer as function of (a) temperature and (b) vertical electric field.

VI. Measurements of DUT with Separate Substrate

The evidence of a lossy C_{oss} charging/discharging process, provided by the experimental results of Section IV, is supported by the above discussed analysis of the internal structure of the DUT. Nevertheless, it is still unknown which of the three capacitors shown in **Fig. 16** contributes most to the observed losses. In the commercial version of the DUT, the substrate is electrically connected to the source inside the package, i.e. $C_{sb\text{-}s}$ is shorted and therefore cannot contribute to E_{PTO}. Hence, the main suspects are $C_{d\text{-}s}$, associated with the lateral structure of the DUT and to the field plate, and $C_{d\text{-}sb}$, distributed along the vertical stack.

To separate these two potential causes of E_{PTO}, two DUT, denominated Separate Substrate (SS) DUT, are packaged without the internal connection between substrate and source, and installed in the half-bridge $T_3 - T_4$ replacing the PTO DUT. The PCB is modified inserting eight solder bridges (jumpers) allowing to connect the source and substrate terminals of both SS DUT to either the source or the drain terminals of the transistors forming the switching half-bridge. As an example, the four jumpers connected to the low-side SS DUT, i.e. T_4, are illustrated in **Fig. 18**, where the drain and source terminals of the low-side transistor of the switching half-bridge, i.e. T_2, are labeled AC and GND respectively. Ideally, each jumper can be either open (0) or close (1), i.e. sixteen (2^4) symmetrical (between the low- and high-side of the half-bridge formed by the SS DUT) configurations of jumpers are possible. Several configurations connect AC to GND, causing the setup to be inoperable. Thus, only the remaining nine configurations are reported in **Table V**, where the numbering defined in **Fig. 18** and the binary coded states of the jumpers are used to differentiate among them.

Each configuration of jumpers leads to a different equivalent capacitance between AC and GND, i.e. excited from the switching half-bridge, which applies v_{PTO} between AC and GND. In first approximation, the additional parasitic capacitance introduced by the open jumpers is not considered, since negligible compared to the contribution of the DUT. Hence, for example, in configuration 0101 (first row of **Table V**) both source and substrate terminals of T_4 are connected to GND and v_{PTO} is applied across its drain and source (connected to substrate) terminals, defining the notation *d-s,sb*. In this case, the capacitors $C_{d\text{-}s}$, $C_{d\text{-}sb}$ and C_{PCB} (where the latter includes all the parasitic capacitors not directly related to T_4) are connected in parallel, hence the charge $Q_{tot,1} = Q_{d\text{-}s} + Q_{d\text{-}sb} + Q_{PCB}$ characterizes this experiment. Since both SS DUT are PTO, $C_{g\text{-}d}$ is again considered in parallel to $C_{d\text{-}s}$ (and not shown explicitly). Differently, configurations 0100 and 0001 (second and third row of **Table V**) impose the series connections ($\oplus$) of capacitors, i.e. $C_{d\text{-}sb} \oplus C_{sb\text{-}s} = C_{d\text{-}sb\text{-}s}$ and $C_{d\text{-}s} \oplus C_{sb\text{-}s} = C_{d\text{-}s\text{-}sb}$. Since these capacitors are known and/or expected to be nonlinear, the corresponding charge variables $Q_{d\text{-}sb\text{-}sb}$ and $Q_{d\text{-}s\text{-}sb}$ must be defined as well. All configurations of the type 0x0x are redundant since they cause the SS DUT to float, i.e. only C_{PCB} is excited by v_{PTO}.

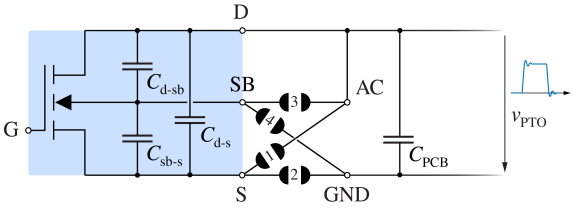


Fig. 18: Equivalent circuit of the DUT and schematic representation of the jumpers allowing to connect the source and substrate terminals of the low-side SS DUT to either AC or GND.

The occurring losses $P_{SS,i}$ can be measured in six distinguishable (non-redundant) experiments for each operating point of interest ($V_{dc} = 400\,\text{V}$ and $I_{sw} = 20\,\text{A}$ are selected), setting the appropriate configuration of jumpers i. Finally, the contribution of each capacitor to $P_{SS,i}$ can be determined.

First of all, each $Q_{tot,i}$ in $\boldsymbol{Q_{tot}}$ can be calculated as

$$Q_{tot,i} = \frac{I_{sw} V_{dc}}{2\ \mathrm{d}v_{PTO,i}/\mathrm{d}t} \tag{7}$$

for every experiment $i = 1, 2, \ldots 6$. $Q_{tot,i}$ is the result of the linear combination, represented by $\mathbf{A}$ and described in **Table V**, of the six unknown charges Q_j forming $\boldsymbol{Q}$, associated with the six identified capacitors, i.e.

$$\begin{bmatrix} Q_{tot,1} \\ Q_{tot,2} \\ \vdots \\ Q_{tot,6} \end{bmatrix} = \boldsymbol{Q_{tot}} = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} Q_{d\text{-}s} \\ Q_{d\text{-}sb} \\ Q_{sb\text{-}s} \\ Q_{d\text{-}sb\text{-}s} \\ Q_{d\text{-}s\text{-}sb} \\ Q_{PCB} \end{bmatrix} = \mathbf{A}\boldsymbol{Q}.$$

To clarify, $A_{i,j} = 1$ indicates that the charge Q_j, and therefore the associated capacitor, is involved in the experiment i (vice versa is true when $A_{i,j} = 0$). $\boldsymbol{Q} = \mathbf{A}^{-1}\boldsymbol{Q_{tot}}$ can be calculated to find the unknown Q_j. The resulting measured value $Q_{d\text{-}s} + Q_{d\text{-}sb} = 37\,\text{nC}$ differs only $10\,\%$ from the corresponding value, i.e. Q_{oss} calculated at $400\,\text{V}$, reported in [17], confirming the accuracy of this measurement procedure. Afterwards, for each experiment i, the average current $I_{i,j}$ determining the flow of Q_j in the associated capacitor can be calculated according to

$$\begin{bmatrix} 1/t_1 \\ 1/t_2 \\ \vdots \\ 1/t_6 \end{bmatrix} \boldsymbol{Q}^{\intercal} \circ \mathbf{A} =$$

$$= \begin{bmatrix} I_{d\text{-}s,1} & I_{d\text{-}sb,1} & 0 & 0 & 0 & I_{PCB,1} \\ I_{d\text{-}s,2} & 0 & 0 & I_{d\text{-}sb\text{-}s,2} & 0 & I_{PCB,2} \\ 0 & I_{d\text{-}sb,3} & 0 & 0 & I_{d\text{-}s\text{-}sb,3} & I_{PCB,3} \\ I_{d\text{-}s,4} & 0 & I_{sb\text{-}s,4} & 0 & 0 & I_{PCB,4} \\ 0 & I_{d\text{-}sb,5} & I_{sb\text{-}s,5} & 0 & 0 & I_{PCB,5} \\ 0 & 0 & 0 & 0 & 0 & I_{PCB,6} \end{bmatrix} = \boldsymbol{I}.$$

t_i corresponds to the time considered to calculate $\mathrm{d}v_{PTO,i}/\mathrm{d}t$, while the notation $\circ\mathbf{A}$ indicates, instead, the element-wise

TABLE V: Possible configurations of the jumpers of **Fig. 18** with associated binary coded states and expressions of $Q_{\text{tot,i}}$ as function of Q_{j}.

J	Connection 1	2	3	4	Note	$Q_{\text{tot,i}}$
	0	1	0	1	*d-s,sb*	$Q_{\text{d-s}} + Q_{\text{d-sb}} + Q_{\text{PCB}}$
	0	1	0	0	*d-s*	$Q_{\text{d-s}} + Q_{\text{d-sb-s}} + Q_{\text{PCB}}$
	0	0	0	1	*d-sb*	$Q_{\text{d-sb}} + Q_{\text{d-s-sb}} + Q_{\text{PCB}}$
	0	1	1	0	*d,sb-s*	$Q_{\text{d-s}} + Q_{\text{sb-s}} + Q_{\text{PCB}}$
	1	0	0	1	*d,s-sb*	$Q_{\text{d-sb}} + Q_{\text{sb-s}} + Q_{\text{PCB}}$
	1	0	1	0	*d,s,sb*	Q_{PCB}
	0	0	0	0		
	1	0	0	0		
	0	0	1	0		

multiplication for $\mathbf{A}$ necessary to zero the elements of $\boldsymbol{I}$ associated with capacitors not involved in the experiment. As a verification of the procedure, $2\sum_j I_{\text{i,j}} = I_{\text{sw}}$, where 2 is necessary to account for the presence of low- and high-side SS DUT.

From the considerations reported in Section IV, it can be assumed that E_{PTO} is proportional to the current charging/discharging the lossy capacitor (neglecting the offset at $^{\text{d}v}/_{\text{d}t} = 0\,^{\text{V}}/_{\text{ns}}$). Therefore, proportionality factors λ_{j} are introduced herein to describe the relationship between $I_{\text{i,j}}$ and the measured losses $P_{\text{SS,i}}$. In particular, each λ_{j} belonging to $\boldsymbol{\lambda}$ can be calculated as

$$\begin{bmatrix} \lambda_{\text{d-s}} \\ \lambda_{\text{d-sb}} \\ \lambda_{\text{sb-s}} \\ \lambda_{\text{d-sb-s}} \\ \lambda_{\text{d-s-sb}} \\ \lambda_{\text{PCB}} \end{bmatrix} = \boldsymbol{\lambda} = \boldsymbol{I}^{-1} \begin{bmatrix} P_{\text{SS,1}} \\ P_{\text{SS,2}} \\ \vdots \\ P_{\text{SS,6}} \end{bmatrix} = \boldsymbol{I}^{-1} \boldsymbol{P}_{\mathbf{SS}}. \tag{8}$$

In the commercial version of the DUT, $C_{\text{sb-s}}$ is shorted, i.e. only $\lambda_{\text{d-sb}}$ and $\lambda_{\text{d-s}}$ are of practical interest.

Finally, since $\lambda_{\text{d-sb}} \approx 20\lambda_{\text{d-s}}$ results from (8), it can be concluded that $C_{\text{d-sb}}$, i.e. the multi-layer III-N buffer separating the Si substrate from the GaN channel, is responsible for up to 95 % of E_{PTO}. As discussed in Section V, this is assumed to originate from the resistivity of the C-doped layers in the III-N buffer. Hence, different samples featuring different vertical internal structures are assessed in the next section, aiming to overcome the C_{oss}-losses.

VII. Improvement of the III-N Buffer Structure

In Section VI, $C_{\text{d-sb}}$ is finally proven to be the major contributor to E_{PTO} measured in Section IV and therefore to E_{sw} measured in Section III. Since, as described in Section V, $C_{\text{d-sb}}$ depends on the technology used to build the III-N buffer, a DUT featuring a different epitaxial stack is analyzed in this section. The modified epitaxial stack is denominated B to differentiate it from the original one, denominated A, considered in all the measurements discussed until this point of the manuscript. It is worth mentioning that the devices based on both epitaxial stacks, i.e. A and B, yield comparable performance both in terms of static lateral device and vertical buffer leakage currents, as well as concerning their dynamic behaviors, e.g. with respect to lifetime models and in terms of measured I_{leak} and dynamic $R_{\text{ds,on}}$. Additionally, the stacks are of similar thicknesses leading to the same contributions to C_{oss}.

To support the latter statements, $R_{\text{ds,on}}$ of two DUT featuring the two considered epitaxial stacks is measured under dynamic conditions and with different stress voltage V_{s} up to 600 V (applied across the drain and source terminals of the DUT in off-state). The results are normalized with respect to $R_{\text{ds,on}}$ measured in the same setup with $V_{\text{s}} = 0\,\text{V}$ (to exclude any other possible dependency, e.g. related to temperature) and compared in **Fig. 19**. Both DUT, i.e. epitaxial stacks A and B, exhibit a good uniformity of $R_{\text{ds,on}}$ with respect to V_{s}, are well comparable between each other and do not feature any increase of $R_{\text{ds,on}}$ in dynamic conditions, similarly to what already reported in **Fig. 7**. To summarize, epitaxial stack B is demonstrated to be equally good as A in terms of dynamic $R_{\text{ds,on}}$ in these conditions.

The results of $E_{\text{PTO-B}}$, i.e. E_{PTO} of the PTO DUT featuring epitaxial stack B, and the associated linear interpolating curve are reported in **Fig. 20** (stars and dashed line respectively) as function of $^{\text{d}v_{\text{PTO}}}/_{\text{d}t}$ for the case of $V_{\text{dc}} = 400\,\text{V}$. For comparison, also the previously measured $E_{\text{PTO-A}}$ (squares and dashed line) and $E_{\text{sw-A}}$ (solid line) with (dots) and without (triangles) $C_{\text{ext}} = 100\,\text{pF}$ are shown always in the case of $V_{\text{dc}} = 400\,\text{V}$ as function of the respective $^{\text{d}v}/_{\text{d}t}$. The modified epitaxial stack enable a reduction of E_{PTO} which amounts up to 73 %, definitely motivating the presented study.

Interestingly, epitaxial stack B shows the same C-level as A according to measurements based on secondary ion mass spectrometry (SIMS). However, it is believed (and subject of on-going research) that the defect band, discussed in Section V as hypothesis for the origin of the C_{oss}-losses, might depend more on the local C-density within certain structural defects

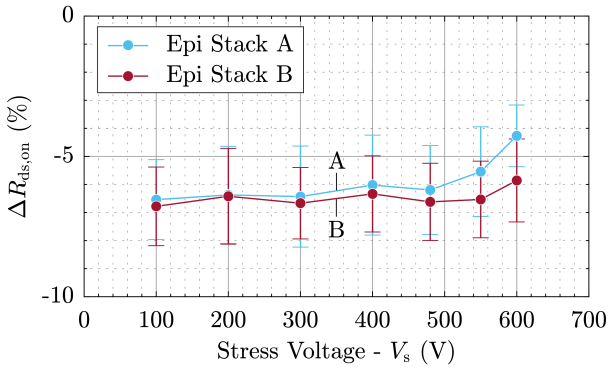


Fig. 19: $R_{\text{ds,on}}$ of the two DUT featuring epitaxial stacks A and B measured in dynamic conditions as function of V_{s} and normalized with respect to $R_{\text{ds,on}}$ measured with $V_{\text{s}} = 0\,\text{V}$. The vertical error bars indicate the standard deviation of $R_{\text{ds,on}}$ calculated within 16 measurements across the whole wafer per each V_{s}. The measured $R_{\text{ds,on}}$ in case $V_{\text{s}} > 0\,\text{V}$ (dynamic) is even smaller compared to the case of $V_{\text{s}} = 0\,\text{V}$ (static), since a small residual amount of positive charges is present in the channel of the DUT after turn-on.

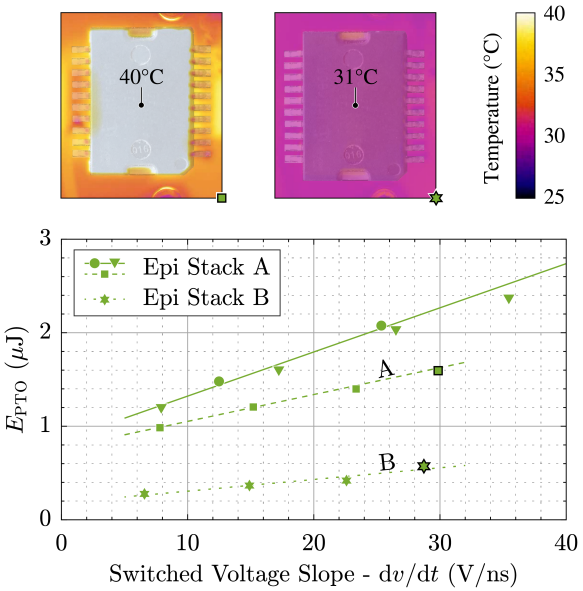


Fig. 20: E_{PTO} as function of $^{\mathrm{d}v_{\mathrm{PTO}}}/_{\mathrm{d}t}$ obtained with different I_{sw} (5 A… 20 A) for $V_{\mathrm{dc}} = 400\,\mathrm{V}$. $E_{\mathrm{PTO\text{-}B}}$ (dotted) is more than 70 % lower than $E_{\mathrm{PTO\text{-}A}}$ (dashed). Additionally, thermal images of the two analyzed PTO DUT featuring different epitaxial stacks: B (right) experiences only one tenth of the temperature increase of A (left).

rather than on the absolute C-level.

The remaining losses visible in **Fig. 20** (stars) may still arise from small residual losses in the vertical internal structure of the DUT featuring the modified epitaxial stack. However, it is also possible that the minimum absolute $E_{\mathrm{PTO\text{-}B}}$ reaches the measurement noise floor of the considered calorimetric measurement setup and/or causes external factors, e.g. the losses occurring in the switching half-bridge, to compromise the measurement accuracy.

To compensate for the possible influence of external sources of loss and therefore validate the findings, a second calorimetric measurement approach, relying on the measurement of the case temperature T_{c} (see **Fig. 5 (a)**) of the PTO DUT with a high definition infrared camera [31], is presented in the following. **Fig. 20** shows, as an example, two infrared images of the two analyzed PTO DUT featuring different epitaxial stacks, and captured after approximately 10 s of their operation in identical conditions ($V_{\mathrm{dc}} = 400\,\mathrm{V}$ and $^{\mathrm{d}v_{\mathrm{ds}}}/_{\mathrm{d}t} \approx 30\,^{\mathrm{V}}/_{\mathrm{ns}}$). They highlight how the PTO DUT based on epitaxial stack A (left) heats up significantly, i.e. $T_{\mathrm{c}} \approx 10\,^{\circ}\mathrm{C} + T_{\mathrm{hs}}$ because of the occurring $E_{\mathrm{PTO\text{-}A}}$ whereas, in contrast, the PTO DUT based on epitaxial stack B (right), heats up only $1\,^{\circ}\mathrm{C} + T_{\mathrm{hs}}$, given the negligible $E_{\mathrm{PTO\text{-}B}}$. The remaining $P_{\mathrm{tot,PTO\text{-}B}}$, causing the recorded minor rise of T_{c} in the second case, could be explained with the losses due to the voltage oscillation present on v_{PTO}. Since the parameters of the two thermal systems, i.e. of the two considered PTO DUT, are measured to be very similar (given that the two setups are physically identical), the temperature rise $T_{\mathrm{c}} - T_{\mathrm{hs}}$ is a good indicator to compare the occurring $P_{\mathrm{tot,PTO}}$. Consequently, the improvement brought by the modified epitaxial stack, visible in the plot of **Fig. 20**, can be at least confirmed with this second and practically independent measurement approach.

The absolute accuracy of the infrared camera based measurement method is still under evaluation, but it generally features several advantages especially if combined with the separate heat-sink concept. In fact, given the higher measurement bandwidth, the same thermal analysis conducted for the (slowest) thermal constant associated with the heat-sink can be exactly repeated for the (faster) one associated with the case of the DUT (cf. **Fig. 5** gray). Hence, the reduced dimensions of the case compared to the heat-sink lead to significantly (from some minutes to few tens of seconds) reduced measurement times, whereas the described simplified thermal model and effective measurement procedure remain valid. Moreover, with a shorter measurement time and limiting the temperature measurement to the area defined by the case of the DUT, external sources of loss, e.g. the switching half-bridge during the measurements of the PTO DUT, are believed to have even less influence on the measurement accuracy.

The presented improvement, derived from the modified epitaxial stack, supports the hypothesis considering the vertical GaN-on-Si structure between the drain contact and the grounded Si substrate as main responsible for the soft-switching losses of III-N power devices. This not only motivates the conducted study, but also increases the interest towards the already existing challenge of providing highly insulating buffer layers with minimal transient response.

VIII. Conclusion

Gallium-Nitride-on-Silicon (GaN-on-Si) High Electron Mobility Transistors (HEMTs) are nowadays the best-in-class power semiconductors [22], but losses associated with their output capacitance C_{oss} severely limit their performance in soft-switching power converters [10].

In this research work, an accurate calorimetric measurement setup was developed to characterize the soft-switching losses of the IGT60R070D1 *CoolGaN*™ enhancement-mode GaN power transistor from *Infineon Technologies*. Subsequently, the setup was adapted to isolate the C_{oss}-losses, which were demonstrated, by means of measurements, to constitute the main share of the observed soft-switching losses. Afterwards, the main technology components and the regions of the internal structure of the device forming C_{oss} were analyzed. Supported by experimental evidences, it was speculated that the resistive behavior of the Carbon related defect band present in the multi-layer III-N buffer, i.e. in the dielectric of the parasitic capacitance between the drain and the substrate of the device, could be the main responsible for the observed losses. Finally, based on this conclusion, a device featuring a modified Gan-on-Si stack was realized and measurements of C_{oss}-losses were repeated to quantify the expected improvement.

C_{oss}-losses appear to be almost entirely eliminated in the new device featuring the modified epitaxial stack. Moreover, it was verified that the enhanced device structure does not introduce any dynamic $R_{\mathrm{ds,on}}$ phenomena. In other words, the study conducted in this work, not only deepened the understanding

about the origin of the C_{oss}-losses, but finally resulted in the realization of a new GaN-on-Si HEMT which potentially does not exhibit any of the two loss mechanisms typically limiting the performance of GaN devices, i.e. dynamic $R_{ds,on}$ phenomena and C_{oss}-losses.

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