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Compensation and Emulation of Output Impedance in Ultra-High Bandwidth Class-D Power Amplifiers

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***Abstract*—The stability limits for an ultra-high bandwidth class-D power amplifier (100 kHz, 800 V DC-link, 10 kW) are derived and characterized for two different use cases and for a given inductance of the line that connects the output of the converter to the load. In the first use case, the additional impedance due to the line is compensated and in the second use case, a controlled inner ohmic-inductive impedance is emulated by the converter. General stability analyses are conducted for simplified representations of the two control concepts, i.e., for compensating the line impedance and emulating an inner impedance. A detailed linearized model of the investigated power amplifier is used to evaluate the effectivenesses of both control concepts and to identify the stability boundaries that apply to the investigated converter system. By way of example, the compensation of the line impedance can decrease the total output impedance of the converter system due to a line inductance of 10 µH from 1.3 Ω to 0.37 Ω at 20 kHz. Furthermore, the compensation of the line impedance is found to be less prone to instability than the emulation of a defined inner impedance. With regard to the inner impedance emulation, the stability analysis discloses the dependency between the maximum allowable values of emulated inner inductance and inner resistance such that the system remains stable, which facilitates the evaluation of the implications of specific modifications of the converter hardware or changes of the structure of the control system on the stability boundaries. Without external inductance, a maximum inner inductance of 430 µH at the stability limit is achieved if the bandwidth of the impedance emulation is limited to 30 kHz. A detailed circuit simulation of the power stage and the digital control unit is used to verify the results of the analysis.**

I. Introduction

Power Hardware-In-the-Loop (PHIL) systems are commonly used to emulate specific grid conditions in order to test and verify grid-connected power systems, e.g., power converters. The maximum frequency up to which the PHIL system can accurately emulate the grid behaviour is limited by the bandwidth of its Real Time Simulator (RTS) and the control bandwidth of its power amplifier [1]. According to [2], where the real-time model is implemented in FPGAs with ARM cores, a fast digital processing unit can be used to achieve a high bandwidth of the RTS. With regard to the power amplifier, a high bandwidth can be achieved with a power converter that allows for operation with a very high switching frequency, e.g., the ultra-high bandwidth class-D power amplifier described in [3] and shown in **Fig. 1**. This converter effectively is a seven-level inverter with three interleaved bridge-legs and each bridge-leg is realized with a three-level flying capacitor topology. The effective switching frequency (at C_1) is $4.8\,\mathrm{MHz}$, the rated load resistance is $5.3\,\Omega$ ($10\,\mathrm{kW}$ at rated rms output voltage of $230\,\mathrm{V}$, DC-link voltage of $800\,\mathrm{V}$), $L_1 = 1.26\,\mu\mathrm{H}$, and $C_1 = 90\,\mathrm{nF}$. According to the results of the optimization of the control system presented in [4], this converter can achieve large-signal bandwidths of more than $100\,\mathrm{kHz}$ with control structures similar to the structures depicted in Fig. 2, i.e., a cascaded control structure with PI voltage controller, P current controller, and Inductor Voltage FeedForward (IVFF) path as shown in **Fig. 2(a)** and the control structure with PI voltage controller, Capacitor Current FeedBack (CCFB), and IVFF path depicted in **Fig. 2(b)**.

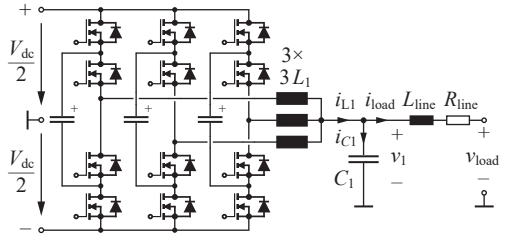

Fig. 1: Circuit of the ultra-high bandwidth amplifier, which is a 10 kW 7-level inverter with 3 interleaved bridge-legs (3L3). Each bridge-leg is implemented as 3-level flying capacitor topology. The output-side components L_{line} and R_{line} model the impedance of the line that connects the output of the converter to the load.

Typically, ultra-high bandwidth class-D power amplifiers are used to provide an output voltage that is independent of the load. This is best achieved if the amplifiers resemble a voltage source with zero output impedance. Respective concepts to achieve very low output impedances of power converters are presented in literature, e.g., in [5], where the inductor current is processed by a suitable transfer function and the result is added to the reference voltage of the control system. In [6] the load current is processed by means of a virtual impedance, composed of inductor and resistor, which resembles the output impedance of the voltage-controlled system, and the obtained voltage is added to the reference voltage. Both methods require knowledge about the output impedance of the amplifier. However, the considered amplifier features a very low output impedance (e.g., $60\,\mathrm{m\Omega}$ at $100\,\mathrm{kHz}$ can be achieved with PI-P-IVFF control as shown in Fig. 9 in [4]). Accordingly, the impedance of the line between the output of the amplifier and the load may dominate the total output impedance of the amplifier system seen by the load (by way of example, the impedance of a line with an inductance of $10\,\mu\mathrm{H}$ is $6.3\,\Omega$ at $100\,\mathrm{kHz}$). Since the impedance of the line between the amplifier and the load is usually not known and/or measured, the approach described in [6] has been modified in this paper such that the difference between the output voltage and the load voltage, $\underline{V}_1 - \underline{V}_{\text{load}}$, which is equal to $(R_{\text{line}} + sL_{\text{line}})\underline{I}_{\text{load}}$, is

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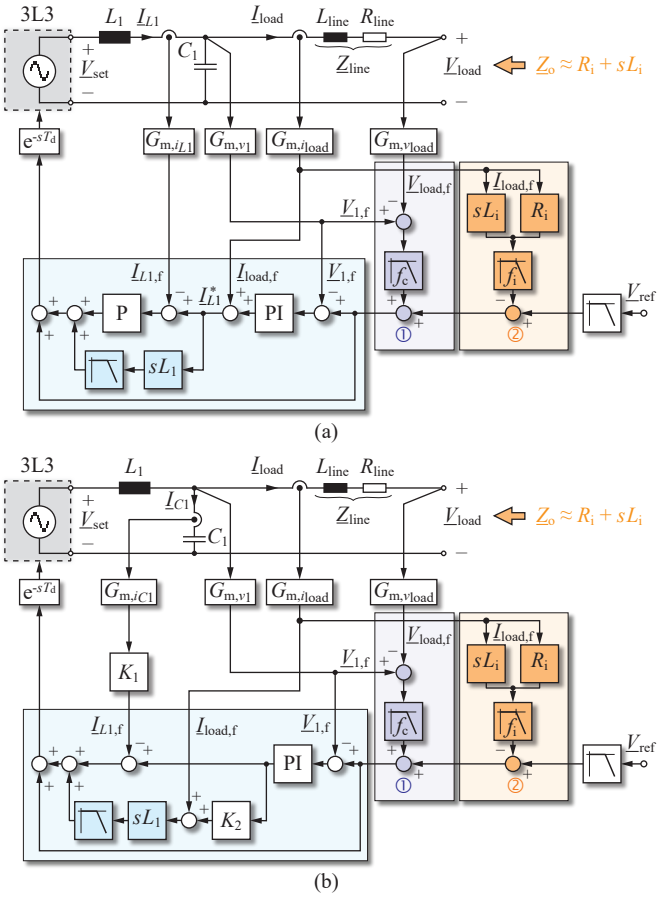

Fig. 2: **(a)** Block diagram of the cascaded control structure with PI voltage controller, P current controller (PI-P), and Inductor Voltage FeedForward (IVFF) path. **(b)** Block diagram of the control structure with PI voltage controller, Capacitor Current FeedBack (CCFB), and IVFF path. Cyan: core parts of the control systems; purple ①: compensation of the voltage across the line connecting the power amplifier output to the load; orange ②: emulation of output impedance. Underlined symbols refer to phasors, e.g., $\underline{V}_{\text{load}} = |\underline{V}_{\text{load}}|\, e^{j\arg(\underline{V}_{\text{load}})}$.

added to the reference voltage. Furthermore, a low-pass filter is inserted to improve stability. The parts marked with ① in Fig. 2(a) and Fig. 2(b) depict the investigated structure.

As opposed to the realization of a very low output impedance, certain applications require the voltage source to feature a defined inner impedance [7]–[10]. In particular in the context of Interface Algorithms for PHIL systems, numerous different methods for emulating defined inner impedances are documented, among which the Ideal Transformer Model (ITM) and the Damped Impedance Model (DIM) are often considered, e.g., in [2], [11]. The block diagrams related to the implementation of the ITM and the DIM are given in Fig. 9 of [2]. The DIM is found to be more robust than ITM, whereas the ITM features a lower complexity than the DIM. Furthermore, the implementation of the DIM in particular requires the impedance of the load to be known, which is not needed for the ITM. For these reasons, the ITM is considered in this paper, which, in case of the investigated ohmic-inductive inner impedance, $\underline{Z}_{\text{i}} = R_{\text{i}} + sL_{\text{i}}$, reveals the commonly known control systems used for impedance emulation, e.g., as presented in [6], [12]: the control system uses the load current to calculate the voltage across the inner impedance, $\underline{V}_{\text{i}} = \underline{Z}_{\text{i}}\underline{I}_{\text{load}}$, and $\underline{V}_{\text{i}}$ is subtracted from the reference voltage. The part marked with ② in Fig. 2(a) and Fig. 2(b) depicts the corresponding part in each control structure, which also includes a low-pass filter with cutoff frequency f_{i}, to achieve improved stability.

This paper presents the findings of comprehensive analyses for the compensation of the line impedance and the emulation of a defined inner impedance. In a first part, general stability analyses are presented in **Section II** for a simplified dynamic model of the amplifier for both, the compensation of the line impedance in Subsection II-A and the emulation of a defined inner impedance in Subsection II-B. The considered simplified model facilitates the derivation of small expressions for assessing stability, which allow the identification of critical aspects in terms of stability constraints. In **Section III**, numerical MATLAB models of the controlled power amplifier are assessed with regard to the effectivenesses of the investigated approaches for compensating the line impedance and emulating a defined impedance and to identify the stability limits. In Subsection III-A it is found that the compensation of the line impedance achieves a reduction of the output impedance for frequencies up to 60 kHz (using a cutoff frequency of $f_{\text{c}} = 100\,\text{kHz}$ for the compensation). Furthermore, due to the employed low-pass filter, the system remains stable also in case of very high line inductances (stability has been evaluated up to 1 mH). With regard to impedance emulation with a cutoff frequency of $f_{\text{i}} = 30\,\text{kHz}$, the concept is found to accurately emulate an example impedance of $\underline{Z}_{\text{i}} = 1\,\Omega + s\,200\,\mu\text{H}$ up to a frequency of 17 kHz or 4 kHz, depending on whether the magnitude error (less than 5%) or the phase error (less than 10°) is considered, respectively. Since the system becomes unstable for high values of R_{i} and/or L_{i}, the characteristics of the maximum allowable values of R_{i} for given values of L_{i} are identified in Subsection III-B. In addition, different modifications are analyzed with the aim to increase the stability boundary towards higher values of R_{i} and L_{i}. The numerical results are verified by means of detail simulations of the circuit.

II. General Stability Analysis

In the course of simplifying the stability analysis, the controlled system (without parts ① and ② in Fig. 2) is replaced by a network that consists of a voltage source, $\underline{V}_{\text{set}}$, and a passive filter network (part Ⓐ in **Fig. 3**). A substantial simplification of the analysis is achieved if it is assumed that $\underline{V}_{\text{set}}$ almost ideally tracks the reference voltage, except for a delay, T_{d} (part Ⓑ in **Fig. 3**), and if the bandwidth-limitation of the controlled system is modelled by the passive filter network. By way of example, the output impedance achieved with the PI-P-IVFF control structure of Fig. 2(a) is approximated by a second-order output filter that features an inductor and an effective capacitor, which is connected in series to a damping resistor and features the values:[1]

$$L_{\text{eff}} = 0.9\,\mu\text{H}, \qquad C_{\text{eff}} = 55\,\text{nF}, \qquad R_{C,\text{eff}} = 1\,\Omega. \tag{1}$$

Based on this, the compensation of the line impedance (part ① in Fig. 2) and the emulation of an inner impedance (part ② in Fig. 2) can be represented by the circuits depicted in **Fig. 3(a)** and **Fig. 3(a)**, respectively (R_{line} is set to zero, to obtain a more comprehensible result).

[1] This approximation is based on the characteristic of the output impedance that results for the controller settings described at the beginning of Section III.

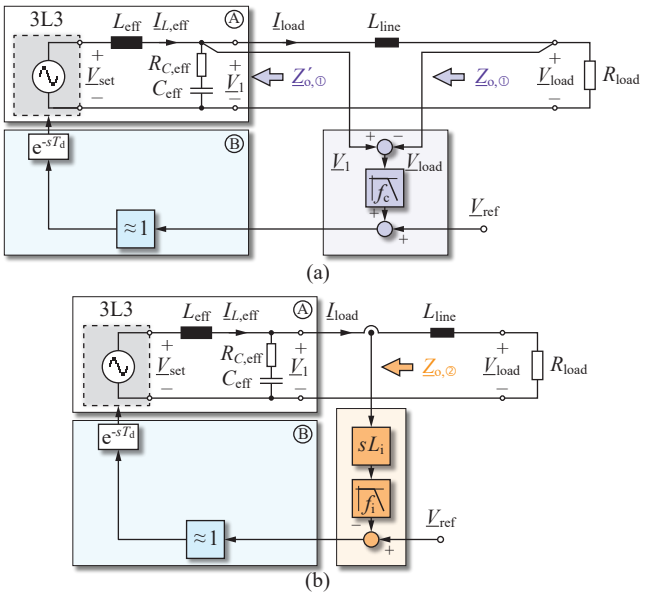

Fig. 3: Simplified circuits of the voltage-controlled power converter with **(a)** the compensation of the line impedance and **(b)** the emulation of an inner impedance. Underlined symbols refer to phasors, e.g., $\underline{V}_{\text{load}} = |\underline{V}_{\text{load}}|\, e^{j\,\arg(\underline{V}_{\text{load}})}$.

A. Compensation of line impedance

The stability analysis for the compensation of the line impedance is conducted at the interface between C_{eff}–$R_{C,\text{eff}}$ and L_{line} in Fig. 3(a),

$$\underline{V}_1 = \underline{V}_{\text{set}} \frac{R_{\text{load}} + sL_{\text{line}}}{R_{\text{load}} + sL_{\text{line}} + \underline{Z}'_{\text{o},①}} = \\ = \underline{V}_{\text{set}} \frac{1}{1 + \frac{\underline{Z}'_{\text{o},①}}{R_{\text{load}} + sL_{\text{line}}}} = \underline{V}_{\text{set}} \frac{1}{1 + \underline{F}_{\text{o,c}}}, \quad (2)$$

since the impedance ratio $\underline{Z}'_{\text{o},①} / (R_{\text{load}} + sL_{\text{line}})$ appears to be the open loop transfer function, $\underline{F}_{\text{o,c}}$, of the closed loop system $\underline{V}_1/\underline{V}_{\text{set}}$ [8], [11]. Thus, $\underline{F}_{\text{o,c}}$ can be tested with known methods, e.g., the Nyquist method, in order to find out whether $\underline{V}_1/\underline{V}_{\text{set}}$ is stable or not.

The expression for $\underline{F}_{\text{o,c}}$ is derived based on the expressions for the voltages $\underline{V}_1$ and $\underline{V}_{\text{set}}$ that apply according to the block diagram of Fig. 3(a). For this, the dependencies of $\underline{V}_1$ and $\underline{V}_{\text{set}}$ on the load current, $\underline{I}_{\text{load}}$, are explicitly expressed by $\underline{I}_{\text{load}}$ (instead of R_{load}),

$$\underline{V}_1 = \underline{V}_{\text{set}} \frac{\underline{Z}_{RC}}{\underline{Z}_L + \underline{Z}_{RC}} - \underline{I}_{\text{load}} \frac{\underline{Z}_L \underline{Z}_{RC}}{\underline{Z}_L + \underline{Z}_{RC}}, \quad (3)$$

$$\underline{V}_{\text{set}} = \left(\underline{V}_{\text{ref}} + \underline{I}_{\text{load}}\, s\, L_{\text{line}} \frac{2\pi f_c}{s + 2\pi f_c} \right) e^{-sT_d}, \quad (4)$$

using $\underline{Z}_L = sL_{\text{eff}}$ and $\underline{Z}_{RC} = R_{C,\text{eff}} + (sC_{\text{eff}})^{-1}$. In an intermediate step, the expression for $\underline{V}_1$ is determined by solving the equation system defined by (3) and (4), which gives

$$\underline{V}_1 = \underline{V}_{\text{ref}} \frac{\underline{Z}_{RC}}{\underline{Z}_L + \underline{Z}_{RC}} e^{-sT_d} \\ - \underline{I}_{\text{load}} \frac{\underline{Z}_{RC}}{\underline{Z}_L + \underline{Z}_{RC}} \left(\underline{Z}_L - s\, L_{\text{line}} \frac{2\pi f_c}{s + 2\pi f_c} e^{-sT_d} \right). \quad (5)$$

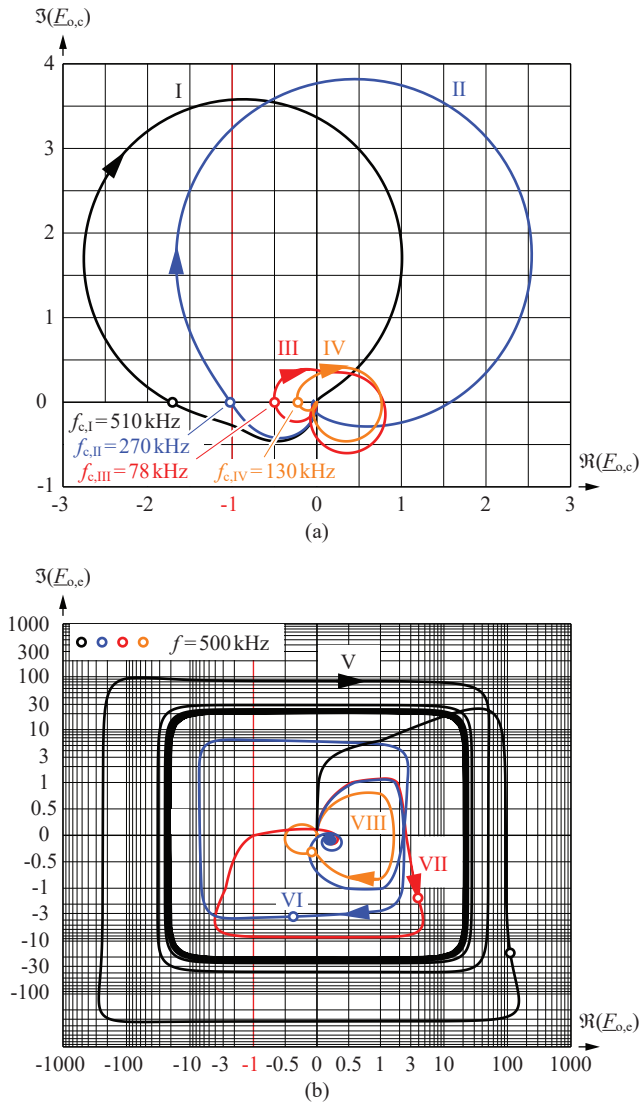

Fig. 4: (a) Nyquist plot of $\underline{F}_{\text{o,c}}$, cf. (6), evaluated for the four different settings I, II, III, and IV described in the text and $L_{\text{line}} = 10\,\mu\text{H}$. The frequencies $f_{\text{c,I}} \ldots f_{\text{c,IV}}$ refer to the frequencies where $\Re(\underline{F}_{\text{o}}) < 0$ and $\Im(\underline{F}_{\text{o}}) = 0$ applies for the first time. **(b)** Nyquist plot of $\underline{F}_{\text{o,e}}$, cf. (7), evaluated for the four different settings V, VI, VII, and VIII described in the text and $L_{\text{i}} = 100\,\mu\text{H}$. Please note that in (b) a symmetric logarithmic representation is used in order to cover the wide value ranges and still maintain an acceptable representation of the details within $-1 < \Re(\underline{F}_{\text{o,e}}) < 1$ and $-1 < \Im(\underline{F}_{\text{o,e}}) < 1$. Both plots have been generated with the effective filter component values given in (1).

Subsequently, the expressions for the inner impedance, $\underline{Z}'_{\text{o},①}$, and the open-loop transfer function, $\underline{F}_{\text{o,c}}$, can be derived,

$$\underline{Z}'_{\text{o},①} = -\frac{\underline{V}_1|_{\underline{V}_{\text{ref}} \to 0}}{\underline{I}_{\text{load}}}$$

$$\Rightarrow \quad \underline{F}_{\text{o,c}} = \underbrace{\frac{\underline{Z}_{RC}}{\underline{Z}_L + \underline{Z}_{RC}}}_{\underline{F}_{\text{o,c,A}}} \underbrace{\frac{sL_{\text{eff}} - sL_{\text{line}} \frac{2\pi f_c}{s+2\pi f_c} e^{-sT_d}}{sL_{\text{line}} + R_{\text{load}}}}_{\underline{F}_{\text{o,c,B}}}. \quad (6)$$

According to (6), the impedance compensation can lead to a substantial decrease of the real part of $\underline{F}_{\text{o,c}}$, which is directly seen if the low-pass filter is removed ($f_c \to \infty$), for zero time delay ($T_d \to 0$), large line inductance ($L_{\text{line}} > L_{\text{eff}}$), and

a low value of the load resistance ($|R_{\text{load}}| < |sL_{\text{line}}|$ at the frequencies where $\underline{F}_{\text{o,c}}$ crosses the real axis with a negative real value close to or less than -1). Even though, the real part of $\underline{F}_{\text{o,c,B}}$ remains greater than -1, the total system can become unstable ($\Re(\underline{F}_{\text{o,c}}) < -1$), because $\underline{F}_{\text{o,c,A}}$ can feature a gain of more than one.

In **Fig. 4(a)**, the characteristics of $\underline{F}_{\text{o,c}}$ are evaluated for the effective filter parameters given in (1), $L_{\text{line}} = 10\,\mu\text{H}$, and four different settings:

I $T_{\text{d}} \to 0$, $f_{\text{c}} \to \infty$, $R_{\text{load}} = 5.3\,\Omega$;
II $T_{\text{d}} = \underline{150\,\text{ns}}$, $f_{\text{c}} \to \infty$, $R_{\text{load}} = 5.3\,\Omega$;
III $T_{\text{d}} = 150\,\text{ns}$, $f_{\text{c}} = \underline{100\,\text{kHz}}$, $R_{\text{load}} = 5.3\,\Omega$;
IV $T_{\text{d}} = 150\,\text{ns}$, $f_{\text{c}} = 100\,\text{kHz}$, $R_{\text{load}} = \underline{20\,\Omega}$.

Without low-pass filter, the system is unstable (settings I and II). By limiting the bandwidth of the impedance compensation, e.g., to 100 kHz, the system becomes stable (III). Furthermore, the stability margin increases if the load resistor is increased (IV).

B. Impedance Emulation

Fig. 3(b) depicts the circuit and the block diagram for emulating an inner inductance of the converter. The stability analysis is conducted at the interface between C_{eff}–$R_{C,\text{eff}}$ and L_{line}, where the open-loop transfer function $\underline{F}_{\text{o,e}} = \underline{Z}_{\text{c,i,}②}/(sL_{\text{line}} + R_{\text{load}})$ results. The derivation of the expression of the effective converter impedance, $\underline{Z}_{\text{c,i,}②}$, is similar to the derivation described in Subsection II-A, leading to

$$\underline{F}_{\text{o,e}} = \underbrace{\frac{\underline{Z}_{RC}}{\underline{Z}_L + \underline{Z}_{RC}}}_{\underline{F}_{\text{o,e,A}}} \underbrace{\frac{sL_{\text{eff}} + sL_{\text{i}}\frac{2\pi f_0}{s+2\pi f_0}\text{e}^{-sT_{\text{d}}}}{sL_{\text{line}} + R_{\text{load}}}}_{\underline{F}_{\text{o,e,B}}}. \tag{7}$$

Compared to (6), $\underline{F}_{\text{o,c,A}} = \underline{F}_{\text{o,e,A}}$ applies, however, a comparison of $\underline{F}_{\text{o,e,A}}$ and $\underline{F}_{\text{o,e,B}}$ reveals two differences: firstly, the numerator contains the sum of the effective filter inductance and the (filtered and phase-shifted) emulated inductance and, secondly, the denominator of $\underline{F}_{\text{o,e,B}}$ does not contain a summand sL_{i}. As a consequence, the emulation of the inductance can lead to $\Re(\underline{F}_{\text{o,e,B}}) < -1$, by reason of $T_{\text{d}} > 0$. This can be directly verified if the low-pass filter in series to sL_{i} is replaced by a unity gain block ($f_{\text{i}} \to \infty$) and a sufficiently large inner inductance is considered, $L_{\text{i}} > L_{\text{eff}}$. Furthermore, (7) reveals that an increased stability margin can be achieved for large R_{load} and L_{line}. Conversely, the stability margin decreases if the bandwidth of the impedance emulation, f_{i}, is decreased.

Fig. 4(b) depicts the characteristics of $\underline{F}_{\text{o,e}}$ for the given effective filter parameters, an emulated inductance of $L_{\text{i}} = 100\,\mu\text{H}$, and for four different settings:

V $T_{\text{d}} = 500\,\text{ns}$, $f_{\text{i}} \to \infty$, $L_{\text{line}} \to 0$, $R_{\text{load}} = 5.3\,\Omega$;
VI $T_{\text{d}} = 500\,\text{ns}$, $f_{\text{i}} = \underline{20\,\text{kHz}}$, $L_{\text{line}} \to 0$, $R_{\text{load}} = 5.3\,\Omega$;
VII $T_{\text{d}} = \underline{150\,\text{ns}}$, $f_{\text{i}} = 20\,\text{kHz}$, $L_{\text{line}} \to 0$, $R_{\text{load}} = 5.3\,\Omega$;
VIII $T_{\text{d}} = 150\,\text{ns}$, $f_{\text{i}} = 20\,\text{kHz}$, $L_{\text{line}} = \underline{20\,\mu\text{H}}$, $R_{\text{load}} = 5.3\,\Omega$.

Without low-pass filter and for a large time delay, the system is unstable (setting V). By only limiting the bandwidth of the impedance emulation to 20 kHz the system remains unstable (VI). In a next step, the time delay is reduced to 150 ns and the system becomes marginally stable (VII). Finally, the inductance of L_{line} is increased to 20 µH and the system becomes stable (VIII).

III. Detailed analysis and verification

The considered control systems shown in Figs. 2(a) and (b) are based on the systems explained in [4], which have been extended by four moving average filters $G_{\text{m},i_{L1}}$, G_{m,v_1}, $G_{\text{m},i_{\text{load}}}$, $G_{\text{m},v_{\text{load}}}$ (12 samples; sampling rate of ADC is 58 MSPS). The moving average filters are used to lower the ripples that are superimposed on the measured currents and voltages and are mainly present at the effective switching frequency of 4.8 MHz and multiples thereof. The controllers have been designed by means of a conventional design procedure, e.g., the current controller or current feedback is designed for a phase margin of 30° and the voltage controller for a gain margin of 10 dB. In case of the PI-P-IVFF control structure shown in Fig. 2(a), the gain of the P current controller is $K_{\text{pi}} = 3\,\text{V/A}$, the PI voltage controller employs $K_{\text{pv}} = 13.8\,\text{mA/V}$ and $T_{\text{iv}} = 127\,\text{ns}$, and the inductor voltage feedforward path uses a low-pass filter with a second-order Bessel characteristic and a cutoff frequency of 5 MHz to limit the bandwidth of the derivative element sL_1. In the course of a first controller design, the PI-CCFB structure, depicted in Fig. 2(b), has been conducted without the IVFF path [i.e., for $sL_1 \to 0$ in Fig. 2(b)]. The obtained feedback gain is $K_1 = 3\,\text{V/A}$ and the PI voltage controller uses $K_{\text{pv}} = 114 \times 10^{-3}$ and $T_{\text{iv}} = 177\,\text{ns}$. Both structures use a reference low-pass filter (1st-order) with a cutoff frequency of 320 kHz, to limit the maximum gain of the reference transfer function to 2 dB and the maximum overshoot of the step response to less than 30 % (for $R_{\text{load}} \to \infty$). The complete (linear) control systems are evaluated in MATLAB and verified with a circuit simulator (GeckoCircuits), using detailed (non-linear) models for the switching stage and the digital control unit (e.g., considering a FPGA clock frequency of 240 MHz). In this Section, the reference case of a purely inductive line impedance of $L_{\text{line}} = 10\,\mu\text{H}$ is considered, which is approximately the inductance of a conventional cable that is 10 m long. Furthermore, either the compensation of the line impedance or the emulation of an inner impedance is considered (not both at the same time).

Fig 5(a) and **Fig 6(a)** depict the frequency responses of the reference transfer functions, $\underline{V}_{\text{load}}/\underline{V}_{\text{ref}}$, of the PI-P-IVFF and the PI-CCFB control structures, respectively. The purple lines and the dashed red lines refer to no load, $R_{\text{load}} \to \infty$, and nominal load, $R_{\text{load}} = 5.3\,\Omega$, respectively. Fig 5(a) and Fig 6(a) reveal highly similar gain and phase responses for the two control structures. Furthermore, the phase characteristics obtained for both control structures are subject to substantial phase lags for frequencies greater than 10 kHz, e.g., at $f = 30\,\text{kHz}$, 25° are observed for the PI-P-IVFF and 24° for the PI-CCFB structure. However, the main part of this phase lag is due to the line impedance, which, at $f = 30\,\text{kHz}$ and full load, is

$$\varphi = \arctan\left(\frac{2\pi f L_{\text{line}}}{R_{\text{load}}}\right) = 20°. \tag{8}$$

The dashed black lines in **Fig. 5(b)** and **Fig 6(b)** refer to the characteristics of the output impedances achieved with the two control structures for $L_{\text{line}} = 10\,\mu\text{H}$. Up to a high frequency of approximately 600 kHz, the characteristics of the output impedances resemble the impedance characteristic of L_{line}, i.e., an impedance of $-24\,\text{dB}\,\Omega$ at $f = 1\,\text{kHz}$ which increases with $20\,\text{dB/decade}$ features a phase of 90°.

Each circle depicted in Fig. 5, Fig. 6, and Fig. 9 refers to

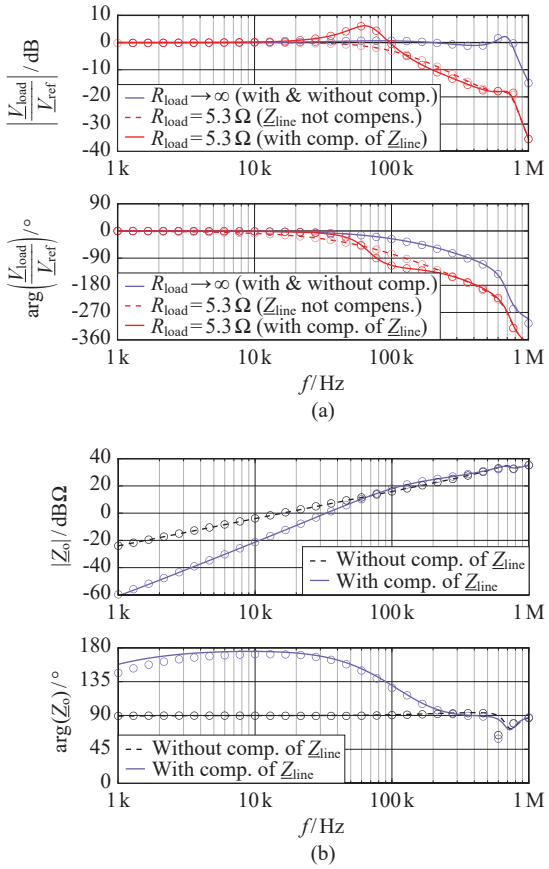

Fig. 5: Frequency characteristics determined for the PI-P-IVFF control structure with and without compensation of the line impedance [① in Fig. 2(a)] for $L_{line} = 10\,\mu H$: **(a)** reference transfer function; **(b)** output impedance. The lines are computed with MATLAB and the circles refer to simulation results obtained for the same operating conditions.

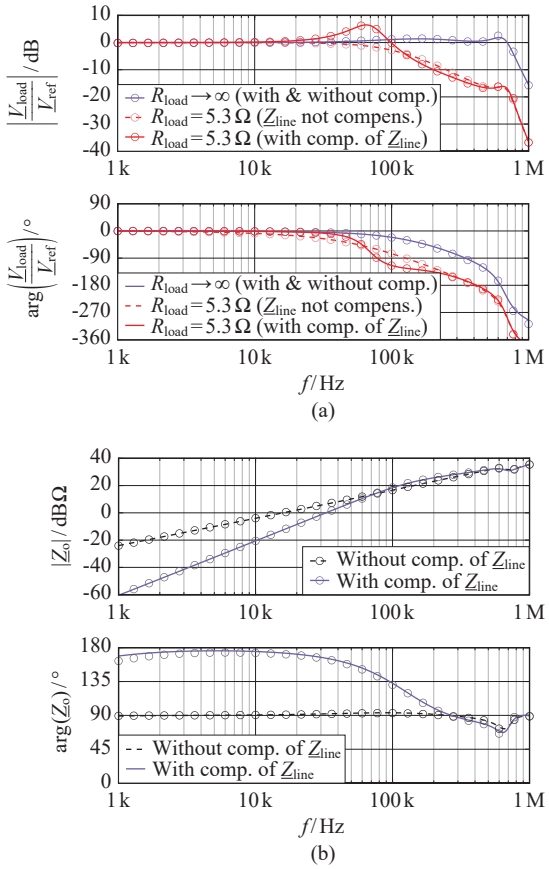

Fig. 6: Frequency characteristics determined for the PI-CCFB control structure with and without compensation of the line impedance [① in Fig. 2(a)] for $L_{line} = 10\,\mu H$: **(a)** reference transfer function; **(b)** output impedance. The lines are computed with MATLAB and the circles refer to simulation results obtained for the same operating conditions.

a gain, a phase, or an impedance that has been obtained from circuit simulation. Except for small deviations of the phases for $f < 10\,kHz$ in Fig. 5(b) and Fig. 6(b), i.e., in case of very low impedances, and a single outlier of the phase at $f = 600\,kHz$ in Fig. 5(b), the simulated and calculated results are in very good agreement.

A. Compensation of the line impedance

The solid red lines in Fig 5(a) and Fig 6(a) present the frequency responses of the reference transfer functions, $\underline{V}_{load}/\underline{V}_{ref}$, that result for the PI-P-IVFF and PI-CCFB control structures if the line impedance is compensated according to the parts marked with ① in Fig. 2(a) and Fig. 2(b). The compensation parts use second-order low-pass filters with Bessel characteristics and a cutoff frequency of $f_c = 100\,kHz$. With this, a reduction of the phase lag is achieved for frequencies less than $60\,kHz$, e.g., at $f = 30\,kHz$, the phase lags decrease to $7°$ (compared to $25°$ for the PI-P-IVFF and $24°$ for the PI-CCFB structures, which result without compensation of the voltage across the line). However, a gain greater than $0\,dB$ is observed for $20\,kHz < f < 100\,kHz$, with a maximum of $6\,dB$ at $64\,kHz$.

The solid purple lines in Fig 5(b) and Fig 6(b) reveal the achieved reduction of the output impedance with the investigated compensation method. For the selected cutoff frequency of $f_c = 100\,kHz$, a decreased output impedance is achieved for frequencies up to $60\,kHz$.

Finally, stability is assessed for both control structures, PI-P-IVFF and PI-CCFB, by means of the root locus plots depicted in Fig. 7, which have been obtained for $1\,\mu H < L_{line} < 1\,mH$ and $f_c = 100\,kHz$.[2] This result confirms that the system remains stable within the considered range of line inductances for both control structures. However, with increasing value of L_{line}, one pole pair approaches the origin on a trajectory with an approximately elliptic shape, which corresponds to an increase of the maximum gain of the reference transfer function. Furthermore, the maximum gain is shifted towards lower frequencies for increasing L_{line}.

Fig. 8 depicts the simulated response of the load voltage to a trapezoidal load current waveform with an amplitude of $100\,A$ and a rate of change of $di_{load}/dt = 4\,A/\mu s$. Without compensation of the line impedance [Fig. 8(a)], a load voltage of $40\,V$ results during the change of the load current, which is due to $L_{line} = 10\,\mu H$. With compensation [Fig. 8(b)], steplike changes of v_{load} are observed at $t = 25\,\mu s$ and $t = 75\,\mu s$, which decay to zero within approximately $11\,\mu s$.

[2]The root loci shown in Fig. 7 and Fig. 10(a) have been calculated with all time delays being replaced by 2nd-order Padé approximations, which was found to give accurate results in case of the investigate system.

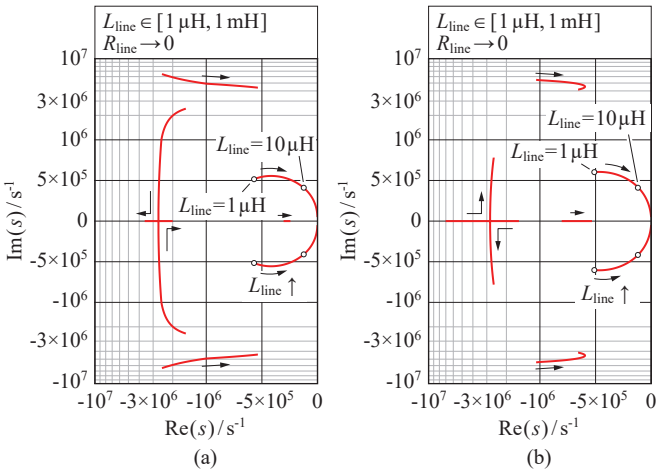

Fig. 7: Root locus plots for the roots of the closed-loop control systems shown in Fig. 2 (from $\underline{V}_{ref}$ to $\underline{V}_{load}$) with compensation of the line impedance, $L_{line} \in [1\,\mu H, 1\,mH]$, $R_{line} \to 0$, and for deactivated emulation of the output impedance ($L_i = R_i = 0$): **(a)** PI-P-IVFF control, **(b)** PI-P-CCFB control. The arrows mark the directions of the root loci for increasing value of L_{line}. The time delays have been replaced by 2nd-order Padé approximations. The real parts of all roots remain negative within the investigated range of line impedance.

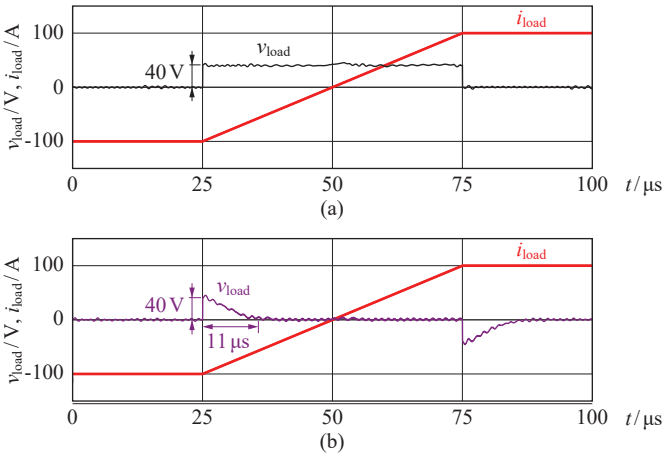

Fig. 8: Simulated waveform of v_{load} for $L_{line} = 10\,\mu H$, in response to a trapezoidal load current waveform with an amplitude of 100 A and a rate of change of $di_{load}/dt = 4\,A/\mu s$: **(a)** uncompensated and **(b)** with compensation of the line impedance. For this simulation, the PI-CCFB control structure has been used.

B. Impedance emulation

Fig. 9(a) and **Fig. 9(b)** depict the frequency characteristics of the reference transfer function and the output impedance, respectively, that result for the bandwidth-limited emulation of $L_i = 200\,\mu H$ and $R_i = 1\,\Omega$ with $f_i = 30\,kHz$ (2nd-order Bessel low-pass filter), for the PI-P-IVFF control structure,[3] and $L_{line} = 10\,\mu H$. The simulation results (circles) confirm the results calculated with MATLAB with respect to gain and phase. According to Fig. 9(b), which includes the frequency response of an ideal impedance equal to $1\,\Omega + s\,200\,\mu H$, the emulated impedance features a low magnitude error up to a frequency of 17 kHz (at $f =$ 17 kHz, the ideal impedance is

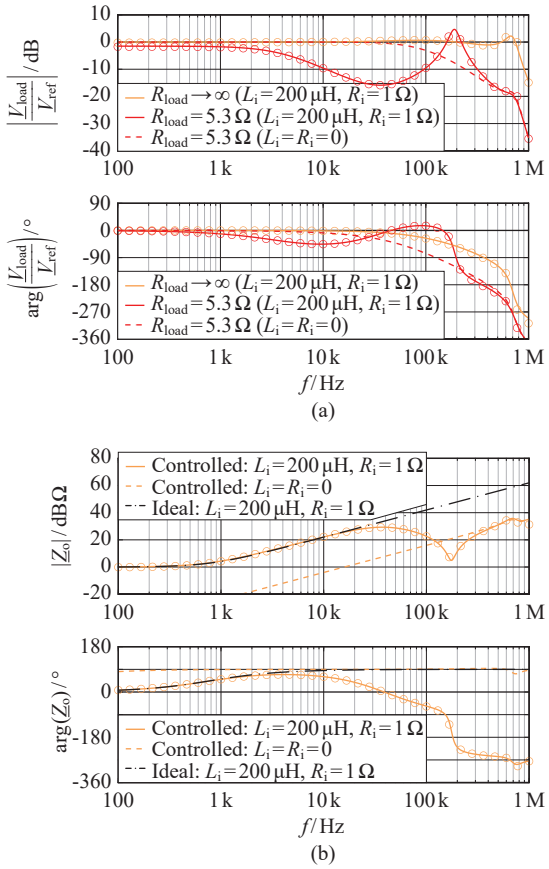

Fig. 9: Frequency characteristics determined for PI-P-IVFF control, $L_{line} = 10\,\mu H$, activated emulation of the inner impedance ($L_i = 200\,\mu H$, $R_i = 1\,\Omega$, $f_i = 30\,kHz$), and deactivated compensation of the line impedance, i.e., with part ② and without part ① in Fig. 2(a): **(a)** reference transfer function; **(b)** resulting output impedance. The lines are computed with MATLAB and the circles denote the simulation results.

21.1 Ω and the emulated impedance is 20.1 Ω). The phase error of the emulated impedance is less than 10° for frequencies below 4 kHz.

The reference transfer function depicted in Fig. 9(a) reveals a resonant gain of 4.7 dB at 190 kHz in case of nominal load, which is not present for $L_i = 0$ and $R_i = 0$ (dotted red line). The observed resonance is related to a complex conjugate pole pair at $s_{1,2} = (-1.4 \times 10^5 \pm 1.2j \times 10^6)\,s^{-1}$ that is part of the root locus plot depicted in **Fig. 10(a)**. This plot, which has been determined for $R_i \in [1\,\Omega, 1\,k\Omega]$, $L_i = 200\,\mu H$, $f_i = 30\,kHz$, and $R_{load} = 5.3\,\Omega$, reveals a pole pair with positive real value for $R_i > R_{i,limit} = 69\,\Omega$, i.e., the system becomes unstable. Based on this finding, the characteristics of $R_{i,limit}(L_i)$ has been computed for different values of L_i, R_{load}, and f_i.[4] **Fig. 10(b)** depicts the resulting characteristics of $R_{i,limit}(L_i)$, which, for increasing values of L_i, first reveals an increase of $R_{i,limit}$. Eventually, $R_{i,limit}(L_i)$ reaches a maximum and decreases to zero if L_i is further increased. In this regard, the maximum feasible value of L_i for stability is characterized by $R_{i,limit}(L_i) = 0$. According to

[3] Similar to Section III-A, nearly the same results have been obtained for the PI-P-IVFF and the PI-CCFB structure. Therefore, only the result for one control structure are shown.

[4] In order to ensure an accurate stability assessment, the characteristics shown in Figs. 10(b), 11, and 12, have been determined with the more robust Nyquist criterion, instead of using Padé approximations together with subsequent evaluations of the root loci.

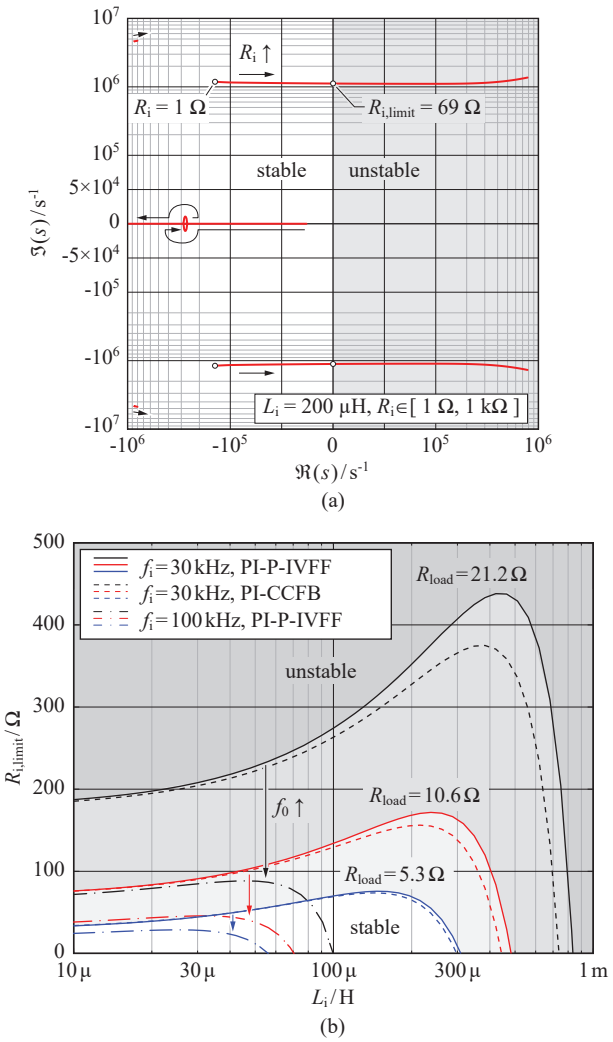

Fig. 10: **(a)** Root locus plot for the closed-loop control systems shown in Fig. 2 (from $\underline{V}_{ref}$ to $\underline{V}_{load}$): $L_i = 200\,\mu H$, $R_i \in [1\,\Omega, 1\,k\Omega]$, $R_{load} = 5.3\,\Omega$, and $f_i = 30\,kHz$ (the arrows indicate the directions of the root loci for increasing R_i); **(b)** Numerically computed stability limits for different control structures and cutoff frequencies, f_i. For both figures, $L_{line} = 10\,\mu H$ applies.

Fig. 10(b), similar characteristics of $R_i(L_i)$ result for the two considered control structures at full load. Furthermore, $R_i(L_i)$ and L_i decrease for increasing load (decreasing value of R_{load}) and increasing cutoff frequency f_i, which confirms the general findings described in Section II-B.

In the course of an evaluation of possible improvements, different modifications of the control structures and circuit parameters have been examined. It is found that the stability limits that are present with PI-P-IVFF control can be increased (by approximately 30 % to 40 % in the considered case) if the load current feedforward is deactivated. Furthermore, a substantial increase of the stability limit can be achieved by connecting a passive inductor to the output of the converter, i.e., by increasing the value of L_{line}. **Fig. 12** depicts the respective result for $L_{line} = 500\,\mu H$. According to this result, inductances up to several millihenry can be emulated. However, it is important to keep in mind that the nominal rms value of the output voltage of the power converter is limited to approximately $\pm 250\,V$. Accordingly, in case of a

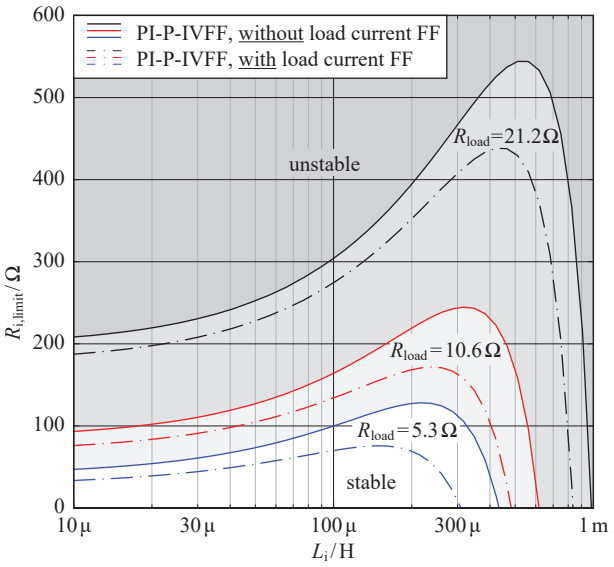

Fig. 11: Computed stability limits for the PI-P-IVFF control structures with and without load current feedforward; $f_i = 30\,kHz$, $L_{line} = 10\,\mu H$.

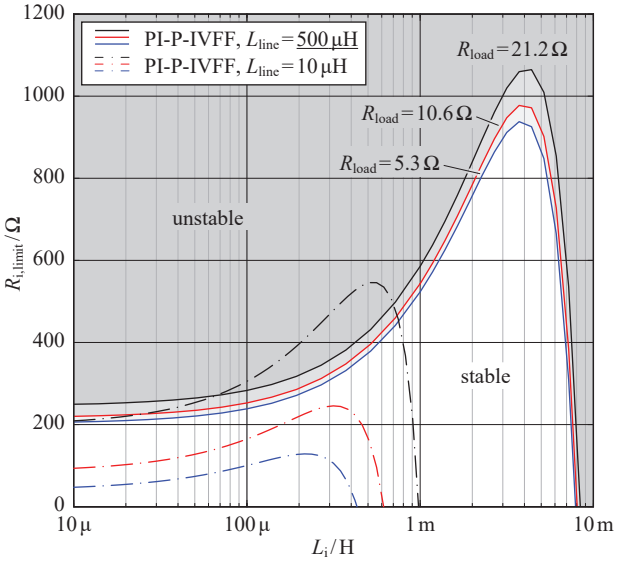

Fig. 12: Computed stability limits for the PI-P-IVFF control structures without load current feedforward, for $f_i = 30\,kHz$ and an increased line inductance of $L_{line} = 500\,\mu H$.

large inner impedance, only very low AC output power can be delivered to a load at high frequencies (e.g., for $L_i = 1\,mH$, $R_{load} = 5.3\,\Omega$, and $f = 20\,kHz$, the resulting rms output voltage at the load resistor is 10.5 V, which gives a power of 21 W). Finally, it is found that an increase of the stability limit, $R_{i,limit}(L_i)$, is feasible by proper adjustment of the output filter, e.g., by increasing the value of L_1 and decreasing the value of C_1 by the same factor. However, such an adjustment may not be feasible due to certain boundary conditions that need to be considered in the course of the design of the converter (e.g., a maximum allowable voltage drop across L_1 at the maximum output frequency).

Fig. 13 presents the simulated waveform of the load voltage that results for a trapezoidal load current with an

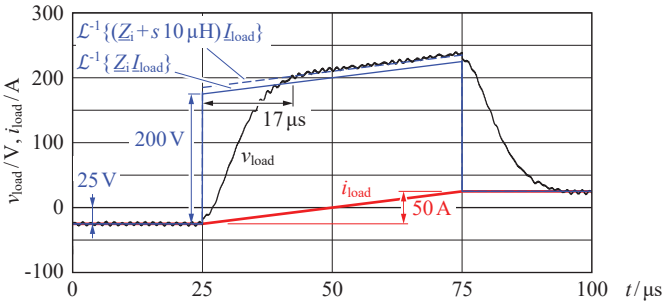

Fig. 13: Simulated response to a trapezoidal load current waveform with an amplitude of 25 A and $\mathrm{d}i_{load}/\mathrm{d}t = 1\,\mathrm{A/\mu s}$. Simulated configuration: PI-P-IVFF control without load current feedback, $L_i = 200\,\mu H$, $R_i = 1\,\Omega$, $L_{line} = 10\,\mu H$.

amplitude of 25 A and a rate of change of the load current of $\mathrm{d}i_{load}/\mathrm{d}t = 1\,\mathrm{A/\mu s}$. This simulation has been conducted for the PI-P-IVFF control structure (without load current feedback), $L_i = 200\,\mu H$, $R_i = 1\,\Omega$, and $f_i = 30\,\mathrm{kHz}$. Compared to the immediate response of the ideal impedance, $\underline{Z}_i = R_i + sL_i$ (solid blue line in Fig. 13), to the change of the gradient of i_{load} at $t = 25\,\mu s$ and $t = 75\,\mu s$, the load voltage, v_{load}, gradually changes and reaches the final value after approximately 17 µs. Furthermore, the output voltage exceeds the solid blue line during $40\,\mu s < t < 76\,\mu s$ in Fig. 13. This is due to the nonzero impedance of the line, $L_{line} = 10\,\mu H$, which leads to an effective impedance of $\underline{Z}_i + sL_{line}$.

IV. Conclusion

The evaluation of a simplified control structure reveals four critical parameters with respect to stability:

1) the time delay of the control system (from the event of the measurement to the instant when the output voltage of the switching stage changes);
2) the cutoff frequencies of the low-pass filters used to limit the bandwidths of impedance compensation and emulation, f_c and f_i;
3) the value of the load resistance;
4) the value of the line impedance, e.g., a large value of L_{line} can lead to instability in case of impedance compensation and a small value of L_{line} reduces the stability boundary (maximum values of L_i, R_i) in case of impedance emulation.

The effectivenesses of the methods for compensating or emulating the output impedance of the converter system have been evaluated with detailed numerical models and comprehensive simulations for two different control structures. This evaluation returns very similar results for both control structures, which indicates that the considered line inductance of $L_{line} = 10\,\mu H$ has a dominating impact on the dynamic performance of the converter system. Furthermore, the impedance compensation method is found to achieve a reduction of the phase lag of the output voltage and a decrease of the total output impedance of the converter system (at the interface to the load, R_{load}), in the frequency range up to 60 kHz (for a cutoff frequency of $f_c = 100\,\mathrm{kHz}$). However, with active compensation of the line impedance, the reference transfer function is subject to a maximum deviation (from 0 dB) of 6 dB at 64 kHz.

The emulation of a defined impedance of $1\,\Omega + s\,200\,\mu H$ with a cutoff frequency of $f_i = 30\,\mathrm{kHz}$ reveals a magnitude error of less than 5% and a phase error of less than 10° in the frequency ranges up to 17 kHz and 4 kHz, respectively. A stability analysis reveals that the maximum allowable value of R_i is linked to the value of L_i. Furthermore, it is found that the following adjustments of the control structure or converter hardware enable an increase of the allowable values for R_i and L_i: the load current feedforward is deactivated in the PI-P-IVFF control structure; the filter inductance is increased and the filter capacitance is decreases by the same factor; a dedicated inductor is placed between the converter and the load.

In a next step, further possible improvements need to be identified in the course of a holistic system optimization, which includes the investigation of the control structures with each of the feedforward paths being enabled or disabled, the optimization of the controller parameters, and the optimization of the cutoff frequencies of the low-pass filters. With this, the optimization aims to identify most suitable settings for impedance compensation and emulation, e.g., aim for large maximum values of L_i and R_i.

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