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Closed-Loop di/dt & dv/dt Control and Dead Time Minimization of IGBTs in Bridge Leg Configuration

Y. Lobsiger,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Closed-Loop $\mathrm{d}i/\mathrm{d}t$ & $\mathrm{d}v/\mathrm{d}t$ Control and Dead Time Minimization of IGBTs in Bridge Leg Configuration

Yanick Lobsiger and Johann W. Kolar
Power Electronic Systems Laboratory
ETH Zurich
Physikstrasse 3, 8092 Zurich, Switzerland
Email: lobsiger@lem.ee.ethz.ch

***Abstract*—In order to optimize the clamped inductive load (hard) switching behavior of IGBTs in voltage source power electronic converters, i.e. to ensure a defined switching behavior independent of the load current level, the DC-link voltage or the junction temperature, in recent publications an IGBT gate drive for controlling $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ has been proposed and experimentally verified for chopper circuits.**

In this paper, the necessary modifications of the gate drive concept for applications with IGBTs in bridge leg configuration are investigated. For the purpose of a safe operation and a minimum distortion of the generated output voltage waveform, a reciprocal interlocking of the bridge leg's IGBTs is introduced in addition. Finally, the proposed concept is experimentally verified for regular operation and for different types of short circuits of the load.

***Index Terms*—Closed-Loop IGBT Gate Driver**

I. Introduction

Insulated Gate Bipolar Transistor (IGBT) modules with anti-parallel free wheeling diodes (FWD) are widely used in clamped inductive load (hard) switching voltage source power electronic converters, e.g. in uninterruptible power supplies (UPS) or AC variable speed drive systems as shown in Fig. 1.

In order to minimize the IGBTs' switching delay times and to ensure a specified switching behavior in the Safe Operating Area (SOA), that is independent of the load current level, the DC-link voltage or the junction temperature, a closed-loop IGBT gate drive concept providing $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control has been proposed, modeled and experimentally verified for chopper applications [1, 2]. This gate drive concept enables a defined trade-off between switching losses and conducted and / or radiated Electromagnetic Interference (EMI) of the power semiconductors.

In this paper, the application of the formerly proposed $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ closed-loop gate drive concept is investigated for voltage source converter topologies with IGBTs in bridge leg configuration. Based on an analysis of the characteristic turn-on and turn-off switching transitions for positive and negative direction of the load current, the gate drive is extended by protective circuits in Section II. In order to ensure a safe operation and a minimization of the dead time interval between the two complementary power transistors in a bridge leg, i.e. the delay time between a turn-off and the complementary turn-on command, a reciprocal interlocking and active dead time minimization is proposed thereafter in Section III. Subsequently, short circuit (SC) detection and turn-off methods for the different SC cases are described in Section IV. A comprehensive experimental verification of the proposed concepts by means of a hardware demonstrator for a 1.2 kV, 300 A bridge leg IGBT module is finally presented in Section V.

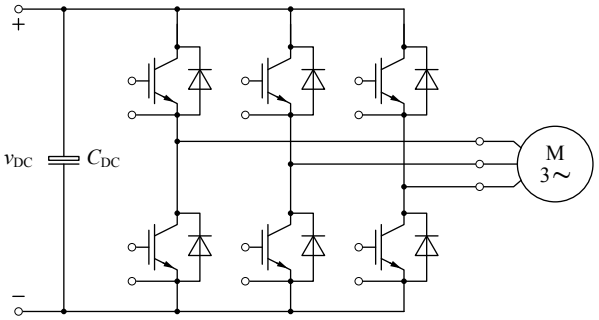

Fig. 1: Schematic diagram of a three-phase AC variable speed drive system representing a typical application example of clamped inductive load switching IGBTs in bridge leg configuration.

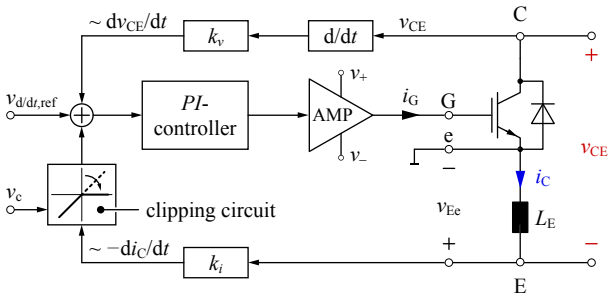

Fig. 2: Block diagram of the basic proposed closed-loop active gate drive concept with joined $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control loops for IGBTs in chopper configurations [1, 2].

II. Safe switching at normal operation

In this section, the application of the formerly proposed $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ closed-loop IGBT gate drive, cf. Fig. 2, for IGBTs in bridge leg configuration is investigated and the need for additional control methods and circuits is identified.

The basic operating principle of this gate drive concept is to control the current and voltage slopes, i.e. $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$, with a PI-controller and a closed-loop approach.

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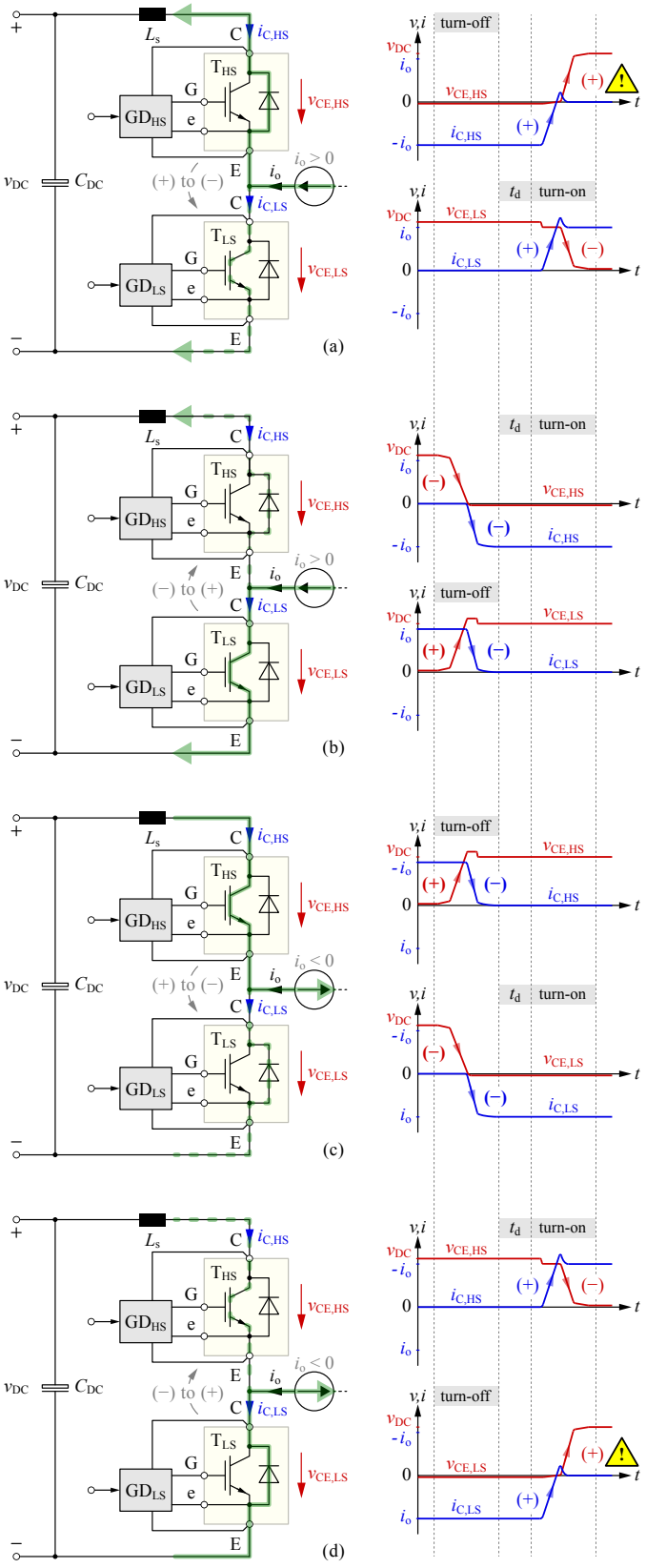

Fig. 3: Current paths and corresponding schematic waveforms of the IGBT currents $i_{\mathrm{C,LS/HS}}$ and voltages $v_{\mathrm{CE,LS/HS}}$ at the switching transients. (a) and (c): transition from positive (+) to negative (−) output voltage; (b) and (d): transition from (−) to (+). (a) and (b): positive sign of the load current i_{o}; (c) and (d): negative sign of i_{o}.

At hard switching, a temporal separation of the current- and voltage slopes is assumed [1], what enables the utilisation of only one common control reference signal, $v_{\mathrm{d/dt,ref}}$, one common PI-control amplifier, and simultaneously active negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and positive $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback signals. To turn-on an IGBT, $v_{\mathrm{d/dt,ref}}$ is set to a constant positive value, which first leads to the control of the rising current, i.e. with a negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback signal, and then to the control of the falling voltage, i.e. with also a negative $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback signal. To initiate a turn-off, $v_{\mathrm{d/dt,ref}}$ is set to a constant negative value, which leads to the control of the rising voltage prior to the control of the falling current.

In chopper applications, where only one IGBT exists per leg, all the switching transients, i.e. the current and voltage commutations between the IGBT and the opposite FWD, are evoked by the IGBT itself, thus no interference from another switching IGBT occurs to the control and to the feedback signals.

Contrary to such chopper circuits, in bridge leg applications, cf. Fig. 1 and Fig. 3, two actively switching power semiconductors with antiparallel FWDs are connected in series between the positive and negative DC voltage rail. This enables an active connection of the output terminal to either the (+) or the (−) DC-link rail independent on the sign of the output and / or load current i_{o}. Such an arrangement of the power semiconductors implies, that their difference in current levels is always equal to the load current,

$$i_{\mathrm{C,LS}} - i_{\mathrm{C,HS}} = i_{\mathrm{o}}, \tag{1}$$

and their sum of voltages equals the DC-link voltage less the voltage drop across the parasitic stray inductance L_{s} in the commutation loop,

$$v_{\mathrm{CE,LS}} + v_{\mathrm{CE,HS}} = v_{\mathrm{DC}} - L_{\mathrm{s}} \frac{\mathrm{d}i_{\mathrm{C,LS/HS}}}{\mathrm{d}t}. \tag{2}$$

As will be shown later, these dependencies in the currents and voltages of the two complementary IGBTs in a bridge leg arrangement will cause unwanted interaction between the control loops on the gate drives of these IGBTs. Prior to that, the different possible types of switching transition will be discussed in the following.

A. *Identification of the possible types of switching transition*

At each output voltage transition, i.e. from (+) to (−) or vice versa, the commutation and the according current paths in the commutation loop depend on the sign of the output current i_{o}. Independent of the direction of the load current the turned-on IGBT is turned-off first and the opposite IGBT is turned-on thereafter, in order to prevent a cross conduction current and / or transient short circuit of the DC-link. The different possible current paths in the bridge leg and the corresponding schematic current and voltage waveforms at the switching transitions are depicted in Fig. 3. Thereby, four different types of switching, denominated as (I) to (IV), can be distinguished as will be explained in the following paragraph.

At the instant of turning-off a turned-on IGBT either its

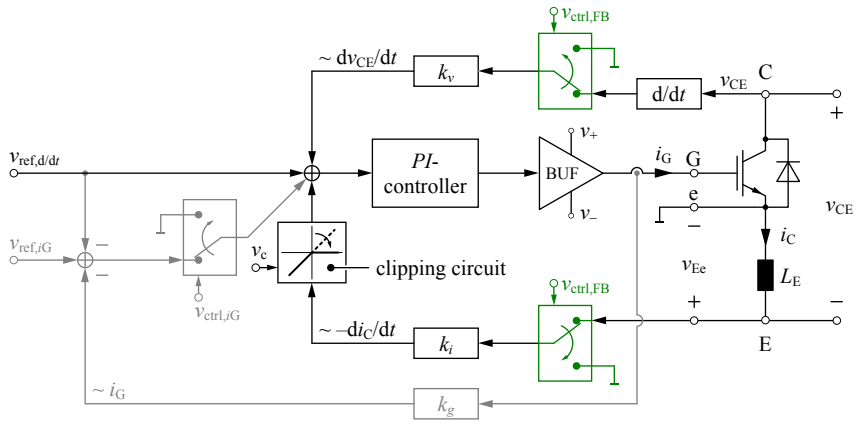

Fig. 4: Block diagram of the formerly proposed closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ IGBT gate drive (dark-colored) with additional gate current control (light-colored) [1, 2] and additional deactivation switches for the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback signals (green-colored) proposed in this paper and / or as required for bridge leg applications.

	$i_{\mathrm{o}} > 0$	$i_{\mathrm{o}} < 0$
$(+)$ to $(-)$	1. $\mathrm{T_{HS}}$ soft turn-off (I)	1. $\mathrm{T_{HS}}$ hard turn-off (II)
transition	2. $\mathrm{T_{LS}}$ hard turn-on (IV)	2. $\mathrm{T_{LS}}$ soft turn-on (III)
$(-)$ to $(+)$	1. $\mathrm{T_{LS}}$ hard turn-off (II)	1. $\mathrm{T_{LS}}$ soft turn-off (I)
transition	2. $\mathrm{T_{HS}}$ soft turn-on (III)	2. $\mathrm{T_{HS}}$ hard turn-on (IV)

TABLE I: Possible types of switching transition.

antiparallel diode or the IGBT itself is conducting the load current. In case the antiparallel diode is conducting, the IGBT is performing a soft turn-off (I), cf. Fig. 3 (a) and (d), since the diode keeps conducting. In the other case where the IGBT is conducting, the current is commutating to the opposite diode and thus the IGBT is performing a hard turn-off (II), cf. Fig. 3 (b) and (c). At turning-on an IGBT either its antiparallel diode or the opposite diode is conducting the load current. In case the antiparallel diode is conducting, the IGBT is performing a soft turn-on (III), cf. Fig. 3 (b) and (c), since the diode keeps conducting. In the other case where the opposite diode is conducting, the current is commutating to the IGBT and thus it is performing a hard turn-on (IV), cf. Fig. 3 (a) and (d). As has been shown, the type of switching for the low- and high-side IGBT depends on the sign of i_{o} as it is summarized in Table I.

Due to symmetry considerations of the low- and high-side, only two different basic switching transition types, denominated as (A) and (B) in the following, can be distinguished.

(A) Soft turn-off (I) followed by hard turn-on (IV), i.e. Fig. 3 (a) and (d)
(B) Hard turn-off (II) followed by soft turn-on (III), i.e. Fig. 3 (b) and (c)

In the following, these two transition types are evaluated regarding unwanted impacts on the closed-loop control of the two complementary IGBT gate drives, and a modification of the gate drive is proposed thereafter.

B. Modification of the closed-loop IGBT gate drive

At the switching transition type (A), cf. Fig. 3 (a) and (d), the turned-on IGBT is turned-off soft first with neither $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ nor $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback, i.e. the gate is discharged fast. After the interlock time, t_{d}, the complementary IGBT is turned-on hard, whereas at its feedback terminals a positive $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and a negative $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback signal occurs, as it is required for the closed-loop control. However, since the two IGBTs are connected in series, their current difference equals the output current, cf. (1), and the sum of their voltages corresponds basically to the DC-link voltage, cf. (2). As a direct consequence, the gate drive of the turned-off IGBT receives a positive $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and an undesired positive $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback signal in its off-state, cf. Fig. 3 (a) and (d). In the case of different absolute values of the positive and negative $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ references of both gate drives or due to tolerances of the reference signals and the feedback gains, any positive difference between the negative reference and positive $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback on the gate drive of the turned-off IGBT would be integrated by the PI-controller. This in turn could lead to a re-turn-on of the power transistor during its off-state. This then would cause an unwanted cross conduction current leading to increased switching losses or even to a short circuit of the DC-link and thus to a malfunction of the converter system.

At the switching transition type (B), cf. Fig. 3 (b) and (c), the turned-on IGBT is turned-off hard first, resulting in positive $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ and negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback signals, that are needed for the closed-loop control, while the complementary IGBT stays is in the off-state. Thereby, the gate drive of this complementary IGBT receives an unwanted negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and a negative $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback signal in its off-state, cf. Fig. 3 (b) and (c). Since at this interval of the switching transients the full DC-link voltage is already occurring across the turning-off IGBT, a precipitate turn-on of the complementary IGBT in this particular case would not lead to a cross conduction current and isn't an issue in principle.

As a consequence, in order to maintain a safe operation

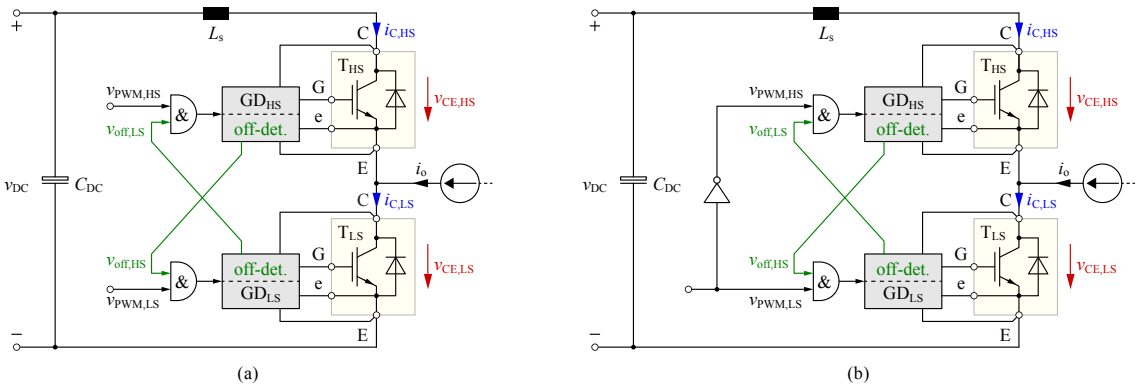

Fig. 5: Shoot through prevention and interlocking time minimization by reciprocal interlocking of the low- and high-side IGBTs by means of IGBT off-state detection for (a) individual PWM signals of the switches or (b) PWM signals derived directly from a single command signal.

of the IGBTs in any case, it is important that the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback of a closed-loop gate drive is disabled once the corresponding IGBT enters its off-state, i.e. once the blocking ability of the semiconductor is achieved. Any externally evoked positive $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ signal then not leads to a recharge of the gate and thus the IGBT stays in its safe off-state. As will be shown in Section IV, disabling the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback is also needed in addition, in order to securely turn-off some particular types of load short circuits.

In practice, as illustrated in Fig. 4, the deactivation of the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback signals could be realized by means of high-speed (video) multiplexers, each with one input connected to the corresponding feedback signal and the other connected to ground. To know whether the IGBT is in off-state and accordingly to detect at which instant the feedbacks need to be disabled, a detection circuit is required that monitors whether the IGBT is in blocking state or not. The most simple solution is here to test, whether the gate voltage v_{Ge} is on a level below the threshold voltage $v_{\mathrm{Ge,th}}$.

This feedback signal deactivation prevents a parasitic turn-on of the IGBTs during their off-state and thus enables the safe switching in normal operating mode.

III. Interlocking and Dead Time Minimization

To ensure a safe operation without shoot-through, a simultaneous turn-on of both IGBTs in a bridge leg has to be strictly avoided. A simple and common solution for this problem is to delay each turn-on command by a preset time interval to ensure an interlocking of the two IGBTs. This interlocking time t_{d} is typically selected for the worst case switching times of the IGBTs at maximum DC-link voltage, load current level, and junction temperature, i.e. at part load condition the turn-on command is delayed more than actually needed. Since this interlocking time leads to a delay of the subsequent IGBT's turn-on, an output voltage distortion, depending on the sign of the load current, occurs especially at part load condition and for a low modulation index M, and must therefore often be compensated [3–5]. In order to potentially avoid this compensation and / or to minimize the output voltage distortion, the interlocking time should ideally be adapted to the actual switching condition.

The just proposed off-state detection circuit of the closed-loop IGBT gate drive, that is indicating the blocking ability of an IGBT and used to ensure the safe operation in normal operating mode, can further be utilized to minimize the interlocking time between the IGBTs in a bridge leg arrangement as shown in Fig. 5. Instead of a large preset delay of the turn-on command, the turn-on of an IGBT can be directly enabled by the signal indicating the blocking ability of the opposite IGBT and vice versa, similar to the concept proposed in [6], with only two additional logic signal isolators. This reciprocal interlocking circuit dynamically adapts the turn-on delay to the load condition, i.e. the actual turn-off time of the complementary IGBT, and thus allows to apply directly inverted PWM gate signals to the low- and high-side gate drive without the need of any interlocking as depicted in Fig. 5 (b), i.e. the number of the gate signals, that need to be generated and distributed from the main control unit, can be halved if desired.

IV. Short Circuit Detection and Turn-Off

At normal operation a safe switching of the IGBTs in a bridge leg is guaranteed by reciprocal interlocking of the complementary transistors and by means of a robust closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control of the switching transients, as it has been explained so far. Nevertheless, a failure of e.g. a gate drive, an IGBT or the load can at any time lead to a short circuit (SC) with a corresponding SC impedance Z_{SC} of the output terminal to either the $(+)$ or the $(-)$ DC-link rail for the topology considered in Fig. 1. Similar as for conventional passive gate drivers, a robust SC detection and a safe SC turn-off is also needed for the closed-loop gate drive. For this purpose the various SC cases must be investigated in the context of the closed-loop gate drive.

There mainly exist two different types of IGBT SC [7], whereby the SC type I corresponds to a turn-on of a turned-off IGBT into an existing SC impedance Z_{SC} at the output terminal of the bridge leg. The associate sequence and the

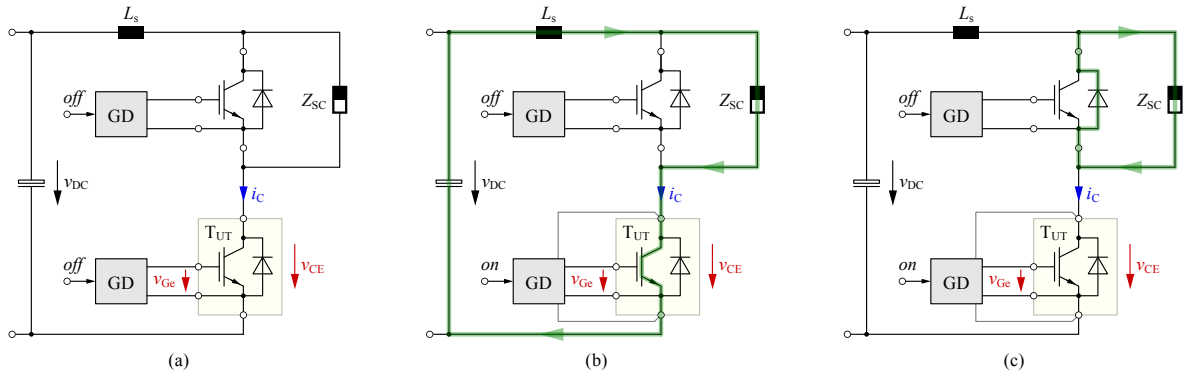

Fig. 6: Sequence (a) to (c) during an IGBT SC type I. (a) The SC impedance Z_{SC} is already present prior to the turn-on of $\mathrm{T_{UT}}$. (b) $\mathrm{T_{UT}}$ gets the turn-on command and evokes the SC by turning-on. (c) $\mathrm{T_{UT}}$'s gate drive detects the SC and turns-off.

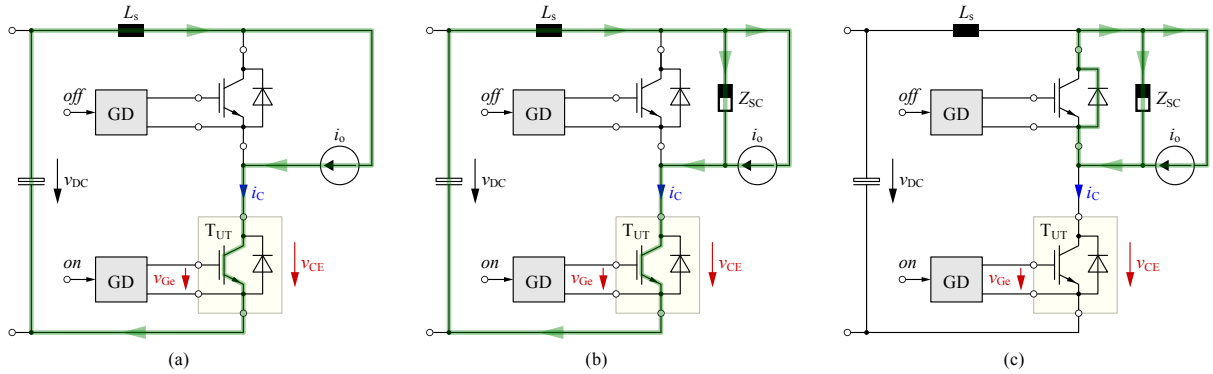

Fig. 7: Sequence (a) to (c) during an IGBT SC type II. (a) $\mathrm{T_{UT}}$ is turned-on and is carrying the load current i_{o}. (b) A SC with the impedance Z_{SC} occurs at the output terminal, i.e. a SC current is evoked. (c) $\mathrm{T_{UT}}$'s gate drive detects the SC and turns-off.

current paths for this type of SC are depicted in Fig. 6. At the SC type II the IGBT is already in the on-state and is carrying the load current i_{o}, when the SC occurs at the output terminal. The corresponding sequence and the current paths are shown in Fig. 7. Independent of the type of the SC, its impedance Z_{SC} can basically feature an arbitrary value, that mainly depends on the location and source for the SC.

For SC type I with a low short circuit impedance Z_{SC} and a small commutation inductance L_{s}, the IGBT's voltage v_{CE} stays close to the (+) DC-link potential during the interval of current rise. This corresponds to the case of hard turn-on switching at nominal operation, i.e. the rate of rise of the current, $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$, is actively controlled to its reference value by the closed-loop gate driver. If the SC is detected in this turn-on interval, it can be turned-off by setting the control reference signal $v_{\mathrm{ref,d}/\mathrm{d}t}$ on the gate drive from the positive to a negative value.

In order to detect this type of SC, typically the current i_{C} must be measured. In practice, there exist various methods to detect a SC type I, such as a shunt resistor in the current path, a sense IGBT, a current transformer, a Rogowski coil with integrator circuit or a gate voltage pattern analyzing circuit [8, 9] to name a few. These circuits could also be used in this case. A more simple and cheaper solution is to utilize the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback signal of the closed-loop control, that is based on the voltage drop across the parasitic bond wire inductance L_{E} in the IGBT module. By means of a simple resettable integrator circuit, as it is depicted in Fig. 8 (a), i_{C} can be measured during the switching transients, i.e. the closed-loop gate drive can very simply be extended by a SC type I detection circuit without the need of an additional current sensing component.

At SC type I with large L_{SC} and at SC type II v_{CE} is low and the IGBT is saturated in the interval where i_{C} is rising, until the current reaches a level where the IGBT starts to desaturate. Thereby, v_{CE} will rise, too. This incidence is typically utilized to detect such a type of SC, i.e. the on-state voltage $v_{\mathrm{CE,on}}$ is monitored after a specific time from the turn-on transients, cf. Fig. 8 (b). However, the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ closed-loop gate drive's basic principle is based on the idea, that i_{C} and v_{CE} are not changing simultaneously, to achieve the desired control [1]. Since this is not true for these now considered SC cases, the additional positive $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback at turn-off would affect the control, i.e. the gate would be discharged extremely fast leading to an unwanted fast SC turn-off and accordingly to a destruction of the device due to overvoltage. As a result, turning-off this type of SC with the closed-loop approach is not reasonable. Accordingly, the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedbacks must be deactivated directly after the turn-on transients. In this case, a safe turn-off of the SC can be achieved by means of the implemented gate current control of the proposed gate drive, cf. Fig. 4, which otherwise is used to control the gate current in the turn-on and turn-

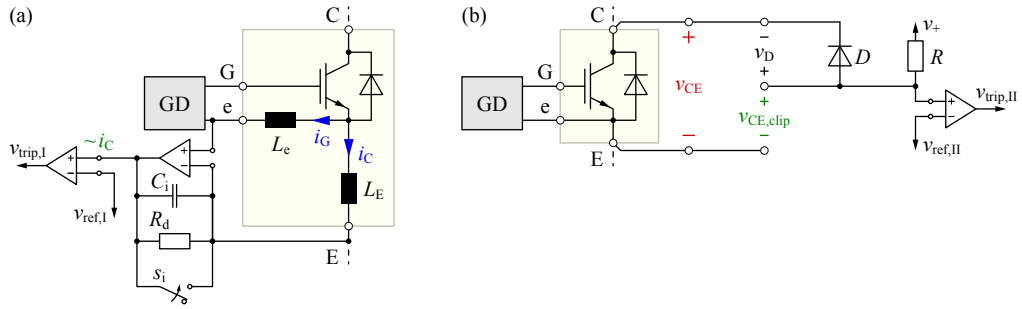

Fig. 8: (a) Proposed i_C measurement and SC type I detection circuit by means of a resettable integrator circuit. (b) v_{CE} clipping circuit to measure v_{CE} in on-state and to detect the SC type II.

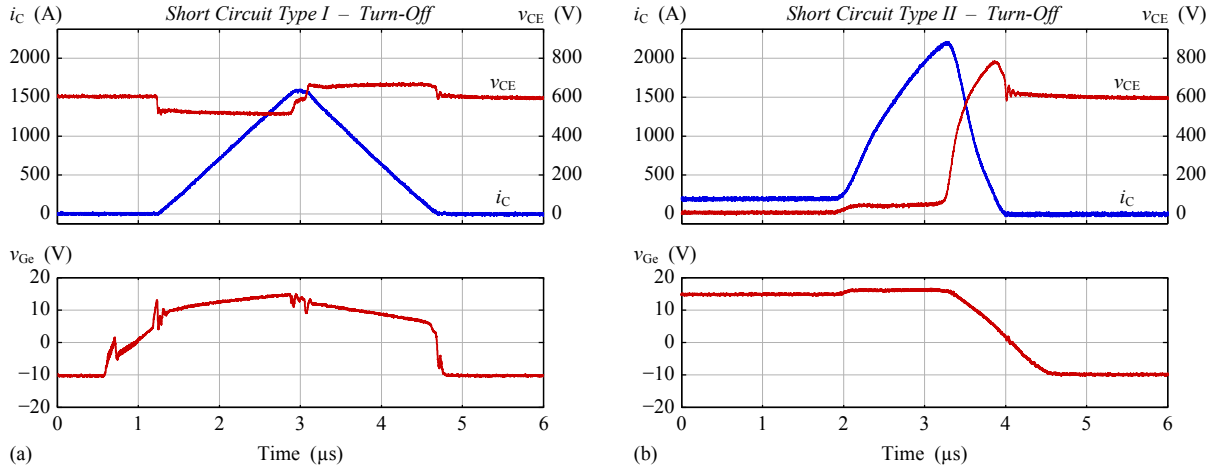

Fig. 9: Measured current and voltage waveforms during the evoking and at turning-off the two different SC types, i.e. (a) shows SC type I and (b) depicts SC type II.

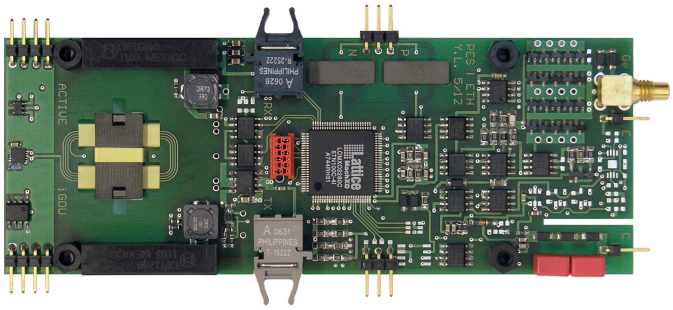

Fig. 10: Prototype of the closed-loop IGBT gate drive; PCB dimensions: 50 mm x 133.3 mm and / or 1.97 in x 5.25 in

off delay intervals of the switching transients. By setting the reference signal for the gate current to a small negative value, this type of SC can safely be turned-off, which is similar to the passive gate drivers that feature an additional high-ohmic gate turn-off path for the case of a SC turn-off.

V. Experimental Results

A hardware prototype of the proposed closed-loop $\mathrm{d}i_C/\mathrm{d}t$ and $\mathrm{d}v_{CE}/\mathrm{d}t$ gate drive was developed, cf. Fig. 10, that contains all described measurement and control circuits. A finite state machine is implemented in the Complex Programmable Logic Device (CPLD) in order to generate the desired trigger and reference signals for the closed-loop control and handle e.g. the deactivation of the feedback signals or the detection of the different types of SC. As IGBT module, a 1.2 kV, 300 A bridge leg IGBT module (Infineon FF300R12MS4) in an EconoDUAL housing has been used.

A. Short circuit turn-off

The two basic types of SC of the load have been experimentally verified according to the proposal in Section IV. Fig. 9 (a) depicts the current and voltage waveforms at the SC type I. Thereby, $\mathrm{T_{UT}}$ was turned-on whereby the complementary IGBT of the bridge leg was already turned-on. The $\mathrm{d}i_C/\mathrm{d}t$ reference signal was set to $1\,\mathrm{kA}/\mu\mathrm{s}$, to turn-on $\mathrm{T_{UT}}$. After the SC was detected by the SC type I detector, cf. Fig. 8 (a), the SC was turned-off safely with a $\mathrm{d}i_C/\mathrm{d}t$ reference of $-1\,\mathrm{kA}/\mu\mathrm{s}$. The waveforms at the SC type II are shown in Fig. 9 (b). Thereby, $\mathrm{T_{UT}}$ was conducting the load current i_o, while a SC was initiated by a fast turn-on of the complementary IGBT. By the desaturation detection circuit, cf. Fig. 8 (b), the SC was detected and also safely turned-off with disabled $\mathrm{d}i_C/\mathrm{d}t$ and $\mathrm{d}v_{CE}/\mathrm{d}t$ feedback signals and a gate current controller reference signal of $-3\,\mathrm{A}$. In accordance with these measurement results, it can be summarized, that the gate drive is able to detect and securely turn-off the two basic types of SC of the load.

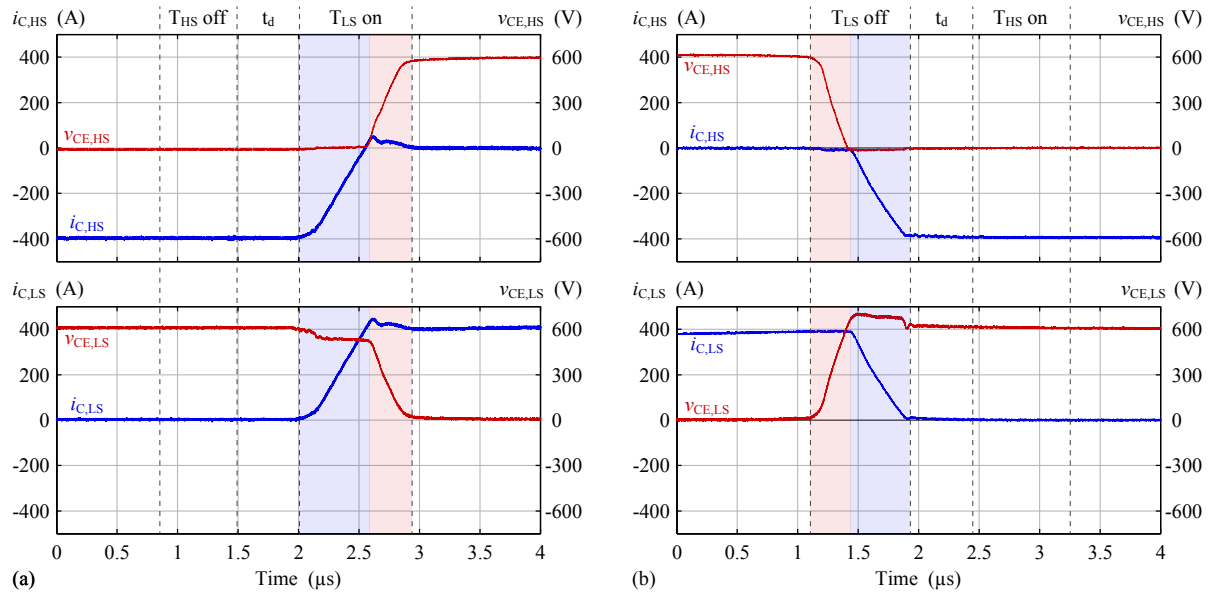

Fig. 11: Measurements at closed-loop control of the two different types of switching transition. (a) equals the switching type (A), i.e. a soft turn-off is followed by a hard turn-on. (b) corresponds to the switching type (B), whereby a hard turn-off leads a soft turn-on.

B. Normal operation

To experimentally verify the safe switching in normal operation, double pulse tests have been performed by means of a hardware prototype. Due to the mentioned symmetry considerations of the low- and high-side, each of the two different types (A) and (B) of switching transition, cf. Section II-A, has only been measured once. The measured current and voltage waveforms are depicted in Fig. 11. Thereby, the absolute value of the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ reference was set to $1\,\mathrm{kA}/\mu\mathrm{s}$ and the absolute value of the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ reference was set to $2\,\mathrm{kV}/\mu\mathrm{s}$. As can be seen, the waveforms are exactly as they were expected to be in Section II. A robust operation of the closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ IGBT gate drive even for IGBTs in bridge leg configurations is thus enabled by the additional circuits and control methods proposed in this paper.

VI. Conclusion

In this paper, a $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ closed loop gate drive formerly proposed by the authors for chopper applications has been extended for IGBTs in bridge leg configuration. A safe operation at normal and short circuit condition is ensured, and the interlock delay time between upper and lower IGBT is minimized. This now enables an application of the closed-loop IGBT gate drive concept in numerous applications such as AC variable speed drives or UPS systems. Therewith, a degree of freedom in the design space of the converter design is gained, which allows to ensure a defined trade-off between switching losses and EMI independent of the load current level, the DC-link voltage or the junction temperature of the power semiconductors. Furthermore, the closed-loop gate control allows to combine IGBTs from different manufacturers for the realization of a converter system without requirement of tuning gate resistors etc. as typically required for conventional gate drive circuits. Accordingly, the proposed gate drive concept also facilitates a minimization of production and / or maintenance costs and therefore could support a widespread application of power electronic converters in industry and renewable energy systems.

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