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# Comparative Evaluation of SiC and Si PV Inverter Systems Based on Power Density and Efficiency as Indicators of Initial Cost and Operating Revenue

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# Comparative Evaluation of SiC and Si PV Inverter Systems Based on Power Density and Efficiency as Indicators of Initial Cost and Operating Revenue

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***Abstract*—In this paper, two three-level three-phase all Si PV inverter topologies are compared to a standard two-level three-phase topology employing SiC-based power transistors. In a comparative evaluation based on multi-objective component modeling, the performance trade-offs between achievable efficiency and power density are systematically analyzed for all systems. On the one hand, this is to investigate the potential of SiC to decrease the system complexity while achieving similar or better performance. The analysis shows that a similar power density and efficiency can be obtained with the SiC two-level system while requiring only one tenth of the chip area when compared to the three-level Si inverters. On the other hand, in a next step, using power density and efficiency as indicators for initial inverter cost and operational revenue, the trade-off analysis will allow to determine the economically optimal system dimensioning.**

***Index Terms*—Photovoltaic systems, SiC semiconductors, Cost benefit analysis, Reliability.**

## I. Introduction

The prolonged research activities undertaken at several semiconductor manufacturers has recently resulted in first commercially available and mature SiC-based power transistors, such as MOSFETs, JFETs and BJTs [1], [2], [3]. In literature, the advantages of SiC- over standard Si-based devices have been discussed for several years and have unanimously found to be the superior blocking voltage capabilities and the significantly decreased switching and conduction losses (exemplarily [4], [5]).

In recent years, the rapidly emerging field of photovoltaic (PV) power converters has been proposed as a major field of application where the cost premium of SiC power transistors can be justified by substantial performance gains. Analyzing the respective literature for three-phase PV inverters, such as [7], [8], [9], [10], [11], it becomes apparent that divergent opinions exist on how to exploit best the performance advantages offered by SiC. In [7], it is recommended to use the low-loss potential of SiC exclusively to maximize the converter efficiency rather than the power density. It is argued that the accumulated operational revenue due to more power fed into the grid will be higher than the savings on smaller passive components. In contrast, [8] suggests to focus on increasing the power density. This can be achieved by employing higher switching frequencies and switches with high rated blocking

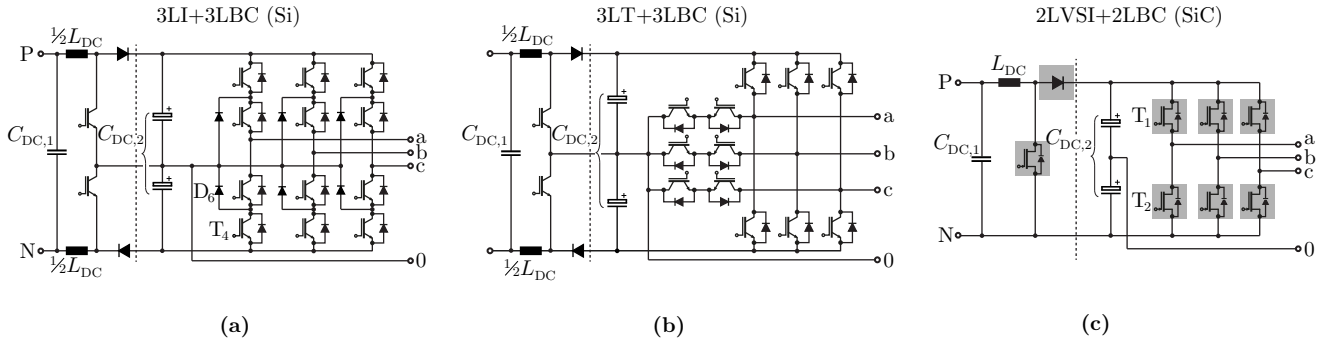


**Fig. 1:** Topologies considered for the comparative analysis between Si- and SiC-based semiconductors in PV inverters. **(a)** Three-level I-type topology with input three-level DC/DC boost converter (3LI+3LBC) employing Si IGBTs and diodes. **(b)** Three-level T-type topology with input three-level DC/DC boost converter (3LT+3LBC) employing Si IGBTs and diodes. **(c)** Two-level voltage source inverter topology with input two-level DC/DC boost converter (2LVSI+2LBC) employing SiC JFETs and diodes (highlighted grey).

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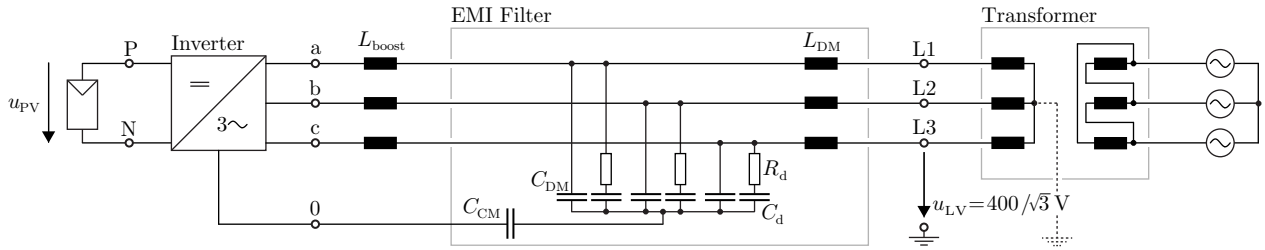


**Fig. 2:** Generic topology of the considered three-phase PV inverter with boost inductors and output $LC$ EMI filter. A $\Delta$-Y transformer connects the 400 V low voltage secondary side (non-public industrial grid) to a European 50 Hz medium voltage grid. With minor adoptions in the filter due to different applicable EMI emission limits [6], the same topology could also be used in a (grounded) public low voltage grid.

voltages of 1700 V. The latter enables omitting the DC/DC boost converter stage which is normally required in 400 V AC grid applications. Finally, [9], [10], [11] pursue a mixed strategy of increasing both efficiency and power density (by means of higher switching frequencies). Switching frequencies of up to 144 kHz are reported.

The main shortcoming of the aforementioned contributions is the lack of a systematic analysis of the optimal mix between efficiency improvement and power density increase. Moreover, except in [11], the impact of increased switching frequencies and faster switching speeds on important converter components, such as the EMI filter, heat sink, PCB or housing is mostly neglected or only qualitatively discussed.

In this paper, the potential of SiC power transistors is investigated by means of comparing two commonly used, high-efficient but rather complex three-level three-phase topologies employing standard Si devices (**Fig. 1(a),(b)**) to a simpler, more industry-friendly and potentially more reliable two-level topology which is equipped with superior SiC devices (**Fig. 1(c)**). All relevant converter components including the EMI filter are considered. On the one hand, the comparison is performed in order to examine the potential of SiC to decrease the system complexity while achieving similar or better performance. On the other hand, the trade-offs between achievable efficiency and power density are systematically analyzed. Since the power density can be seen as an indicator for the initial inverter cost and the efficiency as an indicator for the operational revenue of the inverter, in a next step, this analysis can be used to determine the economically optimal inverter dimensioning.

## II. System Specifications

The generic system topology for the comparative analysis of the selected topologies shown in **Fig. 1** is depicted in **Fig. 2**. The PV inverters with boost inductors and output $LC$ EMI filter are connected to a European 50 Hz medium voltage grid. The RMS line-to-line voltage on the secondary side of the $\Delta$-Y transformer, which is a non-public industrial grid, is assumed to be 400 V with worst case deviations of $\pm 10\,\%$. The same topology could also be used in a public low voltage grid. This would require minor adoptions in the EMI filter due to different EMI emission limits [6]. With focus on a future implementation, the rated system power is chosen to be $P_{\mathrm{r}} = 10\,\mathrm{kW}$. Based on the discussion in [12], the considered MPP voltage range is assumed to be

$$\bar{u}_{\mathrm{PV}} = [450\,\mathrm{V}, 820\,\mathrm{V}]\,, \tag{1}$$

which enables, in conjunction with a DC/DC boost input stage, a temperature range of the solar generator of approximately $-20$ to $70\,^{\circ}\mathrm{C}$ and the use of 600 V and 1200 V rated semiconductors.

A standard sinusoidal PWM modulation scheme with third-harmonic injection has been assumed throughout this work. The boost converters employ the same switching frequency as the respective inverter stage. The three-level boost converters operate with an interleaved switching scheme and duty cycles lower than $D < 0.5$, yielding a doubling of the switching frequency seen by the two DC inductors $1/2 L_{\mathrm{DC}}$. Taking into account that only half the DC voltages are applied, the required total inductance $L_{\mathrm{DC}}$ is one quarter of the respective value for the two-level boost inductor.

## III. Semiconductors

### A. Semiconductor Selection

The semiconductors considered in this work are listed in **Tab. I**. All devices are available in the TO-247 package which facilitates comprehensive switching loss measurements of the selected semiconductors. Paralleling of the devices is not intended, however employment of different devices for the inverter stages and boost converters are considered. For simplicity reasons, the discrete diodes of the 3LI+3LBC and

**Tab. I:** Considered semiconductors and corresponding topologies.

| Device | Material | Description | Topology |
|---|---|---|---|
| IKW$\{30, 50, 75\}$N60T | Si | 600 V T&FS IGBTs with anti-parallel diode | 3LI+3LBC & 3LT+3LBC |
| IKW$\{25, 40\}$N120H3 | Si | 1200 V Highspeed T&FS IGBTs with anti-parallel diode | 3LT+3LBC |
| IJW120R100T1 | SiC | 1200 V 100 m$\Omega$ normally-on JFET with integrated body diode | 2LVSI+2LBC |
| IDW$\{20, 30\}$S120 | SiC | 1200 V Schottky diode | 2LVSI+2LBC |

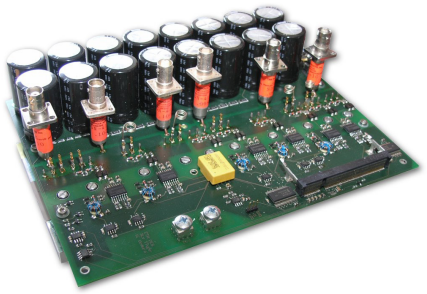

**Fig. 4:** Switching loss measurement test bench implementing a single phase bridge of the inverter stage of each topology.

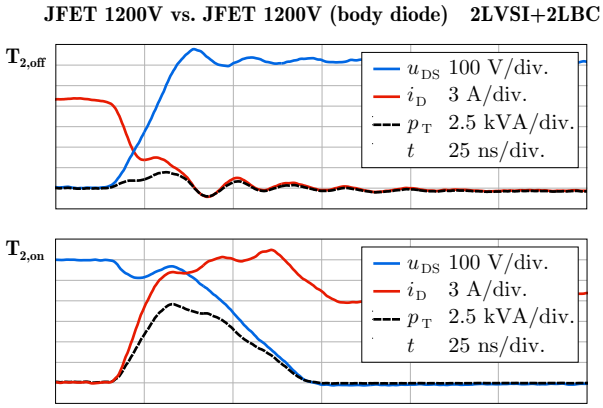


**Fig. 5:** Measured turn-off and turn-on switching loss energies $E_{\text{off}}$, $E_{\text{on}}$ respectively, for the commutation between one of the selected SiC JFETs and the internal body diode of the opposed JFET in the inverter stage of the 2LVSI+2LBC topology ($I_{\text{D}} = 13\,\text{A}$, $U_{\text{DS}} = 600\,\text{V}$, $T_{\text{j}} = 25\,^{\circ}\text{C}$). It can be seen that the turn-off switching transition is close to zero voltage switching (ZVS).

3LT+3LBC topology are implemented using the anti-parallel diodes of the respective 600 V IGBTs.

### *B. Switching Loss Measurements*

A reliable system dimensioning requires accurate performance data of the employed components and materials. However, the datasheet values for the switching losses are often incomplete. Moreover, the switching losses are to a wide degree application and layout dependent. This holds especially true for the 3LT inverter topology where 600 V devices commutate with 1200 V rated devices [14]. Further motivated by the fact that the main intention of this work is the analysis of the impact of using different power transistors (featuring widely varying switching performances), extensive measurements of the switching losses were conducted. For this purpose, the test bench shown in **Fig. 4** has been built which implements a single phase bridge of each of the investigated topologies. For simplicity reasons, it is assumed that the switching loss energies in the boost converter stages are similar to the losses

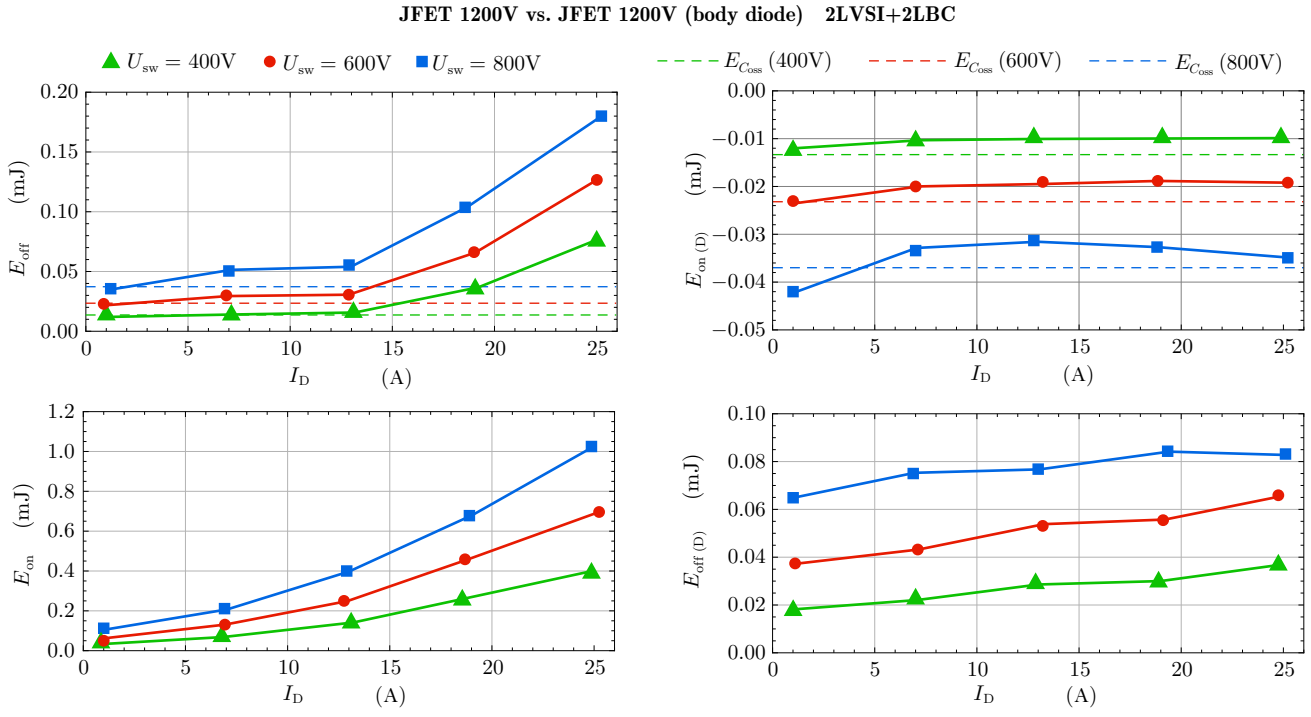


**Fig. 3:** Measured switching loss energies for the selected SiC JFETs employed in the 2LVSI+2LBC inverter stage. For commutating currents $I_{\text{D}} \lesssim 13\,\text{A}$ the turn-off losses $E_{\text{off}}$ largely correspond to the energy stored in the output capacitor $C_{\text{oss}}$ of the device. For this operating range, the switching transitions are close to zero-voltage switching (ZVS, see also **Fig. 5**) [13]. The internal body diode features a similar switching performance as SiC Schottky diodes known for their nearly vanishing reverse recovery current characteristics. It can be seen from the respective figures that most of the diode turn-off losses $E_{\text{off(D)}}$ are due to the charging of $C_{\text{oss}}$, whose energy is released again at turn-on.

**Tab. II:** Employed components and materials and respective dimensioning rules and constraints. $T_{\mathrm{j,max}}$ denotes the maximum admissible semiconductor junction temperature. The worst case ambient temperature is assumed to be $T_{\mathrm{amb,max}} = 40\,^{\circ}\mathrm{C}$. $\Delta i_{\mathrm{L_{DC}}}$ and $\Delta u_{\mathrm{C_{DC,1}}}$ are worst case high-frequency peak-to-peak current and voltage deviations.

| | **Implementation** | **Dimensioning constraints** |
|---|---|---|
| **Cooling system** | Custom Al heat sink with forced air cooling, $CSPI = 9\,\mathrm{W/K\,dm^3}$ [12] | $T_{\mathrm{j,max}} = 125\,^{\circ}\mathrm{C}$ @ $T_{\mathrm{amb,max}} = 40\,^{\circ}\mathrm{C}$ |
| $\boldsymbol{L_{\mathrm{DC}}}$ | Metglas 2605S3A amorphous alloy & foil winding | $\Delta i_{\mathrm{L_{DC}}} = 30\,\%$<br>$T_{\mathrm{L,max}} = 100\,^{\circ}\mathrm{C}$ @ $T_{\mathrm{amb,max}} = 40\,^{\circ}\mathrm{C}$ |
| $\boldsymbol{C_{\mathrm{DC,1}}}$ | EPCOS MKP DC B3277 film 1100 V | $\Delta u_{\mathrm{C_{DC,1}}} = 2\,\%$ |
| $\boldsymbol{C_{\mathrm{DC,2}}}$ | 2× EPCOS B43501 aluminium electrolytic 500 V | Current handling capability, BDEW standard [15] |
| $\boldsymbol{L_{\mathrm{boost}}}$ | Metglas 2605S3A amorphous alloy & foil winding | |
| $\boldsymbol{L_{\mathrm{DM}}}$ | Laminated Si steel & foil winding | BDEW standard [15], CISPR 11 Class A EMI [6] |
| $\boldsymbol{C_{\mathrm{DM}}}$ | EPCOS X2 MKP B3292 E/F 305 V AC | $T_{\mathrm{L,max}} = 100\,^{\circ}\mathrm{C}$ @ $T_{\mathrm{amb,max}} = 40\,^{\circ}\mathrm{C}$ |
| $\boldsymbol{C_{\mathrm{CM}}}$ | EPCOS MKP B3279 400 V AC | |

in the inverter stages when employing the same switches.

The switching loss energies were measured as a function of the commutating drain current $I_{\mathrm{D}}$ and drain source blocking voltage $U_{\mathrm{DS}}$ as well as the semiconductor junction temperature $T_{\mathrm{j}}$. For the 600 V rated IGBTs employed in the 3LI+3LBC topology, good agreement was found with the datasheet values. In contrast, the losses measured for the 3LT+3LBC inverter stage significantly vary from the datasheet values as expected, since 1200 V components commutate with 600 V components. The chip area dependency of the switching loss energies was generally found to be small. Measurement results for the SiC JFETs operating in a half bridge arrangement of the 2LVSI+2LBC inverter stage are shown in **Fig. 3** and **Fig. 5**. In contrast to the investigated Si IGBTs, the switching loss energies of the SiC JFETs are nearly independent from the temperature but exhibit a strong non-linear dependence from the current.

## IV. System Dimensioning

In this section, the dimensioning procedure of the inverter systems is discussed. For the given semiconductors presented in **Sec. III** and different switching frequencies, the achievable efficiency and the required inverter size needs to be estimated. The considered components beside the semiconductors are the cooling system, the passive components in the DC link as well as the AC filter components. The required analytical loss, volume and thermal models are largely taken from [12], [16]. A summary of the employed materials and components as well as the respective dimensioning rules and constraints are given in **Tab. II**. The dimensioning methodology assumes continuous variables and thus allows for arbitrarily sized components or the employment of a non-integer amount. The dimensioning criteria will be discussed in brief, while more detailed information can be found in [12], [16]:

- *Semiconductors and cooling system*: based on a thermal model, the cooling system is dimensioned such that for the worst case $T_{\mathrm{j}}^{*} = T_{\mathrm{j,max}} = 125\,^{\circ}\mathrm{C}$, given $T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$, where $T_{\mathrm{j}}^{*}$ denotes the highest occurring junction temperature [14], [17]. For the semiconductor losses, the methods of [16] were adopted as averaging methods (e.g. [18]) would lead to significant errors due to the strongly non-linear dependency of the switching loss energies of the SiC JFETs (**Fig. 3**). As opposed to [12], the semiconductor loss models were extended so as to include the influence of the junction temperature.
- *DC passives*: the DC inductances are chosen such that the peak to peak ripple currents are limited to 30 % of the fundamental current. The volume is optimized under consideration of the worst case temperature $T_{L,\mathrm{max}} = 100\,^{\circ}\mathrm{C}$ and the flux density saturation. The film capacitors exhibit a worst case high-frequency peak to peak voltage ripple of $\Delta u_{\mathrm{C_{DC,1}}} = 2\,\%$ whereas the ELCO capacitors are designed so as to meet the required current handling capability. Furthermore, the DC-link capacitance needs to be chosen sufficiently high in order to fulfil the fault-ride-through requirements according to [15].
- *$L_{boost}$ and LC filter*: the AC filter elements are chosen so as to comply with the CISPR 11 EMI Class A limits [6] and the medium voltage grid harmonics requirements defined in [15]. A single filter stage after the boost inductors proved sufficient to achieve the identified required attenuation values [19]. After computing the required inductance values, the respective coils are, in the same manner as the DC coils, optimized with respect to the volume.
- *Constant losses*: Constant losses independent from the topology and switching frequency of $P_{\mathrm{aux}} = 5\,\mathrm{W}$ for the auxiliary supply and DSP unit are accounted for.

## V. Performance Comparison

This section presents the results of the comparative evaluation of the topologies shown in **Fig. 1**. The trade-offs between total volume and European efficiency [20] is graphically depicted in **Fig. 8**, whereas **Fig. 6** and **Fig. 7** give more detailed information on the loss and volume breakdown for the employed components.

For the considered switching frequency range $f_{\mathrm{sw}} = [4, 24]\,\mathrm{kHz}$ it can be seen that the 2LVSI+2LBC topology achieves the highest efficiencies of all considered topologies. This is exclusively due to the low switching and conduction

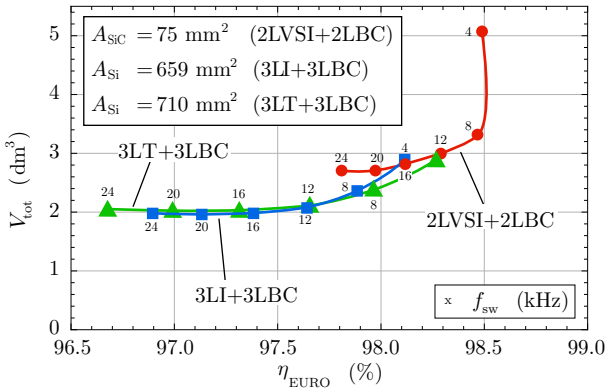


**Fig. 8:** Trade-off analysis between European efficiency $\eta_{\text{EURO}}$ and total inverter volume $V_{\text{tot}}$, parameterized by the switching frequency $f_{\text{sw}}$. $U_{C_{\text{DC,1}}} = 600\,\text{V}$, $U_{C_{\text{DC,2}}} = 650\,\text{V}$. Constant chip areas $A_{\text{Si}}$ and $A_{\text{SiC}}$ have been assumed (independent from the switching frequency) for all topologies. The indicated values each represent the sum of the chip areas of all semiconductors employed in the topologies: the combinations IKW50N60T (3LI+3LBC), IKW50N60T/IKW40N120H3 (3LT+3LBC) and IJW120R100T1/IDW20S120 (2LVSI+2LBC) were found to be the optimal selections guaranteeing the lowest overall losses. The nearly equal efficiencies of the 2LVSI+2LBC for 4 and 8 kHz are a result of the balanced sum of switching losses and losses in the passives (see **Fig. 6**).

losses of the employed SiC devices. In contrast, the 3-level Si topologies are suitable for higher power densities due to small EMI filters and DC passives. An interesting area for further investigations lies in between where all topologies achieve a similar performance ($V_{\text{tot}} \approx 3\,\text{dm}^3$, $\eta_{\text{EURO}} \approx 98.2\,\%$). Here, it can be concluded that with SiC a similar performance regarding efficiency as well as size of the passives can be achieved while offering a simpler and more standard topology. Moreover, the SiC 2LVSI+BC topology requires only one tenth of the chip area when compared to the Si systems. Eventually, for frequencies around 20 kHz, the total volume of all topologies reaches a minimum and starts to gradually increase again with even higher frequencies. This is due to several reasons:

- The total capacitor size is nearly constant (**Fig. 7**) due to the bulk volume associated with the DC-link capacitor $C_{\text{DC,2}}$. Its volume does not change as the required current handling capability is constant over frequency. The capacitor volume thus represents a virtual lower limit of the achievable volume.
- The required AC filter inductance and capacitance values do not proportionally scale with $1/f_{\text{sw}}$ as a result of the fixed emission limits defined in the considered standards [6], [15].
- High-frequency losses in the inductors (proximity losses, losses due skin effect, high-frequency core losses) increase with rising frequency and eventually limit the volume reduction due to lower required inductance values considerably.
- Increased switching frequencies yield higher switching losses and thus a larger heatsink. This ultimately outweighs the volume savings on the remaining passive components.

Due to the above discussed effects, the investigation of higher

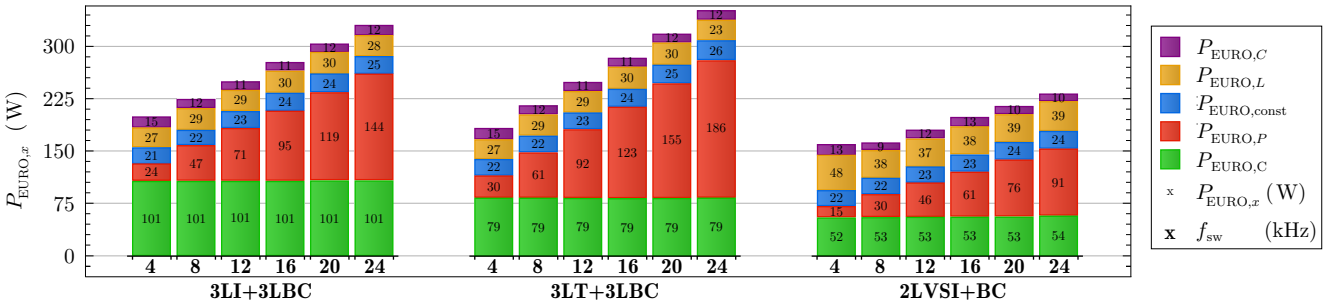


**Fig. 6:** Breakdown of the losses for the employed components and for different switching frequencies $f_{\text{sw}}$. $P_{\text{EURO},C}$ and $P_{\text{EURO},L}$ are the total losses in the capacitors and inductors, respectively. $P_{\text{const}} = P_{\text{aux}} + P_{\text{fan}}$, where $P_{\text{fan}}$ are the (load independent and hence constant) fan losses of the cooling system. $P_{\text{EURO,C}}$ represent the total conduction losses and $P_{\text{EURO,P}}$ the total switching losses. All depicted losses are weighted according to the European efficiency weighting formula.

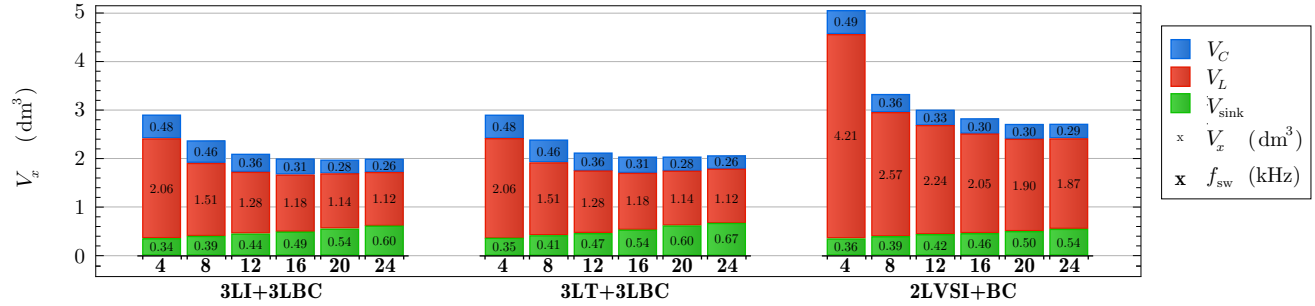


**Fig. 7:** Volume breakdown of of the employed components for different switching frequencies $f_{\text{sw}}$. $V_C$ is the total capacitor volume, $V_L$ the total inductor volume and $V_{\text{sink}}$ the volume of the required heatsink.

switching frequencies seems only be meaningful if different core materials (e.g. ferrites), alternative winding geometries (e.g. solid round or Litz wire) as well as multi-stage filter topologies are taken into account.

In a next step, the trade-off analysis shown in **Fig. 8** will allow to determine the initial costs (depending on the volume and component mix, by means of cost models as presented in [21]) and the operational revenues (depending on the efficiency and feed-in tariffs). This will further facilitate the identification of the optimal topology and switching frequency from an economical point of view.

## VI. Conclusion

Numerous contributions have shown a potential for significant performance gains in the field of PV inverters by means of employing advanced SiC-based power transistors. Whereas the opinions on how to exploit best the superior performance of SiC devices diverge, this paper proposes to increase the converter reliability by simplifying the employed topology on the one hand, and to systematically investigate the trade-off between efficiency and achievable power density on the other hand.

The trade-off analysis based on switching loss measurements and multi-objective modeling has shown that the two-level all SiC system can achieve a similar performance regarding efficiency and volume of the passives as the advanced three-level all Si topologies. Moreover, the required SiC chip area is approximately ten times smaller than the respective total Si chip areas. This can serve as an indication for the economical benefit of using SiC in PV inverters despite higher semiconductor cost.

The obtained trade-off analysis can be used to determine the meaningful range of application of Si and SiC for PV inverters with nominal power between 10 and 50 kW. In a next step, the designs with the highest economical benefit will be identified. This can be achieved by using cost models allowing to estimate the initial inverter costs depending on the inverter bill of material, combined with estimations of the operational revenue depending on the inverter efficiency. Ultimately, the selected candidate systems will be implemented to verify the theoretical investigations. Additional work should focus in more detail on the inductor model and filter topology. Alternative core materials, winding geometries and the use of multi-stage EMI filters have to be checked for their ability to further decrease the power density at higher switching frequencies.

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