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Analytical Calculation of the Residual ZVS Losses of TCM-Operated Single-Phase PFC Rectifiers

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ABSTRACT Triangular-current-mode (TCM) modulation guarantees zero-voltage-switching across the mains cycle in AC-DC power converters, eliminating hard-switching with a minor ≈30% penalty in conduction losses over the conventional continuous current mode (CCM) modulation scheme. TCM-operated converters, however, include a wide variation in both switching frequency and switched current across the mains cycle, complicating an analytical description of the key operating parameters to date. In this work, we derive an analytical description for the semiconductor bridge-leg losses in a TCM AC-DC converter, including the rms current and/or conduction losses, switching frequency, and switching losses. For SiC MOSFETs, we introduce a new loss model for switching losses under zero-voltage-switching, which we call "residual ZVS losses". These losses include the constant C_{oss} losses found in previous literature but must also add, we find, turn-off losses that occur at high switched currents. The existence and modeling of these turn-off losses, which are due to currents flowing through the Miller capacitance and raise the inner gate source voltage to the threshold level and accordingly limit the voltage slew rate, are validated on the *IMZA65R027M1H* 650V SiC MOSFET. The complete loss model – and the promise of TCM for high power density and high efficiency – is validated on a 2.2 kW hardware bridge-leg demonstrator, which achieves a peak 99.6% semiconductor efficiency at full load. The proposed, fully-analytical model predicts bridge-leg losses with only 12% deviation at the nominal load, accurately including residual ZVS losses across load, modulation index, and external gate resistance.

INDEX TERMS AC-DC power converters, power MOSFET, rectifiers, silicon carbide, soft switching, wide band gap semiconductors, zero voltage switching.

I. INTRODUCTION

Power-dense and efficient AC-DC power conversion [1] is a fundamental building block for grid-interface converters as well as electric drives, and, ultimately, a key to the successful and widespread integration of renewable energy into the energy mix. In particular, kW-scale, single-phase AC-DC converters serve as power-factor-correction (PFC) rectifier input stages for, e.g., data center power supply modules, on-board electric (EV) chargers, and PFC rectifier front-ends for low-power variable speed motor drive systems in heating, ventilation, and air conditioning (HVAC) and servo drives in industry automation and robotics, where nearly 90% of all drive systems worldwide are below 1 kW in rated power [2].

Conventionally, boost-type PFC rectifiers consisted of a diode bridge front-end, a boost inductor, and a transistor and freewheeling diode pair. Bridgeless – that is, without the diode bridge front-end – topologies were later introduced with 2 boost-type bridge-legs each with a superjunction (SJ) Si MOSFET and a freewheeling SiC Schottky diode (the "dual-boost PFC rectifier" [3]), and later improved with synchronous rectification to eliminate the on-state voltage drop of the diodes. This final step resulted in the bridgeless totem-pole

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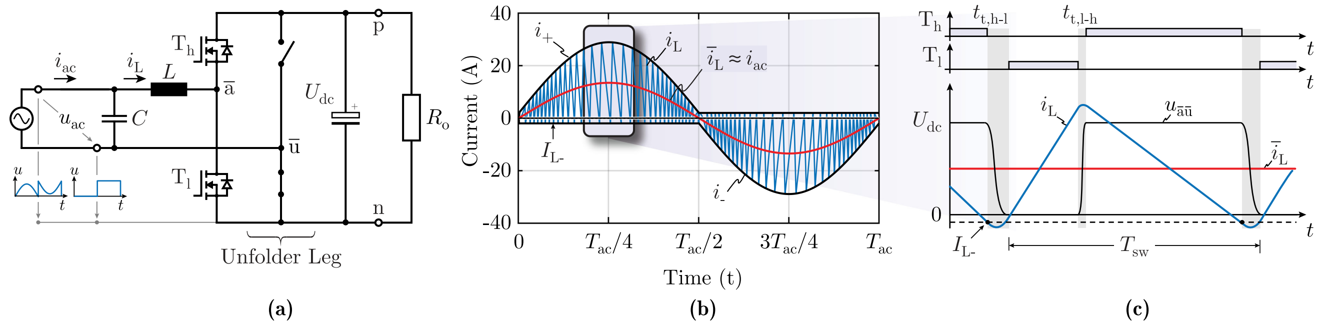


FIGURE 1. (a) Single-phase PFC rectifier in a totem-pole and/or full-bridge structure, where one bridge-leg operates at switching frequency, and the other operates at line frequency. (b) The characteristic TCM inductor current and mains current waveforms are shown for a 2.2 kW, 230 V_{rms} to 400 V PFC rectifier with a minimum turn-off current of I_{L-} (within the positive mains half-cycle) and a fundamental current component of i_{ac} (with low f_{sw} to highlight the current waveform). (c) Characteristic waveforms for the time interval highlighted in (b), including the gate signals of T_h and T_l (cf. (a)), where $t_{t,h-l}$ and $t_{t,l-h}$ represent the current-dependent transition times from the high-side switch to the low-side switch, and vice versa, respectively. $u_{\bar{a}\bar{u}}$ is the switch-node voltage.

and/or full-bridge arrangement of Fig. 1(a), the preferred topology for single-phase AC-DC power conversion today.

This topology utilizes one high-frequency switching leg, often implemented with SiC MOSFETs or GaN high-electron-mobility transistors (HEMTs), and one line-frequency switching leg as an unfolder, typically implemented with SJ Si MOSFETs designed to minimize the conduction losses. Under continuous conduction mode (CCM) operation, also known as pulse width modulation (PWM), the high-frequency bridge-leg operates with a constant switching frequency and the duty cycle is set to sinusoidally shape the mains current and thus, define the output power. In this mode, the inductor current ripple is relatively small and, during each half-cycle, one turn-on transition in the high-frequency bridge-leg is hard while the other is soft under zero-voltage conditions (assuming an average output current much larger than the current necessary for soft-switching). In an effort to further improve the power density of these converters and avoid hard commutation of early MOSFETs (and later of Si SJ MOSFETs), however, designers have proposed new modulation schemes with full zero-voltage-switching (ZVS) [4], [5], including the widely-adopted triangular current mode (TCM) operation [6]–[9], which is shown in Fig. 1(b) and, in detail, in Fig. 1(c) with transition times from low-side to high-side $t_{t,l\text{-}h}$ and high-side to low-side $t_{t,h\text{-}l}$.

TCM modulation confers significant benefits to the simultaneous pursuit of high efficiency and high power density. Firstly, and most importantly, the voltage across the power MOSFETs is reduced to zero before turn-on, eliminating the dominant switching loss component of the energy stored in the parasitic output capacitor, C_{oss}. These switching losses are eliminated without requiring auxiliary circuits, as only the control of the main power circuit is modified, and this control can be implemented using modern digital signal processing devices (e.g. DSPs and FPGAs) and simple sensing circuits. When combined with novel wide-bandgap semiconductors that have both low on-resistance and an output capacitance that is both small and linear (relative to Si SJ MOSFETS), the higher rms current in TCM ($\approx$ 15% higher than in CCM, resulting in $\approx$ 30% higher conduction losses) is easily tolerated and the switching frequency can be increased even further.

Under TCM modulation (and closely-related schema for soft-switching, including critical conduction and quasi-square-wave), AC-DC power converters with SiC MOSFETs and 400 V or 800 V DC-links have reached switching frequencies as high as 650 kHz [10], [11]. With GaN power semiconductors, designers have pushed switching frequencies into the MHz regime [12] (as high as 3 MHz [13], [14]) and simultaneously achieved efficiencies over 99% and power densities well over 100 Win^{-3} [15], [16]. Despite these demonstrated improvements and the widespread adoption of TCM schemes, though, there does not exist a straightforward method to calculate the power semiconductor losses in a TCM operated rectifier or inverter, eliminating the ability to optimize power semiconductor selection, thermal design, or switching frequency with limited effort.

In the paper, we seek to fill this critical literature gap, deriving an analytical power semiconductor loss calculation for TCM rectifiers even in the presence of *(a)* current-dependent ZVS losses and *(b)* the wide variation in switching frequency seen in TCM converters (Section II). The soft-switching (or C_{oss}) losses occur during the process of resonantly charging and discharging the parasitic output capacitor of the semiconductor and may be current-dependent [17]. These are combined with current-dependent turn-off losses in zero-voltage-switched converters, and we term this power dissipated as the "residual ZVS losses" that, with conduction losses, comprise the power semiconductor losses in a TCM converter. This loss model is proposed and validated with measurements on a next-generation 650 V SiC MOSFET in Section III. Section IV introduces the analytical expressions for the semiconductor losses and in Section V, we validate the analytical equations and loss model in a 2.2 kW PFC rectifier, a typical power level [12]–[14] used in, for example, data center applications and industrial automation (see specifications in Table 1). Finally, Section VI summarizes the key findings of the paper,

TABLE 1. Single-Phase AC-DC Converter Specifications

$P_{o,max}$	U_{dc}	U_{ac}	ω_{ac}	L
2.2 kW	400 V	120-230 V_{rms}	2π 50 Hz	11.5 μH

including the unification of competing theories on C_{oss} losses in SiC MOSFETs.

II. TCM OPERATING BEHAVIOR

To ascertain the power semiconductor losses in TCM, we first must describe the fundamental operating waveforms, preferably with analytical solutions. With the sought-after residual ZVS losses dependent on both frequency (soft-switching losses are the product of energy dissipated per cycle and frequency) and current (both soft-switching and turn-off losses depend on current), and both switching frequency (f_{sw}) and switched current varying across the mains cycle, this description is fundamental to an accurate loss prediction.

A. ANALYTICAL DESCRIPTION

With a fundamental ac voltage of $u_{ac}(t) = \hat{u}_{ac}\sin(\omega_{ac}t)$ with peak $\hat{u}_{ac}$ and DC-link voltage U_{dc}, the modulation index is:

$$M = \frac{\hat{u}_{ac}}{U_{dc}} = 0.4\ldots 0.81. \tag{1}$$

The fundamental current i_{ac} is in phase with the voltage ($i_{ac}(t) = \hat{i}_{ac}\sin(\omega_{ac}t)$), as is required for PFC operation. In TCM operation, an opposite-polarity current is selected to ensure ZVS during each half of the mains cycle, shown in Fig. 1(b-c) as $I_{L-} < 0$ A for the positive half of the mains cycle. With a peak ac current of $\hat{i}_{ac}$, the current bands during the positive half of the mains cycle ($u_{ac} \geq 0$ V) are:

$$i_{+}(t) = |I_{L-}| + 2\hat{i}_{ac}\sin(\omega_{ac}t) \quad i_{-}(t) = -|I_{L-}|, \tag{2}$$

and during the negative half of the mains cycle ($u_{ac} < 0$ V), the current bands are:

$$i_{+}(t) = |I_{L-}| \quad i_{-}(t) = -|I_{L-}| + 2\hat{i}_{ac}\sin(\omega_{ac}t). \tag{3}$$

With these bands defined, we introduce the "ZVS current ratio" as the ratio between the current selected to achieve ZVS and the fundamental peak current, or:

$$\gamma = \frac{|I_{L-}|}{\hat{i}_{ac}}. \tag{4}$$

The opposite polarity current, $I_{L-} < 0$ A, must be selected such that ZVS is guaranteed across the full mains cycle. From the $u - Zi$ diagram analysis in [8] that considers both the rectifier and the inverter cases, the characteristic impedance to guarantee ZVS is:

$$Z = \sqrt{\frac{L}{2C_{oss,Q}}}, \tag{5}$$

where $2C_{oss,Q}$ is the total charge-equivalent output capacitance of the bridge-leg semiconductors ($C_{oss,Q,Th} + C_{oss,Q,Tl} = 2C_{oss,Q}$). For rectifier operation, ZVS is guaranteed (even with $I_{L-} = 0$ A) with $M \leq 0.5$. At larger modulation indices, the minimum required turn-off current is required at the voltage peak ($u_{ac} = \hat{u}_{ac}$) as:

$$|I_{L-}| \geq I_{min} = \frac{U_{dc}}{Z}\cdot\sqrt{|2M-1|}. \tag{6}$$

For inverter operation, similarly, ZVS is guaranteed with $M \geq 0.5$. The minimum current requirement occurs at the voltage zero-crossing ($u_{ac} = 0$ V) as:

$$|I_{L-}| \geq I_{min} = \frac{U_{dc}}{Z}, \tag{7}$$

which is the worst-case condition over the entire operating space and therefore defines the minimum required opposite-polarity current $|I_{L-}|$.

Assuming the resonant transition is *(a)* much shorter than the on-time and off-time of the bridge-leg transistors and *(b)* the additional current from the resonant transition is small, we can make a triangular current approximation, and derive analytical equations for the switching frequency f_{sw} across the mains cycle and the rms current through the inductor ($I_{L,rms}$) and the power devices $I_{h,rms}$ and $I_{l,rms}$.

First, the on- and off-time for the high-side switch T_h, during the positive half-cycle, are defined with

$$\begin{cases} t_{on}(t) = \dfrac{L\Delta i_L(t)/U_{dc}}{1 - M\,|\sin(\omega_{ac}t)|} \\ t_{off}(t) = \dfrac{L\Delta i_L(t)/U_{dc}}{M\,|\sin(\omega_{ac}t)|}, \end{cases} \tag{8}$$

with the bridge-leg inductance L, a mains angular frequency ω_{ac}, and the time-dependent peak-to-peak current ripple $\Delta i_L(t) = 2|I_{L-}| + 2\hat{i}_{ac}|\sin(\omega_{ac}t)|$. The expressions for t_{on} and t_{off} have to be exchanged during the negative half-cycle due to the operation of the unfolder bridge-leg. The switching period definition $T_{sw}(t) = t_{on}(t) + t_{off}(t) = 1/f_{sw}(t)$, however, is true in both the positive and negative half-cycle and the switching frequency for both rectifier and inverter operation is:

$$f_{sw}(t) = \frac{U_{dc}}{2L\hat{i}_{ac}}\,\frac{M|\sin(\omega_{ac}t)| - M^2\sin^2(\omega_{ac}t)}{\gamma + |\sin(\omega_{ac}t)|} \tag{9}$$

and the global maximum $f_{sw,max}$ occurs at $\zeta = |\sin(\omega_{ac}t^{*})| = \sqrt{\gamma^2 + \frac{\gamma}{M}} - \gamma$ (see Fig. 2(a.i)) and is:

$$f_{sw,max} = \frac{U_{dc}}{2L\hat{i}_{ac}}\cdot\frac{M\zeta - M^2\zeta^2}{\gamma + \zeta}. \tag{10}$$

With the triangular shape of the inductor current i_L, the local inductor rms current $i^2_{L,rms} = \frac{1}{T_{sw}}\int_0^{T_{sw}} i_L^2(t)\mathrm{d}t$ over a switching period $T_{sw} = 1/f_{sw}$ is determined by the positive and negative current limits as:

$$i^2_{L,rms}(t) = \frac{1}{3}\left[i_{+}^2(t) + i_{+}(t)i_{-}(t) + i_{-}^2(t)\right], \tag{11}$$

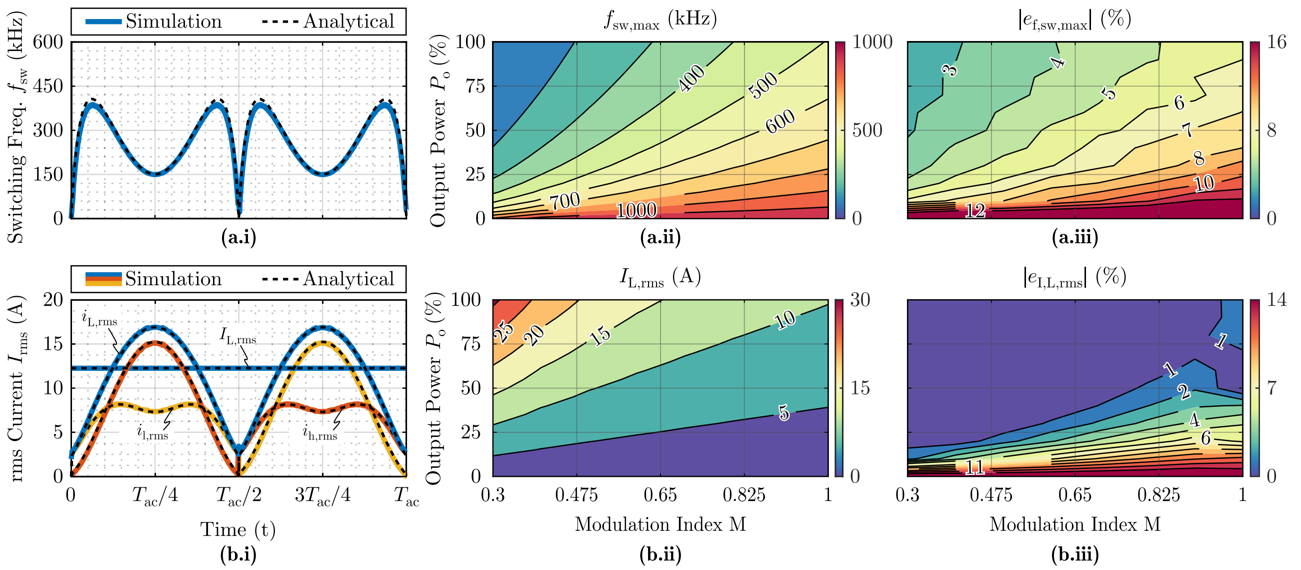


FIGURE 2. Comparison of the analytically-calculated and numerically-simulated (a.i) local switching frequency f_{sw} and (b.i) transistor local rms currents $i_{h,rms}$ and $i_{l,rms}$ over one mains cycle $T_{ac} = 1/f_{ac}$ for the specifications of Table 1 with $U_{ac} = 230\,V_{rms}$, an assumed $C_{oss,Q} = 370$ pF of the bridge-leg power transistor, and a constant turn-off current of $I_{L-} = -4$ A. (ii) shows (a) the analytically-calculated maximum switching frequency $f_{sw,max}$ and (b) the analytically-calculated global inductor rms current $I_{L,rms}$ over the operating area and (iii) shows the absolute error of this prediction compared to the numerical simulation.

which can also be written as $i^2_{L,rms}(t) = i^2_{h,rms}(t) + i^2_{l,rms}(t)$, due to the triangular current approximation. The instantaneous (local) rms current across the mains cycle is shown in Fig 2(b.i).

Therefore, we can find the local high-side and low-side switch rms currents, $i_{h,rms}$ and $i_{l,rms}$, which determine the conduction losses. These are given as:

$$i^2_{h,rms}(t) = i^2_{L,rms}(t) \cdot d(t), \tag{12}$$

$$i^2_{l,rms}(t) = i^2_{L,rms}(t) \cdot [1 - d(t)], \tag{13}$$

with the instantaneous duty cycle $d(t) = u_{\bar{a}n}(t)/U_{dc}$ of:

$$d(t) = \begin{cases} M\,|\sin(\omega_{ac}t)| & \text{if} \quad u_{ac}(t) > 0\text{ V} \\ 1 - M\,|\sin(\omega_{ac}t)| & \text{if} \quad u_{ac}(t) \leq 0\text{ V}. \end{cases} \tag{14}$$

These local rms values can then be used to calculate the global rms currents, as, for example, $I^2_{L,rms} = \frac{1}{T_{ac}} \int_0^{T_{ac}} i^2_{L,rms}(t)\mathrm{d}t$ for the inductor current. With the current bands of Eqn. (2) and Eqn. (3), the global inductor rms current is:

$$I_{L,rms} = \hat{i}_{ac}\sqrt{\frac{1}{3}\left(2 + \frac{4}{\pi}\gamma + \gamma^2\right)}. \tag{15}$$

For $\gamma = 0$, the inductor rms current is $I_{L,rms} = \hat{i}_{ac}\sqrt{\frac{2}{3}}$, for 33% more conduction losses than in CCM (neglecting any ripple).

The unfolder operation ensures symmetrical operation in the high-frequency bridge-leg, allowing for a simple determination of the switch global rms currents as $I_{h,rms} = I_{l,rms} = \frac{1}{\sqrt{2}} I_{L,rms}$.

B. SIMULATION VALIDATION

The analytical expressions for the frequency f_{sw} and the various currents, including $I_{L,rms}$, are compared to the results from `GeckoCIRCUIT` [18] numerical simulations in Fig. 2 to validate the proposed equations. The simulations are carried out with the specifications of Table 1 with $U_{ac} = 230\,V_{rms}$, an assumed $C_{oss,Q} = 370$ pF of each power transistor, and a constant turn-off current of $I_{L-} = -4$ A to ensure full ZVS (as analyzed later, in Section V).

Firstly, the analytically calculated and simulated local switching frequency f_{sw} (Fig. 2(a.i)) and transistor local rms currents $i_{h,rms}$ and $i_{l,rms}$ and inductor rms current $i_{L,rms}$ (Fig. 2(b.i)) are compared over one mains cycle ($T_{ac} = 1/f_{ac}$) for an ac voltage of 230 V_{rms} and a maximal power of 2.2 kW. The agreement between the derived analytical expressions and the numerical simulations is very good, with small deviations that are then further explored across the operating space.

In Fig. 2(a.ii), the analytically-calculated maximum switching frequency across ac voltage (including the considered application range from 120 V_{rms} to 230 V_{rms}) and output power is shown, varying between 100 kHz and 1100 kHz. The maximum switching frequency occurs at no-load operation. This prediction is then compared to numerical simulations in Fig. 2(a.iii). Because the calculation ignores the resonant transition times, the calculated switching frequency is always higher than the simulated switching frequency. Across the operating space, though, the absolute error remains below 6%

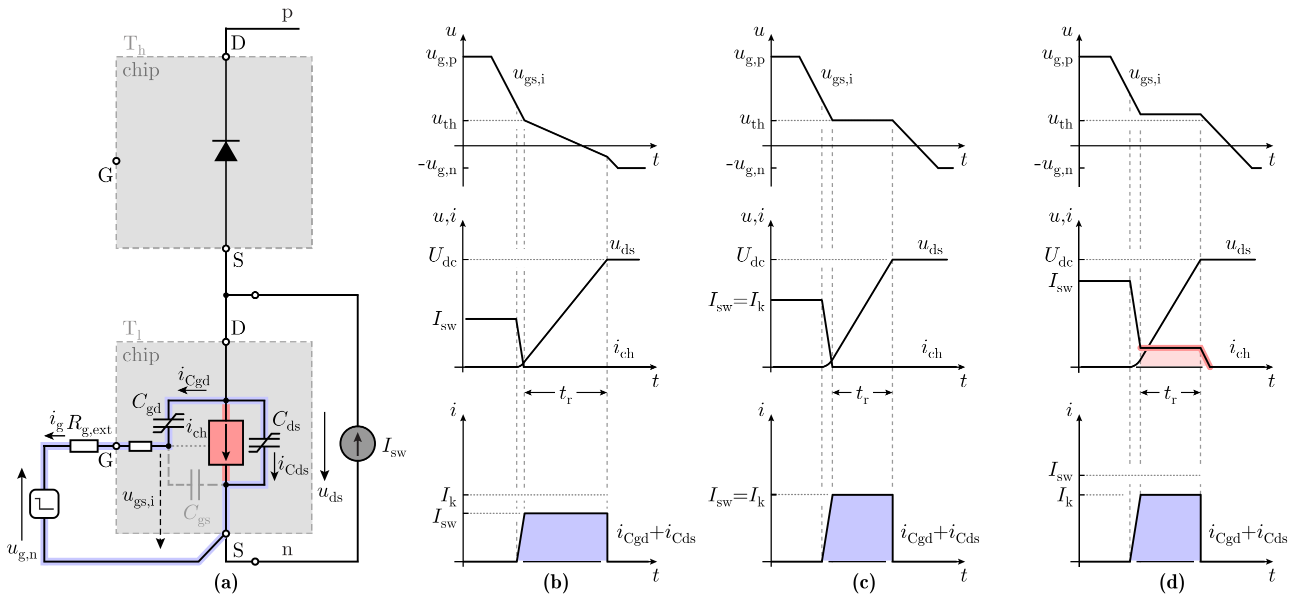


FIGURE 3. (a) Equivalent circuit of the high-frequency bridge-leg of Fig. 1(a) for the T_l turn-off switching transition, where the switch-node voltage changes from the negative DC-link rail n to the positive DC-link rail p. The upper power transistor is only visualized schematically and the shown drain-source capacitance C_{ds} considers the parasitic capacitances $C_{ds,Tl}$, $C_{oss,Th}$, and C_{par}. The switched current I_{sw} is taken as constant during the turn-off transition. (b-d) Turn-off switching transitions at increasing current levels, from below I_k (b) to equal to I_k (c) to above I_k (d). At high currents above the kink current, I_{kink}, residual ZVS losses occur due to the significant overlap between the drain-source voltage (u_{ds}) and the channel current i_{ch} of T_l. The time behavior of the inner gate-source voltage ($u_{gs,i}$) of T_l is based on a straight-line approximation.

for full-load operation and below 16% even at the worst-case of zero-load operation.

Similarly, Fig. 2(b.ii) shows the calculated inductor rms current over the operating area, with the minimum rms current ($I_{L,rms,min} = |I_{L-}|/\sqrt{3} = 2.3$ A) corresponding to no-load operation, and Fig. 2(b.iii) shows the error between this calculation and the simulated current. Again, because the analytical equations ignore the resonant transition times (where inductor current increases), the analytical prediction is always smaller than the current values obtained from simulation. However, since the resonant transitions are only a small fraction of the total period, the error at full load is smaller than 1%. The error increases with lower power levels but never exceeds 14%.

Overall, the proposed analytical expressions accurately describe the key parameters and waveforms in TCM operation, and we can confidently apply them to determine the total power semiconductor losses. First, though, the remaining switching losses that occur during ZVS operation must be determined, and we combine the well-known soft-switching (or C_{oss}) losses [17], [19]–[28] with turn-off losses to describe the total switching losses under ZVS, which we term "residual ZVS losses."

III. RESIDUAL ZVS LOSSES

Soft-switching losses occur during the resonant charge-discharge process of the parasitic output capacitance in a power semiconductor, and are well-characterized in a breadth of device types [19]–[28]. In SiC MOSFETs, in particular, recent literature has found that these soft-switching losses per cycle are independent of du_{ds}/dt and are therefore constant with switched current [17], [29]. In ZVS implementations, however - like the TCM topology here - the measured "switching" losses are higher-than-expected and increase with current, necessitating the inclusion of an additional switching loss mechanism beyond C_{oss} losses. While comprehensive analytical models of switching behavior have been previously given (for example, [30], [31]), we focus on a minimum-complexity equivalent circuit (and resulting equations) to ascertain the core driver of these residual ZVS losses.

Fig. 3(a) shows the equivalent circuit present during the turn-off transition of the low-side switch (T_l in Fig. 1(a)) and the corresponding waveforms are shown in Fig. 3(b), assuming the inductor current is flowing during the whole switching transition in the indicated direction and that the dead-time is large enough to guarantee zero-voltage turn-*on* of T_h) for complete ZVS [5]. C_{ds} represents the equivalent output capacitance between D and S, including the drain-source capacitance of T_l, the output capacitance of T_h (only indicated with a free-wheeling diode to which I_{sw} commutates) and any additional parasitic capacitances, i.e. $C_{ds} = C_{ds,Tl} + C_{oss,Th} + C_{par}$. While this turn-*off* transition is typically ignored when considering the losses in unipolar power semiconductors, there is an unmistakable remnant voltage-current overlap at enhanced load current during this time in ZVS converters that may result in large and non-negligible losses [32], as shown in Fig. 3(d).

A. TURN-OFF TRANSITION ANALYSIS

This turn-off transition is now analyzed in detail to ascertain the source, mechanisms, and dependencies of these residual ZVS losses. During turn-off, the switched current I_{sw} is taken as constant, and commutates from the channel (i_{ch}) to charge the output capacitor (C_{ds} with current i_{Cds}) and the Miller capacitor (C_{gd} with current i_{Cgd}). As the switched current I_{sw} increases, the switching voltage transition is expected to occur more rapidly due to higher capacitor charging current, which increases the voltage slew of the transition $\mathrm{d}u_{ds}/\mathrm{d}t = U_{dc}/t_r$. This indeed occurs – to a point.

As the switched current I_{sw} increases, i_{Cgd} also increases with the current divider $C_{gd}/(C_{ds} + C_{gd})$ between the gate-drain and equivalent drain-source capacitance. The gate current is assumed to be determined by the gate drive circuit as $i_g = (u_{gs,i} + |u_{g,n}|)/R_g$, with the inner gate-source voltage $u_{gs,i}$, the negative gate driver voltage magnitude $u_{g,n} = |u_{g,n}| \geq 0$ V, and the total gate resistance $R_g = R_{g,int} + R_{g,ext}$. As long as the current through the Miller capacitance i_{Cgd} is smaller than the gate drive current i_g, $i_{Cgd} < i_g$, the gate-source capacitance is discharged and the channel is closed before the drain-source voltage u_{ds} starts rising significantly, cf. Fig. 3(b). This case results in ideal ZVS with no turn-off losses beyond C_{oss} and gating losses, and a voltage slew rate $\mathrm{d}u_{ds}/\mathrm{d}t$ that is proportional to I_{sw}:

$$\frac{\mathrm{d}u_{ds}}{\mathrm{d}t} = \frac{I_{sw}}{C_{ds} + C_{gd}} \approx \frac{I_{sw}}{C_{eff}}, \tag{16}$$

with $C_{eff} = 2C_{oss,Q} + C_{par}$.

During this transition, the following order of operations occurs, assuming that in the active region the relationship between the gate-source voltage and the channel current is linear and defined by the transconductance g. Firstly, the gate-source capacitance is discharged to some level (with no effect on the power circuit), and once the (inner) gate-source voltage $u_{gs,i}$ reaches this level, $u_{gs,i} = u_{th} + I_{sw} \cdot g$, the channel current starts decreasing, a decay that we assume to be linearly proportional to the difference of $u_{gs,i}$ and the threshold voltage u_{th} (Fig. 3(b)). With the high-side diode still blocking, the switched current I_{sw} that no longer flows through the channel (i_{ch}) must flow through the capacitances $C_{ds} + C_{gd}$, building up the drain-source voltage quadratically (for a linear decrease in channel current). With a fast change in channel current, the voltage-current overlap during this time period can be (and has been, in prior art) neglected. Once the channel current has fully commutated to the output capacitcances, the gate-drain current is determined by the voltage slew and the Miller capacitance, and the gate-source capacitor continues to discharge. When $i_{Cgd} < i_g$, the discharge of the gate-source capacitance continues at a reduced slope, and once the voltage transition has finished, the full gate current again discharges the gate-source capacitance and the slope increases until the transition is completed.

As I_{sw} is further increased, we first encounter the corner case $i_{Cgd} = i_g$ with $u_{gs,i} = u_{th}$, (Fig. 3(c)), which we call the "kink current" I_k:

$$I_k = \left(i_{Cgd} + i_{Cds}\right)\Big|_{max} = \frac{u_{th} + |u_{g,n}|}{R_g}\left(1 + \frac{C_{ds}}{C_{gd}}\right). \tag{17}$$

In this case, the switched current $I_{sw} = I_k$ is again split between C_{ds} and C_{gd}, but the current through the Miller capacitance from the voltage slew $\mathrm{d}u_{ds}/\mathrm{d}t$ equals the gate driver current, i.e. $i_{Cgd} = i_g$. Therefore, $u_{gs,i}$ remains at the threshold voltage u_{th} and no charge is removed from the gate-source capacitor (see Fig. 3(c)). As the gate-drain current is defined by the gate driver current, $i_{Cgd} = i_g \approx (u_{th} + |u_{g,n}|)/R_g$, the slew rate at the kink current is:

$$\left.\frac{\mathrm{d}u_{ds}}{\mathrm{d}t}\right|_k = \frac{I_k}{C_{ds} + C_{gd}} \approx \frac{I_k}{C_{eff}}. \tag{18}$$

If I_{sw} is increased beyond the kink current I_k, the gate-source capacitance is discharged only to a voltage that remains slightly higher than the threshold voltage u_{th} (Fig. 3(d)), and the channel remains turned *on* and conducts the switched current (to reiterate, taken as constant) that cannot flow through the combination of the gate-source and drain-source capacitances. This causes voltage-current overlap losses, which are deemed "residual ZVS losses" here. With the gate-source voltage above the threshold voltage, the continued channel current slightly expedites the voltage transition, resulting in a voltage slew rate of:

$$\frac{\mathrm{d}u_{ds}}{\mathrm{d}t} = \frac{1}{C_{eff}}\begin{cases} I_{sw} & \text{if} \quad I_{sw} < I_k \\ I_k + s \cdot (I_{sw} - I_k) & \text{if} \quad I_{sw} \geq I_k, \end{cases} \tag{19}$$

with the slope s dependent on the MOSFET transconductance g as $s = \frac{I_k}{g(u_{th} + |u_{g,n}|)}$.

As soon as the voltage transient is completed, the gate-source voltage drops, the device turns off fully, the remaining channel current commutates to the high-side device, and the transition is completed.

B. EXPERIMENTAL VALIDATION OF TURN-OFF TRANSITION WAVEFORMS

To validate the proposed model and conceptual waveforms of Fig. 3, we measure the turn-off transition across drain currents of a 650 V, 27 mΩ 4-pin SiC MOSFET from Infineon *IMZA65R027M1H* operated with $|u_{g,n}| = 3$ V and $R_{g,ext} = 24.3\ \Omega$ (a relatively large gate resistance is selected for better visualization) in a half-bridge setup. The waveforms of the drain-source voltage u_{ds}, the gate-source voltage u_{gs} (measured with the Tektronix IsoVu [33]), and the gate current i_g (measured indirectly via the voltage drop of the external gate resistor) are shown during the turn-off transition in Fig. 4 and in Fig. 5. The saturation of the $\mathrm{d}u_{ds}/\mathrm{d}t$ is shown in Fig. 4, where the measured drain-source voltage during the turn-off transition (solid lines) is compared to a linear-scaled version of the 2.5 A transition (dashed lines, which correspond to an ideal ZVS transition), an operating point well below the kink current of 6.4 A (calculated using the fitted model parameters of Table 2, as detailed below). The voltage slew rate clearly

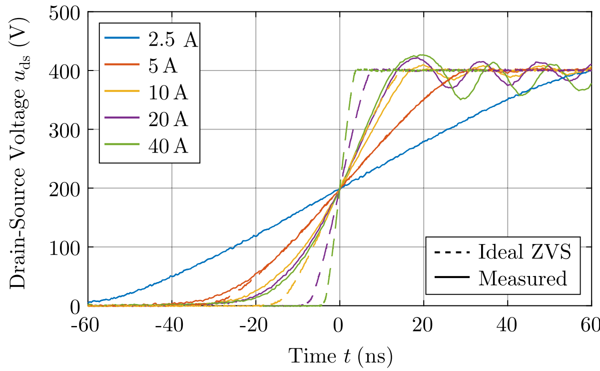


FIGURE 4. Drain-source voltage u_{ds} at turn-off for different load currents, measured for the *IMZA65R027M1H* operated with $R_{g,ext} = 24.3\ \Omega$ and $|u_{g,n}| = 3$ V (solid lines). For comparison, linearly-scaled waveforms of the 2.5 A transition measurement are shown (dashed lines), which would correspond to ideal ZVS transitions without saturation effects. For currents above the kink current of 6.4 A, the voltage slew rate clearly saturates.

TABLE 2. Model Parameter of the *IMZA65R027M1H*

	C_{eff}	u_{th}	$R_{g,int}$	$1+\frac{C_{ds}}{C_{gd}}$	s
Estimated	646 pF	7 V	4 Ω	18	0.2
Datasheet	640 pF	7 V	3 Ω	-	-

shows the expected saturation effect for currents above the kink current.

The internal threshold voltage u_{th}, the quantity that determines device behavior, can be translated into an externally-measurable quantity $u_{th,ext}$ by assuming a resistive voltage divider in the gate path between the external $R_{g,ext}$ and the device-internal gate resistance $R_{g,int}$, and is given as:

$$u_{th,ext} = \left(u_{th} + \left|u_{g,n}\right|\right) \frac{R_{g,ext}}{R_{g,int} + R_{g,ext}} - \left|u_{g,n}\right|. \quad (20)$$

For the given operating conditions, this results in $u_{th,ext} = 5.6$ V, a threshold that is highlighted in Fig. 5 and consistent with the level at which the behavior change of the MOSFET occurs. Even with the non-constant Miller region of SiC MOSFETs [34], [35], the measurements align well with the proposed waveforms of Fig. 3. Particularly, the increased gate-source voltages and gate currents at higher switched currents indicate the predicted presence of a channel current during the turn-off transition.

In examining the measurements of Fig. 4 and Fig. 5, we also observe ringing in all measured waveforms of u_{ds}, u_{gs}, and i_g for switched currents above the kink current. This is attributed to the remnant channel current commutating to the high-side switch very quickly, exciting the parasitic power loop inductance and causing the observed ringing. A small fraction of this inductance is coupled with the gate-to-kelvin-source connection, and even this small ringing is seen in the gate-source voltage measurement of Fig. 5.

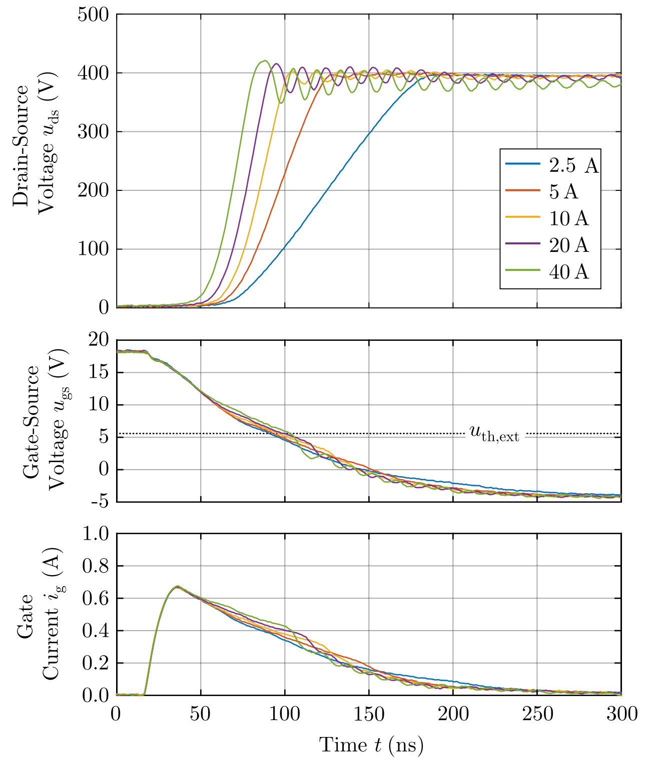


FIGURE 5. Measured drain-source voltage u_{ds}, gate-source voltage u_{gs}, and gate current i_g during turn-off of the *IMZA65R027M1H* operated with $R_{g,ext} = 24.3\ \Omega$ and $|u_{g,n}| = 3$ V, across switched currents (also shown in Fig. 4). $I_k = 6.4$ A for this operating condition. These waveforms and the highlighted voltage level of $u_{th,ext} = 5.6$ V, which corresponds to the conversion of the (internal) threshold voltage u_{th} into an externally measurable quantity using Eqn. (20), match the theoretical waveforms and considerations of Fig. 3.

C. RESIDUAL ZVS LOSS MODELLING

Because the total switched current is constant during the turn-off period, the current that cannot flow through C_{gd} (and C_{ds}) must flow through the channel as

$$i_{ch} = I_{sw} - I_k \quad (21)$$

leading to an energy loss due to the voltage-current overlap for currents $I_{sw} \geq I_k$. The total energy loss in the zero-voltage-switched power semiconductor, then, can be written as:

$$E_{sw}(I_{sw}) = \begin{cases} E_0 & \text{if} \quad I_{sw} < I_k \\ E_0 + k \cdot (I_{sw} - I_k) & \text{if} \quad I_{sw} \geq I_k, \end{cases} \quad (22)$$

where E_0 represents the constant C_{oss} losses in SiC MOSFETs [17] plus the gating losses, and is therefore a current-independent, device-specific term. The factor $k = \frac{1}{2}U_{dc}^2 / \frac{du_{ds}}{dt}$ includes the voltage slope $\frac{du_{ds}}{dt}$, which, according to Eqn. (19), is dependent on the switched current. Assuming $s \approx 0$ as an approximation, the voltage slope is constant, $\frac{du_{ds}}{dt} = \frac{du_{ds}}{dt}|_k = \frac{I_k}{C_{eff}}$ (for $I_{sw} \geq I_k$) and we can introduce a current-independent approximation of k, $\tilde{k} = \frac{1}{2}U_{dc}^2 / \frac{du_{ds}}{dt}|_k = \frac{1}{2}U_{dc}^2 C_{eff} / I_k$.

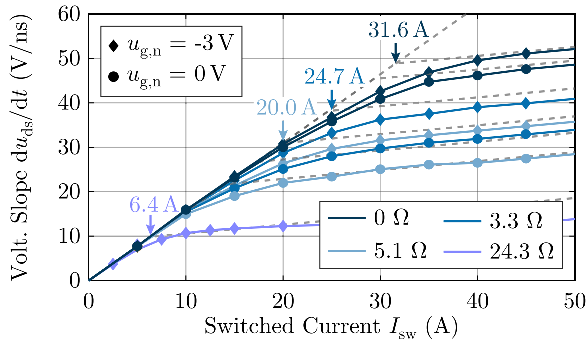


FIGURE 6. Measured du_{ds}/dt of the *IMZA65R027M1H* for a bridge-leg (U_{dc} = 400 V) across switched currents I_{sw}. Four external gate resistors $R_{g,ext}$ = 0 Ω (dark blue), 3.3 Ω (blue), 5.1 Ω (light blue), 24.3 Ω (violet) and two gate driver voltages $|u_{g,n}|$ = 0 V (circles) and $|u_{g,n}|$ = 3 V (diamonds) are used to show the variation in I_k predicted by Eqn. (17). The results of the kink model (cf. Eqn. (17) and Eqn. (19)) are overlaid with indicated kink currents to validate the proposed approach.

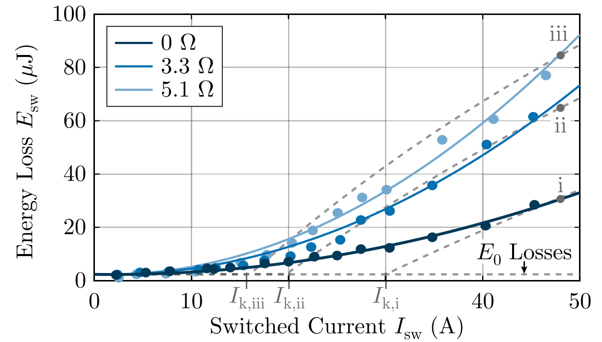


FIGURE 7. Measured soft-switching energy losses E_{sw} of the *IMZA65R027M1H* for a full bridge-leg (U_{dc} = 400 V) across switched currents I_{sw}, with adapted deadtimes to ensure complete soft-switching transitions. Three external gate resistors $R_{g,ext}$ = 0 Ω (dark blue, i), 3.3 Ω (blue, ii), 5.1 Ω (light blue, iii) are used to show the variation in I_k predicted by Eqn. (17) considering $|u_{g,n}|$ = 1 V. The results of the proposed model (cf. Eqn. (17), Eqn. (19), and Eqn. (22)) are overlaid to validate the proposed approach.

To fit and validate the model, further measurements are conducted on the previously-introduced half-bridge setup. Double-pulse experiments are conducted for three additional gate resistors ($R_{g,ext} = 0\,\Omega$, $3.3\,\Omega$, $5.1\,\Omega$) and two turn-off voltages ($|u_{g,n}| = 0$ V, 3 V), with the results shown in Fig. 6. The du_{ds}/dt measurements are also shown for $R_{g,ext} = 24.3\ \Omega$ and $|u_{g,n}| = 3$ V for completeness, as it verifies the kink current model even for large gate resistors. Voltage slew rates du_{ds}/dt are evaluated between 10% and 90%.

Based only on the du_{ds}/dt measurements, the critical device parameters of Table 2 can be estimated – from which the kink current I_k and the coefficient k can be simply calculated. The maximum voltage slew rate results in the C_{eff} and s parameters of $C_{eff} = 646$ pF (which corresponds to twice the charge equivalent output capacitance between 40 V and 360 V, i.e. 2 × 320 pF) and s is considered to be 0.2 for small gate resistors, i.e. for $R_{g,ext} < 6\,\Omega$. For larger resistance values (e.g. $R_{g,ext} = 24.3\ \Omega$), the value of s drops, for example to 0.1. The remaining parameters are derived based on estimated kink currents and result in $1 + \frac{C_{ds}}{C_{gd}} = 18$, $u_{th} = 7$ V (which corresponds to the datasheet value of the extracted threshold voltage from the typical transfer characteristic), and $R_{g,int} = 4\,\Omega$, which is slightly larger than that specified in the datasheet ($R_{g,int} = 3\ \Omega$).

The resulting kink currents for $R_{g,ext} = 0\ \Omega$, $3.3\,\Omega$, $5.1\ \Omega$, and $24.3\ \Omega$ according to the proposed model are, respectively, $I_k = 29.3$ A, 17.3 A, 14.0 A for $|u_{g,n}| = 0$ V and $I_k = 31.6$ A, 24.7 A, 20.0 A and 6.4 A for $|u_{g,n}| = 3$ V, with the latter set highlighted in Fig. 6. We note here that for the combination of large negative gate drive voltage magnitudes and small gate resistors, a gate drive current limit of approximately 1.7 A must be included in the analysis due to the limited gate driver fall time (10 ns), which is similar to the corresponding voltage rise/fall time of the SiC MOSFET $t_R = 8$ ns (at 50 Vns^{-1}, cf. Fig. 6).

Finally, the switching losses under ZVS are calorimetrically measured [36] and shown in Fig. 7. The negative gate driver voltage magnitude is $|u_{g,n}| = 1$ V during the measurements (due to a voltage drop within the gate driver circuitry that occurs when switching the devices between 500 kHz-1 MHz), which leads to $E_0 = 2.4\,\mu$J.

The kink currents and resulting voltage slew rates (for $s = 0.2$) and the results of the residual ZVS loss model are shown overlaid in both Fig. 6 and Fig. 7, with the calculations relying on the fitted model parameters given in Table 2. The largest deviation between model and measurements appears at the kink current. This occurs because the model does not include the non-linearity of C_{dg}, which is largest at $u_{ds} = 0$ V, and the voltage slew rate limitation occurs at lower currents than specified by the kink current.

Even with these approximations and simplifications – using only voltage slope measurements, ignoring temperature effects, and neglecting the non-linearities of the respective capacitances with voltage – the model and measurements agree closely, with the loss model predicting the current (I_k at which the losses start to increase beyond the constant C_{oss} losses) for all three gate resistors. The maximum voltage slew rate and existence of an asymptote is also well-predicted by the proposed model, as shown in Fig. 6. The key results are given in the top half of Table 3 for the measured device.

As an important aside, we note that this analysis clearly indicates the need for high-performance gate drive solutions with low gate resistances and large negative gate driver voltage magnitudes, which push out the kink current. The only downside of an increased negative gate driver voltage is the increase in gate drive losses, but a voltage increase from $|u_{g,n}| = 0$ V to 3 V only increases the fixed gating energy loss from 1.13 µJ to 1.45 µJ per cycle. This energy loss increase of 0.32 µJ is negligible compared to the constant part of $E_0 = E_G + 5\%E_{oss} = 1.13\,\mu\text{J} + 1.11\,\mu\text{J} = 2.24\,\mu\text{J}$ (considering a C_{oss}-related energy loss of only 5% E_{oss} [17]). This

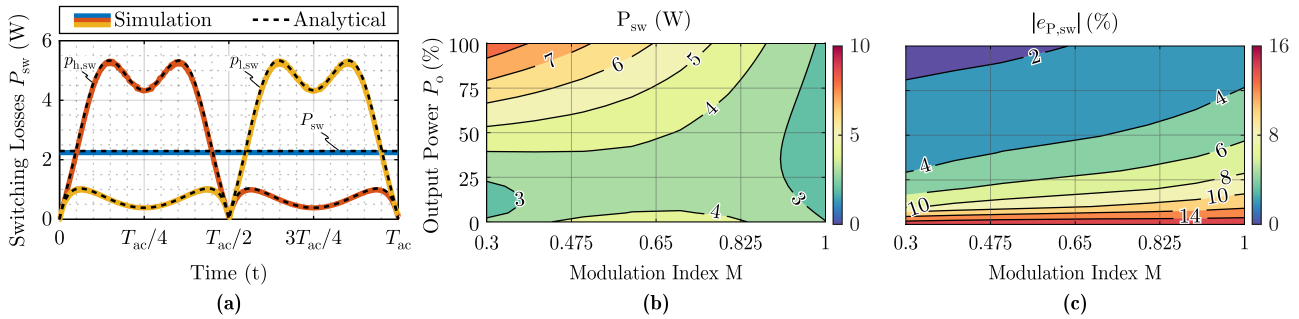


FIGURE 8. **(a) Comparison of the analytically calculated and simulated switching losses for $R_{g,ext} = 3.3\ \Omega$, modulation index $M = 0.81$ ($U_{ac} = 230\,V_{rms}$), and full load power (2.2 kW) over one mains cycle. (b) Switching loss across the operating area for $R_{g,ext} = 3.3\ \Omega$ and (c) absolute error in switching loss between proposed analytical calculation and GeckoCIRCUIT simulation.**

TABLE 3. **Calculated and Fitted Switching Loss Coefficients for a 650 V SiC MOSFET (*IMZA65R027M1H*) Operated At $U_{dc} = 400$ V and Under ZVS, Valid for $E_{sw} = a + bI_{sw} + cI_{sw}^2$ With $I_{sw} > 0$ A for $|u_{g,n}| = 1$ V**

Coefficient	$R_{g,ext} = 0\,\Omega$	$R_{g,ext} = 3.3\,\Omega$	$R_{g,ext} = 5\,\Omega$
I_k in A	30.0	19.7	16.0
$\left.\frac{du_{ds}}{dt}\right\vert_k$ in V/ns	46.4	30.5	24.8
$\tilde{k}$ in µJ/A	1.7	2.6	3.2
E_0 in µJ	2.4	2.4	2.4
a in µJ	2.4	2.4	2.4
b in nJ/A	-46.1	-85.4	-95.3
c in nJ/A^2	13.2	30.1	37.9

clearly motivates the selection of the highest-possible negative gate driver voltage magnitude, which is typically limited by the maximum rating of the device.

Finally, while this derived model predicts the behavior accurately, the loss estimation is difficult to implement analytically due to the discontinuity at I_k. The residual ZVS losses can, instead, be approximated by a quadratic loss model [36] as (for $I_{sw} > 0$ A):

$$E_{sw}(I_{sw}) = a + bI_{sw} + cI_{sw}^2, \tag{23}$$

where a, b, and c are switch-dependent switching loss coefficients and I_{sw} is the switched current. These fittings are overlaid on the measured losses in Fig. 7 with the coefficients of Table 3. The coefficient a is selected to be equal to E_0 (which also includes a fixed gating loss of 1.3 µJ per cycle). Unlike the discontinuous loss model, these coefficients have no physical meaning (e.g. $b < 0$) but still approximate the measured losses under ZVS accurately from 10 A to 50 A of switched current. In Appendix A, the switching characteristics of a SiC MOSFET from a different voltage class and manufacturer (1.2 kV, 16 mΩ 4-pin SiC MOSFET *C3M0016120K* from Wolfspeed) are measured, further validating the model's predictions of voltage slew rate, kink current, and soft-switching losses.

We find, then, that the complete switching losses under ZVS across current are predicted by the proposed model. The residual ZVS losses, further, can be accurately approximated with a continuous quadratic loss function, and we can use this to analytically determine the total power semiconductor losses in the TCM operated converter-of-interest.

IV. POWER SEMICONDUCTOR LOSSES IN TCM

The total power semiconductor losses in a TCM converter, then, comprise the conduction losses – based on the rms currents derived in Section II – and the switching loss model of the previous section, where residual ZVS losses were determined as a function of current. The local conduction losses are:

$$p_{h,cond}(t) = R_{ds} i_{h,rms}^2(t), \tag{24}$$

$$p_{l,cond}(t) = R_{ds} i_{l,rms}^2(t), \tag{25}$$

which are mainly determined by the local rms currents of Eqn. (12) and Eqn. (13).

The local switching losses are the product of the switching frequency (determined in Eqn. (9) and validated in Fig. 2(a)) and the energy loss, which is a function of the turn-off current:

$$p_{h,sw}(t) = f_{sw} E_{sw}(i_+(t)) \tag{26}$$

$$p_{l,sw}(t) = f_{sw} E_{sw}(i_-(t)). \tag{27}$$

Again, the analytical predictions are compared to the results from GeckoCIRCUIT numerical simulations (with the quadratic fit loss model), this time for the switching losses. Fig. 8(a) shows the comparison of the local switching losses over one mains cycle $T_{ac} = 1/f_{ac}$ for an external gate resistor of $R_{g,ext} = 3.3\ \Omega$. Again, we find an accurate proposed model of residual ZVS losses and, further, show the accuracy of the quadratic loss approximation. In Fig. 8(b), the switching losses are shown over the complete operating area of modulation index and load, and we highlight the current-dependency of the switching losses (which would not be included in the C_{oss}-loss-only model). Fig. 8(c) shows the relative error between the calculated and predicted switching losses, where we find excellent matching that degrades somewhat at light loads due to the error in switching frequency prediction (see Fig. 2(a.iii)).

With each loss component determined analytically in previous sections of the paper, we can now find the total conduction and switching losses across the considered modulation range,

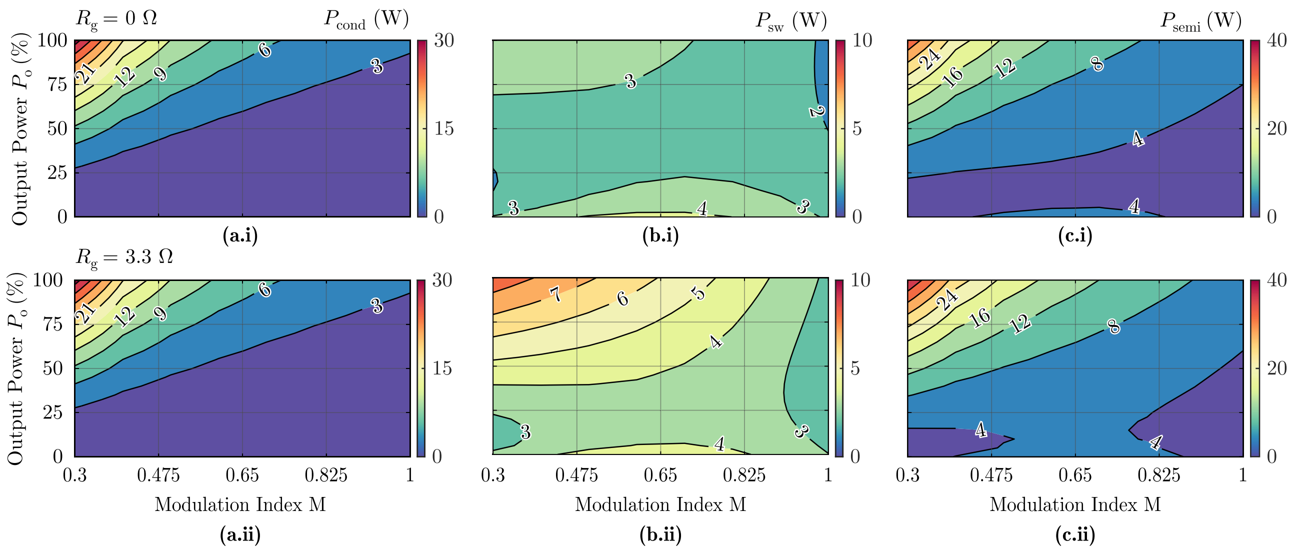


FIGURE 9. Analytically-calculated (a) conduction P_{cond}, (b) switching P_{sw}, and (c) total semiconductor losses $P_{semi} = P_{cond} + P_{sw}$ for the power semiconductor bridge-leg under the specifications given in Table 1. Evaluated for (i) $R_{g,ext} = 0\ \Omega$ and (ii) $R_{g,ext} = 3.3\ \Omega$ to highlight the importance of the residual ZVS losses in the bridge-leg performance of TCM converters.

load, and turn-off current for ZVS. The average conduction losses are:

$$P_{cond} = R_{ds}\frac{\hat{i}_{ac}^2}{3}\left(2 + \frac{4}{\pi}\gamma + \gamma^2\right). \quad (28)$$

The relative conduction losses with respect to the output power $P_o = MU_{dc}\hat{i}_{ac}/2$, result in $\frac{P_{cond}}{P_o} = \frac{2}{3}\frac{R_{ds}}{MU_{dc}}(2 + \frac{4}{\pi}\gamma + \gamma^2)\hat{i}_{ac}$ and increase with the current level.

The average switching losses of the bridge-leg are $P_{sw} = \frac{1}{T_{ac}}\int_0^{T_{ac}} p_{h,sw}(t) + p_{l,sw}(t)dt$ leading to

$$P_{sw} = \frac{MU_{dc}}{L\hat{i}_{ac}}E_{sw}, \quad (29)$$

with the average energy loss E_{sw} as function of M, $\hat{i}_{ac}$, and γ:

$$\begin{aligned} E_{sw} = &\left(1 - \frac{2M}{\pi} + \gamma M\right)a + \left(\frac{2}{\pi} - \frac{M}{2}\right)b\hat{i}_{ac} \\ &+ \left(1 - \frac{8M}{3\pi} + \gamma^2 - \gamma^2\frac{2M}{\pi} + \gamma^3 M\right)c\hat{i}_{ac}^2 \\ &+ \frac{4\gamma}{\pi}\frac{1+\gamma M}{\sqrt{\gamma^2-1}}\left(a + \gamma^2 c\hat{i}_{ac}^2\right)\arctan\left(\frac{1-\gamma}{\sqrt{\gamma^2-1}}\right). \end{aligned} \quad (30)$$

The relative switching losses are obtained by $\frac{P_{sw}}{P_o} = \frac{E_{sw}(M,\hat{i}_{ac},\gamma)}{E_{L,pk}}$ with $E_{L,pk} = L\hat{i}_{ac}^2/2$. Finally, the total semiconductor losses are $P_{semi} = P_{cond} + P_{sw}$.

These analytical switching and conduction loss expressions are evaluated across modulation index M and output power in Fig. 9 for a TCM converter of Table 1 using the *IMZA65R027M1H* SiC MOSFET with two different values of external gate resistors, **(i)** 0 Ω and **(ii)** 3.3 Ω. Conduction losses are shown in Fig. 9(a), which, as expected, do not change between the gate resistance values. Switching losses (Fig. 9(b)) – even under ZVS, we must recall – significantly increase at the higher gate resistance, as I_k is lowered and the residual ZVS losses climb rapidly with current. The $R_{g,ext} = 3.3\ \Omega$, case, however, sees the maximum du_{ds}/dt reduced from 50 $\mathrm{Vns^{-1}}$ to 35 $\mathrm{Vns^{-1}}$, cf. Fig. 6, which may be beneficial for EMI performance.

In the next section, the total loss predictions of Fig. 9(c) – and, therefore, the proposed model and analytical expressions – are validated in a hardware prototype.

V. EXPERIMENTAL VERIFICATION

The constructed hardware prototype to validate the theoretical results is shown in Fig. 10, with the filter implemented externally for flexibility. The 2.2 kW hardware prototype includes both a high-frequency (*IMZA65R027M1H* SiC MOSFETs) and an unfolder bridge-leg (*UF3SC065007K4S* SiC MOSFETs), DC-link capacitors, and the required sensor suite for control and monitoring, including a zero-crossing detection (ZCD) circuit [1] that obviates the need for a high-bandwidth current sensor.

The gate loop inductance is minimized through optimal placement and routing to support operation with a 0 Ω external gate resistor. A high-performance gate driver, TI's UCC27531, ensures the lowest possible residual ZVS losses through high-current-sink capabilities of up to 5 A and fast rise/fall times in the range of 10 ns, and we operate the gate drive at the maximum recommended positive gate voltage (+18 V) to minimize on-resistance and close to the absolute maximum of the negative gate voltage (−2 V), although during operation the negative drive voltage is measured at −1 V and this value is used for the following loss predictions.

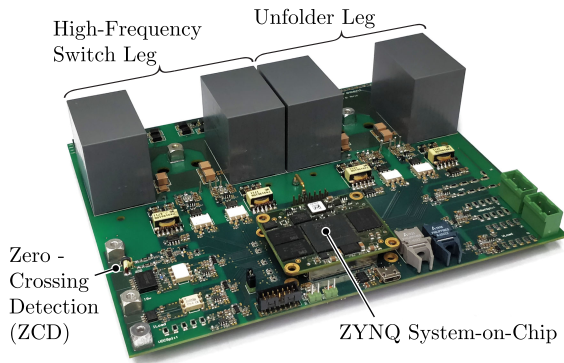
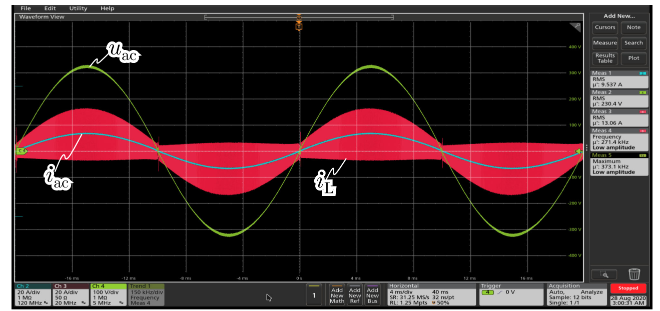
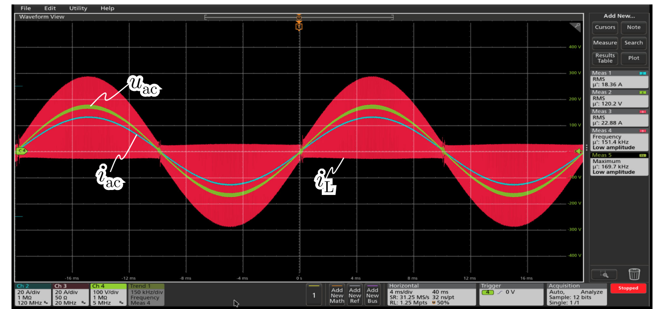


FIGURE 10. **2.2 kW hardware demonstrator (referenced to Fig. 1(a)), to validate the proposed analytical model of bridge-leg losses, switching frequency, and rms currents in a TCM converter. The hardware demonstrator includes both a high-frequency (realized with *IMZA65R027M1H* SiC MOSFETs) and an unfolder bridge-leg that can be realized with e.g., *UF3SC065007K4S* SiC MOSFETs. A zero-crossing detection (ZCD) circuit and the ZYNQ System-on-Chip are used for sensing and to ensure the inductor current is controlled to the calculated limits. The filter is implemented externally for extensibility and reconfiguration in testing.**



(a)



(b)

FIGURE 11. **Measured oscilloscope waveforms in the hardware demonstrator of Fig. 10 of phase voltage (u_{ac}), phase current (i_{ac}), and inductor current (i_L) for (a) 230 V_{rms} at full load, and (b) 120 V_{rms} at full load. The filter inductor is 11.5 μH, the turn-off current is $|I_{L-}| = 4$ A, and the external gate resistance is $R_{g,ext} = 0\ \Omega$. The voltage scale is 100 V/div, the current scale is 20 A/div, and the time scale is 4 ms/div.**

With a charge-equivalent output capacitance of $C_{oss,Q,Th} = C_{oss,Q,Tl} = 370$ pF at $U_{ds} = 400$ V for the *IMZA65R027M1H* SiC MOSFETs, the worst-case turn-off current requirements are 2.6 A at 230 V_{rms} for rectifier operation (given by Eqn. (6)) and 3.2 A at zero output voltage for inverter operation (given by Eqn. (7)). The ZCD, further, requires a small opposite-direction current for correct operation, resulting in 3.96 A minimum current when the 140 ns circuit delay (including the 20 ns switch turn-on time) is considered. To achieve ZVS under all conditions and ensure correct operation of the ZCD circuit, then, a turn-off current of $|I_{L-}| = 4$ A is selected.

Because it is only switched twice per line cycle, the unfolder bridge-leg only incurs conduction losses, and the lowest R_{ds} devices with a sufficient voltage rating can be selected, i.e., the *UF3SC065007K4S* SiC cascode MOSFET from United SiC (11.7 mΩ at 125 °C). At the worst-case operating point (full power at 120 V_{rms}), the inductor rms current is 23 A and the unfolder bridge-leg losses are 6.2 W.

Fig. 11 shows the measured oscilloscope waveforms of the hardware prototype of phase voltage (u_{ac}), phase current (i_{ac}), and inductor current (i_L). For all measured waveforms, an 11.5 µH air-core inductor is used for the filter inductor, with a 3 µF filter capacitor used for the 230 V_{rms} measurement (Fig. 11(a)) and an 11 µF filter capacitor used for the 120 V_{rms} one (Fig. 11(b)). These waveforms confirm correct operation of the hardware prototype under TCM modulation and we move to validate the proposed loss models.

Semiconductor bridge-leg losses are calculated and measured for 230 V_{rms} and 120 V_{rms} with 0 Ω and 3.3 Ω external gate resistors. The dead time is adjusted to minimize the diode conduction time. As Fig. 12 shows, the proposed fully-analytical model accurately predicts the measured semiconductor losses for the TCM hardware prototype. For all operating conditions, bridge-leg losses are predicted within 1 W at full load and within 0.9 W at 40% load. The maximum prediction error never exceeds 14% and is below 3% for most of the operating space. The worst-case partial load prediction error occurs at 40% load and $R_{g,ext} = 0\ \Omega$, with an 0.88 W underestimation (13.6%) for the 120 V_{rms} condition. At full load, the worst-case prediction error occurs with $R_{g,ext} = 3.3\ \Omega$ and 230 V_{rms}, with an underestimation of 0.99 W (11.9%). These small differences are attributed to the resonant transition times, which are neglected in the analytical model, and the remaining diode conduction losses.

Further, the E_0 losses (C_{oss}-related losses plus gating losses) are indicated in Fig. 12 to separate the contributions of these losses, which are constant with current, from the residual ZVS losses identified in this paper. At light load, the E_0 losses comprise nearly all of the semiconductor losses, while towards the nominal load – the operating point that typically drives the design of the cooling system – the residual ZVS losses must be considered for an accurate loss estimation. More tangibly, with $R_{g,ext} = 0\ \Omega$ and 230 V_{rms}, E_0 losses are 98.9% of switching losses at no load but only 48.7% at full load. Similarly, at $R_{g,ext} = 3.3\ \Omega$ and 120 V_{rms}, E_0 losses are 94.5% of switching losses at no load but only 9.3% at full load. The hardware prototype achieves a peak semiconductor efficiency of 99.6% at 230 V_{rms} at full load and 99.3% at 120 V_{rms} at 40% load. At low power levels, we see that the semiconductor

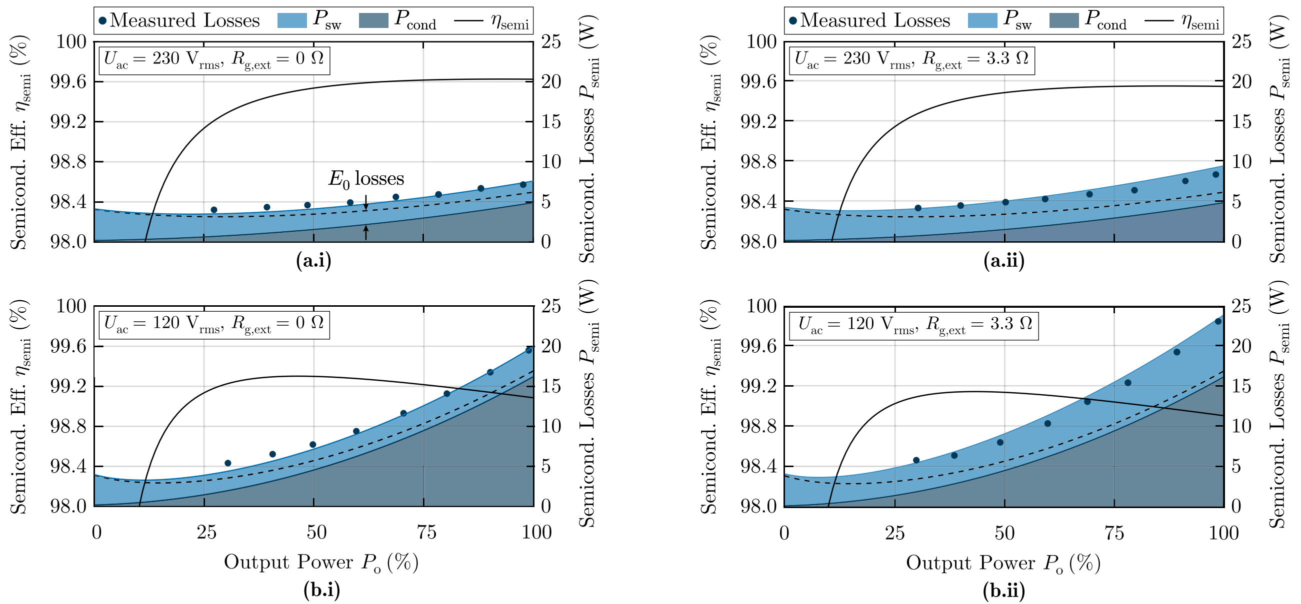


FIGURE 12. Calculated and measured semiconductor bridge-leg losses in the hardware prototype of Fig. 10 operating in TCM for (a.i) 230 V$_{rms}$ and $R_{g,ext} = 0$ Ω, (a.ii) 230 V$_{rms}$ and $R_{g,ext} = 3.3$ Ω, (b.i) 120 V$_{rms}$ and $R_{g,ext} = 0$ Ω, and (b.ii) 120 V$_{rms}$ and $R_{g,ext} = 3.3$ Ω. The total calculated losses P_{semi} are broken out into conduction losses P_{cond} and switching losses P_{sw} – with the E_0 losses, which comprise the majority of semiconductor losses at light load, indicated – and the measured semiconductor losses are shown as circles. The maximum error between predicted and measured losses is 1.0 W over the full load range.

losses rise due to the higher switching frequency, an increase that could be mitigated by increasing $|I_{L\text{-}}|$ (which would increase conduction losses but lower total losses).

The hardware prototype demonstrates the exceptional efficiencies achievable in AC-DC converters operating with TCM modulation, but, more importantly, proves the validity and efficacy of the proposed model to accurately predict bridge-leg losses with a fully-analytical solution.

VI. CONCLUSION

Triangular-current-mode (TCM) operation of AC-DC converters eliminates hard-switching losses with a rms current increase of only $\approx 15\%$ ($\approx 30\%$ increase of conduction losses) over continuous current mode (CCM) modulation, unlocking power-dense and highly-efficient inversion and rectification for this key power processing block. With switched current *and* switching frequency variation across the mains cycle, however, an analytical description of the bridge-leg losses has eluded the field.

Literature has diverged on the current-dependence of soft-switching losses in SiC MOSFETs (compare [17] to [19] and [23]). With the introduction here of the residual losses that occur *even under zero-voltage-switching* above a threshold current (the "kink current"), this work unifies the field, finding constant C_{oss}-only losses at low switched currents and current-dependent soft-switching losses above the kink current. It is interesting to note that recent work on GaN HEMTs has found a similar switching loss dependence – again under ZVS conditions on the negative gate-driver voltage in a different class of power devices [37].

In the end, the simple and accurate analytical descriptions of switching frequency, rms currents, and semiconductor losses under TCM operation open the opportunity for optimized converters without time-consuming numerical simulations, a powerful and extensive tool for the next generation of AC-DC power conversion.

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APPENDIX A
SWITCHING LOSS MEASUREMENTS ON A 1.2 kV, 16 mΩ 4-PIN SIC MOSFET

To verify the model across different blocking voltage classes of SiC MOSFETs, we also measure the switching losses on the 1.2 kV, 16 mΩ 4-pin SiC MOSFET *C3M0016120K* from Wolfspeed. An identical procedure to that outlined in Section III is repeated, with $\mathrm{d}u_{ds}/\mathrm{d}t$ measurements using the double-pulse test for two external gate resistors (here, ($R_{g,ext} = 0$ Ω and $R_{g,ext} = 5.1$ Ω) and two turn-off voltages (here, $|u_{g,n}| = 0$ V and $|u_{g,n}| = 5$ V). The results are shown in Fig. 13 and Fig. 14.

We use only the $\mathrm{d}u_{ds}/\mathrm{d}t$ measurements of Fig. 13 to fit the model parameters, which are reported in Table 4. The parameters C_{eff} and s result directly in $C_{eff} = 666$ pF (which corresponds to twice the charge equivalent output capacitance between 80 V and 720 V, or 2×313 pF), with s taken as $s = 0.2$ for simplicity. The remaining parameters are derived based on the estimated kink currents, resulting in $1 + \frac{C_{ds}}{C_{gd}} = 19.5$,

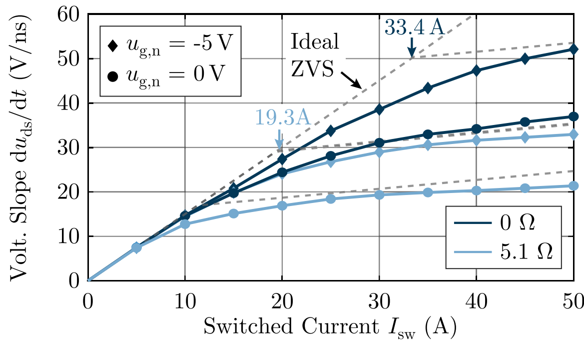

FIGURE 13. Measured du_{ds}/dt of the *C3M0016120K* for a bridge-leg (U_{dc} = 800 V) across switched currents I_{sw}. Two external gate resistors $R_{g,ext}$ = 0 Ω (dark blue), 5.1 Ω (light blue) and two gate driver voltage magnitudes $u_{g,n}$ = 0 V (circles) and $|u_{g,n}|$ = 5 V (diamonds) are used to show the variation in I_k predicted by Eqn. (17). The results of the model (cf. Eqn. (17), Eqn. (19)), are overlaid to validate the proposed approach.

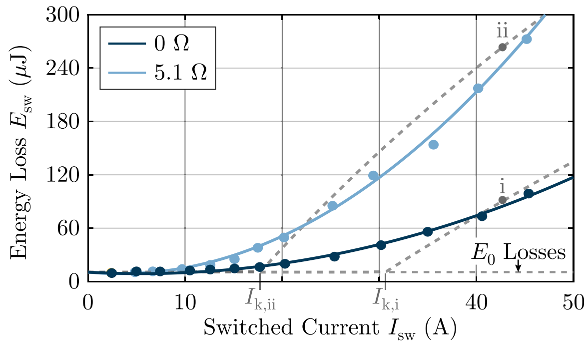

FIGURE 14. Measured soft-switching energy losses E_{sw} of the *C3M0016120K* for a full bridge-leg (U_{dc} = 800 V) across switched currents I_{sw}, with adapted deadtimes to ensure complete soft-switching transitions. Two external gate resistors $R_{g,ext}$ = 0 Ω (dark blue, i), 5.1 Ω (light blue, ii) are used to show the variation in I_k predicted by Eqn. (17) considering the measured $|u_{g,n}|$ = 4 V. The results of the model (cf. Eqn. (17), Eqn. (19), and Eqn. (22)), are overlaid to validate the proposed approach.

TABLE 4. Model Parameter of the *C3M0016120K*

	C_{eff}	u_{th}	$R_{g,int}$	$1+\frac{C_{ds}}{C_{gd}}$	s
Fit	666 pF	7 V	7 Ω	19.5	0.2
Datasheet	626 pF	6.5 V	2.6 Ω	-	-

u_{th} = 7 V (which corresponds to the datasheet value of the extracted threshold voltage of 6.5 V for the given typical transfer characteristic), and $R_{g,int}$ = 7 Ω, which is larger than specified in the datasheet (2.6 Ω). The resulting kink currents are I_k = 19.3 A ($R_{g,ext}$ = 0 Ω) and 11.5 A ($R_{g,ext}$ = 5.1 Ω) for $u_{g,n}$ = 0 V and 33.4 A ($R_{g,ext}$ = 0 Ω) and 19.3 A ($R_{g,ext}$ = 5.1 Ω) for $u_{g,n}$ = 5 V, as shown in Fig. 13.

Switching losses are again measured calorimetrically [36] with the two external gate resistors. During the experiments, the negative gate driver voltage magnitude was measured at $|u_{g,n}|$ = 4 V (due to a voltage drop within the gate drive, which also occurs during *in-situ* operation), leading to

TABLE 5. Calculated and Fitted Switching Loss Coefficients for a 1.2 kV SiC MOSFET (*C3M0016120K*) Operated At U_{dc} = 800 V and Under ZVS, Valid for $E_{sw} = a + bI_{sw} + cI_{sw}^2$ With I_{sw} > 0 A

Coefficient	$R_{g,ext} = 0\,\Omega$	$R_{g,ext} = 5\,\Omega$
I_k in A	30.6	17.7
$\left.\frac{du_{ds}}{dt}\right\|_k$ in V/ns	46.0	26.6
$\tilde{k}$ in μJ/A	5.6	9.7
E_0 in μJ	10.5	10.5
a in μJ	10.5	10.5
b in nJ/A	-607	-1021
c in nJ/A^2	55	152

E_0 = 10.5 μJ with gating losses included. The measured switching losses under ZVS are shown in Fig. 14, and the key results are given in Table 5. Again, the proposed model accurately predicts the maximum voltage slew rate, the existence of an asymptote, the current at which switching losses increase rapidly above E_0, and, in the end, the switching losses for the 1.2 kV SiC MOSFET.

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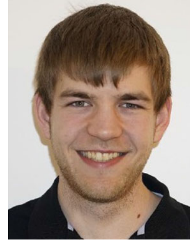

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