Power Electronic Systems
Laboratory

Proceedings of the 22nd IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2021), Virtual Conference, Bogotá, Colombia, November 2-5, 2021

New Third-Harmonic Injection Modulation Reducing the DC-Link Energy Buffer Requirement of Phase-Modular Three-Phase Isolated PFC AC/DC Converter Systems

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***Abstract*—Realizing an isolated three-phase AC/DC converter system with three front-end single-phase PFC rectifier modules referenced to a common star point allows low DC-link voltage levels of 400 V in contrast to standard three-phase boost-type PFC rectifiers operating with a DC-link of 800 V. Hence, the usage of superior 600 V GaN switches instead of 1.2 kV SiC MOSFETs and accordingly a high system efficiency is enabled. The main drawback of this phase-modular approach, however, is that each of the modules is subject to a twice-mains frequency power pulsation, which is inherent in single-phase AC/DC operation, and requires bulky electrolytic DC-link capacitors to buffer the pulsating input power. In this paper, a new modulation method is presented which takes advantage of the three-phase and/or star connection of the three single-phase PFC rectifier modules and injects a common-mode (zero-sequence) component, e.g., a 3rd harmonic voltage component into the AC-side voltage formation of the rectifier switching stages, which shifts part of the power pulsation to higher frequencies and accordingly reduces the low-frequency peak-to-peak voltage ripple and RMS current of the DC-link capacitors. A detailed analysis reveals that this method allows to cut the DC-link capacitor volume by up to 30 % without the need of increasing the DC-link voltage reference setpoint or increasing the voltage rating of the capacitors and power semiconductors.**

***Index Terms*—AC/DC converter, three-phase, modular, harmonic injection**

I. Introduction

Standard isolated three-phase (3-Φ) AC/DC converter systems are realized by combining a two-level boost-type Power Factor Correction (PFC) rectifier with an isolated DC/DC converter as illustrated in **Fig. 1a**. There, a high DC-link voltage of approximately $800\,\mathrm{V}$ results, and accordingly, $1.2\,\mathrm{kV}$ Silicon Carbide (SiC) power semiconductors are employed [1]. Alternatively, as highlighted in **Fig. 1b** three single-phase (1-Φ) PFC rectifier stages followed by individual isolated DC/DC converters can be joined in a common star point $\bar{N}$ [2]–[5], where low DC-link voltages of approximately $400\,\mathrm{V}$ are sufficient for phase current control and allow the usage of $600\,\mathrm{V}$ semiconductors. There, in each rectifier stage advantageously a fast-switching Gallium Nitride (GaN) half-bridge is employed in combination with a low on-state resistance Silicon (Si) Super Junction (SJ) unfolder bridge-leg, enabling ever-higher efficiencies close to, or even above $99\,\%$ [6] [7]. As analyzed in [8], a multi-level converter with six or more levels would be required for an $800\,\mathrm{V}$ DC-link 3-Φ AC/DC converter to meet or exceed the efficiency of a phase-modular two-level $400\,\mathrm{V}$ DC-link converter. Accordingly, this paper focuses on the modular approach with three 1-Φ PFC rectifier stages in star connection as depicted in **Fig. 1b**.

Here, the main downside is that each module is inherently subject to a twice-mains frequency input power pulsation: For example, a 1-Φ converter module in **Fig. 1b** with an average DC-link voltage of $400\,\mathrm{V}$ and a nominal input power of $3.3\,\mathrm{kW}$, requires a DC-link capacitor of approximately $800\,\mu\mathrm{F}$ to maintain the twice-mains frequency DC-link peak-to-peak voltage ripple safely below $40\,\mathrm{V}$. Note, that for the standard converter presented in **Fig. 1a** the time varying input powers of the three bridge-legs add up to a constant instantaneous power flow into the DC-link and accordingly, the DC-link capacitor only serves for the filtering of switching frequency power pulsation components and substantially lower capacitor values can be selected.

Typically, the low-frequency input power pulsations of the phase modules of the converter system in **Fig. 1b** are buffered using electrolytic DC-link capacitors, which consume a substantial share of the converter volume, and eventually limit the system lifetime [9] [10]. To reduce the DC-link capacitor volume and to ultimately enable ever-higher rectifier power densities, the usage of an active power pulsation buffer [11] [12], or the processing of the pulsating input power by the subsequent isolated DC/DC converters [5] is discussed in literature. However, both approaches result in an increased realization effort and complexity.

This paper proposes a modulation strategy that allows to reduce the DC-link energy buffering requirement by means of injecting a common-mode voltage [13] [14] between the grid

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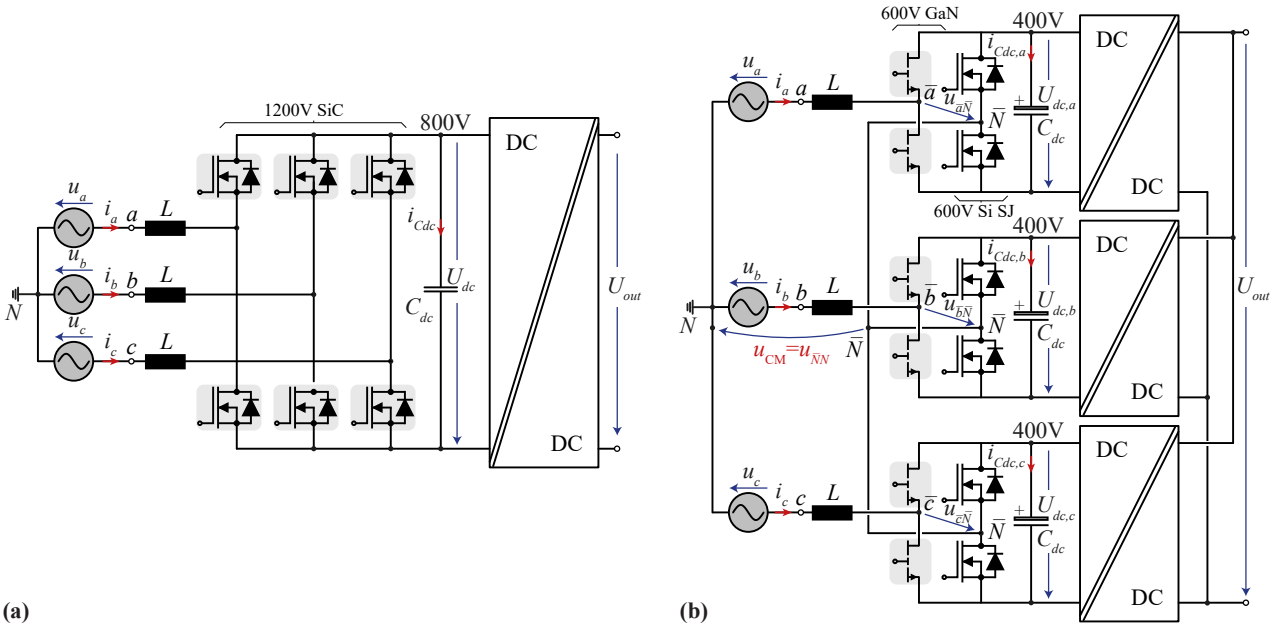

Fig. 1. (a) Standard isolated 3-Φ AC/DC converter system comprising a PFC rectifier front-end followed by an isolated DC/DC stage. For operation in 400 V and 480 V (line-to-line, RMS) mains, 800 V are typically selected as DC-link voltage level. **(b)** Alternative phase-modular realisation of the AC/DC converter employing a star-connection of 1-Φ PFC rectifier modules with individual isolated DC/DC converter stages and DC-link voltages around 400 V.

star point N and the star point $\bar{N}$ of the AC/DC converter modules in **Fig. 1b**. No additional hardware is required for the implementation of this modulation concept detailed in **Section II-A**, where **Section II-B** further discusses limits for the minimum allowable DC-link capacitor value imposed by grid current controllability and semiconductor blocking voltage constraints. A control concept realizing the harmonic injection strategy is then presented in **Section II-C** and verified by means of circuit simulations in **Section II-D**. Subsequently, **Section III** briefly discusses an equivalent modulation method for *delta*-connected 1-Φ PFC rectifier modules, i.e., the injection of a common-mode *current* circulating in the delta arrangement. Finally, in **Section IV**, the main findings of this paper are recapitulated and potential paths for further research are outlined.

II. Star-Connected Phase-Modular Converter

A. Operation Principle

The reference values of the input voltages $u_{\bar{a}\bar{N}}$,$u_{\bar{b}\bar{N}}$,$u_{\bar{c}\bar{N}}$ of the PFC rectifier stages with respect to the common star point $\bar{N}$ (cf., **Fig. 1b**) are set such that the three grid input currents i_a,i_b,i_c are in phase with the respective grid voltages u_a,u_b,u_c. The converter equivalent circuit is shown in **Fig. 2a.i**, where the converter bridge-legs are represented by high-frequency $u_{\bar{a}\bar{N}\sim}$,$u_{\bar{b}\bar{N}\sim}$,$u_{\bar{c}\bar{N}\sim}$ and low-frequency (defined by the local average values over a pulse interval) $\bar{u}_{\bar{a}\bar{N}}$,$\bar{u}_{\bar{b}\bar{N}}$,$\bar{u}_{\bar{c}\bar{N}}$ voltage sources. **Fig. 2a.ii** further differentiates the Differential-Mode (DM) and Common Mode (CM) components of the input voltages of the rectifier switching stages, where a virtual star point $\bar{N}'$ is formed. Since there is no hard (or low impedance in low frequency) connection between the grid star point N and the converter star point $\bar{N}$, the low-frequency CM voltage $u_{\mathrm{CM}} = \bar{u}_{\bar{N}'\bar{N}}$ does not drive any current and, accordingly, represents a degree of freedom for the modulation strategy, and can be varied while PFC operation with sinusoidal grid currents is maintained.

Basically, any CM voltage u_{CM} could be injected, but in favour of keeping a balanced and symmetric 3-Φ system, u_{CM} should only be formed by 3rd, 9th, 15th, etc. harmonic components with reference to the grid frequency. In the subsequent analysis, for simplicity, only a 3rd harmonic component, i.e., a 150 Hz component for a 50 Hz grid will be used with

$$u_{\mathrm{CM}}(t) = M_3 \hat{U}_{\mathrm{ac}} \sin(3\omega t), \tag{1}$$

where $\hat{U}_{\mathrm{ac}}$ is the peak line-to-neutral grid voltage (with respect to the grid star point N), ω denotes the angular frequency of the grid, and $M_3 = \hat{U}_{\mathrm{CM}}/\hat{U}_{\mathrm{ac}}$ is the 3rd harmonic modulation index. Accordingly, the PFC rectifier stage low-frequency input voltage of the module $j \in \{a, b, c\}$ results to

$$\bar{u}_{\bar{j}\bar{N}}(t) = \hat{U}_{\mathrm{ac}} \sin(\omega t + \theta_j) + u_{\mathrm{CM}}(t), \tag{2}$$

with $\theta_a = 0, \theta_b = -\frac{2\pi}{3}, \theta_c = -\frac{4\pi}{3}$. The low-frequency module input power $\bar{p}_{\bar{j}}$ is then defined by $\bar{u}_{\bar{j}\bar{N}}$ and the corresponding low-frequency grid current $\bar{i}_j$ as

$$\bar{p}_{\bar{j}}(t) = \bar{u}_{\bar{j}\bar{N}}(t) \cdot \bar{i}_j(t). \tag{3}$$

Fig. 2b depicts the 3-Φ grid voltages, the low-frequency module input voltages, as well as the low-frequency CM voltage within one mains period for $M_3 = 1/6$, i.e., the harmonic modulation index typically selected in the standard 3-Φ system of **Fig. 1a** to maximize the DC-link voltage utilization [13].

To evaluate the impact of the CM voltage component on the

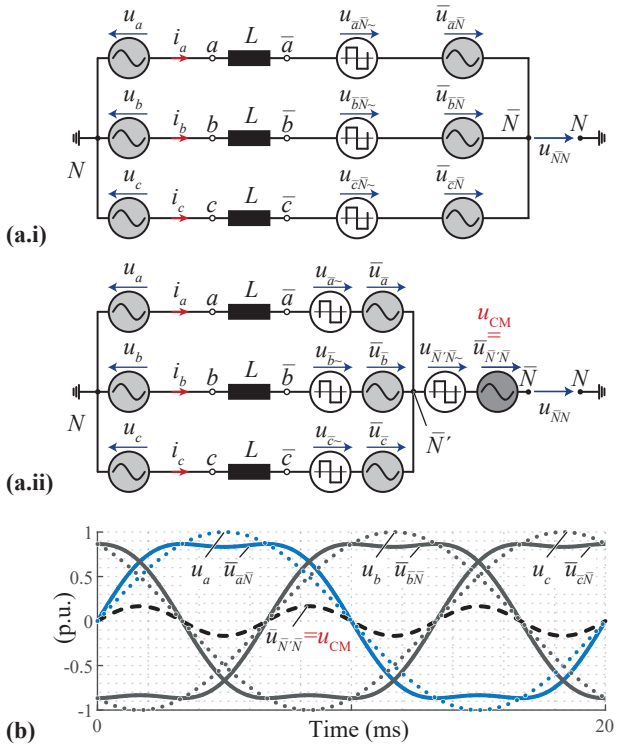

Fig. 2. AC-side equivalent circuit of the converter shown in **Fig. 1b** with **(a.i)** separate low-frequency and high-frequency and **(a.ii)** separate DM and CM module input voltage sources of the PFC rectifier switching stages. **(b)** Waveforms of the grid phase voltages and of the low-frequency components of the input voltages of the rectifier switching stages and of the injected CM voltage.

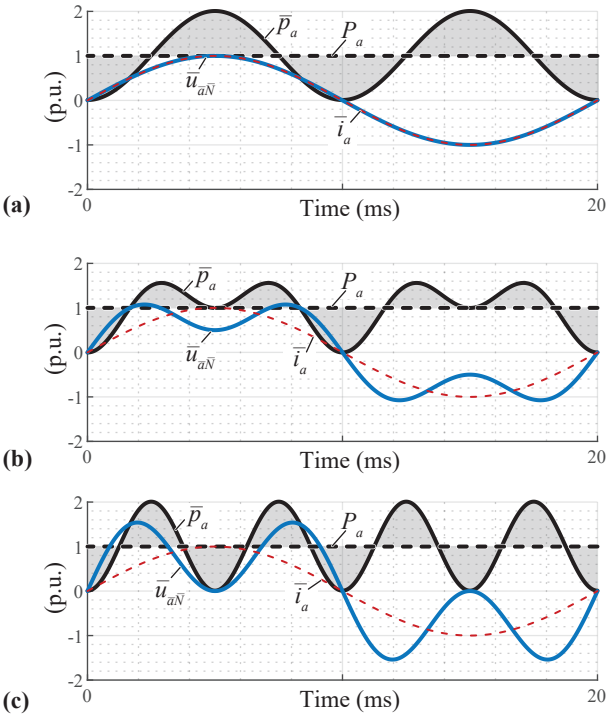

Fig. 3. Phase a switching stage low-frequency input voltage $\bar{u}_{\bar{a}\bar{N}}$, current $\bar{i}_{\mathrm{a}}$ and power $\bar{p}_{\mathrm{a}}$ within one mains period for a 3rd harmonic modulation index of **(a)** $M_3 = 0$, **(b)** $M_3 = 0.5$ and **(c)** $M_3 = 1.0$. Note, that the average input power P_{a} is represented by a dashed line and is not impacted by M_3.

power flow of a converter phase module, **Fig. 3** depicts the module a low-frequency switching stage input voltage $\bar{u}_{\bar{a}\bar{N}}$, current $\bar{i}_{\mathrm{a}}$ and power $\bar{p}_{\mathrm{a}}$ for different harmonic modulation indices: Without any CM injection (i.e., $M_3 = 0$, cf., **Fig. 3a**), the power pulsation occurs purely at twice the grid frequency (i.e., at 100 Hz for a 50 Hz grid). The energy buffered in the DC-link capacitor $E(t) = \int (p_{\mathrm{a}}(t) - P_{\mathrm{a}})\,\mathrm{d}t$ (with maximum value ΔE) is defined by the difference between the instantaneous input power p_{a} and the average power P_{a} related to a mains period [11]. By employing a value of $M_3 = 0.5$ in **Fig. 3b**, the module input voltage $\bar{u}_{\bar{a}\bar{N}}$ comprises an according 3rd harmonic voltage component, while the sinusoidal input current remains. Accordingly the input power flow time behavior is manipulated, which now shows a reduced amplitude, as well as additional higher frequency components. Still, the same average input power P_{a} is drawn from the grid as in **Fig. 3a**, while the value of ΔE is reduced by approximately 35 %. Finally, with $M_3 = 1.0$, the peak value of the pulsating input power p_{a} in **Fig. 3c** is identical to **Fig. 3a**, however, oscillates at twice the frequency compared to $M_3 = 0$ and accordingly, here, ΔE is reduced to 50 %, thus reducing the energy storage requirement of the DC-link to half. However, this would come at a cost of 50 % larger peak input voltage $\bar{u}_{\bar{a}\bar{N}}$, which would consequently require a higher DC-link voltage, which should

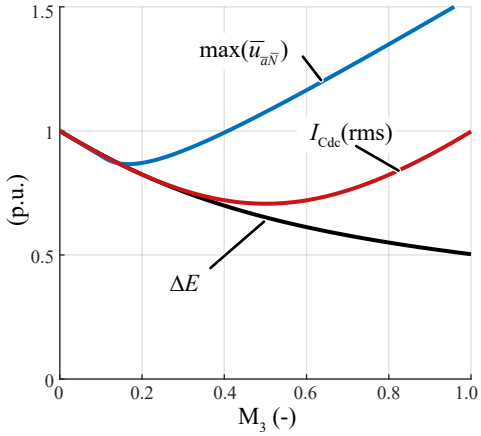

Fig. 4. Impact of the 3rd harmonic injection index M_3 on the maximum value of $\bar{u}_{\bar{a}\bar{N}}$, the RMS value of the DC-link capacitor current, I_{Cdc}, and the power pulsation buffer requirement in terms of energy, ΔE. M_3=0 represents the conventional purely sinusoidal modulation of the rectifier stages of the phases (cf., **Fig. 3a**).

be avoided as the rating of the employed DC-link (electrolytic) capacitors is typically 450 V.

The trade-off between the reduction of the energy buffer requirement and the peak input voltage is given in **Fig. 4**, together with the (low-frequency) RMS current of the DC-link capacitor.

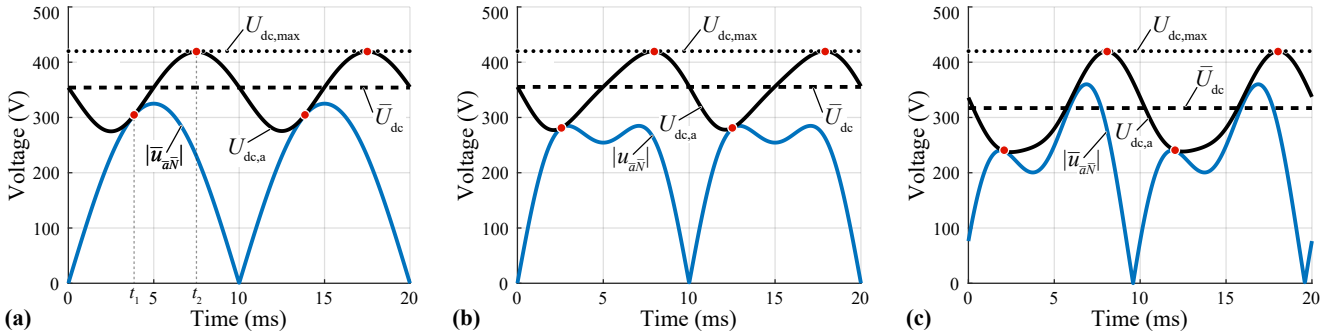

Fig. 5. Theoretical module a DC-link voltage $U_{\mathrm{dc,a}}$ and absolute value of the low-frequency rectifier input voltage $|\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}|$ within one mains period for $\hat{U}_{\mathrm{ac}} = 325\,\mathrm{V_{pk}}$, a module input power of 3.3 kW and **(a)** standard operation with $M_3 = 0$, $C_{\mathrm{dc}} = 208\,\mu\mathrm{F}$ and $\bar{U}_{\mathrm{dc}} = 352\,\mathrm{V}$, **(b)** $M_3 = 0.22$ ($\phi_3 = 0$), $C_{\mathrm{dc}} = 170\,\mu\mathrm{F}$ and $\bar{U}_{\mathrm{dc}} = 352\,\mathrm{V}$, as well as **(c)** $M_3 = 0.33$ ($\phi_3 = 45°$), $C_{\mathrm{dc}} = 140\,\mu\mathrm{F}$ and $\bar{U}_{\mathrm{dc}} = 317\,\mathrm{V}$.

B. Minimum DC-Link Capacitance Considerations

The minimum capacitance value of an electrolytic DC-link capacitor is defined by either the maximum DC-link voltage variation and/or the maximum RMS current ripple criterion based on capacitor lifetime considerations [10]. In contrast, when employing capacitor technologies with high voltage ripple capability (e.g., film or multi-layer ceramic capacitors), the minimum DC-link capacitance value of each module $j \in \{a, b, c\}$ is defined by, a grid and/or input current controllability constraint [15]

$$\bar{u}_{\bar{\mathrm{j}}\bar{\mathrm{N}}}(t) \leq U_{\mathrm{dc,j}}(t), \tag{4}$$

as well as a maximum DC-link voltage value $U_{\mathrm{dc,max}}$ imposed by either the admissible semiconductor blocking voltage or the DC-link capacitor rated voltage

$$U_{\mathrm{dc,j}}(t) \leq U_{\mathrm{dc,max}}. \tag{5}$$

Fig. 5a displays theoretical voltage waveforms for standard purely sinusoidal modulation ($M_3 = 0$) with a minimum DC-link capacitance value of $C_{\mathrm{dc}} = 208\,\mu\mathrm{F}$, where for 600 V GaN semiconductors criterion (5) results to $U_{\mathrm{dc,max}} = 420\,\mathrm{V}$ when considering a standard blocking voltage margin of 30 %. Note, that the average DC-link voltage $\bar{U}_{\mathrm{dc}}$ over a mains period (highlighted by a dashed line in **Fig. 5**) is a degree of freedom for the modulation. When aiming for the minimum DC-link capacitor value $C_{\mathrm{dc,min}}$, $\bar{U}_{\mathrm{dc}}$ is selected such that both $\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}(t = t_1) = U_{\mathrm{dc,a}}(t = t_1)$ and $U_{\mathrm{dc,a}}(t = t_2) = U_{\mathrm{dc,max}}$ occur within one half mains period (cf., **Fig. 5a**).

For comparison, the main voltage waveforms for a 3rd harmonic injection of $M_3 = 0.22$ and a minimum DC-link capacitor value $C_{\mathrm{dc}} = 170\,\mu\mathrm{F}$ are shown **Fig. 5b**, again respecting $U_{\mathrm{dc,max}} = 420\,\mathrm{V}$. It becomes obvious that compared to the theoretical considerations in **Section II-A** (DC-link capacitance reduction of up to 30 % without an elevated input voltage by means of 3rd harmonic injection), a limited capacitance reduction of only 18 % results here. The reason for this lies in the fact that the waveforms in **Fig. 5b** are ill-conditioned in a sense that the maximum value of the input voltage $\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}$ results in the close vicinity of the DC-link voltage $U_{\mathrm{dc,a}}$ minimum value. Accordingly, values of $M_3 > 0.22$ do not allow a further reduction of $C_{\mathrm{dc,min}}$ compared to $M_3 = 0.22$. To overcome this limitation, **Fig. 5c**

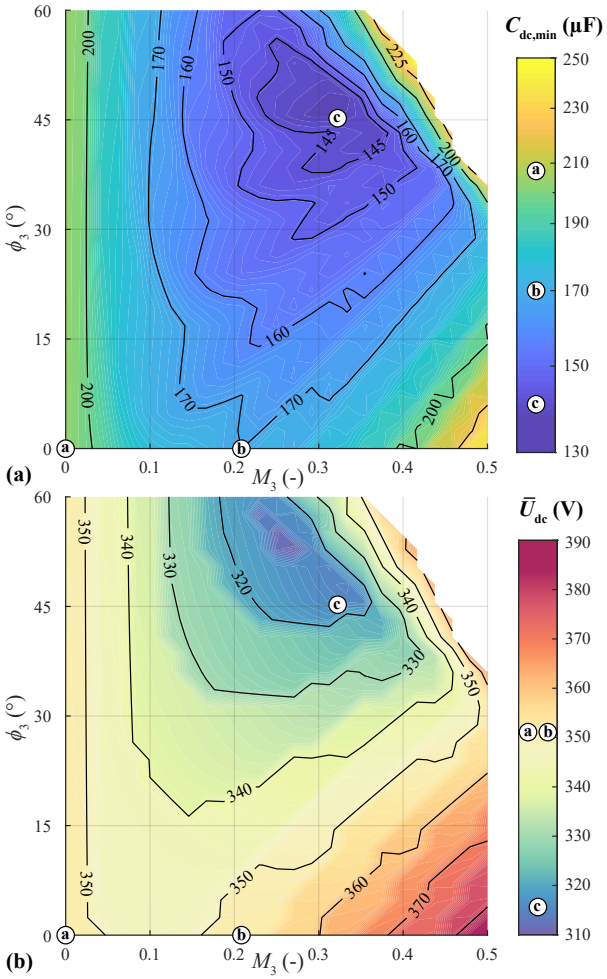

Fig. 6. (a) Impact of the 3rd harmonic injection modulation index M_3 and angle ϕ_3 (cf., (6)) on the minimum DC-link capacitance value $C_{\mathrm{dc,min}}$. **(b)** Corresponding average DC-link voltage values $\bar{U}_{\mathrm{dc}}$ within one grid period. The highlighted parameter sets ⓐ-ⓒ refer to the waveforms shown in **Fig. 5a-c**. Capacitance values $C_{\mathrm{dc,min}}$ above 250 µF (and the corresponding values of $\bar{U}_{\mathrm{dc}}$) are not displayed and accordingly the top right corners are left blank.

displays voltage waveforms for operation with a 3rd harmonic voltage *phase-shifted* by an angle ϕ_3 as

$$u_{\mathrm{CM}}(t) = M_3 \hat{U}_{\mathrm{ac}} \sin(3\omega t + \phi_3), \tag{6}$$

with $M_3 = 0.33$, $\phi_3 = 45°$ and a capacitance value $C_{\mathrm{dc}} = 140\,\mu\mathrm{F}$ (i.e., reduced by 33 % compared to **Fig. 5a**). Note, that although the maximum input voltage value ($\bar{u}_{\bar{\mathrm{a}}\bar{\mathrm{N}}}$) is increased compared to the waveforms in **Fig. 5a,b**, both constraints (4) and (5) are respected.

To allow further insights on the impact of the 3rd harmonic voltage injection, **Fig. 6a** and **b** display the minimum eligible DC-link capacitance value $C_{\mathrm{dc,min}}$ and the corresponding average DC-link voltage $\bar{U}_{\mathrm{dc}}$, respectively, as a function of the 3rd harmonic modulation index M_3 and angle ϕ_3. There, the modulation parameters of **Fig. 5a-c** corresponding to **(a)** the minimum capacitance value for operation without harmonic injection, **(b)** harmonic injection in phase with the grid voltages (up to 18 % reduction of $C_{\mathrm{dc,min}}$), and **(c)** phase-shifted harmonic injection (up to 33 % reduction of $C_{\mathrm{dc,min}}$) are highlighted.

It is important to mention that in practical implementations a certain margin against the limits (4) and (5) needs to be maintained, which can be achieved by selecting a capacitance value e.g., 10 % to 20 % larger than $C_{\mathrm{dc,min}}$.

C. Control Concept

The block diagram of a cascaded control of the PFC rectifier input stages of **Fig. 1b** considering a 3rd harmonic CM voltage injection u^*_{CM} is depicted in **Fig. 7**: The outer (low-bandwidth) controller RU_{dc} receives a DC-link voltage reference U^*_{dc} and compares it to the grid frequency average of the three DC-link voltages.

The reason to regulate the average of the three DC-link voltages and not the individual DC-link voltage is, that the three modules are mutually coupled due to the open star point $\bar{N}$. If, in case of individual DC-link voltage control loops the DC-link voltage of, e.g., module a would be higher, this module would aim to decrease its input power by decreasing the corresponding input current resulting in a higher switching stage input voltage. Due to the effective series connection of the modules in a star arrangement (cf., **Fig. 1b**, **Fig. 2a**), this would lead to effectively lower input voltages of the modules b and c, which now would strive to maintain a certain power flow by building up higher input currents, which finally would need to return via phase a but be in conflict with the phase a current reduction requirement, potentially rendering the system unstable [3].

Here, in contrast, the module with the on average highest voltage transfers slightly more power, i.e., similar to a resistive behavior and the 3-Φ system remains balanced [16]. The controller RU_{dc} defines an equal power reference for all modules $j \in \{a, b, c\}$ which can be used to calculate the required conductivity G^*_j and therewith the current reference of each phase i^*_j. This current reference is then compared to the measured input current, and fed into an underlying current controller Ri_j which outputs a reference for the voltage to

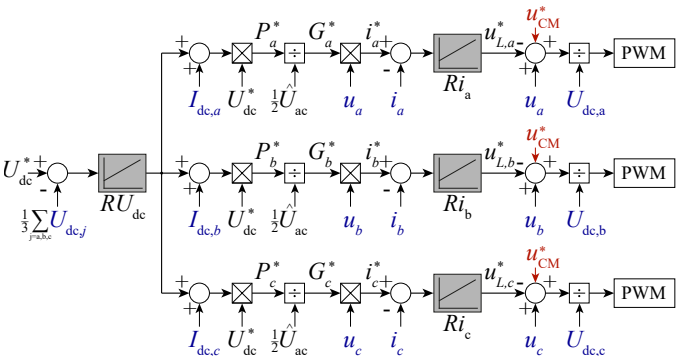

Fig. 7. Block diagram of a cascaded control of the PFC rectifier input stages of **Fig. 1b** considering a 3rd harmonic CM voltage injection u^*_{CM}.

be applied across the input (boost) inductor L, $u^*_{\mathrm{L},j}$, in order to control the input current i_j. This value is then subtracted from the measured grid phase voltage feed-forward, u_j, and the arbitrarily injected CM voltage reference, u^*_{CM}, to finally generate the PWM signals. It's worth mentioning, that the CM reference voltage u^*_{CM} could also be impressed actively by a dedicated CM voltage regulator.

D. Simulation

Fig. 8 depicts 3-Φ steady-state module input voltages, input currents, and the variation of the DC-link voltages from a closed-loop circuit simulation with the control structure according to **Fig. 7**. There, 3rd harmonic modulation indices of M_3 = 0, 0.2 and 0.4 are considered. According to **Fig. 4**, up to M_3=0.4 can be injected without increasing the peak of the low-frequency switching stage input voltage $\bar{u}_{\bar{\mathrm{j}}\bar{\mathrm{N}}}$ above the peak $\hat{U}_{ac}$ of the grid phase voltage, which is in line with the results in **Figs. 8(a-c.i)**. For all cases the input currents are balanced, cf., **Figs. 8(a-c.ii)**, but it is noteworthy that the current ripple envelopes change for different M_3 values, as the duty cycle variation changes over the mains period for each case. For instance, assuming U_{dc} = 400 V, with M_3=0, the duty cycle at e.g., $\omega t = \frac{\pi}{2}$ (i.e., at the peak of the grid current i_{a}) is $d \approx 0.81$, whereas for M_3=0.4 the duty cycle at $\omega t = \frac{\pi}{2}$ is $d \approx 0.49$, leading to a locally larger current ripple. It is worth highlighting again, that the adapted modulation strategy impacts the high-frequency inductor current waveforms, but does not introduce a low-frequency harmonic distortion.

Finally, and most importantly, the voltage ripple of the DC-link capacitors seen in **Figs. 8(a-c.iii)** is reduced due to the shift of part of the power pulsation to higher frequencies. Furthermore, the RMS currents stress on C_{dc} is lowered. The DC-link voltage ripple is reduced for M_3=0.2 and M_3=0.4 by 17.3 % and 29.6 %, and the RMS value of i_{Cdc} is reduced by 16.8 % and 26.8 %, respectively, hence, allowing for an according DC-link capacitance reduction.

III. Delta-Connected Phase-Modular Converter

Fig. 9a depicts a phase-modular AC/DC converter realisation employing a *delta*-connection of 1-Φ PFC rectifier modules

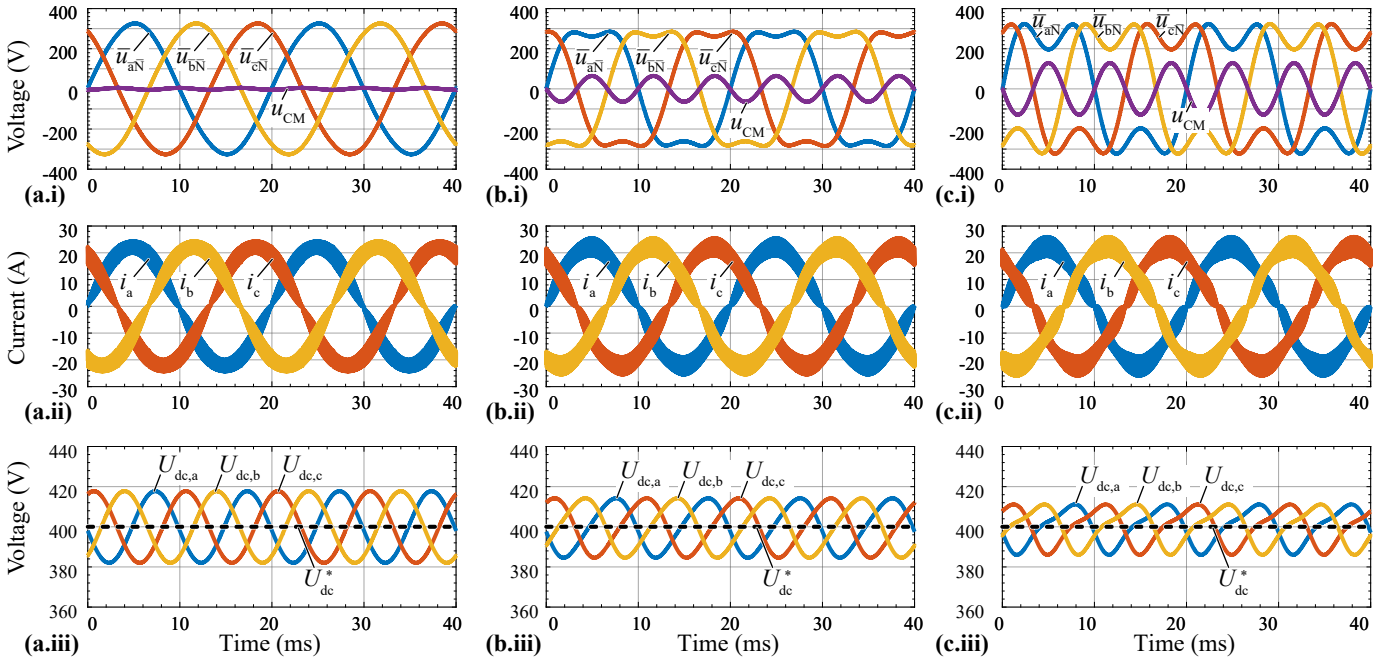

Fig. 8. Circuit simulation results for the **(i)** low-frequency input voltages of the PFC rectifier switching stages, $\bar{u}_{\bar{a}\bar{N}}$,$\bar{u}_{\bar{b}\bar{N}}$,$\bar{u}_{\bar{c}\bar{N}}$, **(ii)** grid input currents i_a,i_b,i_c , and **(iii)** DC-link voltages $U_{dc,a}$,$U_{dc,b}$,$U_{dc,c}$ for different 3rd harmonic modulation indices, of **(a)** M_3=0, **(b)** M_3=0.2, and **(c)** M_3=0.4. Simulation parameters: power 3x 3.3 kW, switching frequency 140 kHz, L=100 µH, C_{dc}=800 µF and U^*_{dc}=400 V.

with individual isolated DC/DC stages. The DC-link voltage levels are around 700 V (assuming a 400 V RMS line-to-line mains) such that 900 V SiC power semiconductors can be employed in combination with a 900 V Si SJ unfolder bridge-leg. Note, that, compared to the converter in **Fig. 1b** the grid input currents are reduced by a factor of $\sqrt{3}$ and hence semiconductors with a higher on-state resistance (and lower chip area) can be employed. Further, input line-failure redundancy can be achieved by extending the circuit of **Fig. 9a** with a simple thyristor circuitry [17].

The AC-side equivalent circuit of this converter is shown in **Fig. 9b**, where again (cf., **Fig. 2**) the converter bridge-legs are represented by high-frequency and low-frequency (defined by the local average values over a pulse interval) voltage sources. As discussed in [18]–[20], a CM current i_0 circulating inside the delta-connection of the three 1-Φ modules can be generated and **Fig. 9c** displays the resulting low-frequency grid and module input currents within one mains period for a CM current amplitude equal to $1/6$ of the sinusoidal grid current amplitude. According to (3) and similar to the harmonic voltage injection discussed in **Section II**, the CM current i_0 allows here to shape the module input power flow in such a way that the DC-link capacitance requirement can be again reduced substantially. In this context it is interesting to also refer to harmonic injection techniques proposed in [21] for the minimization of low power 1-Φ AC/DC converters.

IV. Conclusions

Modular isolated 3-Φ AC/DC converter systems comprising three 1-Φ PFC rectifier modules in star connection feature a low DC-link voltage level of approximately 400 V (assuming a 400 V RMS line-to-line mains), and hence allow the usage of 600 V GaN semiconductors and extremely high-efficient converter system realizations. However, for conventional sinusoidal modulation this modular approach requires large DC-link capacitors in each module to buffer the pulsating input power inherent to 1-Φ AC/DC power conversion.

In this paper, a novel 3rd harmonic injection modulation for phase-modular 3-Φ isolated AC/DC converter systems is presented. The extension of the input voltage formation of the PFC rectifier stages with a 3rd harmonic component results in a shift of part of the power pulsation to higher frequencies, resulting in a reduced DC-link buffer capacitance requirement (and hence, the associated component volume) by more than 30 %. A cascaded control structure enabling the reduced energy buffering constraint while maintaining sinusoidal grid currents is derived and verified by means of closed-loop circuit simulations. Further, a corresponding harmonic *current* injection method for a delta-connected converter is briefly outlined.

Finally, it is important to point out that the analysis of this paper was limited to the injection of a 3rd harmonic voltage component, whereas a large number of harmonic injection strategies was developed for 3-Φ inverter (and rectifier) systems [22]. Hence, future research could consider the impact of harmonic injection waveforms other than the 3rd harmonic and could consider the switching frequency ripple of the phase currents and/or DM and CM high-frequency noise generation besides the DC-link buffering requirement.

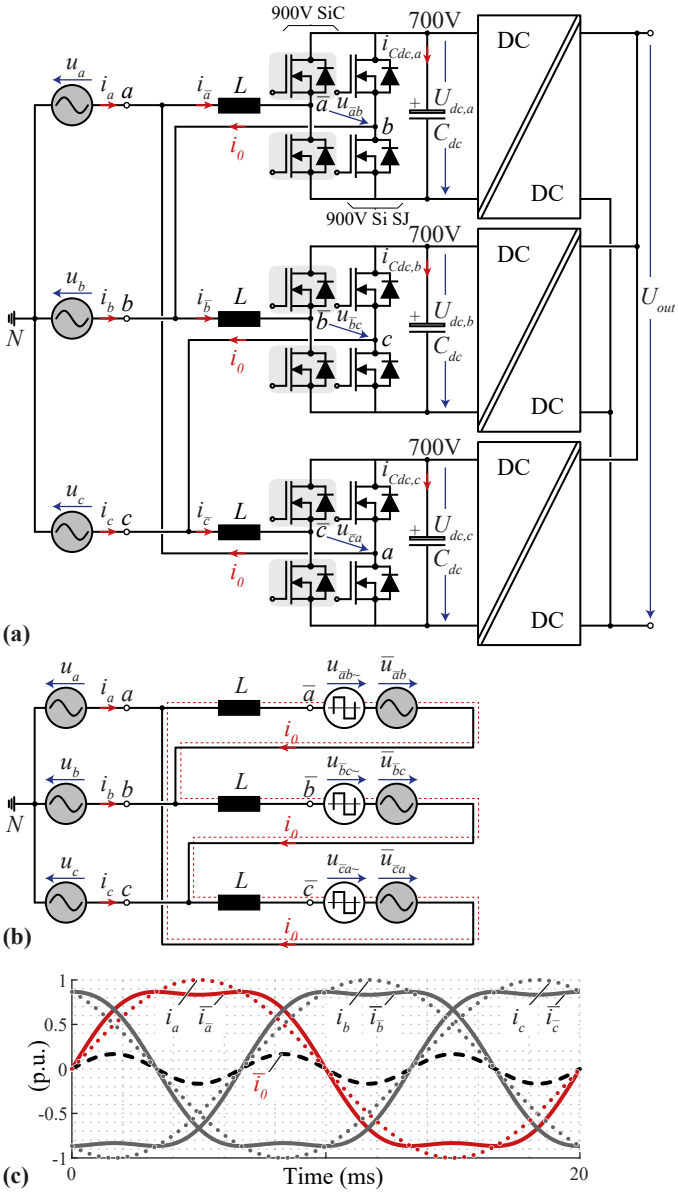

Fig. 9. (a) 3-Φ phase-modular AC/DC converter realisation employing a *delta*-connection of 1-Φ PFC rectifier modules with individual isolated DC/DC stages and DC-link voltages around 700 V. **(b)** AC-side equivalent circuit of the converter shown in **(a)** with separate low-frequency and high-frequency equivalent input voltage sources of the PFC rectifier stages. **(c)** Waveforms of the grid phase currents and of the low-frequency components of the input currents of the rectifier switching modules and of the CM current i_0 circulating inside the delta-connection.

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