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***Abstract*—Efficient energy conversion in low-voltage applications has gained more attention due to increasing energy costs and environmental issues. Accordingly, three-level converters have been discussed as an alternative to the standard two-level voltage-source converter because they offer an increased efficiency at higher switching frequencies. From a system perspective, the benefits of using three-level converters are not only limited to the converter itself, but there are additional positive impacts on the surrounding such as on the load machine losses or on the electromagnetic interference input filter volume. In this paper, a holistic comparison of advanced three-level topologies against the two-level topology is given. Simple analytical calculations and measurements show the benefits and the optimization potential concerning several aspects, such as the necessary semiconductor chip area, the harmonic losses in the load machine and in filter components, and the volume of passive components.**

***Index Terms*—Comparison, losses, three-level, volume.**

I. Introduction

INCREASED energy costs and environmental issues led to an emphasis on efficient converter topologies. Purchase costs are reconsidered, keeping the operating expenses in mind. One possible way to achieve a higher converter efficiency is to shift toward lower switching frequencies and increased material usage such as large conductor diameters or paralleling switching devices. A second main aspect besides efficiency is technical performance. Many applications require high switching frequencies to fulfill control performance requirements, to reduce acoustic noise, or to reduce the volume and weight of passive components in order to reach a high power density. However, the insulated gate bipolar transistor (IGBT)-based two-level converter (2LC) is still used for most applications in industry, although it suffers from excessive losses if the switching frequency is increased. Therefore, it is difficult to fulfill both the efficiency requirements and the technical performance requirements with the 2LC.

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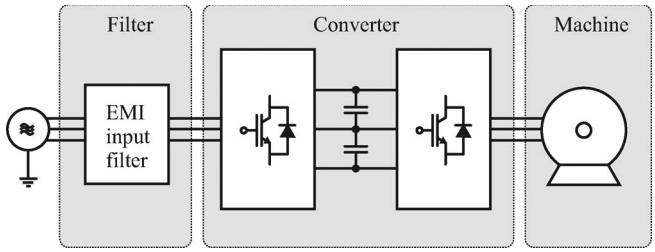

Fig. 1. Three-phase ac–dc–ac converter system including its surrounding consisting of a load machine and an input EMI filter.

Accordingly, three-level converters have been discussed for low-voltage applications [1], [2]. Despite the increased complexity and/or higher initial costs, the outstanding efficiency at higher switching frequencies due to the low switching losses makes three-level topologies attractive for certain applications.

From a system perspective, the benefits of using three-level converters are not only limited to the converter itself. The main parts of such a modern three-phase ac–dc–ac converter system are depicted in Fig. 1. On the grid side, usually, an electromagnetic interference (EMI) input filter is necessary to attenuate the current harmonics. There, the three-level output voltage waveform allows to reduce the necessary boost inductance and, consequently, the boost inductor volume and its losses. On the machine side, the harmonic losses in the machine are reduced considerably if a three-level voltage waveform is applied. Accordingly, there is less additional heating of the machine, and ideally, no derating of the machine is necessary. Further positive impacts are reduced machine isolation stress and reduced overvoltages due to long motor cables [3], which can be a problem in 2LC applications [4].

In this paper, the competitiveness of advanced three-level topologies for low-voltage applications is analyzed under several aspects. The optimization potential concerning the choice of topology, the volume and losses of passive components, the harmonic losses in the electrical load machine, and the necessary overall semiconductor chip area is highlighted. Consequently, a holistic comparison not limited to the power electronic converters themselves but including the impact on the surrounding is given. The considered power range is limited to $P_0 = 5$–50 kW as the used loss models and chip area models would change. Nevertheless, the basic findings are assumed to be similar for different system power levels.

The three considered topologies are presented in Section II. A short discussion on the implementation effort and the complexity is given. Among the 2LC and the three-level neutral

point clamped converter (3LNPC^2) [5], also the three-level T-type converter ($3\text{LT}^2\text{C}$) [5]–[10] is part of the comparison. Its characteristics ideally fit the requirements of many low-voltage applications. It is shown that, in contrast to a two-level topology, the losses in the three-level topologies distribute over many semiconductor dies and the increase of the junction temperatures is comparably small. The loss distribution profile among the semiconductor devices is strongly dependent on the operating point. It is therefore possible to adapt the semiconductor chip sizes and to design bridge-leg modules for mass production optimized for a certain application/operating range (e.g., power factor correction (PFC) rectifier modules or solar inverter modules).

In Section III, the necessary semiconductor chip area is calculated for each topology. The chip area is one of the main quantities determining the total semiconductor costs. For higher switching frequencies ($f_s > 14$ kHz), the total semiconductor chip area of a three-level topology can even be smaller than for the standard 2LC.

In Section IV, the benefits arising from the three-level output voltage concerning the harmonic losses in the electrical load machine are discussed and proved with measurements using a prototype of the $3\text{LT}^2\text{C}$ which is able to switch its output voltage waveform from two-level modulation to three-level modulation during operation.

Finally, the volume and the losses of passive components such as the dc-link capacitors and the EMI filter components are compared in Section V.

Due to the reduction of losses in filter components and the load machine, these additional benefits can even outperform the 2LC employing SiC Schottky diodes. It is shown that, in particular, the $3\text{LT}^2\text{C}$ is a competitive alternative to the 2LC if a high switching frequency and a high efficiency are required.

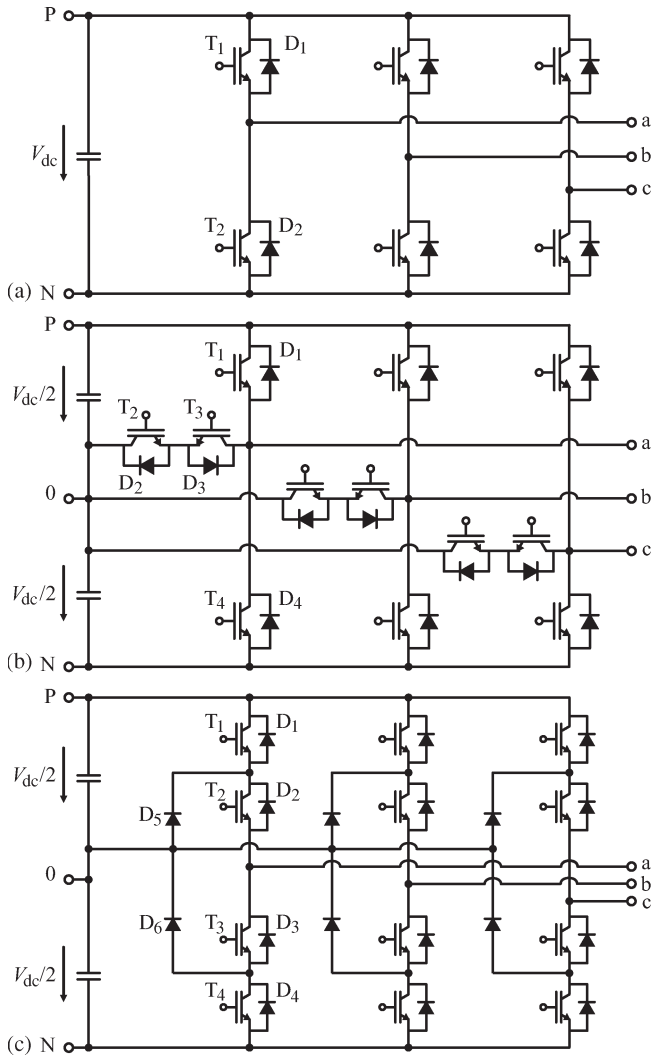

Fig. 2. Topologies of the (a) 2LC, (b) $3\text{LT}^2\text{C}$, and (c) 3LNPC^2.

II. Considered Topologies

The comparison given in this paper is limited to the three topologies depicted in Fig. 2, namely, the 2LC, the 3LNPC^2, and the $3\text{LT}^2\text{C}$. Although there exist alternatives, e.g., more complex three-level converter approaches such as the split-inductor converter [11], active clamped three-level topologies [12], or three-level matrix converters [13], the considered topologies are the most competitive for low-voltage applications. A further alternative to the presented topologies is the three-level flying capacitor converter 3LFC^2 [14]. As the space vector modulation with switching loss optimal phase clamping used for the other topologies is not directly applicable to the 3LFC^2, it is not considered in this comparison.

The 2LC [cf. Fig. 2(a)] has established itself as the standard industry solution for low-voltage applications. It is simple and inexpensive, although the efficiency suffers if the switching frequency is increased due the high switching losses. Alternatively, SiC diodes can be used in order to reduce the switching losses, although the costs increase considerably if similar pulse-current ratings as for Si diodes have to be achieved.

The 3LNPC^2 [cf. Fig. 2(c)] is widely used in medium-voltage applications such as traction inverters. There, the main benefits are reduced switching losses and the ability to split the necessary blocking voltage into two series-connected devices. This is no benefit in low-voltage applications because switches which could block the full dc-link voltage are available and the conduction losses increase for bipolar devices if two devices with half of the blocking voltage are connected in series compared to one device providing the full blocking voltage. The 3LNPC^2 suffers from an increased amount of semiconductors (six diodes and four IGBTs per bridge leg) and an increased amount of isolated gate drive voltage supplies (six additional ones compared to the 2LC). However, a clear benefit is the comparatively low switching losses. The switching frequency can be increased if necessary without losing much efficiency (cf. [15]).

The $3\text{LT}^2\text{C}$ [cf. Fig. 2(b)] is an extension of the 2LC with an active bidirectional switch to the dc-link midpoint. It can be built with switches having different voltage ratings. The upper and lower switches (T_1 and T_4) have to block the whole dc-link voltage, whereas the bidirectional switch to the midpoint has to block only half of the dc-link voltage. By using switches with lower voltage rating for the bidirectional switch, the conduction losses and the switching losses can both be reduced. Contrary to the 3LNPC^2, there are no series-connected devices that have

to block the whole dc-link voltage; therefore, the conduction losses can again be reduced. It makes the 3LT^{2}C especially efficient for medium switching frequencies (8–24 kHz) frequently used in industrial low-voltage applications.

The 3LT^{2}C uses only four diodes and four IGBTs per bridge leg. It can be built with only one additional isolated gate drive supply compared to the 2LC if the bidirectional switch to the midpoint is configured in common-collector configuration. The modulation complexity is equivalent to that of the 3LNPC^2, as the same modulation schemes can be used. It is not necessary to implement a current-dependent commutation sequence [1]. The 3LT^{2}C basically combines the positive aspects of the 2LC such as low conduction losses, small part count, and a simple operation principle with the advantages of the 3LNPC^2 such as low switching losses and superior output voltage quality.

Alternatively, the 3LT^{2}C can be implemented with series-connected IGBTs replacing the single switches T_1 and T_4 if it is used for medium-voltage applications as proposed in [16] and [17]. There, the topology is also known as neutral-point-piloted converter or transistor clamped converter.

The consumed gate drive power is slightly increased for the three-level topologies compared to the 2LC. As the considered switches obtain similar gate charges for comparable semiconductor chip areas and the net switching frequency is the same for all three topologies, the main difference in the total consumed gate drive power is due to the losses in the total number of gate drive circuits and isolated supplies.

The number of measurement circuits basically stays the same for all topologies. The only difference is due to the split dc link, as two voltage measurement circuits are required for the three-level topologies. The number of necessary pulsewidth-modulation (PWM) units doubles for both three-level topologies compared to the 2LC. Concerning the software effort, the complexity slightly increases for the three-level topologies as additional effort has to be put into subsector detection, dc-link balancing, and vector lookup tables.

A. *Efficiency Comparison and Semiconductor Utilization*

In a first step, the achievable efficiency of the three topologies for a power rating of $P_0 = 10$ kW, for a dc-link voltage of $V_{\mathrm{dc}} = 650$ V, and for using the same switches is calculated. The operating point is set to an output voltage amplitude of $\hat{V}_1 = 325$ V, a current amplitude of $\hat{I}_1 = 20.5$ A, and a current-to-voltage displacement angle of $\varphi_1 = 0^\circ$ or 180° depending on whether inverter or rectifier operation is considered. Although this comparison is not completely fair, it gives a first insight into the typical characteristics. A more balanced comparison is given in Section III where the chip sizes are adapted for each topology.

An algorithm described in [15] has been used to calculate the efficiency for all three topologies. The algorithm incorporates the space vector modulation and includes a switching loss optimal clamping scheme (discontinuous PWM; cf. [18] and [19]) for all three topologies. For the three-level converters, the adopted switching loss optimal clamping scheme can lead to a periodic voltage unbalance in the series-connected dc-link capacitors which can be compensated according to Pou *et al.* [20].

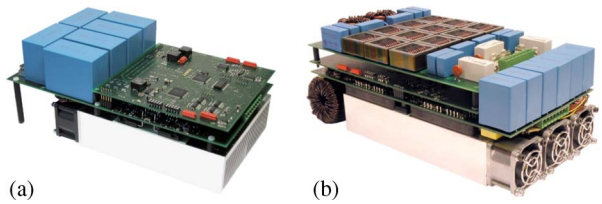

Fig. 3. (a) Prototype of the 99% efficient 3LT^{2}C. (b) Prototype of the 48-kHz switching frequency Si/SiC three-level neutral point clamped (NPC) back-to-back converter.

The compensation ensures that the output voltage is generated correctly, although the link is not exactly balanced.

The Infineon Trench and Field Stop 1200 V IGBT4 and the 600 V IGBT3 series have been chosen as reference devices because of their good documentation and data availability. For this initial comparison, the 2LC is assumed to be built with Infineon IKW40T120 1200-V 40-A IGBTs/diodes, and the 3LNPC^2 is built with Infineon IKW50N60T 600-V 50-A IGBTs/diodes. Unfortunately, no devices with equivalent current rating are available for the two voltage ratings. The 3LT^{2}C is assumed to mix the two switch types mentioned before, so both IKW40T120 and IKW50N60T are used.

It is important to take into consideration that the switching losses of the 3LT^{2}C are influenced by the combination of different switch types. The turn-on switching loss energy of the 1200-V IGBT will be lower if the commutating diode is only 600 V rated due to the considerably lower reverse recovery charge. In the same manner, the 600-V-device turn-on loss energy will be higher if the commutating diode is a 1200-V device. Switching transients have been recorded directly at the 3LT^{2}C prototype [cf. Fig. 3(a)] over a range of commutation voltages, currents, and temperatures. Passive 1:100 voltage probes (bandwidth of 400 MHz) and passive ac current transformers (bandwidth of 100 MHz) directly mounted to the pins of the implemented discrete TO-247 packages enabled a measurement of the loss energies with a minimum influence on the commutation inductance. A detailed description of the prototype and the achieved performance can be found in [21].

In Table I, the resulting switching loss energies and the deviation from the data-sheet values are summarized. It can be seen that the 1200-V-IGBT turn-on energy is 24% lower and the 600-V-IGBT turn-on energy is 94% higher than the data-sheet values (the data-sheet switching loss energies are linearly scaled to the operating parameters at hand, i.e., a commutation voltage of $V_{\mathrm{c}} = 325$ V, a current of $I_{\mathrm{out}} = 25$ A, and a junction temperature of $T_{\mathrm{j}} = 125$ °C for this comparison). In order to verify the conduction loss model, the forward voltage drops of each semiconductor have been determined experimentally for several currents and junction temperatures. The characteristics given in the data sheets are accurate and can be used instead.

A simple thermal model was included in the calculation in order to determine the mean junction temperatures and to adapt the loss models. Piecewise linear interpolation in between the experimental data points determined for several junction temperatures has been used in order to adapt the switching loss models as well as the conduction loss models with the temperature. The thermal model consists of a heat

TABLE I
MEASURED SWITCHING LOSS ENERGIES FOR $V_c = 325$ V, $I_{out} = 25$ A, AND $T_j = 125$ °C

Energy	Measurement	Datasheet	Difference
$E_{T1,on}$	1.20 mJ	1.58 mJ	−24 %
$E_{T1,off}$	1.59 mJ	1.68 mJ	−5 %
$E_{D1,off}$	1.13 mJ	1.12 mJ	+1 %
$E_{T3,on}$	1.26 mJ	0.65 mJ	+94 %
$E_{T3,off}$	0.72 mJ	0.68 mJ	+6 %
$E_{D3,off}$	0.34 mJ	0.41 mJ	−17 %

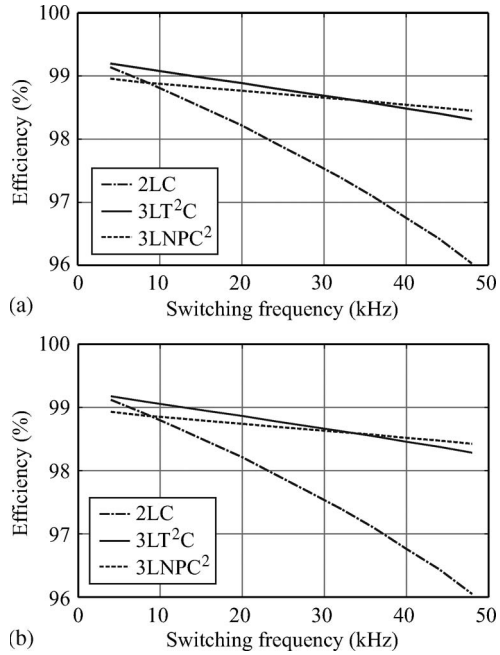

Fig. 4. Efficiency comparison between the different topologies for (a) inverter operation with $\hat{V}_1 = 325$ V, $\hat{I}_1 = 20.5$ A, and $\varphi_1 = 0°$ and (b) rectifier operation with $\varphi_1 = 180°$. Switch types: Infineon IKW40T120 and IKW50N60T.

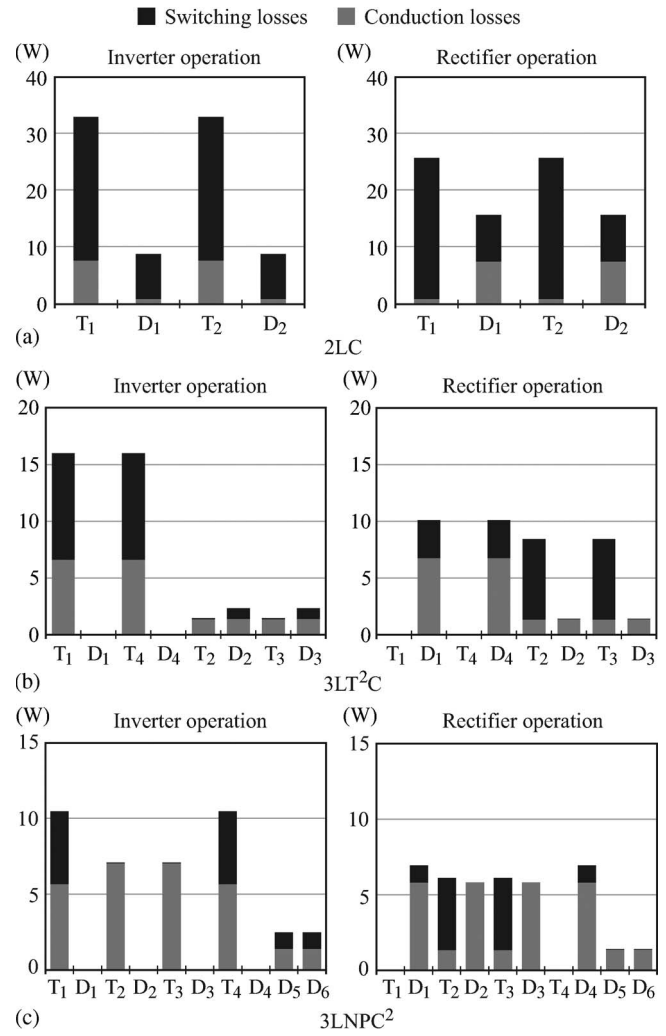

Fig. 5. Loss distribution over the individual semiconductors ($\hat{V}_1 = 325$ V, $\hat{I}_1 = 20.5$ A, $\varphi_1 = 0°$, 180°, and $f_s = 32$ kHz). (a) 2LC. (b) 3LT^{2}C. (c) 3LNPC^2.

sink with forced air cooling ($R_{sa} = 0.12$ K/W), an isolation foil ($R_{cs} = 0.51$ K/W) for each discrete device, and the thermal resistances of the semiconductors given in the data sheet ($R_{jc,T1} = 0.45$ K/W, $R_{jc,D1} = 0.81$ K/W, $R_{jc,T2} = 0.45$ K/W, and $R_{jc,D2} = 0.8$ K/W). The junction temperatures converge to their final value after a few iterations of the loss calculation algorithm.

The pure semiconductor efficiency is depicted in Fig. 4(a) for inverter operation. The achieved efficiencies for rectifier operation are depicted in Fig. 4(b) and are very similar.

The efficiency of the 3LT^{2}C is outstanding for medium switching frequencies from 6 to 30 kHz. For a switching frequency above 30 kHz, the 3LNPC^2 is superior. The main benefit of the 3LT^{2}C comes from the reduced switching losses because the commutation voltage of the 1200-V devices is only $V_{dc}/2$ as opposed to V_{dc} for the 2LC. Compared to the 3LNPC^2, the conduction losses are lower because there are no two devices in series in the current path in each phase.

Another interesting property of both three-level topologies is the stationary loss distribution profile over the individual semiconductor devices. The loss calculation algorithm provides the mean power losses in each semiconductor chip for each topology. The loss distribution of the 2LC is depicted in Fig. 5(a) for a switching frequency of $f_s = 32$ kHz. The difference between inverter operation and rectifier operation is not distinct; in both cases, the IGBT chip shows considerably higher losses than the diode. Therefore, discrete packages containing an IGBT and an antiparallel diode are often optimized such that the IGBT chip area is considerably larger than the diode chip area. Naturally, if the switching frequency is reduced, the loss distribution profile changes because the conduction losses become dominant, as is shown in Fig. 6(a) for a switching frequency of $f_s = 8$ kHz.

The loss distribution profile is completely different for the three-level topologies. There, the difference between the inverter and the rectifier operation is more pronounced. There are usually devices which generate almost no losses depending on the operating point. The loss distribution profile of the 3LT^{2}C is depicted in Fig. 5(b). For the inverter operation, nearly no losses occur in the diodes D_1 and D_4, and for the rectifier operation, the IGBTs T_1 and T_4 are almost not loaded.

The situation is similar with the 3LNPC^2 [cf. Fig. 5(c)]. Nearly no losses occur in T_1 and T_4 for the rectifier operation. On the contrary, for the inverter operation, the diodes D_1–D_4 show no losses, and the switching losses are concentrated in

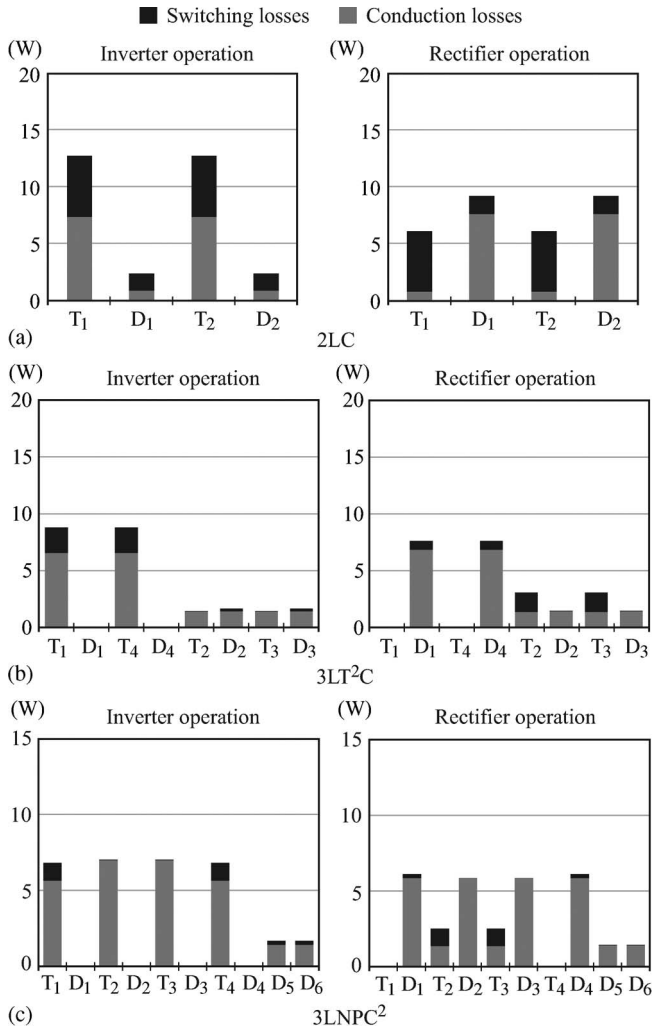

Fig. 6. Loss distribution over the individual semiconductor ($\hat{V}_1 = 325$ V, $\hat{I}_1 = 20.5$ A, $\varphi_1 = 0°$, $180°$, and $f_s = 8$ kHz). (a) 2LC. (b) 3LT^{2}C. (c) 3LNPC^2.

T_1 and T_4. This property was the main reason for the introduction of the active-neutral-point-clamped topology [12] where two additional IGBTs allow a more equal distribution of the losses among the semiconductors [22]. For a lower switching frequency, the characteristic distribution is similar; only the switching losses reduce [cf. Fig. 6(c)].

A different approach was suggested in [1]. Instead of producing general-purpose three-level bridge-leg modules, the distinct loss profile could be utilized to optimize bridge-leg modules specified for a certain application/operating point. Pure rectifier modules could be used in PFC applications, whereas pure inverter modules could be used for solar inverter applications. Naturally, this approach is only feasible for mass market applications. By implementing only a minimum chip size for devices which do not show any losses, the costs could be reduced.

A further possibility to profit from the loss distribution was shown in [15] where a prototype of a three-level NPC back-to-back converter with SiC Schottky diodes was presented [cf. Fig. 3(b)]. If an application requires extraordinary high switching frequencies in the range of 100 kHz, the switching losses of the 3LNPC^2 could be reduced by employing 600-V SiC Schottky diodes. Instead of replacing all six diodes of the NPC bridge leg, it is sufficient to replace D_5 and D_6 for the inverter operation or D_1 and D_4 for the rectifier operation in order to save costs. The inner diodes D_2 and D_3 should not be replaced with SiC Schottky diodes because they do not have any switching losses.

Similarly, for the 3LT^{2}C, the diodes D_1 and D_4 could be replaced with 1200-V SiC Schottky diodes if the topology is used for rectifier applications and a very high switching frequency is required. Replacing the 600-V diodes for the inverter application is not suggested as the switching losses are dominated by the 1200-V-IGBT turn-on losses which would not be reduced considerably anymore, as the normal 600-V diodes have already reduced the reverse recovery share of the turn-on losses (cf. Table I).

III. Semiconductor Chip Area Comparison

In the previous section, it was shown that the loss distribution over the individual semiconductor devices can be very uneven, depending on the operating point if three-level topologies are considered.

It is therefore advisable to reduce the chip sizes of the semiconductor chips with low power losses. Nowadays, the chip sizes in modules are overdimensioned because they are designed as general-purpose modules which could work in any operating point. It is neglected that, e.g., solar inverter or active rectifier modules always work with nearly constant modulation index and phase lag. The fundamental frequency is fixed to 50 or 60 Hz, so only the mean chip losses are important, and no peak power losses due to electrical standstill as, e.g., for variable speed drive inverter systems, could occur. If a big manufacturer for a mass product takes the decision for a converter topology, it should account for the possibility to produce a module optimized for this special application in order to reduce the semiconductor costs. Naturally, this makes only sense for fairly high product volume and if the converter failure modes are well defined. For many applications, pulse-current capability has to be guaranteed, or failure currents have to be conducted during a certain time period, which increases the necessary semiconductor area for all considered topologies.

The following chip area optimization has to be clearly understood as an optimization for the mentioned operating points; no reserves for fault cases are included.

The main idea is to adapt the chip sizes for each topology so that the junction temperature of each element reaches a mean value of $T_j = 125$ °C. Accordingly, the chip area for elements with low losses will be decreased, and the area of elements with high losses will be increased. In order to perform this chip size optimization, the conduction loss model, the switching loss model, and the thermal model have to be adapted with the semiconductor chip area A. A flowchart of the adaption algorithm is depicted in Fig. 7.

The chip area of each element is limited to a minimum of $A_{\min} = 4$ mm^2. This is due to unmodeled side effects becoming dominant for small chip sizes and due to the limits in the bonding technology.

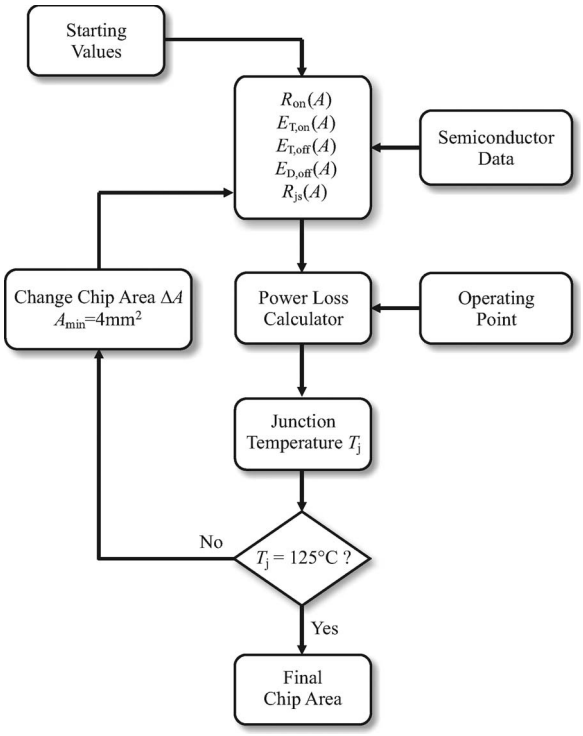

Fig. 7. Diagram of the chip area optimization algorithm.

A. Chip Area-Based Loss Modeling

The semiconductor loss models have to be adapted to account for a variable chip size. The approach has been presented in [23] for a semiconductor area-based comparison of an indirect matrix converter, a current source converter, and a two-level voltage source converter.

In a first step, the chip areas of several devices from the Infineon Trench and Field Stop 1200 V IGBT4 and the 600 V IGBT3 series were determined by opening the discrete devices. In a next step, the conduction characteristics specified in the data sheets are fitted to the determined chip area. The conduction characteristics can be approximated with a simple model consisting of a forward voltage drop V_{f} which is independent of the chip area and a differential resistance $R_{\mathrm{on}}(A)$ which is inversely proportional to the chip area A. Consequently, the conduction losses $P_{\mathrm{c,x}}$ of each device x can be modeled as follows:

$$P_{\mathrm{c,x}}(A,i) = V_{\mathrm{f,x}} \cdot i + k_{\mathrm{c,x}} \cdot \frac{1}{A} \cdot i^2. \tag{1}$$

The parameters $V_{\mathrm{f,x}}$ and $k_{\mathrm{c,x}}$ are given in Table II.

Similarly to the conduction losses, also the switching losses are adapted with the chip area. The data-sheet values with the proposed gate resistors are linearly scaled to the same switched current and the same commutation voltage. The switching loss energies E_{y} for the relevant switching transients y (IGBT turn-on, IGBT turnoff, and diode turnoff) of each device are approximated with simple linear models given by

$$E_{\mathrm{y}}(A,v,i) = (m_{\mathrm{y}} \cdot A + q_{\mathrm{y}}) \cdot v \cdot i. \tag{2}$$

TABLE II
PARAMETERS OF THE CHIP AREA-DEPENDENT LOSS MODELS

Conduction loss model		
Device x	$V_{\mathrm{f,x}}$	$k_{\mathrm{c,x}}$
$T_{1200\mathrm{V}}$	$0.8\,\mathrm{V}$	$1.29\,\Omega\mathrm{mm}^2$
$D_{1200\mathrm{V}}$	$0.8\,\mathrm{V}$	$0.55\,\Omega\mathrm{mm}^2$
$T_{600\mathrm{V}}$	$0.8\,\mathrm{V}$	$0.52\,\Omega\mathrm{mm}^2$
$D_{600\mathrm{V}}$	$0.8\,\mathrm{V}$	$0.24\,\Omega\mathrm{mm}^2$
Switching loss model		
Transient y	m_{y}	q_{y}
$T_{\mathrm{on,1200V}}$	$-0.562\,\mathrm{nJ/(VAmm^2)}$	$213\,\mathrm{nJ/(VA)}$
$T_{\mathrm{off,1200V}}$	$-0.519\,\mathrm{nJ/(VAmm^2)}$	$237\,\mathrm{nJ/(VA)}$
$D_{\mathrm{off,1200V}}$	$-1.93\,\mathrm{nJ/(VAmm^2)}$	$174\,\mathrm{nJ/(VA)}$
$T_{\mathrm{on,600V}}$	$0.895\,\mathrm{nJ/(VAmm^2)}$	$52.9\,\mathrm{nJ/(VA)}$
$T_{\mathrm{off,600V}}$	$0.566\,\mathrm{nJ/(VAmm^2)}$	$69.3\,\mathrm{nJ/(VA)}$
$D_{\mathrm{off,600V}}$	$0.022\,\mathrm{nJ/(VAmm^2)}$	$41.8\,\mathrm{nJ/(VA)}$
$T^*_{\mathrm{on,1200V}}$	$-0.562\,\mathrm{nJ/(VAmm^2)}$	$162\,\mathrm{nJ/(VA)}$
$T^*_{\mathrm{on,600V}}$	$0.895\,\mathrm{nJ/(VAmm^2)}$	$103\,\mathrm{nJ/(VA)}$

The parameters m_{y} and q_{y} are given in Table II. The constant part q_{y}, which is independent of the chip area A, is dominating for the considered chip sizes. In general, the switching loss energies scaled to the same current and the same commutation voltage do not vary much with the chip area A if IGBTs are considered because a large chip is usually switched faster using a smaller gate resistor.

For the T-type topology, the fitted switching loss energy curves have been simply shifted to the points determined with the test setup. As described in Section II-A, it is assumed that only the turn-on switching transients $T^*_{\mathrm{on,1200\ V}}$ and $T^*_{\mathrm{on,600\ V}}$ are influenced by the combination of different switch types in the $3\mathrm{LT}^2\mathrm{C}$.

Finally, the thermal model was adapted. The same thermal behavior for all chip types is assumed, and according to Friedli and Kolar [23], the thermal resistor is given by

$$R_{\mathrm{th,js}}(A) = 23.94 \frac{K}{\mathrm{Wmm}^2} \cdot A^{-0.88}. \tag{3}$$

The heat sink is assumed to be on a constant temperature of $T_{\mathrm{sink}} = 80\ ^\circ\mathrm{C}$. The junction temperature of each device can be calculated with (4)

$$T_{\mathrm{j}} = T_{\mathrm{sink}} + R_{\mathrm{th,js}}(A) \cdot P_{\mathrm{tot}}(A). \tag{4}$$

The thermal and the loss models are all linear and very simple. As the main goal of this chip area comparison is not to give precise predictions of the achievable efficiency but a relative comparison of the semiconductor effort of the considered converter topologies, the accuracy of the models is sufficient. The basic findings will not change significantly if more accurate models are used.

B. Chip Area Optimization Results

The optimization algorithm calculates the losses for each topology and adapts the chip sizes until each element reaches a junction temperature of $T_{\mathrm{j}} = 125\ ^\circ\mathrm{C}$. This process also affects the total losses and the converter efficiency. Interestingly, the efficiency decreases only slightly because the chip area is reduced only for elements with low losses, and therefore, the absolute loss increase is very small.

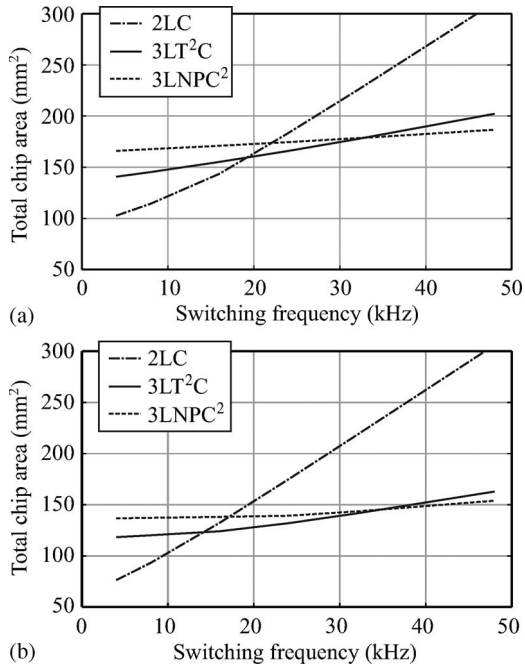

Fig. 8. Comparison of the total semiconductor area depending on the switching frequency. (a) Inverter operation with $\hat{V}_1 = 325$ V, $\hat{I}_1 = 20.5$ A, and $\varphi_1 = 0°$ and (b) rectifier operation with $\varphi_1 = 180°$.

If all chip sizes are summed up, the total chip area for a topology and the corresponding operating point are found. The total chip area is directly related to the costs of a power module.

The calculation results are depicted in Fig. 8. The total chip area is calculated for the three different topologies depending on the switching frequency.

Surprisingly, the total chip area of the 3LT^{2}C is lower than for the 2LC already for a switching frequency above 14 kHz in rectifier operation [cf. Fig. 8(b)]. The area increase with the switching frequency is the lowest for the 3LNPC^2 because of the small switching losses. At a switching frequency of 48 kHz, the necessary chip area for the 2LC is nearly twice the area of the 3LNPC^2. A similar dependence for the total chip area can be observed for the inverter operation [cf. Fig. 8(a)], although the chip area allocation to the different devices changes.

With Fig. 8, the general belief that a three-level topology would need more silicon chip area than a corresponding two-level topology is disproved. The part count and the count for external circuitry such as gate drives and isolated voltages is increased, but the total chip area can be even lower for high switching frequencies.

IV. Comparison of the Harmonic Machine Losses

In the previous sections, it was shown that the three-level topologies have some very advantageous properties such as a high efficiency at high switching frequencies and a low chip area requirement. There, the considerations have been limited to the converter itself. In this section, the comparison is extended to the surrounding of the converter, beginning with the load machine.

Harmonic machine losses due to the pulsed converter output voltage increase the machine losses considerably [24]. Not only the direct losses due to the harmonics but also the change in the operating point due to the additional heating is important and affects the efficiency negatively [25], [26].

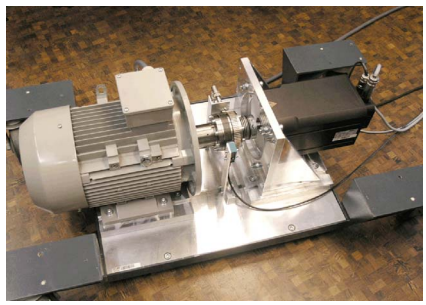

Fig. 9. Machine test bench with an induction machine and the PMSM load machine. Torque and speed are measured with a wireless torque transducer (Magtrol TF 210).

The harmonic machine losses depend on numerous manufacturing-specific machine parameters such as lamination thickness, winding type, and slotting and are difficult to calculate and to measure [27]. Depending on the switching frequency, the harmonic losses consist not only of ohmic losses but also of iron losses. For higher switching frequencies ($f_\mathrm{s} > 10$ kHz), the harmonic ohmic losses are negligible, and the harmonic iron losses are mainly due to eddy-current iron losses (cf. [28]–[30]). A promising approach to estimate the influence of different topologies and modulation schemes is the harmonic loss-factor curve [30]. This machine-specific curve can be determined experimentally with harmonic injection methods and allows to calculate the harmonic machine losses if the voltage spectrum of the applied stator voltage is known.

In this paper, a similar approach was chosen. The harmonic losses of a standard 7.5-kW induction machine (ecoDrives ACA 132 SB-2/HE) have been measured for several switching frequencies and for the two-level modulation and three-level modulation. The induction machine is mounted on a test bench and coupled to a permanent-magnet synchronous machine (PMSM) load machine (LST-158-4-30-560) as shown in Fig. 9. The parameters of the induction machine were determined using standard no-load and blocked-rotor tests and are summarized in Table III. In order to measure the harmonic losses, the precision power analyzer Yokogawa WT3000 was configured in such a way that it automatically subtracts the fundamental active power component from the total measured active power. The phase currents were measured with the internal 30-A resistive shunt inputs. The measurement window was set to 250 ms, and a linear averaging over 64 measurement values was performed. The harmonic power is concentrated at the switching frequency and is assumed to generate negligible mean torque [31]; therefore, only losses are generated at the switching frequency. The measurement accuracy of the harmonic losses is given with approximately $\pm 10\%$ for the two-level waveform and with approximately $\pm 40\%$ for the even smaller harmonic losses of the three-level waveform.

The prototype of the 3LT^{2}C was used to generate a three-level and a two-level output voltage. It is able to set the switching frequency in the range of $f_\mathrm{s} = 4$–24 kHz and to

TABLE III
PARAMETERS OF THE INDUCTION MACHINE

Parameter	Variable	Value
Nominal power	P_{n}	7.5 kW
Nominal efficiency	η_{n}	89.6 %
Nominal voltage	U_{n}	230 V
Nominal current	I_{n}	13.7 A
Nominal torque	T_{n}	24.7 Nm
Nominal speed	n_{n}	2900 rpm
Main inductance	L_{m}	169.6 mH
Stator stray inductance	$L_{\sigma\mathrm{s}}$	3 mH
Rotor stray inductance	$L_{\sigma\mathrm{r}}$	3 mH
Stator resistance	R_{s}	0.46 Ω
Rotor resistance	R_{r}	0.59 Ω
Core loss resistance	$R_{\mathrm{c,n}}$	830 Ω
Friction losses	$P_{\mathrm{fric,n}}$	285 W

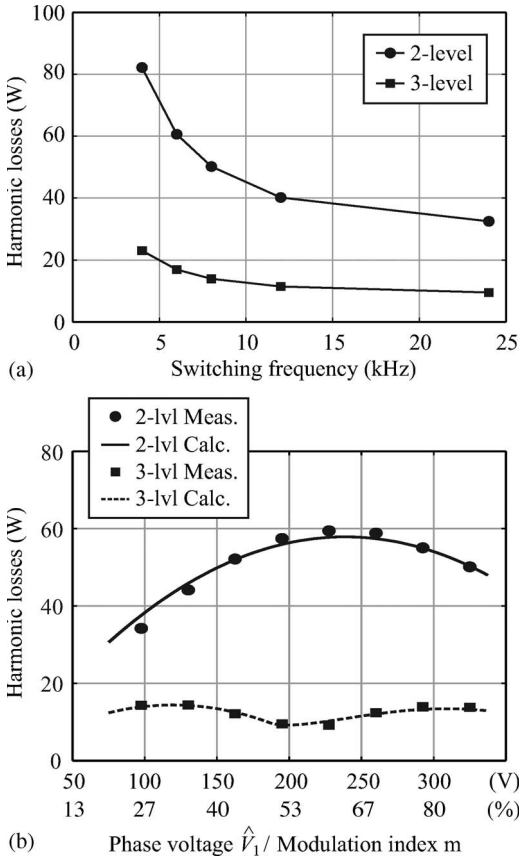

Fig. 10. (a) Measured harmonic machine losses as a function of the switching frequency ($\hat{V}_1 = 325$ V). (b) Measured and calculated harmonic machine losses as a function of the peak output voltage ($f_{\mathrm{s}} = 8$ kHz).

change from two-level modulation to three-level modulation and vice versa during operation.

The harmonic losses for several switching frequencies and for the two-level modulation and three-level modulation are depicted in Fig. 10(a). The measurements were taken under quasi-no-load conditions, and therefore, only friction and windage losses of the induction machine and the PMSM load machine were occurring. It can be seen that the harmonic losses decrease for higher switching frequencies but stagnate on a certain value.

The dependence of the harmonic machine losses on the modulation index m is shown in Fig. 10(b). Whereas there is a maximum at about $m = 0.6$ for the two-level inverter, there are two local maxima at $m = 0.3$ and $m = 0.8$ and a local minimum at $m = 0.55$ with the three-level inverter. According to Ruderman *et al.* [29], [32], this dependence can be approximated analytically under the assumption of dominant eddy-current iron losses. This condition is satisfied for high switching frequencies ($f_{\mathrm{s}} > 10$ kHz), and it is equivalent to having all switching frequency voltage harmonics in the approximately constant high-frequency range of the loss-factor curve (cf. [30]). If the harmonic ohmic losses and the hysteresis iron losses are neglected, the additional harmonic machine losses P_{harm} due to the PWM supply can be calculated with

$$P_{\mathrm{harm}} = k^*_{\mathrm{eddy}} \cdot \sum_{h>1} V_{\mathrm{h}}^2 = k^*_{\mathrm{eddy}} \cdot \left(V_{\mathrm{rms}}^2 - V_{(1),\mathrm{rms}}^2 \right) = k^*_{\mathrm{eddy}} \cdot \Delta V_{\mathrm{rms}}^2. \quad (5)$$

Here, V_{rms} denotes the rms value of the phase voltage, and $V_{(1),\mathrm{rms}}$ denotes the rms value of the fundamental frequency voltage component. The ripple voltage rms value ΔV_{rms} can be calculated analytically. A solution for the generic N-level inverter was presented in [29], assuming a high pulse number and a modulation scheme using the nearest three space vectors for the output voltage generation. This condition is satisfied by standard space vector modulation (SVM) and sinusoidal PWM schemes. For the two-level inverter, the squared ripple voltage rms value is given with

$$\Delta V_{\mathrm{rms,2lvl}}^2 = \frac{V_{\mathrm{dc}}^2}{3} \left(\frac{2}{\pi} m - \frac{1}{2} m^2 \right). \quad (6)$$

The modulation index is defined as $m = \hat{V}_1 \cdot \sqrt{3}/V_{\mathrm{dc}}$. For the three-level inverter, the squared ripple voltage rms value is given as

$$\Delta V_{\mathrm{rms,3lvl}}^2 = \begin{cases} \frac{V_{\mathrm{dc}}^2}{3} \cdot a & 0 \le m < \frac{1}{2} \\ \frac{V_{\mathrm{dc}}^2}{3} \cdot (a+b) & \frac{1}{2} \le m < 1 \end{cases}$$

$$a = \frac{1}{\pi} m - \frac{1}{2} m^2$$

$$b = -\frac{1}{2} + \frac{1}{\pi} \arcsin\left(\frac{1}{2m} \right) + \frac{2}{\pi} \sqrt{m^2 - \frac{1}{4}}. \quad (7)$$

The loss constant $k^*_{\mathrm{eddy}} = 2.03\ \mathrm{mW/V^2}$ was determined with the measured harmonic machine losses of the two-level inverter at $\hat{V}_1 = 325$ V and $f_{\mathrm{s}} = 8$ kHz. Although the condition of having only eddy-current losses is not completely satisfied at this switching frequency, the calculated harmonic losses over the modulation index using (6) and (7) and the previously determined loss constant match the measured losses accurately [cf. Fig. 10(b)].

The relative reduction of the harmonic machine losses when changing from a two-level to a three-level inverter supply is, in a first approximation, independent of the machine size, the power rating, the dc-link voltage, and the switching frequency as long as the assumption of dominant eddy-current iron losses holds. The ratio of the expected harmonic machine losses using a two-level and a three-level inverter supply over the modulation index is shown in Fig. 11. The ratio reaches a minimum of

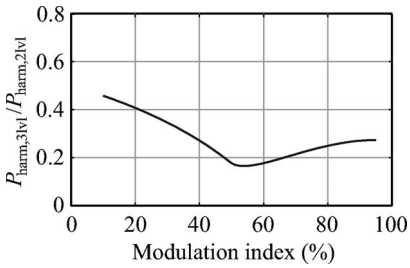

Fig. 11. Ratio of harmonic machine losses using a two-level and a three-level inverter supply.

16.5% at $m = 0.55$ and is approximately equal to 25% for a modulation index typical for nominal output voltage operation ($m = 0.7 \ldots 0.9$).

Boglietti *et al.* suggested a similar approach for machine iron loss prediction under PWM supply in [33]–[35]. They suggest to calculate the total machine iron losses with PWM supply as

$$P_{\mathrm{i}} = \eta^2 \cdot P_{\mathrm{hys,sin}} + \chi^2 \cdot P_{\mathrm{eddy,sin}}$$
$$\eta = \frac{|v|_{\mathrm{avg}}}{|v_{(1)}|_{\mathrm{avg}}} \approx 1, \quad \chi = \frac{V_{\mathrm{rms}}}{V_{(1),\mathrm{rms}}}. \tag{8}$$

$P_{\mathrm{hys,sin}}$ and $P_{\mathrm{eddy,sin}}$ are the hysteresis and eddy-current iron losses under sinusoidal supply, η is the ratio of the average rectified stator voltage $|v|_{\mathrm{avg}}$ to the average fundamental rectified stator voltage $|v_{(1)}|_{\mathrm{avg}}$, and χ is the ratio of the rms voltage to the fundamental rms voltage. For high pulse numbers, η is nearly equal to one. If the harmonic ohmic losses are neglected, the additional harmonic machine losses are given as

$$P_{\mathrm{harm}} \approx P_{\mathrm{i}} - P_{\mathrm{hys,sin}} - P_{\mathrm{eddy,sin}}$$
$$= (\chi^2 - 1) \cdot P_{\mathrm{eddy,sin}} = \left(\frac{V_{\mathrm{rms}}^2}{V_{(1),\mathrm{rms}}^2} - 1 \right) \cdot P_{\mathrm{eddy,sin}}$$
$$= \frac{\Delta V_{\mathrm{rms}}^2}{V_{(1),\mathrm{rms}}^2} \cdot P_{\mathrm{eddy,sin}}. \tag{9}$$

If the loss constant k_{eddy}^* is assumed to be independent of the frequency and flux density, (9) reduces to

$$P_{\mathrm{harm}} = \frac{\Delta V_{\mathrm{rms}}^2}{V_{(1),\mathrm{rms}}^2} \cdot k_{\mathrm{eddy}}^* \cdot V_{(1),\mathrm{rms}}^2 = k_{\mathrm{eddy}}^* \cdot \Delta V_{\mathrm{rms}}^2 \tag{10}$$

which is the same result as (5). Therefore, the two approaches give the same result if the mentioned assumptions such as high switching frequency, dominant eddy-current iron losses, and negligible harmonic hysteresis and harmonic ohmic losses are applied.

A. System Efficiency Optimization

The measurements revealed that the harmonic machine losses decrease with higher switching frequencies. On the contrary, the converter switching losses will increase. In order to find the optimal switching frequency, which results in minimum losses of the overall system, the harmonic machine losses, the converter switching losses, and their sum are depicted in Fig. 12(a) for the 2LC, in Fig. 12(b) for the 3LT^{2}C, and in Fig. 12(c) for the 3LNPC^2. The switching losses have been calculated for rated speed and torque using a fixed loss optimal clamping modulation scheme for a current lag of 30°. The harmonic machine losses have been measured at no-load condition. Although there are some variations of the harmonic machine losses under loaded conditions, they are small for high switching frequencies and are neglected (cf. [30]).

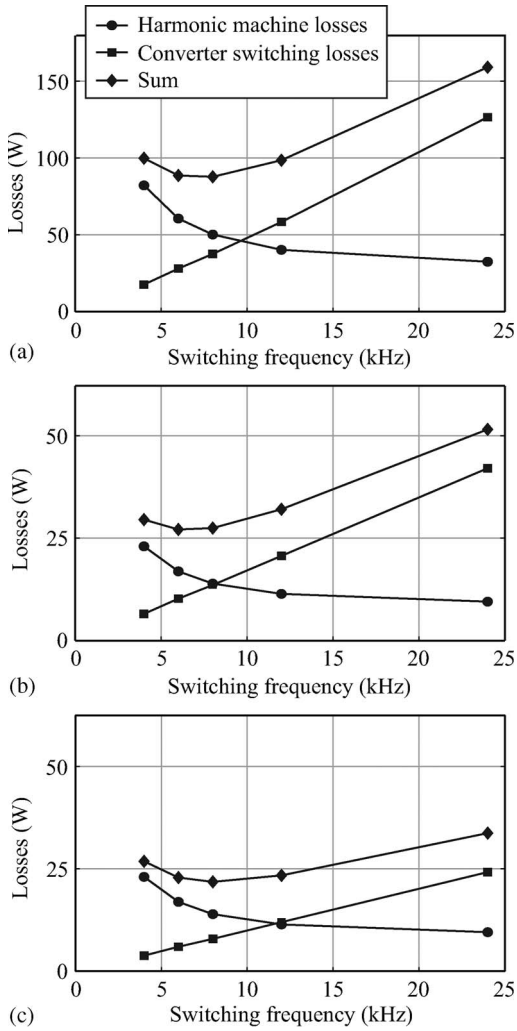

Fig. 12. Optimization of the switching frequency-dependent loss components with (a) the 2LC, (b) the 3LT^{2}C, and (c) the 3LNPC^2. The harmonic machine losses are measured during nearly no-load condition, and the switching losses are calculated for nominal operation.

The minimum of the total switching frequency-dependent losses is at $f_{\mathrm{s}} = 6$ kHz for the 3LT^{2}C, at $f_{\mathrm{s}} = 7$ kHz for the 2LC, and at $f_{\mathrm{s}} = 8$ kHz for the 3LNPC^2. The minimum occurs for all converters at a relatively low switching frequency. A higher switching frequency therefore does not reduce the total losses and should only be chosen if necessary for improving the dynamic performance, reducing the converter volume, or reducing the acoustic noise.

Although this approach allows no statements for the optimal switching frequency of an arbitrary machine and converter combination, the results will potentially be similar for comparable machines and power ratings.

If the overall system efficiency is considered, not only the harmonic losses are important. The major part is given by

the machine losses at the fundamental frequency that can be minimized using loss optimal control schemes. These control schemes have again an impact on the converter efficiency which was shown in [21], where an optimized variable speed drive using the $3LT^2C$ was presented.

V. Volume and Losses of Passive Components

The surrounding of an ac–ac converter includes also the grid side where, usually, an EMI filter is placed in order to comply with specific regulations. There, the boost inductance is most important as it filters the pulsed converter voltage. In between the input stage and the output stage, usually, a dc-link capacitor is placed. Besides the heat sink, the boost inductors and the dc-link capacitors mainly determine the total converter volume. It is therefore important to know how these elements are influenced by the chosen topology. In this section, simple estimations for the change of the dc-link capacitor volume and the boost inductor volume are given when changing from a two-level topology to a three-level topology.

A. DC-Link Capacitor

First, the dc-link capacitor is considered. There are numerous ways to determine the necessary dc-link capacitance. For applications with a load machine, often, a certain decoupling between the input and the output stage is desired, and a certain energy storage should be provided for ride-through operation. Another design criterion is the maximum allowed voltage overshoot if a sudden load drop occurs. In both cases, the relative change in capacitor volume if changing from a two-level topology to a three-level topology is the same. According to (11) and (12), the capacitance of the three-level topology $C_{3\mathrm{lvl}}$ is twice the capacitance of the two-level topology $C_{2\mathrm{lvl}}$ if the same energy has to be stored. Due to the series connection of $C_{3\mathrm{lvl}}$, the total installed capacitance increases by a factor of four

$$\frac{1}{2}\cdot C_{2\mathrm{lvl}}\cdot V_{\mathrm{dc}}^2 = 2\cdot\frac{1}{2}\cdot C_{3\mathrm{lvl}}\cdot\left(\frac{V_{\mathrm{dc}}}{2}\right)^2 \tag{11}$$

$$2\cdot C_{2\mathrm{lvl}} = C_{3\mathrm{lvl}}. \tag{12}$$

The voltage rating of the capacitors in the three-level topology has to be only $V_{\mathrm{dc}}/2$. Theoretically, the capacitor volume scales linearly with the capacitance and with the square of the rated voltage. However, these theoretical scaling factors do not fully apply here since, for the small capacitor values considered, manufacturing-specific effects become dominant. The volume per capacitance for different rated voltages (cf. Fig. 13) was determined using data-sheet values from the EPCOS MKP foil capacitor series (B32774, B32776). For a designed minimum capacitance of $C_{2\mathrm{lvl}} = 25\ \mu$F, the necessary total installed capacitance for the three-level topologies would increase to 100 μF. The total capacitor volume increases approximately by a factor of two.

B. Boost Inductor

A similar analysis can be done for the required boost inductance. Although there are several ways to determine the necessary value, most often, a maximum peak-to-peak current ripple $\Delta i_{\mathrm{pp,max}}$ relative to the current fundamental amplitude for rated power is specified. The location of the current ripple maximum is depending on the relation between the dc-link voltage and the phase voltage amplitude and also depends on the implemented modulation scheme. While it is simple to find the maximum current ripple for the two-level topology, it is more involving for the three-level topology, particularly if the space vector modulation with loss optimal clamping scheme is considered. The basic approach is described in the Appendix.

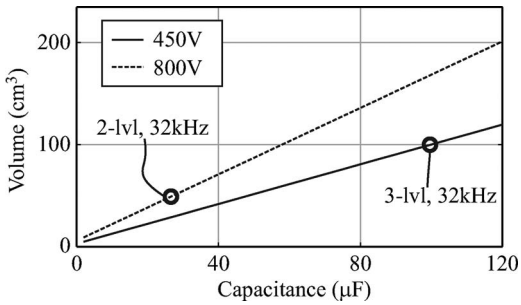

Fig. 13. Comparison of the volume of the total installed dc-link capacitance.

In order to simplify the comparison, the current ripple Δi_{pp} at the peak of the fundamental current is considered instead of the maximum current ripple $\Delta i_{\mathrm{pp,max}}$. This can be justified because the boost inductors are often designed near to the limit of saturation and already show a certain drop of the inductance (e.g., -20%) at the peak of the fundamental current. The inductor is then specified to have the required inductance at the peak current and often shows an increased inductance at a lower current.

For PFC operation and a sufficiently small boost inductance, the current space vector can be assumed to be approximately in phase with the converter output voltage space vector. Therefore, the current ripple at the peak of the fundamental current occurs at an electrical angle of the output voltage space vector of $\varphi_{\mathrm{V}} = 0^\circ$. The required inductances for a given Δi_{pp} can be calculated with (13) for a two-level topology and with (14) for a three-level topology, respectively,

$$L_{2\mathrm{lvl}} = \frac{1}{f_{\mathrm{s}}} d_{\mathrm{V1on,2lvl}} \frac{2/3V_{\mathrm{dc}} - \hat{V}_1}{\Delta i_{\mathrm{pp}}} \tag{13}$$

$$L_{3\mathrm{lvl}} = \frac{1}{f_{\mathrm{s}}} d_{\mathrm{VL1on,3lvl}} \frac{2/3V_{\mathrm{dc}} - \hat{V}_1}{\Delta i_{\mathrm{pp}}}. \tag{14}$$

The parameter $d_{\mathrm{V1on,2lvl}}$ specifies the relative on-time of the active voltage space vector V_1 [cf. Fig. 15(a)], whereas $d_{\mathrm{VL1on,3lvl}}$ specifies the relative on-time of the active voltage space vector V_{L1} [cf. Fig. 15(b)]. Due to the three-level modulation, $d_{\mathrm{VL1on,3lvl}}$ is smaller than $d_{\mathrm{V1on,2lvl}}$. If the same peak-to-peak current ripple is allowed for the two-level and the three-level topology, the reduction of the boost inductance can be calculated directly as

$$\frac{L_{3\mathrm{lvl}}}{L_{2\mathrm{lvl}}} = \frac{d_{\mathrm{VL1on,3lvl}}}{d_{\mathrm{V1on,2lvl}}} = \frac{2M\sin\left(\frac{\pi}{3}\right)-1}{M\cos\left(\frac{\pi}{6}\right)} = \frac{2}{3}\cdot\frac{3\hat{V}_1 - V_{\mathrm{dc}}}{\hat{V}_1}. \tag{15}$$

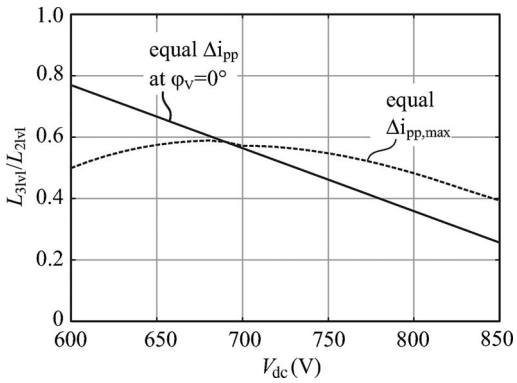

Fig. 14. Reduction of the required boost inductance when changing from a two-level topology to a three-level topology if an equal current ripple has to be achieved.

For $V_{\mathrm{dc}} = 650$ V and $\hat{V}_1 = 325$ V, the ratio is given with

$$\frac{L_{3\mathrm{lvl}}}{L_{2\mathrm{lvl}}} = 66\%. \tag{16}$$

The achievable reduction of the inductance is dependent on the dc-link voltage as depicted in Fig. 14. There, also the achievable reduction of the boost inductance for an equal maximum peak-to-peak current ripple $\Delta i_{\mathrm{pp,max}}$ is shown.

The inductor volume for a thermally limited design for a given core material theoretically scales linearly with the inductance [36] and with the square of the peak current. As the peak current does not change, the inductor volume can be reduced by the same amount

$$V_{\mathrm{L,3lvl}} = 0.66 \cdot V_{\mathrm{L,2lvl}}. \tag{17}$$

Usually, the volume of the three boost inductors is considerably larger than the volume of the dc-link capacitors, and therefore, the total volume of the passive components reduces for three-level converters compared to the two-level case. The remaining components of the EMI filter do not change considerably if the peak-to-peak current ripple in the boost inductor remains the same.

The losses of the passive components are dominated by the boost inductor losses, and the losses of the foil dc-link capacitors are negligible in comparison.

As described in [36], if a thermally limited inductor design is considered, the losses can increase proportionally to the inductor surface. As the inductance scales with the volume, the losses are related to the inductance by

$$P_{\mathrm{L}} \propto L^{2/3}. \tag{18}$$

Accordingly, the relative reduction of the inductor losses can be calculated with

$$\frac{P_{\mathrm{L,3lvl}}}{P_{\mathrm{L,2lvl}}} = \left(\frac{L_{3\mathrm{lvl}}}{L_{2\mathrm{lvl}}}\right)^{2/3} = 0.66^{2/3} = 0.76. \tag{19}$$

The losses in the boost inductors can be reduced approximately by 25% when changing from a two-level topology to a three-level topology. Again, the loss reduction is increased for a higher dc-link voltage, i.e., a loss reduction of 33% can be achieved for $V_{\mathrm{dc}} = 700$ V.

VI. Conclusion

In this paper, a holistic comparison between two-level and three-level three-phase converters for low-voltage applications was given. The achievable efficiency and the required total semiconductor chip area were calculated for three different topologies, namely, the 2LC, 3LT^{2}C, and 3LNPC^2. It was shown that an outstanding efficiency can be achieved especially with the 3LT^{2}C in the medium switching frequency range. The losses of the three-level topologies increase only slightly with the switching frequency and are distributed over several devices. Therefore, the chip area can be reduced and is, in total, even lower than for the 2LC for high switching frequencies (e.g., for $f_{\mathrm{s}} > 16$ kHz in the rectifier operation). The optimization potential for three-level bridge-leg modules concerning the loss distribution over the different devices was highlighted. It is possible to design a three-level module for the pure inverter or pure rectifier operation in order to reduce semiconductor costs.

In a second step, the comparison was extended to the surrounding of the converter. The impact of the three-level modulated output voltage on the harmonic losses of an induction machine was experimentally investigated. It was shown that these harmonic losses reduce by a factor of four, leading to considerably less heating and degradation of the machine.

Finally, the volume of the passive components such as the dc-link capacitors and the boost inductors was compared, and a simple estimation of the achievable loss reduction in the boost inductors when changing from a two-level to a three-level topology was given.

In summary, from a system perspective, the benefits of using three-level converters are not only limited to the converter itself, but there are additional positive impacts on the surrounding. If all these aspects are considered, three-level converters can be competitive alternatives to the standard 2LC even for low-voltage applications.

Appendix

The current ripple in the boost inductors can be derived by considering the applied voltages over the boost inductance as depicted in Fig. 15. If the space vectors are split into their fundamental and harmonic components, the equation for the current is given with

$$L \cdot \frac{d}{dt}\left(\underline{i}_{1,(1)} + \underline{i}_{1,(\mathrm{n})}\right) = \underline{V}_{1,(1)} + \underline{V}_{1,(\mathrm{n})} - \underline{V}_{\mathrm{g},(1)}. \tag{20}$$

Here, $\underline{V}_{\mathrm{g},(1)}$ denotes the grid voltage space vector, $\underline{V}_{1,(1)}$ and $\underline{V}_{1,(\mathrm{n})}$ are the fundamental and the harmonic component of the converter output voltage, respectively, and $\underline{i}_{1,(1)}$ and $\underline{i}_{1,(\mathrm{n})}$ are the fundamental and the harmonic component of the current space vector, respectively. The current ripple is defined by the harmonic component according to

$$L \cdot \frac{d}{dt}\underline{i}_{1,(\mathrm{n})} = \underline{V}_{1,(\mathrm{n})} = \underline{V}_1 - \underline{V}_{1,(1)}. \tag{21}$$

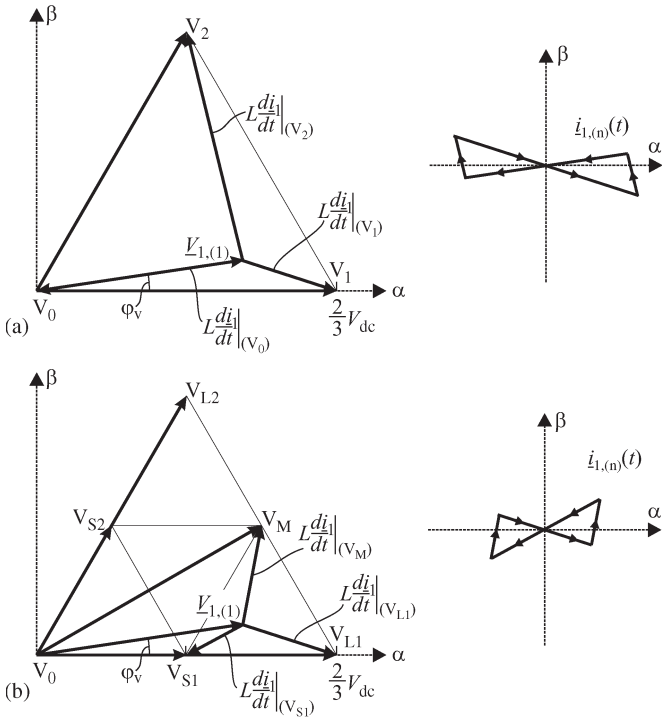

Fig. 15. Space vector diagrams for (a) two-level modulation and (b) three-level modulation. The diagram of the current ripple $\underline{i}_{1,(n)}(t)$ can be constructed by considering the applied voltages over the boost inductance.

It can be seen that the current ripple is driven by the difference between the applied discrete converter output voltage space vectors and the fundamental component. During a modulation cycle, the three closest voltage space vectors are used to generate the required fundamental component of the converter output voltage space vector. Considering the position of $\underline{V}_{1,(1)}$ depicted in Fig. 15, the space vector sequence

$$V_1 - V_2 - V_0 - V_2 - V_1 \tag{22}$$

is applied for two-level modulation, and the space vector sequence

$$V_{\mathrm{L1}} - V_{\mathrm{M}} - V_{\mathrm{S1}} - V_{\mathrm{M}} - V_{\mathrm{L1}} \tag{23}$$

is applied for three-level modulation. The current ripple diagram of $\underline{i}_{1,(n)}(t)$ can therefore be constructed with the turn-on times of the corresponding voltage space vectors.

Now, the current ripple in a phase-oriented design can be found by the projection of the current ripple diagram on the three single phases (a,b,c) using the following equations:

$$i_{1,(n),a}(t) = i_{1,(n),\alpha}(t) \tag{24}$$

$$i_{1,(n),b}(t) = -\frac{1}{2} i_{1,(n),\alpha}(t) + \frac{\sqrt{3}}{2} i_{1,(n),\beta}(t) \tag{25}$$

$$i_{1,(n),c}(t) = -\frac{1}{2} i_{1,(n),\alpha}(t) - \frac{\sqrt{3}}{2} i_{1,(n),\beta}(t). \tag{26}$$

The maximum of the current ripple $\Delta i_{\mathrm{pp,max}}$ is found by sweeping the electrical angle of the output voltage space vector φ_{V} over 0°–60° and taking the maximum ripple of the three phases. As the system is completely symmetrical, it is sufficient to consider only the first 60°.

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