Optimal Design of a 5kW/dm^3 / 98.3% Efficient TCM Resonant Transition Single-Phase PFC Rectifier

J. Biela, D. Hassler, J. Miniböck and J.W. Kolar
ETH Zurich, Power Electronic Systems Laboratory
Email: biela@lem.ee.ethz.ch; www.pes.ee.ethz.ch

***Abstract*—In many applications single-phase PFC rectifiers should meet the demand for a high efficiency and a high power density at the same time. Depending on the weighting of these two design criteria, different topologies could be advantageous. As has been shown, with bridgeless PFC rectifiers an ultra high efficiency of 99.3% or a high power density of 5.6kW/dm^3 could be realised. However, due to the hard switching operation it is not possible to achieve an exceptional efficiency and power density at the same time. Furthermore, SiC Schottky diodes are required for highly compact or highly efficient systems. Therefore, a triangular current mode (TCM), resonant-transition single phase PFC rectifier concept is presented in this paper, which overcomes both limitations. Besides a design procedure for optimising the chip area, also a simple and robust control concept, where a novel zero crossing detection concept is included, is explained and a prototype system as well as measurement results are presented for validating the concept and the design procedure.**

I. Introduction

Over the last decades, the development of converter systems was mainly targeting higher power densities ρ and lower costs [1]–[5]. A power loss reduction and/or increase of the efficiency η was only indirectly required, as the surface area available for loss dissipation decreases with decreasing converter volume. However, due to environmental concerns, high efficiency became more and more important, so that today at least two design requirements, i.e. high power density and high efficiency, have to be met. Accordingly, a multi-objective design optimisation has to be performed, where the best possible compromise must be found between the two conflicting criteria, since a higher efficiency usually leads to a lower power density.

In the design process, a large number of parameters must be determined and constraints in different physical domains, as e.g. magnetic or thermal properties, and EMI issues must be considered. This is complicated by the fact that many of the design parameters take influence not only on a single design aspect but on different converter properties as given e.g. for the switching frequency, which influences the losses in the semiconductors, the cooling system, the design of the magnetics, etc. Accordingly, the set of parameter values which results in an optimal design is difficult to identify.

Based on multi-domain converter models [3], [8]–[10], an optimal mapping of the design parameters into the system Performance Space could be performed as described in [11]. There, different design criteria or quality indices could be considered and/or the best compromise of the required system level performances could be determined. Such an optimisation has been performed for single-phase bridgeless PFC rectifiers in [7], [11], where it was demonstrated that an exceptional efficiency or a very high power density is possible based on bridgeless PFC rectifiers. However, it is not possible to reach ultra high efficiency and ultra high power density at the same time.

This could be proven by calculating the limiting curve of the bridgeless PFC rectifier concept in the ρ-η-plane as described in [12]. The limiting lines are generally called Pareto-Front [13] and they reveal in the considered case the compromise between efficiency and power density. In [12] (cf. Fig. 13 in section IV) the Pareto-Fronts for conventional and for bridgeless PFC rectifiers are derived and validated by

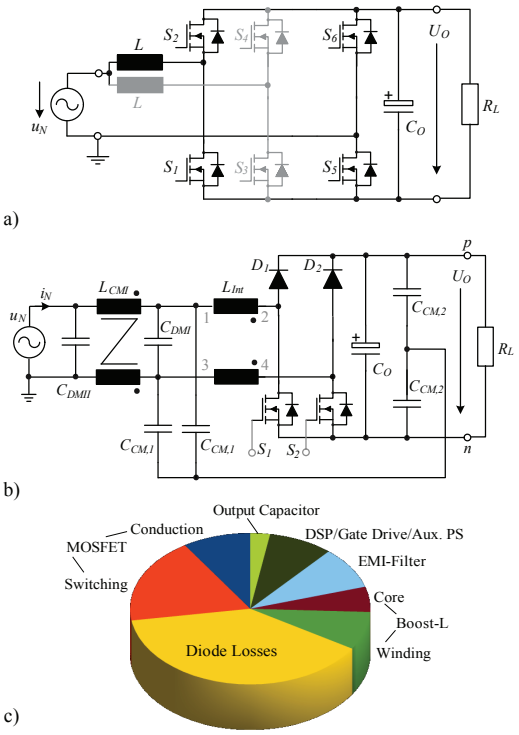

Fig. 1: a) Schematic of the Triangular-Current-Mode (TCM) resonant-transition PFC rectifier [6], which enables ultra high efficiency and high compactness at the same time. Switches S_1-S_4 shape the input current, so that it shows a sinusoidal local average value in phase with the mains voltage. There, more than two legs can be interleaved in order to reduce the input ripple current. Switches S_5 and S_6 are the common return path for the current shaping leg(s). These two switches only change their state at the zero crossings of u_N; switch S_5 is constantly turned on when $u_N > 0$ and S_6 when $u_N < 0$.
b) Schematic of a bridgeless PFC rectifier suitable for ultra compact or ultra efficient realisations. c) Loss distribution in the optimised 99.3% efficient 3.2kW bridgeless PFC rectifier with the schematics given in b). In order to reduce the switching losses, the ultra efficient PFC rectifier operates at a switching frequency of only 16kHz. Further details are given in [7].

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prototype systems.

These Pareto-Fronts in the ρ-η-Performance-Map clearly show the performances limits of the different topologies and it could be seen that a high power density of e.g. 5kW/dm^3 and a high efficiency of e.g. >98% could not be realised with the bridgeless/conventional PFC rectifier topologies at the same time. This fundamental limitation is due to the switching losses in the MOSFETs and the conduction losses of the freewheeling diodes, what could be seen for example in Fig. 1c), where the loss distribution of the ultra efficient bridgeless PFC rectifier is shown.

The switching losses in the MOSFETs are caused by the parasitic capacitances of the MOSFETs and the boost diodes which must be discharged/charged each time the MOSFETs turns on. This additionally prevents replacing the freewheeling diodes with synchronous rectifiers, since a MOSFET employed instead of a diode would exhibit a relatively large nonlinear capacitance, which would cause large turn-on current peaks resulting in higher switching losses and even in higher total losses. In order to achieve a ultra high efficiency of 99.3%, the switching frequency has to be limited to values below 20kHz for the bridgeless PFC rectifier. This, however, results in large inductors and consequently in a low power density. Furthermore, SiC Schottky diodes are required to avoid reverse recovery losses, which would significantly deteriorate the system efficiency.

In order to avoid the capacitive switching losses and the need for SiC diodes due to hard switching, a Triangular-Current-Mode (TCM) resonant-transition PFC rectifier as shown in Fig. 1a) has been proposed in [6], [14]. There, the resonance between an inductor and the MOSFET output capacitors is used to achieve zero voltage switching (ZVS) condition for the switches as will be explained in detail in **section** II. A similar principle has been applied for example in [15]–[20] for inverter drives and in [21] for a buck converter.

In **section** II furthermore a calculation procedure for determining the switching times, the component currents and the losses is presented. Based on this procedure the optimal chip area for minimal converter losses is derived. In **section** III the implementation of a timing based control in a CPLD/DSP is explained and a simple, low loss and fast concept for detecting the zero crossings of the inductor current, which is required for the control concept, is proposed. Finally, in **section** IV a prototype system and measurement results are presented.

II. Modelling of TCM resonant-transition PFC rectifier

As stated already in the introduction, a fundamental limitation of the hard switched PFC rectifier concepts is the fact that the output capacitance of the MOSFETs and the boost diodes are causing losses at the MOSFET's turn on and prevents replacing the freewheeling diodes with synchronous rectifiers.

A. Basic Operation

In order to avoid the capacitive losses occurring for hard switching, a TCM resonant-transition PFC with a switching scheme according to Fig. 2 could be used. At the top of this figure an equivalent circuit of the converter given in Fig. 1a) with only a single half bridge leg (e.g. MOSFETs S_1 and S_2 in Fig. 1a) for shaping the input current is shown. This equivalent circuit is valid for the positive mains cycle, where switch S_5 is constantly turned on and not shown in Fig. 2.

In Fig. 2b) the control signals, the voltage across MOSFET S_1, and the inductor current i_L are shown for one switching period T_P. The turn-off current I_S of switch S_1 is always chosen so, that the energy stored in inductor L is large enough to increase voltage u_{C1} up to U_O in order to enable ZVS turn on of switch S_2 after the resonant transition time T_{RT1}. With S_2 turned on, the energy stored in L is transferred to the output capacitor and S_2 acts as synchronous rectifier.

Due to capacitors C_{P1} and especially C_{P2}, which shows a large capacitance for $u_{C1} \approx U_O$, current i_L in L reverses after the time interval T_{off}, so that again energy is stored in L for a resonant-transition of u_{C1} down to zero. Assuming, that

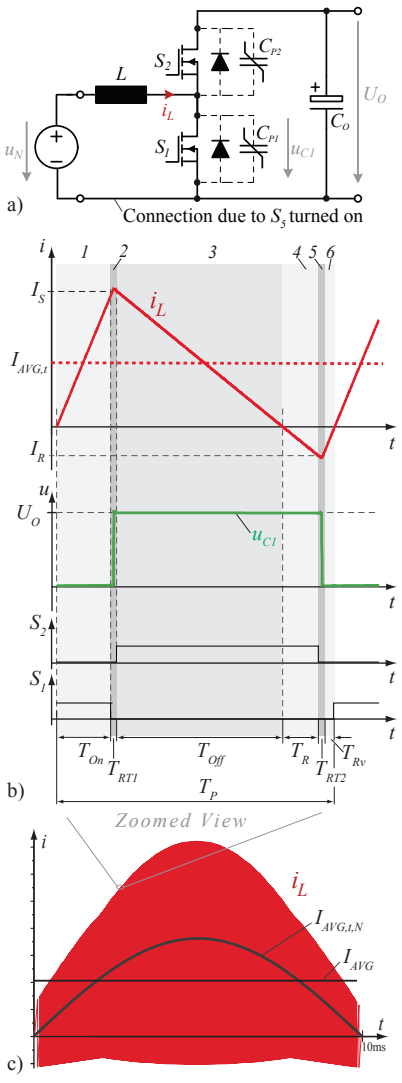

Fig. 2: a) Simplified schematic of a bridge leg of the TCM resonant-transition PFC rectifier (e.g. S_1 and S_2 in Fig. 1a) for positive mains voltage u_N. In the schematic also the nonlinear parasitic output capacitors $C_{P\nu}$ of the MOSFETs are shown. b) Waveforms of the inductor current i_L and of the voltage u_{C1} across the lower MOSFET. In c) the waveform of the inductor current i_L and the average current I_{AVG} for half a mains cycle is shown. There, the negative current could be seen, which is required for the resonant-transition of u_{C1} from U_O to 0. The waveform of i_L in b) is a zoomed view of c).

the mains voltage u_N is smaller than $U_O/2$ and neglecting losses, switch S_2 can be turned off at the zero crossing of i_L (i.e. T_R=0 in Fig. 2b) and due to the resonance of L and $C_{P1}||C_{P2}$ voltage u_{C1} reaches zero. Shortly thereafter switch S_1 is turned on at zero voltage and the new cycle starts.

In case $u_N > U_O/2$, the resonance of L and $C_{P1}||C_{P2}$ is not enough to bring u_{C1} down to zero. Therefore, switch S_2 is kept turned on for time T_R after T_{off} when i_L reverses, so that finally the negative amplitude of i_L is increased as shown in Fig. 2. Time T_R is chosen so, that enough energy is stored in L for decreasing u_{C1} down to zero. As soon as i_L is equal to I_R or after time T_R, switch S_2 is turned off and u_{C1} resonates down to zero and S_1 is turn on at ZVS condition.

With this control scheme, the boost diodes can be replaced with synchronous rectifier MOSFETs without causing additional capacitive switching losses. This allows a significant reduction of the conduction losses in the semiconductors. However, the RMS currents in the boost inductor and in switches S_1/S_2 are larger than for the conventional PFC rectifier, as for $u_N > U_O/2$ an additional negative current I_R for achieving ZVS must be generated. With an increased I_R also I_S must be increased in order not to change $I_{AVG,t}$, which is the average current during a switching period. This $I_{AVG,t}$ should show a sinusoidal time behaviour equal to $I_{AVG,t,N}$ (cf. (7)) as shown in Fig. 2c) and/or its average over half a mains cycle should be equal to the average mains current I_{AVG} required for the desired output power.

The larger RMS current could be compensated by increasing the chip area of S_1/S_2 and/or by reducing the R_{DSon} and consequently the conduction losses. However, for a larger chip area again the RMS current values must be increased as the parasitic capacitances C_{P1} and C_{P2} have a larger value. Furthermore, the gate drive losses increase as the gate charge increases with the chip area. Thus, there is an optimal value for the chip area resulting in minimal overall losses as will be shown below.

The MOSFETs S_1-S_4 connected to an inductor in Fig. 1a) are operating at a high switching frequency and due to the resonant-transition with ZVS conditions. With these MOSFETs the input current is shaped. The return path for the inductor currents is provided by MOSFETs S_5 and S_6, which change their switching state at each zero crossing of the mains voltage, i.e. at very low frequency. This common return path used for all fast switching legs simplifies the control and reduces the circuit complexity.

Due the return path operating at low frequency, the output of the rectifier is always connected to the mains. Consequently, the potential of the output voltage with respect to ground varies only twice during one mains cycle, so that the generated CM current is relatively small. By interleaving several stages also the DM input ripple could be decreased significantly, so that only a small EMI filter is necessary. Further details about the synchronisation of interleaved bridge legs can be found in [22].

B. Calculation of the Inductor Current

For designing the rectifier and choosing the optimal chip area, the currents in the components, the amplitudes I_S and I_R as well as the timing must be known. These are calculated by a numerical procedure based on the equations for the time intervals $1 \ldots 6$ shown in Fig. 2, which are explained in the following.

Interval 1 – T_{On}: During T_{On} switch S_1 is closed and the inductor current increases linearly, i.e. current I_S could be calculated by

$$I_S = \frac{u_N}{LT_{On}}. \tag{1}$$

There, the mains voltage could be assumed to be constant, as the switching period is much shorter than the mains cycle.

Interval 2 – T_{RT1}: After time T_{On}, switch S_1 is turned off and the resonant-transition begins. This could be described by the nonlinear differential equation

$$L\frac{\mathrm{d}^2 q_C(t)}{\mathrm{d}t^2} + u_{C1}\left(q_C(t), t\right) = u_N, \tag{2}$$

where $q_C(t)$ is the sum of the charge stored in C_{P1} and C_{P2}. In (2) voltage u_{C1} is described as function of q_C, which can be derived based on data sheet information of the output capacitances of the applied MOSFETs. The differential equation is numerically solved with a Implicit Rosenbrock Runge-Kutta method with degree three interpolant and the time, where $u_{C1} = U_O$ is fulfilled, is iteratively determined. There, it is also checked whether ZVS condition is achieved and the inductor current $I_{S,RT1}$ at the end of T_{RT1} is determined.

Interval 3 – T_{Off}: With $u_{C1} = U_O$ switch S_2 could be turned on at ZVS condition and the energy stored in L is transferred to the output capacitor. The duration of T_{Off} is given by

$$T_{Off} = \frac{I_{S,RT1}}{(U_O - u_N(t))L} \tag{3}$$

and at the end of interval T_{Off} the mains current is zero, $i_L(t) = 0$.

Interval 4 – T_R: Assuming $u_N \geq U_O/2$, switch S_2 is kept turned on after the zero crossing of i_L and the current continues to decrease linearly, so that I_R is given by

$$I_R = \frac{U_O - u_N}{LT_R}. \tag{4}$$

For $u_N < U_O/2$ this interval is skipped, i.e. T_R=0.

Interval 5 – T_{RT2}: After T_R or after the zero crossing of i_L in case $u_N < U_O/2$, switch S_2 is turned off and a second resonant-transition starts, that brings u_{C1} down to 0. The calculation is performed analogously to interval T_{RT1}, but the nonlinear differential equation is

$$L\frac{\mathrm{d}^2 q_C(t)}{\mathrm{d}t^2} + u_{C1}\left(q_C(t), t\right) = U_O - u_N. \tag{5}$$

At the end of T_{RT2} switch S_1 is turned on at ZVS condition.

Interval 6 – T_{Rv}: Finally, the current in L linearly increases from $I_{S,RT2}$ at the end of T_{RT2} down to zero. There, time T_{Rv} is

$$T_{Rv} = \frac{I_{S,RT2}}{u_N(t)L}. \tag{6}$$

After time T_{Rv}, the next cycle starts with slightly modified mains voltage and required $I_{AVG,t}$.

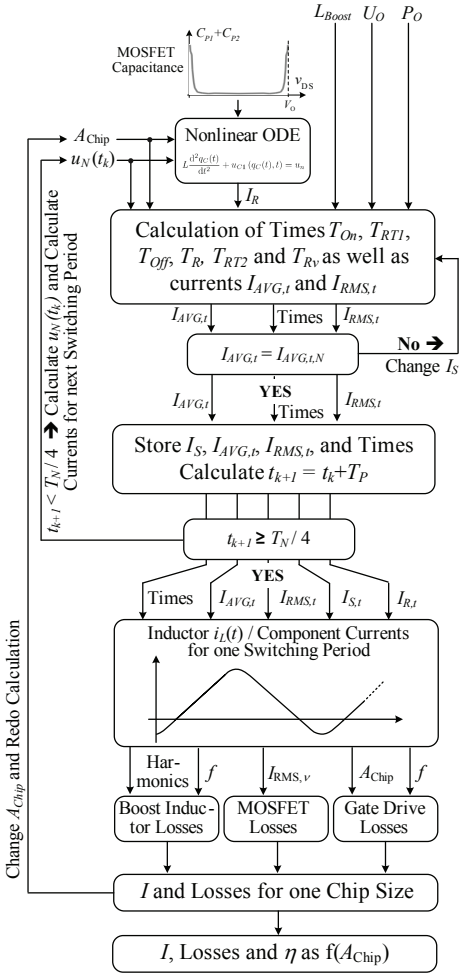

Fig. 3: Calculation procedure for the component currents and losses based on the equations presented in section II-B.

C. Calculation Procedure

With the equations presented in the previous section, the time behaviour of the mains/inductor current for each switching period can be calculated. This is dependent on the chip area A_{Chip} of the MOSFETs as the output capacitances C_{P1} and C_{P2} linearly depend on the chip area. In order to calculate the optimal chip area, first the component currents must be determined as function of A_{Chip}.

This is performed by the procedure shown in Fig. 3. The starting point is the value of the mains voltage $u_N(t)$ for the considered switching period. Based on this and the considered chip area, the required negative current I_R for achieving ZVS conditions is calculated with the nonlinear ODE (2) and the MOSFET capacitance as function of the voltage.

Next, the average $I_{AVG,t}$ and the RMS $I_{RMS,t}$ current as well as the length of the time intervals T_{On}, T_{RT1}, T_{Off}, T_R, T_{RT2} and T_{Rv} for the considered switching period must be calculated. There, current I_S respectively the on-time T_{On} is adjusted, so that the average current $I_{AVG,t}$ for the considered switching period is equal to the required mains average current

$$I_{AVG,t,N} = \frac{P_O}{U_{N,RMS}} u_N(t_k), \tag{7}$$

where t_k defines the position of the considered switching period within the mains period. This is performed with an iterative algorithm that starts with the value for I_S of the last switching period and increases the value until the condition is met. In the first switching period, i.e. at the beginning of the mains cycle $I_S = 0$ is chosen as starting value.

As soon as the condition $I_{AVG,t} = I_{AVG,t,N}$ is met, the values for the current switching period are stored and t_k as well as $u_N(t_k)$ are adjusted for the next switching period and the described procedure starts again. This is repeated until all the values are calculated for a quarter of a mains period. Based on these values the values for the remaining mains cycle are determined. There, it is assumed, that the switching periods are symmetric around $T_N/4$, what is approximately true in case the switching frequency is much higher than the mains frequency.

With the currents and times, the time behaviour of the mains/inductor current and the component currents are determined. Furthermore, the MOSFET conduction as well as the gate drive losses and the harmonics of the inductor current, which are required for calculating the HF winding and the core losses of the inductor, are calculated.

These calculations are performed for different chip areas, so that finally the losses are given as function of A_{Chip}.

D. Optimal Chip Area

In Fig. 4 the resulting losses for the TCM resonant-transition PFC rectifier with the specifications shown in Table II are given as function of the chip area for full output power and for 20% of the nominal load. There, also the gate drive losses are considered, since these also depend on the chip area and have a significant influence on the optimal chip area in the TCM PFC rectifier. For the inductor losses a magnetic core E42 made of ferrite material N87 and a litz wire with 420 strands each with a diameter of 0.071mm has been considered. The core losses are calculated with the approach presented in [23] and for the winding losses also the skin and the proximity effect losses are included.

Additionally, the constant losses for the controller/auxiliary supply, the ohmic losses for the EMI filter and the losses in the output capacitor due to the high ripple current are considered.

As could be seen, with decreasing output power the optimal chip area decreases rapidly and in order to achieve a high efficiency for wide operation range for the prototype system shown in Fig. 11 a relative chip area of 1, i.e. a realisation of a switch with a single MOSFET STW77N65M5, has been chosen.

E. Losses as Function of Time

Based on the calculation procedure given in Fig. 3 the losses and the output power for each switching period have been calculated separately. With these values the efficiency of the TCM resonant-transition PFC rectifier could be calculated as function of time as shown in Fig. 5. There also the output power as function of time and the system efficiency η_{AVG}, which is defined by the average losses and the average output power over half a mains period, i.e. is not equal to the average value of η=f(t), are given.

If the efficiency of the PFC rectifier is measured in DC-DC operation with an input voltage of $v_N \approx 208$V and an

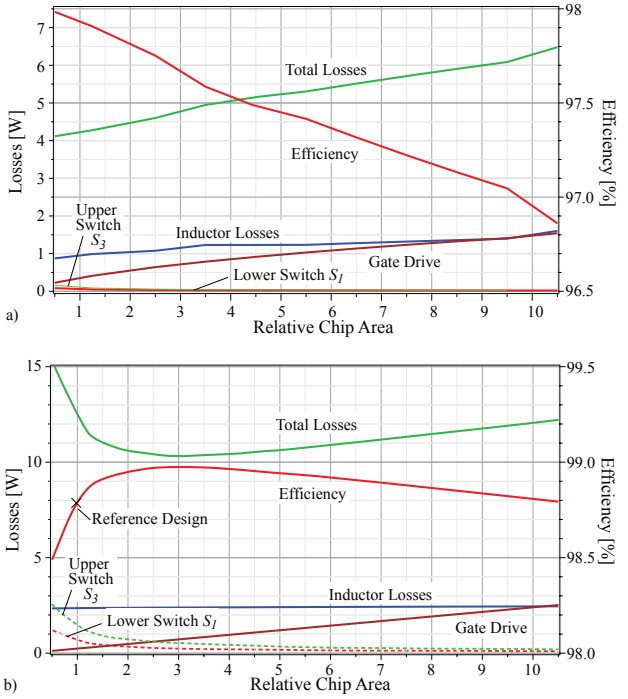

Fig. 4: Variable Losses in a 1kW TCM resonant-transition PFC rectifier with the specifications given in Table II as function of the chip area including losses for the EMI-filter, the output capacitor and the control, which are not shown separately. In a) the loss distribution at 20% output power and in b) for 100% output power are shown.

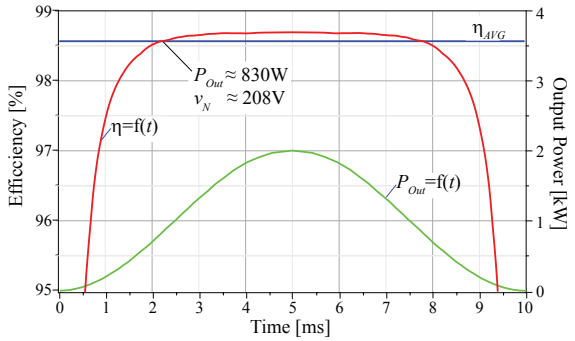

Fig. 5: Efficiency of a TCM resonant-transition PFC rectifier as function of time for half a mains cycle. There, the efficiency is calculated for each switching period with the current value of the output power and the losses.

output power of P_{Out}≈830W, the system efficiency for AC-DC operation could be directly determined as could be seen in Fig. 5. There, highly accurate electrical measurements are relatively easily possible, due to the DC-DC operation, i.e. no phase information must be measured.

III. Control Implementation

Based on the procedure presented in section II-C the current waveforms and also the timing signals can be determined. In Fig. 6 the average and the RMS current as well as I_S and I_R are given for a quarter of a mains cycle. Additionally, also the switching period T_P and the on-time T_{On} are shown as example.

Based on this information a control concept, which requires information about the zero crossing of the inductor current, is presented in the following. There, also a new, simple and robust concept for detecting the zero crossings is proposed.

A. Control based on Zero Crossing Detection

The control method is based on the zero crossings of the inductor current i_L and the values of T_{On} as well as T_R as given in Fig. 2.

A block diagram of the control implementation is given in Fig. 7, where a PFC rectifier circuit with one fast switching leg and one leg operating at mains frequency is used as example. The basic concept also could be applied to circuits with interleaved fast switching legs, where additionally a controller for the phase shift between the legs is required as described in [22].

The control circuit consists of a DSP, which determines the timing signals, and a CPLD, which generates the switching signals based on external trigger signals (i.e. the zero crossings of i_L). Solving (1)-(6) online in the DSP would require a high computational effort, so that in the DSP a Look-Up-Table (LUT) with the off-line calculated values for T_{On} and T_R as function of the output voltage U_O, the mains voltage u_N and the average current I_{AVG} are stored.

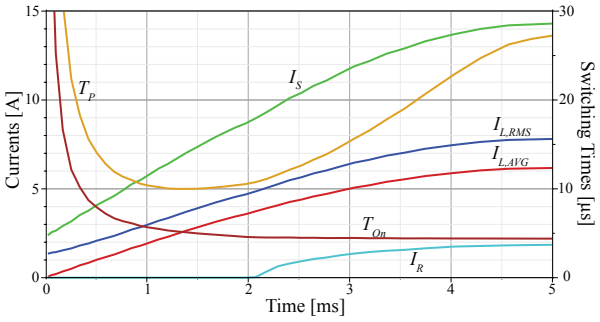

Fig. 6: Currents and times for the resonant-transition PFC rectifier with the waveforms given in Fig. 2b). The values are calculated with the procedure shown in Fig. 3.

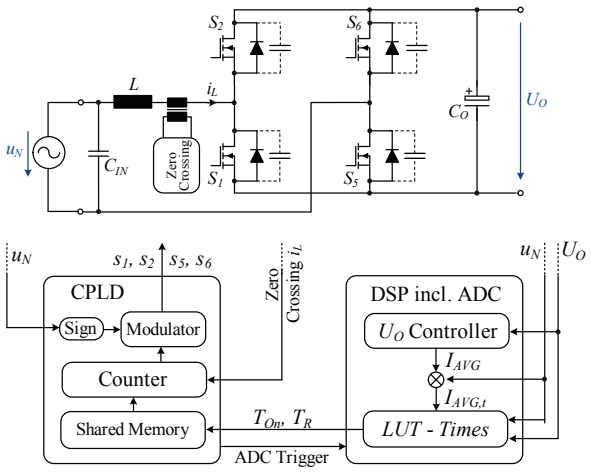

Fig. 7: Block diagram of the control circuit for the TCM resonant-transition PFC rectifier. As example a PFC rectifier with one fast switching bridge leg and one bridge leg operating at low frequency is shown. The control concept could also be used for interleaved rectifiers, where a controller for controlling the phase shift of the interleaved bridge legs would have to be added.

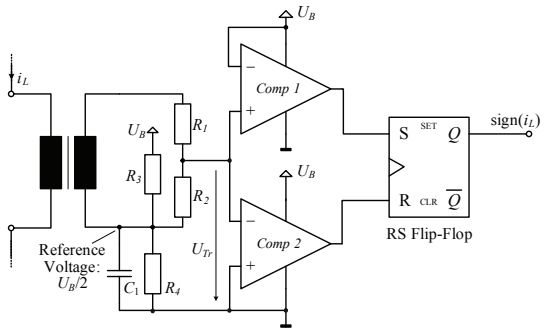

Fig. 8: Zero crossing detection circuit consisting of a small transformer, two comparators and a RS flip-flop. Resistors R_3 and R_4 generate a reference voltage $U_B/2$ that is stabilised with C_1. With R_1 and R_2 the output voltage of the transformer is divided by ≈ 4.4. These resistors additionally limit the current flowing into the input of the comparator, when $U_{Tr} > U_B$ or $U_{Tr} < 0$.

The U_O controller provides the required I_{AVG} which is multiplied by the scaled u_N in order to obtain the average value $I_{AVG,t}$ for the considered switching period. With this value and U_O, u_N the values for T_{On} and T_R are taken from the LUT. There also some interpolation is performed between the stored values.

The values for T_{On} and T_R are transferred to the CPLD via a 12-bit wide bus. 11 bits are used for the payload and one bit is used as the data ready strobe signal. In the CPLD T_{On} and T_R are loaded into a counter – T_{On} at the negative-to-positive zero crossing and T_R at the positive-to-negative zero crossing of i_L. The counter generates then the timing signals, which are used in the modulator to determine the switching signals for the 4 MOSFETs. There, the sign of u_N is important to drive the right switches.

1) Zero Crossing Detection: The control described in the previous section requires information about the zero crossing of the inductor current for the timing. In order to achieve a high efficiency, the zero crossing detection circuit must have low losses, so that shunt based concepts are not appropriate at higher power levels.

In the following a simple concept utilising a small transformer, that is driven into saturation and that has very low losses, good noise immunity and high accuracy is proposed [24]. The schematic of the detection circuit is depicted in Fig. 8 and consists of a small transformer, two comparators, a RS Flip Flop, which could be realised in the CPLD applied for generating the switching signals, and a few resistors/capacitors.

First, the operation of the transformer is explained with Fig. 9, where in a) the B-H loop of the transformer core and in b) the inductor current/ comparator signals are shown. The excursion along the H-axis is directly proportional to the inductor current i_L. In the following the operation is explained based on the points 1-7 shown in Fig. 9a) and b):

- The current starts at 0 and rises towards point 2. In the B-H loop the flux starts at the remanence flux density B_R and rises with the current towards point 2. With the changing flux a voltage is induced on the secondary side of the transformer. This voltage is divided by the voltage divider R_1 and R_2 and is significantly larger than U_B, so that the output of comparator $Comp\ 1$ is high, i.e. input S of the flip-flop is high (cf. Fig. 9b).

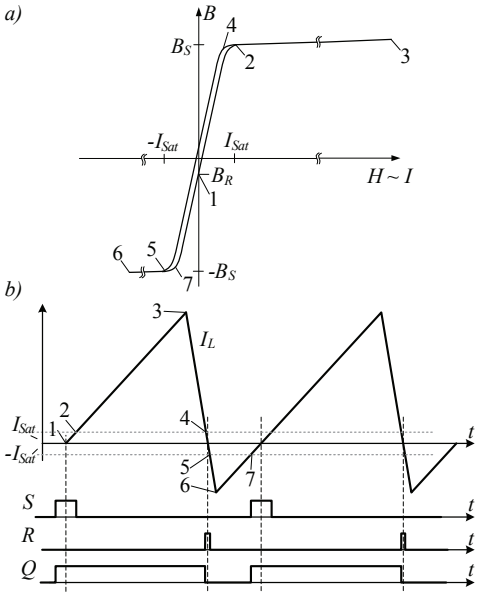

Fig. 9: a) B-H loop of the transformer used in the detection circuit given in Fig. 8. (Please note that the H-axis is enlarged, so that the small hysteresis loop could be seen.) b) Waveforms of the inductor current with the points corresponding to the numbers along the B-H loop. Additionally, the output signals of the comparators and the flip-flop are depicted. (The saturation current is enlarged for better visibility in the graphs.)

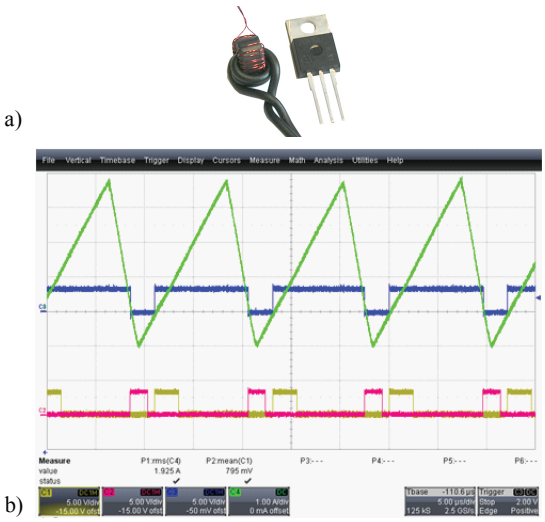

Fig. 10: a) Photo of the transformer for the zero crossing detection circuit shown in Fig. 8 and b) measured waveforms during DC-DC test operation. (In a) additionally a TO220 package is shown as size reference.)

- At point 2, the transformer saturates at the saturation current I_{Sat}, which is much smaller than the maximal operating current.
- Between point 2 and 3 the relative permeability μ_r is approximately 1, so that the change of the flux density B with the rising H-field/input current i_L is small. Consequently, only a small voltage is induced in the secondary winding of the transformer (Faraday Law). The circuit is designed so, that neither of the two comparator outputs is high during this interval. At point 3 i_L reaches

TABLE I: Parameters of Zero Crossing Detection Circuit.

Core	VITROPERM 500 F (T60006-L2009-W914)
Primary Turns	3
Secondary Turns	30
Initial Inductance	229μH
Resistor R_1	82kΩ
Resistor R_2	360kΩ
Resistor R_3 & R_4	3.3kΩ
Capacitor C_1	1μF
Comparator	TLV3502

its maximum.

- With decreasing current from point 3 to 4, also the flux density slightly decreases, but again only a small voltage is induced in the secondary, so that the output of the flip-flop is not changed.
- At point 4, i_L becomes smaller than I_{Sat} and the relative permeability μ_r increases from 1 to a several 10000, when the core leaves saturation. Between point 4 and 5, i.e. between $+I_{Sat}$ and $-I_{Sat}$, the flux density B changes from $+B_S$ to $-B_S$. This large variation of the flux density induces a voltage in the secondary winding. Since the flux is decreasing the induced voltage is negative, so that comparator $Comp$ 2 has a positive output signal, which resets the flip-flop via its reset input R (cf. Fig. 9 b).
- At point 5, the core saturates again at $-I_{Sat}$ and $-B_S$, so that between point 5 and 6 $\mu_r \approx 1$ and only a small voltage is induced in the secondary.
- At point 6, the negative peak current is reached and the current increases again. Still $\mu_r \approx 1$ and the induced voltage is small.
- At point 7, i_L reaches the negative saturation current $-I_{Sat}$ and rises towards point 2, so that the core leaves saturation again and a positive voltage is induced on the secondary due to the flux density rising from $-B_S$ to $+B_S$. This results in a high signal at the output of $Comp$ 1 setting also the output of the flip-flop.

The detection circuit is designed so, that the saturation occurs already at small currents, i.e. the induced voltage pulses are generated approximately at the zero-crossing of the current. In fact the magnetic flux density changes slightly before the zero-crossing of the current, so the voltage pulse is starting shortly before the zero crossing. This, however, could be easily compensated in the control circuit.

To have a fast saturating transformer, a core with a small cross section area and a high permeability is best to use. For this prototype a Vacuumschmelze VITROPERM 500 F core and a detection circuit with the data given in Table I is used. The cross sectional area of the core was reduced to approximately 30% of the original value by cutting the laminated tape.

For the considered detection circuit, the saturation current and magnetising inductance are:

$$I_{Sat} = \frac{B_S A_{FE}}{N A_L} = \frac{1.2\text{T} \cdot 0.3 \cdot 0.059\text{cm}^2}{3 \cdot 0.3 \cdot 25.5\mu\text{H}} = 92.5\text{mA} \quad (8)$$

$$L = N^2 A_L \approx 69\mu\text{H}, \quad (9)$$

for the modified core.

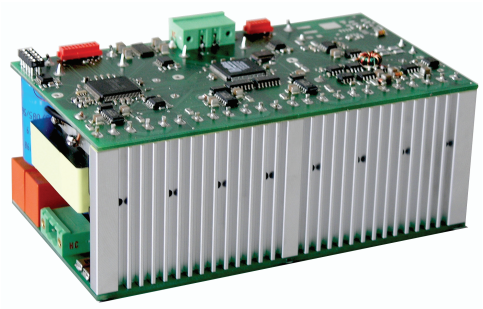

Fig. 11: Laboratory prototype of the ultra efficient and ultra compact 3kW TCM resonant-transition PFC rectifier with the specifications and components given in Table II. Dimensions: 137×56×78mm^3, power density: 5kW/dm^3, efficiency ≈ 98.3%.

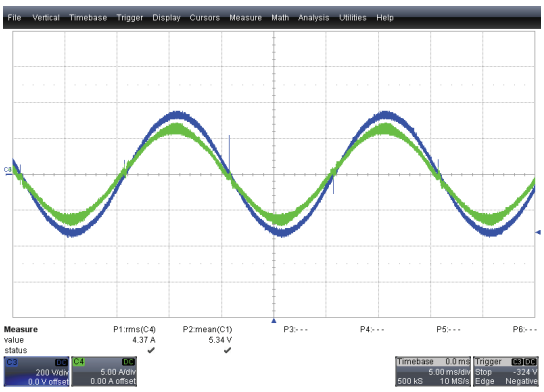

Fig. 12: Measured mains voltage and current for the prototype system shown in Fig. 11 for P_{Out}=1kW and with a DM-filter (L_{DM}50μH and C_{DM}=4μF).

Since the sensor is in series to the boost inductor, the effective boost inductance increases by the magnetising inductance as long as i_L is smaller than the saturation current I_{Sat}. This, however, does not significantly influence the circuit operation, if the saturation current is much smaller than the operating current. The magnetising inductance of the saturated core is negligible for the PFC operation.

In Fig. 10 the utilised measurement transformer and measured waveforms for DC-DC operation are given. These waveforms nicely validate the explained operation.

IV. Experimental Results

In order to validate the presented control method and calculations for designing the system, the 1kW prototype system of the TCM resonant-transition PFC as given in Fig. 11b) has been built. It has a power density of 5kW/dm^3 at an efficiency of 98.3%. In Fig. 12 measurement results for nominal output power are shown, where it could be seen, that the mains current is sinusoidal and the system operates as predicted.

As already mentioned in the introduction, in [12] the Pareto-Fronts for a conventional PFC rectifier and for a bridgeless PFC system have been calculated. The results are shown in Fig. 13, where also the performance of prototype systems is depicted. For the bridgeless PFC two different technology sets, one optimised for efficiency (natural convection, large inductor volume, low loss EMI-filter, etc.) and one optimised for power density (forced air cooling, small inductor volume, compact auxiliary power supply, etc.) are considered. The green curve

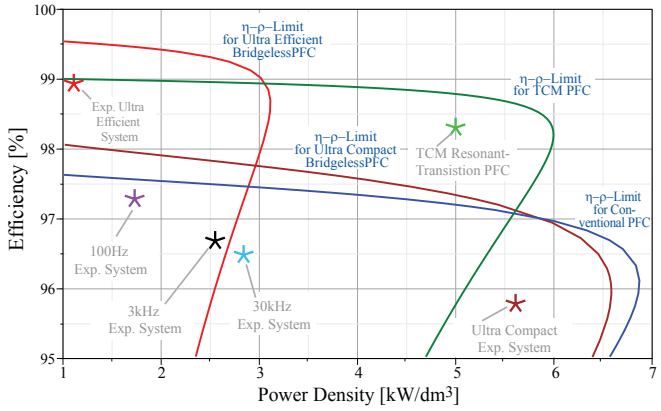

Fig. 13: Pareto Fronts in the power density – efficiency plane (ρ-η plane) for the conventional, the bridgeless and the TCM resonant-transition PFC rectifier. The Pareto-Front defines the maximal achievable performance for a compromise between power density and efficiency. For the bridgeless PFC concept two technology sets – one facilitating high power density and one high efficiency – are shown.

TABLE II: Specifications of the considered single phase PFC rectifiers.

Output power P_O	3kW
Line voltage U_N	230±10%
Output voltage U_O	400V
Ambient Temperature	45°C
MOSFETs S_1-S_4	STW77N65M5
Boost-L Core	E42/21/15
Boost-L Winding	25 × 420 Strands ×71μm
Output Capacitor	5× 450V/68μF (Vishay 198 PHR-SI)

in Fig. 13 represents the Pareto-Front for the presented TCM resonant-transition PFC rectifier and the green star shows the performance of the prototype system in Fig. 11.

In this figure it could be nicely seen that with the TCM resonant-transition PFC rectifier a high power density and a high system efficiency could be realised at the same time. Thus, the proposed concept enables performance values, which cannot be achieved with conventional approaches.

V. Conclusion

In this paper, equations and a design procedure for a Triangular Current Mode (TCM) resonant-transition PFC rectifier are presented, that allow to determine the optimal set of operating parameters for minimal losses. With the optimised operating parameters and due to the ZVS operation enabled by the presented modulation, the rectifier system achieves an outstanding power density and efficiency at the same time. This is validated by a 3kW prototype system with a power density of 5kW/dm^3 and an efficiency of 98.3%, for which also measurement results are presented.

Furthermore, the implementation of the control based on timing signals and the detection of the zero crossings of the discontinuous inductor current is explained. There, also a new, simple and low loss concept for zero crossing detection with small saturating transformers is proposed and experimentally verified.

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