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Comprehensive Comparative Evaluation of Single- and Multi-Stage Three-Phase Power Converters for Photovoltaic Applications

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Abstract

***Abstract*—For utility-scale photovoltaic (PV) power plants, the trend goes towards larger installations with reduced levelized costs of electricity. Further cost reductions can be achieved by modular and redundant inverter topologies, which enable higher reliabilities and a better overall system availability. In this paper, a comparative evaluation of selected three-phase single- and multi-stage voltage source inverters with rated power of 50 kW for modular utility-scale PV plants is presented. Based on detailed loss, volume and thermal models, the inverter systems are designed according to a variety of constraints and standards covering a wide range of practical issues, such as grid codes, EMI requirements and lifetime considerations. Finally, for different operational switching frequencies, the optimal topologies are identified by means of an analysis regarding achievable efficiencies, power density and required semiconductor chip areas.**

I. Introduction

Due to environmental concerns, power generation from photovoltaic (PV) energy sources has rapidly increased in the past years. In both residential and utility-scale PV energy systems, there has been an ongoing trend towards larger installations with increased rated power. Higher energy yield, reduced balance of system (BOS) costs as well as less maintenance effort are the driving factors behind this trend [1], [2], [3]. Although smart grid interoperability and grid support functionalities gain increasing importance, further cost reductions and efficiency improvements remain key requirements for a continuingly growing PV penetration. In this context, modular and redundant inverter topologies for utility-scale PV plants are expected to have a large potential, as they enable easier maintenance and a better overall system reliability, both leading to lower levelized costs [1]. Increased inverter lifetimes matching those of the PV panels will further help saving costs. Therefore, three-phase systems with comparably small DC link capacitances are preferred since they allow for the use of highly efficient and durable film capacitors [4]. Consequently, it remains to be investigated, which of the numerous known three-phase topologies is the optimal choice for the converter modules of such modular redundant utility-scale PV plants.

In literature, there have been many contributions dealing with the comparison of three-phase PV inverters. In [3], approximate achievable efficiencies, semiconductor requirements and different input side DC/DC stages of a wide selection of three-phase voltage source inverters (VSI) is discussed in a qualitative manner. A quantitative comparison of various current source inverters (CSI) and VSIs is presented in [5], [6], where the focus is mainly on the analysis of the respective semiconductor losses. Finally, a more detailed comparative evaluation of three-phase VSIs is performed in [7], [8], where some of the inductor losses [8] as well as the losses occurring in the capacitors [7], [8] are taken into account. In addition to that, [7] qualitatively discusses the required component volumes for a given frequency.

In the above mentioned contributions, the quantitative examinations are mainly focused on the inverter efficiencies, whereas the discussion of other aspects, such as inverter size, remains, if present, qualitative. Furthermore, variable switching frequencies as well as detailed loss models for passive components, especially inductors and output filters, are mostly missing. However, due to their considerable share of the overall inverter costs [9] and volume, taking into account the passives is essential for a meaningful comparison.

In this work, a systematic and in-depth evaluation of selected three-phase single- and multi-stage VSI topologies with rated power of 50 kW, suitable for modular utility-scale plants, is performed. A comprehensive and meaningful comparison is enabled by incorporating the following performance aspects into the analysis, which is done for different operational switching frequencies:

- Weighted European efficiency
- Required semiconductor chip area
- Volumes of passive components and heat sink

After presenting the selected topologies and system specifications in **Section II**, in **Section III**, detailed loss, volume and thermal models of all relevant system components are derived. Subsequently, in **Section IV**, the systems are dimensioned and finally comparatively evaluated in **Section V** in order to identify the optimal topologies for the given application.

II. System Description

The generic system topology considered in this paper is a three-phase PV inverter with output filter connected to a

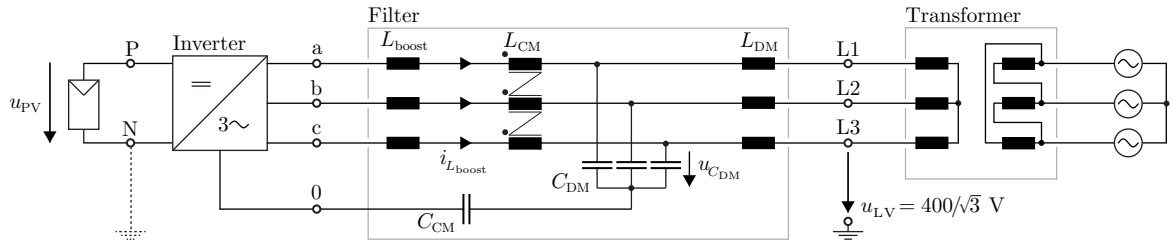

Fig. 1: Generic topology of the considered three-phase PV inverter with output LCL filter. A Δ-Y transformer connects the 400 V low voltage secondary side to a European 50 Hz medium voltage grid. In the US, the negative rail "N" of the floating secondary must normally be grounded according to the National Electricity Code (NEC) 690 [10]. In case the DC-link mid-point "0" is not available, a split variant of C_{CM} with equivalent total capacitance and connection to the positive and negative DC-link rails "01" and "02" is employed (see **Fig. 2** and **Fig. 3**).

European 50 Hz medium voltage grid (**Fig. 1**). The RMS line-to-line voltage on the secondary side of the Δ-Y transformer is assumed to be 400 V with worst case deviations of $\pm 10\,\%$.

A. Specifications

The considered rated system power is $P_0 = 50\,\mathrm{kW}$. The input voltage of the inverter, which is the solar generator voltage u_{PV}, is highly temperature dependent. Assuming a temperature range of -20 °C to 80 °C, the minimum and maximum MPP voltage (the voltage related to the maximum power point of the solar generator and thus the voltage of interest to be tracked by the inverter) approximately vary by a factor of 1.8 [11]. With regard to the selected topologies in **Sec. II-B** and the available semiconductor devices, two ranges of the MPP voltage are chosen,

$$\bar{u}_{\mathrm{PV,L}} = [450\,\mathrm{V}, 820\,\mathrm{V}]\,, \tag{1}$$

$$\bar{u}_{\mathrm{PV,H}} = [650\,\mathrm{V}, 1160\,\mathrm{V}]\,. \tag{2}$$

As the ratio between maximum solar generator voltage (which is the open loop voltage) and minimum MPP voltage can be up to a factor 2, with the chosen MPP voltage ranges, maximum inverter input voltages of 900 V and 1300 V result. Consequently, the lower MPP voltage range $\bar{u}_{\mathrm{PV,L}}$ enables the use of 1200 V semiconductors (600 V devices in 3-level inverters). However, a input side DC/DC boost converter is required to

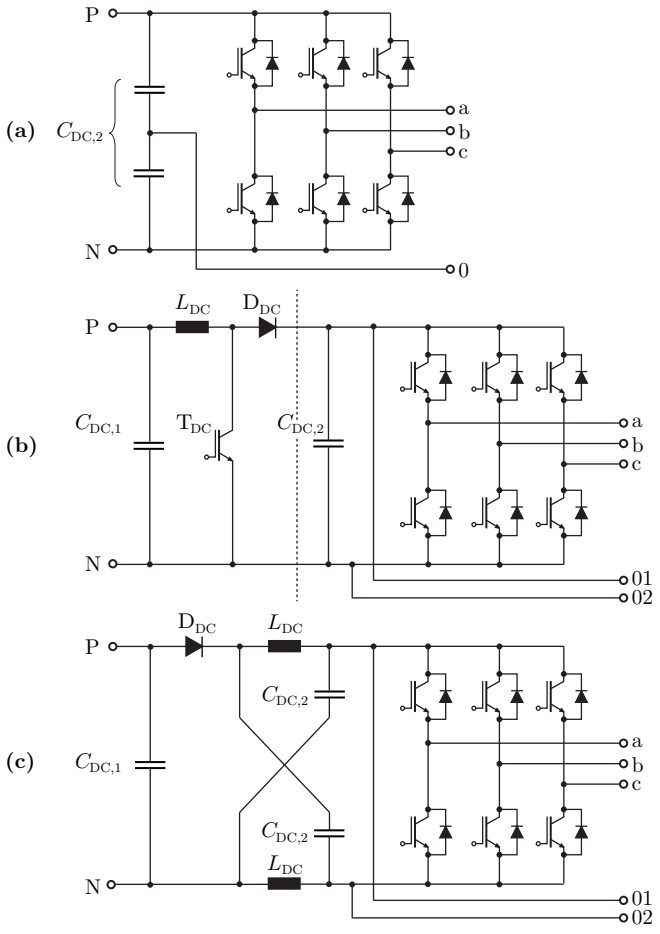

Fig. 2: Considered single- and multi-stage topologies. Single-stage 2-level VSI (2LVSI) **(a)**. 2-level VSI with adjusting input side DC/DC boost converter (2LVSI+BC) **(b)**. 2-Level Z-source inverter (2LZSI) **(c)**.

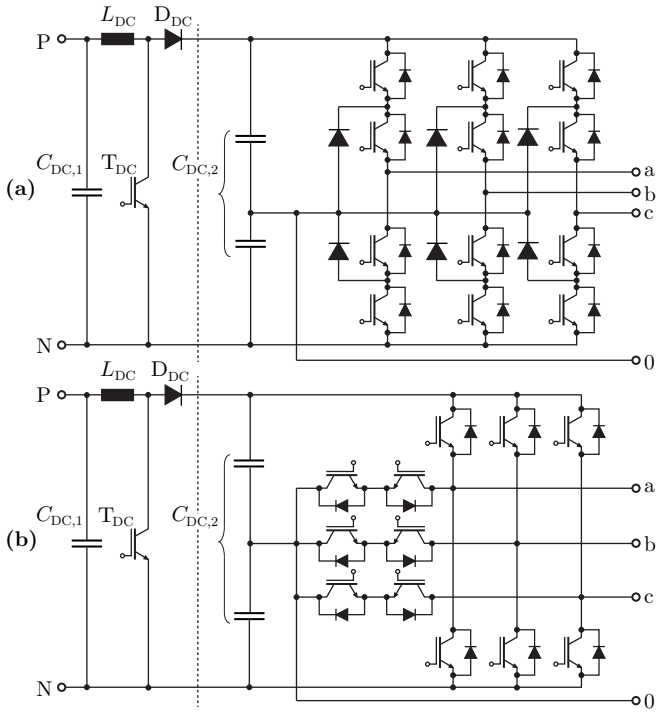

Fig. 3: Considered 3-level topologies with input side DC/DC boost converters. 3-level I-type topology (3LI+BC) **(a)**. 3-level T-type topology (3LT+BC) **(b)**.

ensure the minimum DC-link voltage of 650 V in order to feed power into a $(400+10\,\%)$ V grid. In contrast, the higher MPP range $\bar{u}_{\mathrm{PV,H}}$ is intended for single-stage inverters with either 1700 V or 1200 V (3-level topologies) rated semiconductors.

The considered range of semiconductor switching frequencies is

$$f_{\mathrm{sw}} \in \bar{f}_{\mathrm{sw}} = [4\,\mathrm{kHz}, 16\,\mathrm{kHz}]\,, \tag{3}$$

where 4 kHz is a relatively low frequency as known from drive systems and 16 kHz would allow to avoid audible operating noise. A standard sinusoidal PWM modulation scheme with third-harmonic injection has been assumed throughout this work. For the control of the Z-network of the 2LZSI, the maximum constant boost control strategy has been implemented [12].

B. Inverter Topologies

Two basic comparisons are performed in this paper. Motivated by [9], [13], the advantages and disadvantages of an input side DC/DC stage to adjust the varying solar generator voltage are investigated. For this purpose, the basic 2-level VSI topology with (2LVSI+BC) and without (2LVSI) boost converter are considered (**Fig. 2**). This selection is complemented by the 2-level Z-source inverter (2LZSI), which can be seen as hybrid between a single- and a two-stage inverter. In a second step, two 3-level topologies, i.e. the I-type (3LI+BC) and T-type (3LT+BC) variant with boost converters as shown in **Fig. 3**, are included into the comparison.

As ancillary grid services are gaining more and more importance [1], [3], CSI topologies are not analyzed due to their limited ability of reactive power generation [6].

C. Output Filter

An *LCL* filter as depicted in **Fig. 1** is considered for all topologies and switching frequencies. It combines differential mode (DM) and common mode (CM) filter elements. Note that for the 2LVSI+BC and 2LZSI topologies, the DC-link mid-points "0" are not available. Therefore, a split variant of the common mode capacitor C_{CM} is assumed, which can be connected to the positive and negative DC-link rails, "01" and "02", respectively.

III. Modeling Approach

Based on available components and materials, analytical loss, volume and thermal models for all active and passive components are presented in this section. Furthermore, equations for the average and RMS currents, as well as expressions describing the high frequency (HF) ripple voltages and currents, have been derived and verified by extensive simulations. Due limited space, however, a detailed discussion of the latter cannot be presented here.

A. Semiconductors and Heat Sink

The semiconductor loss and thermal models have been derived based on a selection of IGBT modules from Infineon:

- FSxxxR07NxE4, 2-level sixpack 600 V IGBT 4
- FSxxxR12KT4 B11, 2-level sixpack 1200 V IGBT 4
- FSxxxR17PE4, 2-level sixpack 1700 V IGBT 4
- F3LxxxR06WxE3 B11, 3-level I-type phase leg 600 V IGBT 3

Module families with the same or, if not available, similar packages and current ratings were chosen.

1) Loss models: based on the work in [14], with reference to measurements on samples and datasheet values, the chip die sizes A_{Si} were linearly fitted as a function of the current rating I_{N}. This enables the use of the following conduction loss model,

$$P_{\mathrm{C}}(A_{\mathrm{Si}}, i) = U_{\mathrm{fw}} \cdot i + \frac{R_{\mathrm{on,N}} \cdot A_{\mathrm{Si,N}}}{A_{\mathrm{Si}}} \cdot i^2, \tag{4}$$

where U_{fw} is the forward voltage drop and i the current flowing through the device. The subscript "N" denotes nominal datasheet values. In a first approximation, the switching losses P_{P} can be modeled independent from A_{Si},

$$P_{\mathrm{P}}(u, i, f_{\mathrm{sw}}) = E_{\mathrm{P,N}} \cdot \frac{u}{U_{\mathrm{N}}} \cdot \frac{i}{I_{\mathrm{N}}} \cdot f_{\mathrm{sw}}, \tag{5}$$

where u is the blocking voltage across the semiconductor device, if switching overvoltages are neglected. Finally, given the gate voltage U_{GE}, the gate driver losses can be estimated by

$$P_{\mathrm{GD}}(A_{\mathrm{Si}}, f_{\mathrm{sw}}) = E_{\mathrm{GD,N}} \cdot \frac{A_{\mathrm{Si}}}{A_{\mathrm{Si,N}}} \cdot U_{\mathrm{GE}} \cdot f_{\mathrm{sw}}. \tag{6}$$

2) Thermal Model: the thermal model of the semiconductor junction temperature T_{j} includes a chip area dependent thermal resistance $R_{\mathrm{th,js}}(A_{\mathrm{Si}})$ and can be described by

$$T_{\mathrm{j}}(A_{\mathrm{Si}}, u, i) = T_{\mathrm{sink}} + R_{\mathrm{th,js}}(A_{\mathrm{Si}}) \cdot (P_{\mathrm{C}}(A_{\mathrm{Si}}, i) + P_{\mathrm{P}}(u, i))\,, \tag{7}$$

where T_{sink} denotes the temperature of the heat sink. Knowing the average semiconductor losses $P_{\mathrm{Si,avg}}$, the required heat sink volume V_{sink} can be approximated by [15]

$$V_{\mathrm{sink}} = \frac{P_{\mathrm{Si,avg}}}{(T_{\mathrm{sink}} - T_{\mathrm{amb}})\, CSPI}, \tag{8}$$

where T_{amb} is the ambient temperature. The cooling system performance index $CSPI$ is defined as follows [16],

$$CSPI = \frac{G_{\mathrm{th,sa,N}}}{V_{\mathrm{sink,N}}}, \tag{9}$$

where $G_{\mathrm{th,sa,N}}$ denotes the thermal conductance between the surface of the heat sink and the ambient. A $CSPI$ of 9 $\mathrm{W/K\ dm^3}$ has been calculated based on the heat sink LA 7 150 from Fischer Elektronik [17].

B. Passive Components

1) Inductors: the inductor models are based on foil windings and U-shaped cores with a single air gap. Tape wound cores made of iron-based amorphous alloy 2605S3A from Metglas have been considered for the AC boost and CM inductors L_{boost} and L_{CM}, respectively, and all DC side inductors L_{DC}. Laminated steel is used for the remaining DM inductors L_{DM}. The core losses are calculated by means of the Steinmetz equation,

$$P_{\text{core}}(V_{\text{core}}, \hat{B}, f_{\text{sw}}) = k \cdot f_{\text{sw}}^{\alpha} \cdot \hat{B}^{\beta} \cdot V_{\text{core}}, \tag{10}$$

where $\hat{B}$ is the peak flux density and V_{core} the volume of the core. The parameters k, α and β are obtained from data sheet values by means of least square approximations [18]. The winding losses $P_{\text{wdg,LF}}$ caused by the low-frequency (LF) fundamental currents i_{LF} can be calculated by

$$P_{\text{wdg,LF}}(\vec{d}, N_{\text{turns}}, T_{\text{wdg}}, i_{\text{LF}}) = R_{\text{wdg,DC}}(\vec{d}, N_{\text{turns}}, T_{\text{wdg}}) \cdot i_{\text{LF}}^2, \tag{11}$$

with $R_{\text{wdg,DC}}$ as the DC resistance of a winding depending on the inductor geometry $\vec{d}$, the number of turns N_{turns} and its temperature T_{wdg}. As analytical functions which consider non-ideal effects (such as the fringing field of the air gap) are difficult to derive, the high frequency (HF) losses $P_{\text{wdg,HF}}$ have been calculated by means of 2D FEM simulations. Large numbers of simulations have been performed to derive interpolated multi-dimensional functions depending on $\vec{d}$, N_{turns}, f and i_{HF}, which are suitable for numerical optimizations. An overall error of less than $\leq \pm 15\,\%$ between FEM simulations and numerical calculations was observed.

A thermal model for determining the winding and core temperatures has been derived based on [19]. It assumes a homogenous inductor temperature $T_L = T_{\text{core}} = T_{\text{wdg}}$ and models thermal natural convection to the ambient, which is the dominant heat transfer mechanism for the considered temperature range (see **Section IV-C**),

$$T_L(\vec{d}, N_{\text{turns}}, T_L, P_{\text{core}}, P_{\text{wdg}}) = T_{\text{amb}} + R_{\text{th},L}(\vec{d}, N_{\text{turns}}, T_L) \cdot (P_{\text{core}} + P_{\text{wdg}}). \tag{12}$$

Following the approach taken in [20], all HF losses are approximated considering sinusoidal HF ripple currents und flux densities with constant amplitude. The amplitudes are chosen to be equal to the worst case ripple occurring over the fundamental period for a given modulation index or duty cycle, respectively.

2) Capacitors: the following film capacitors have been selected:

- Split DC capacitors: EPCOS MKP DC LSI 600 V and 800 V series.
- Other DC capacitors: EPCOS MKP DC 1100 V series.
- AC filter: EPCOS X2 MKP 305 V AC series.

Datasheet values have been used to derive linear models of the volumes and equivalent series resistances as a function of the capacitance. The life expectancy LE of the capacitors can be approximated by [21]

$$LE(u) = LE_{\text{N}} \cdot \frac{U_{\text{N}}}{u}^{8} \cdot 2^{\frac{T_{\text{N}} - T_{\text{amb}}}{10}}. \tag{13}$$

IV. Dimensioning Procedure and Design Constraints

A. Employed Components

Tab. I summarizes the employed components, materials and solar generator voltage ranges of all topologies. The associated models and detailed component information can be found in **Section III**. Note that in case of the 3LT+BC, where the currents commutate from 600 V to 1200 V rated devices, the switching loss data sheet values have been modified according to the measurements in [14]. For simplicity reasons, the 1200 V sixpack module models have been used for the DC side semiconductors T_{DC} and D_{DC}.

TABLE I: Employed components, materials and solar generator voltage ranges of the selected topologies. Detailed information on the component types and manufactorers can be found in **Section III**.

	2LVSI	**2LVSI+BC**	**2LZSI**	**3LI+BC**	**3LT+BC**
Voltage range	$\bar{u}_{\text{PV,H}}$	$\bar{u}_{\text{PV,L}}$	$\bar{u}_{\text{PV,L}}$	$\bar{u}_{\text{PV,L}}$	$\bar{u}_{\text{PV,L}}$
Inverter stage	1700 V	1200 V	1200 V	600 V (I-type)	1200 V [1)] 600 V [1)]
T_{DC}, D_{DC}	-	1200 V	1200 V	1200 V	1200 V
$\boldsymbol{L}_{\text{DC}}$	-	Amorphous alloy			
$\boldsymbol{C}_{\text{DC,1}}$	-	1100 V	1100 V	1100 V	1100 V
$\boldsymbol{C}_{\text{DC,2}}$	2 × 800 V	1100 V	1100 V	2 × 600 V	2 × 600 V
$\boldsymbol{L}_{\text{boost}}$, $\boldsymbol{L}_{\text{CM}}$	Amorphous alloy				
$\boldsymbol{L}_{\text{DM}}$	Laminated steel				
$\boldsymbol{C}_{\text{DM}}$, $\boldsymbol{C}_{\text{CM}}$	305 V AC				

[1)] Modified switching loss data according to [14]

B. Semiconductor Chip Area and Heat Sink

The semiconductor area is chosen such as to ensure a maximum junction temperature of $T_{\text{j}} = 125\,^{\circ}\text{C}$ at rated currents and for phase angles $\varphi \in \left[-\frac{\pi}{2}, \frac{\pi}{2}\right]$. The heat sink temperature is assumed to be $T_{\text{sink}} = 80\,^{\circ}\text{C}$ with a worst case ambient temperature of $T_{\text{amb}} = 40\,^{\circ}\text{C}$. The design procedure is described in more detail in [14].

C. Passive Components

1) DC Inductors: all DC inductances L_{DC} are chosen such that the maximum peak to peak current ripples are 20% of the respective nominal DC currents. The total DC inductor volume is minimized for a given maximum inductor temperature $T_L = 100\,^{\circ}\text{C}$ at a worst case ambient temperature $T_{\text{amb}} = 40\,^{\circ}\text{C}$.

2) DC Capacitors: all DC capacitors $C_{\text{DC,1}}$ and $C_{\text{DC,2}}$, respectively, are designed so as to exhibit a worst case peak to peak voltage ripple of 1% of their respective nominal DC voltage. On the one hand, this guarantees a sufficiently stable DC-link voltage and on the other hand a stable MPP tracking, which allows for an optimal PV energy harvesting. Furthermore, all capacitors must feature a lifetime of more than 20 years.

3) LCL Filter: the design procedure of the LCL filter is summarized in **Fig. 4**. Different types of constraints and standards have been considered. In a first step, L_{boost} and C_{DM} are chosen so as to limit the DM peak to peak current ripple $\Delta i_{L_{\text{boost}}}^{\text{DM}}$ to 10 % of the associated fundamental peak current and to limit the DM peak to peak voltage ripple $\Delta u_{C_{\text{DM}}}^{\text{DM}}$ to 2.5 % of the fundamental peak grid voltage. In practice, these ripples allow for sufficiently accurate current and voltage measurements for the inverter control. In a next step, the value of L_{DM} is chosen. The total DM filter attenuation must be sufficiently large so that the remaining DM emissions after

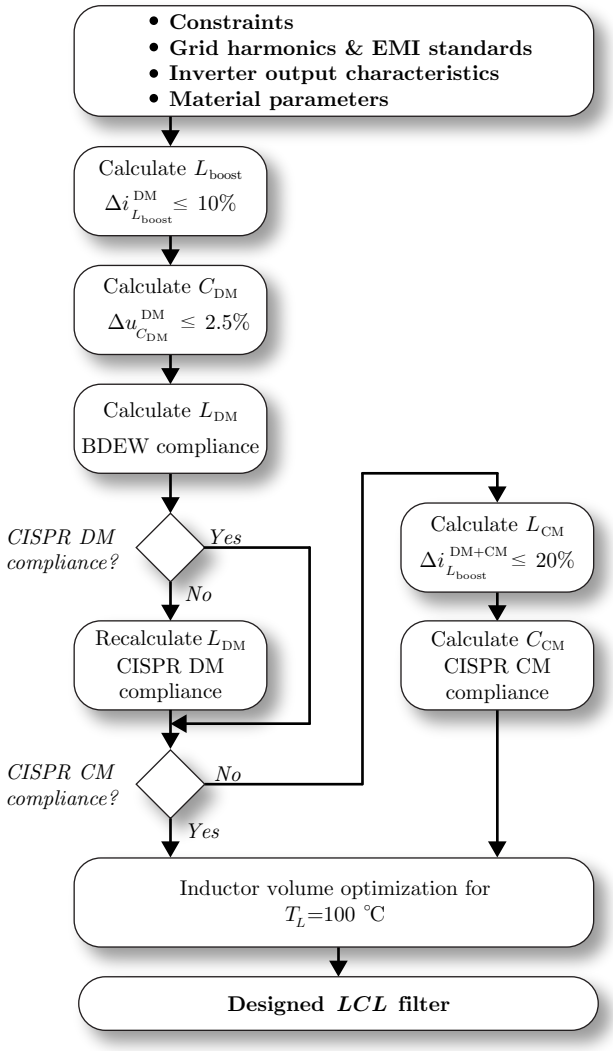

Fig. 4: Design procedure for the LCL filter as depicted in **Fig. 1**.

the filter comply with the grid harmonics limits defined in the technical guideline "Generating Plants Connected to the Medium-Voltage Network" from BDEW [22], and the CISPR 11 Class B EMI standard [23]. The derivation of the applicable limits is described in [24]. The partially filtered (by L_{boost}) CM emissions must also be within the CISPR 11 limits. If this is not the case, additional CM filter elements L_{CM} and C_{CM} are required which generate sufficient CM attenuation and limit the flowing CM currents $i_{L_{\text{boost}}}^{\text{CM}}$ (via C_{CM}), so that the total current ripple $i_{L_{\text{boost}}}^{\text{DM+CM}}$ in L_{CM} is limited to 20 %. Finally, given the computed component values, an optimization algorithm searches for the lowest possible inductor volumes for a maximum inductor temperature $T_L = 100\,^{\circ}\text{C}$ at a worst case ambient temperature $T_{\text{amb}} = 40\,^{\circ}\text{C}$. The designed filters exhibit a maximum reactive power consumption of less than 5 % of the rated power P_0.

V. Comparative Evaluation

A. Definition of Performance Indices

Following [15], normalized performance indices are defined which allow for a meaningful comparative evaluation independent from the system dimensioning:

- For the calculation of the European efficiency η_{EURO}, typical solar generator temperatures of 25, 45 and 65 °C were considered. As the temperatures correspond to different solar generator voltages $u_{\text{PV}} \in \bar{u}_{\text{PV},x}$, different inverter efficiencies result, which are then equally weighted,

$$\eta_{\text{EURO}} = \frac{\eta_{\text{EURO,25\,°C}} + \eta_{\text{EURO,45\,°C}} + \eta_{\text{EURO,65\,°C}}}{3}. \quad (14)$$

  Note that in case of the lower MPP voltage range $\bar{u}_{\text{PV,L}}$ the solar generator voltage at 25 °C is above 650 V and hence high enough for feed-in. This implies reduced losses in the boost converter stages and Z-source impedance network as their boost function can be turned off. Additionally, a constant power consumption of $P_{\text{aux}} = 25\,\text{W}$ of the auxiliary supply was assumed.
- The relative total semiconductor chip area of IGBTs and diodes is calculated according to

$$\tilde{A}_{\text{Si,tot}} = \frac{\sum_n A_{\text{Si,S},n} + \sum_n A_{\text{Si,D},n}}{P_0}. \quad (15)$$

  Further characteristic quantities are defined in the following:
- Relative total conduction losses of IGBT switches and diodes, weighted according to the European efficiency,

$$\gamma_{\text{C}} = \frac{\sum_n P_{\text{S,C,EURO},n} + \sum_n P_{\text{D,C,EURO},n}}{P_0}; \quad (16)$$

- Relative total switching losses of IGBT switches and diodes, weighted according to the European efficiency,

$$\gamma_{\text{P}} = \frac{\sum_n P_{\text{S,P,EURO},n} + \sum_n P_{\text{D,P,EURO},n}}{P_0}; \quad (17)$$

- Relative boxed volumes of inductors and capacitors,

$$\rho_L^{-1} = \frac{\sum_n V_{L,n}}{P_0}, \quad (18)$$

$$\rho_C^{-1} = \frac{\sum_n V_{C,n}}{P_0}; \quad (19)$$

- Relative total power density,

$$\rho_{\text{tot}} = \frac{P_0}{V_{\text{sink}} + \sum_n V_{L,n} + \sum_n V_{C,n}}. \quad (20)$$

B. Comparison of Performances

In this subsection, the results of the dimensioning procedure described in **Section IV**, which is based on the models of **Section III**, are evaluated and compared for the topologies selected in **Section II**. **Fig. 5** shows a variety of performance indices of all topologies for $f_{\text{sw}} = 4\,\text{kHz}$. **Fig. 6(a)** depicts the European efficiency η_{EURO} versus the relative total power density ρ_{tot} for the entire switching frequency range $\bar{f}_{\text{sw}}$, whereas **Fig. 6(b)** compares the relative total volume ρ_{tot}^{-1} against the required relative total semiconductor chip area $\tilde{A}_{\text{Si,tot}}$. **Tab. II** gives detailed insight into the loss and volume

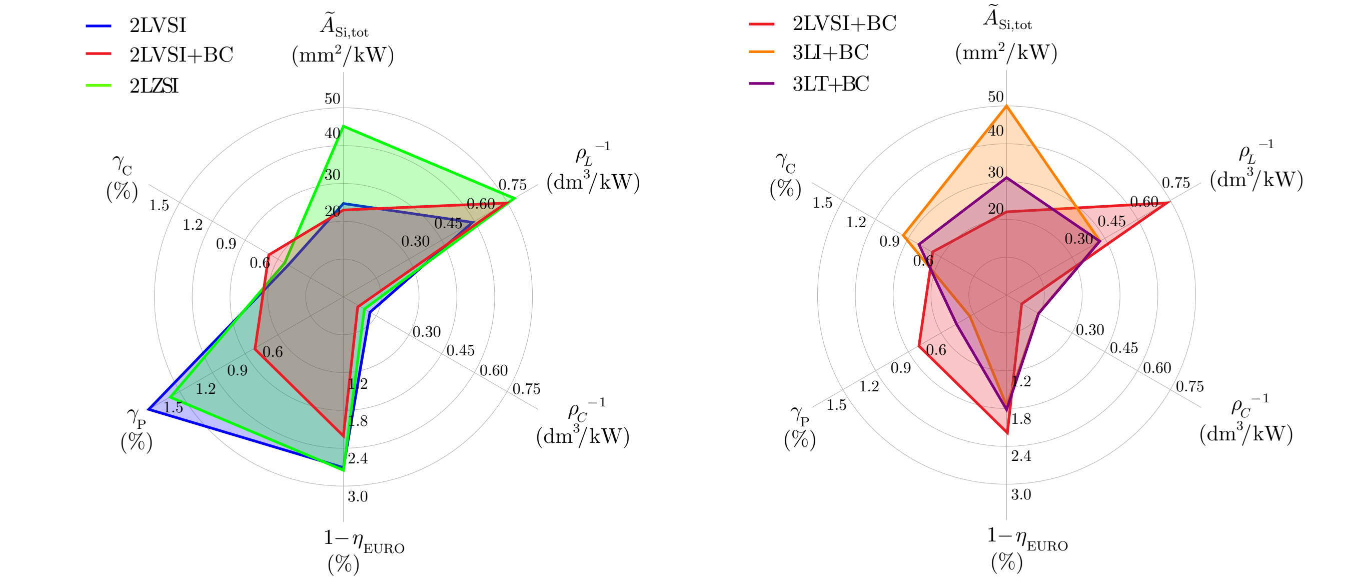

Fig. 5: Comparison of the investigated topologies regarding relative total semiconductor chip area $\tilde{A}_{\text{Si,tot}}$, relative boxed volumes of inductors and capacitors ρ_L^{-1}, ρ_C^{-1}, relative total losses $1-\eta_{\text{EURO}}$ and relative semiconductor switching and conduction losses γ_{P}, γ_{C}, for a switching frequency of 4 kHz.

TABLE II: Relative volumes ρ_x^{-1} (in dm³/kW) and weighted losses $1-\eta_{x,\text{EURO}}$ (in %) of the LCL filter, the passive components in the DC networks and of the heat sink as a function of the switching frequency f_{sw} (in kHz).

		2LVSI		**2LVSI+BC**		**2LZSI**		**3LI+BC**		**3LT+BC**	
	f_{sw}	ρ_x^{-1}	$1-\eta_{x,\text{EURO}}$	ρ_x^{-1}	$1-\eta_{x,\text{EURO}}$	ρ_x^{-1}	$1-\eta_{x,\text{EURO}}$	ρ_x^{-1}	$1-\eta_{x,\text{EURO}}$	ρ_x^{-1}	$1-\eta_{x,\text{EURO}}$
LCL filter	4	0.602	0.300	0.602	0.300	0.602	0.300	0.327	0.185	0.327	0.185
	8	0.347	0.241	0.347	0.241	0.347	0.241	0.186	0.128	0.186	0.128
	12	0.337	0.385	0.283	0.250	0.283	0.250	0.137	0.118	0.137	0.118
	16	0.285	0.407	0.234	0.250	0.234	0.250	0.135	0.234	0.135	0.234
DC network	4	0.124	<0.001	0.180	0.118	0.225	0.162	0.253	0.112	0.253	0.112
	8	0.062	<0.001	0.101	0.087	0.126	0.120	0.137	0.081	0.137	0.081
	12	0.041	<0.001	0.073	0.074	0.091	0.098	0.096	0.068	0.096	0.068
	16	0.031	<0.001	0.061	0.069	0.074	0.089	0.078	0.063	0.078	0.063
Heat sink	4	0.071	-	0.056	-	0.078	-	0.052	-	0.069	-
	8	0.113	-	0.074	-	0.126	-	0.061	-	0.074	-
	12	0.160	-	0.094	-	0.177	-	0.067	-	0.080	-
	16	0.208	-	0.116	-	0.229	-	0.078	-	0.091	-

TABLE III: Semiconductor chip area $\tilde{A}_{\text{Si},x}$ (in mm²/kW), conduction losses $\gamma_{\text{C},x}$ and switching losses $\gamma_{\text{P},x}$ (in %) in the inverter stages and the DC networks as a function of the switching frequency f_{sw} (in kHz).

		2LVSI			**2LVSI+BC**			**2LZSI**			**3LI+BC**			**3LT+BC**		
	f_{sw}	$\tilde{A}_{\text{Si},x}$	$\gamma_{\text{C},x}$	$\gamma_{\text{P},x}$	$\tilde{A}_{\text{Si},x}$	$\gamma_{\text{C},x}$	$\gamma_{\text{P},x}$	$\tilde{A}_{\text{Si},x}$	$\gamma_{\text{C},x}$	$\gamma_{\text{P},x}$	$\tilde{A}_{\text{Si},x}$	$\gamma_{\text{C},x}$	$\gamma_{\text{P},x}$	$\tilde{A}_{\text{Si},x}$	$\gamma_{\text{C},x}$	$\gamma_{\text{P},x}$
Inverter stage	4	27	0.52	1.81	17	0.52	0.66	34	0.42	1.47	44	0.81	0.16	25	0.67	0.31
	8	64	0.39	3.61	23	0.45	1.30	61	0.37	2.95	45	0.80	0.31	28	0.62	0.63
	12	124	0.35	5.40	29	0.41	1.95	92	0.34	4.42	51	0.76	0.47	33	0.58	0.94
	16	207	0.34	7.20	37	0.38	2.60	127	0.33	5.89	60	0.73	0.62	40	0.54	1.26
DC network	4	-	-	-	6	0.15	0.18	12	0.13	0.16	6	0.15	0.18	6	0.15	0.18
	8	-	-	-	9	0.14	0.35	25	0.13	0.31	9	0.14	0.35	9	0.14	0.35
	12	-	-	-	13	0.14	0.53	43	0.12	0.47	13	0.14	0.53	13	0.14	0.53
	16	-	-	-	17	0.13	0.70	64	0.12	0.62	17	0.13	0.70	17	0.13	0.70

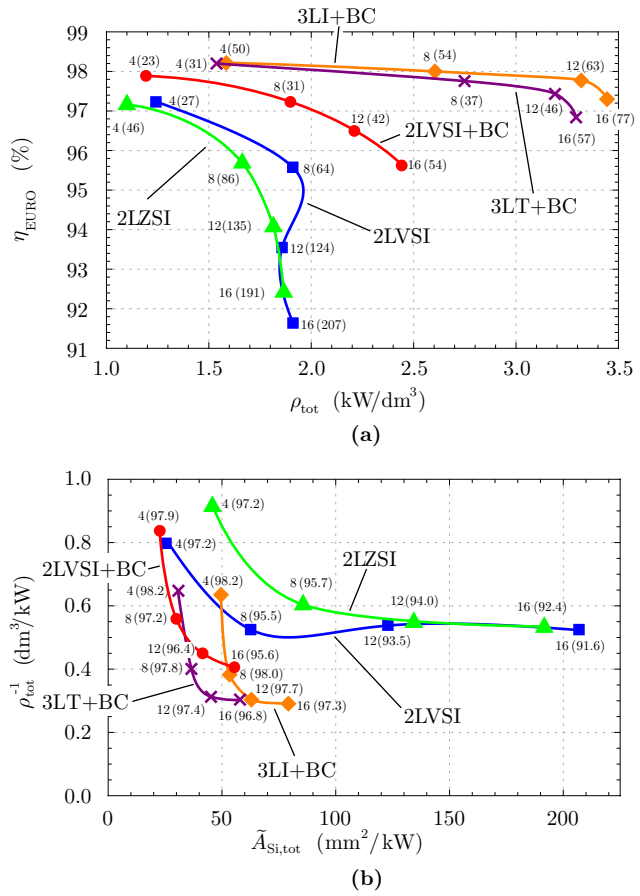

Fig. 6: European efficiency η_{EURO} versus relative power density ρ_{tot} and relative semiconductor chip area $\tilde{A}_{\mathrm{Si,tot}}$ (brackets, mm^2/kW) as a function of the switching frequency f_{sw} (kHz) **(a)**. Relative total volume ρ_{tot}^{-1} versus relative semiconductor chip area $\tilde{A}_{\mathrm{Si,tot}}$ and European efficiency η_{EURO} (brackets, %) as a function of f_{sw} (kHz) **(b)**.

contributions of all passive components as well as the heat sink, whereas **Tab. III** presents the required semiconductor chip area and corresponding losses of the different inverter types and DC networks. Finally, **Tab. IV** and **Tab. V** give an overview of the resulting passive component values of the DC networks and the LCL filter.

1) 2LVSI: although the 2LVSI features the highest power density of all 2-level topologies at 4 kHz, the predicted advantages [13] of a single-stage inverter over inverters including a boost stage could not be confirmed in general. The 2LVSI features an overall efficiency which is lower than for the 2LVSI+BC (**Fig. 6**). This is mainly due to the high DC-link voltages and the slow switching behavior of the employed 1700 V IGBTs, both leading to the highest switching losses γ_{P} of all topologies over the entire frequency range (**Tab. III**). For switching frequencies around approximately $f_{\mathrm{sw}} = 8\,\mathrm{kHz}$, the power density cannot be further increased (**Fig. 6**). On the one hand, this is due to the large required heat sink volumes $\rho_{\mathrm{sink}}^{-1}$ (**Tab. II**). On the other hand, large CM inductors become necessary, which is due to the higher DC-link voltage range $\bar{u}_{\mathrm{PV,H}}$ when compared to the other topologies (**Tab. V**).

2) 2LVSI+BC: despite the additional losses in the boost converter stage (**Tab. II**, **Tab. III**), the 2LVSI+BC features

TABLE IV: Component values (in µH, µF) of the different DC networks for $f_{\mathrm{sw}} = 4\,\mathrm{kHz}$. The values for other switching frequencies can be calculated by multiplication of the values in the table with $\frac{4\,\mathrm{kHz}}{f_{\mathrm{sw}}}$.

	2LVSI	**2LVSI+BC**	**2LZSI**	**3LI+BC**	**3LT+BC**
L_{DC}	-	1576	2 × 860	1576	1576
$C_{\mathrm{DC,1}}$	-	152	589	152	152
$C_{\mathrm{DC,2}}$	555	961	2 × 503	885	885

TABLE V: LCL filter component values (in µH, µF) as a function of the switching frequency f_{sw} (in kHz).

	f_{sw}	L_{boost}	L_{DM}	C_{DM}	L_{CM}	C_{CM}
2LVSI	4	2516	350	37.6	0	0.0
	8	1258	314	18.8	0	0.0
	12	839	303	12.5	208	1.5
	16	629	297	9.4	156	1.1
2LVSI+BC 2LZSI	4	2516	350	37.6	0	0.0
	8	1258	314	18.8	0	0.0
	12	839	303	12.5	0	2.7
	16	629	297	9.4	0	2.0
3LI+BC 3LT+BC	4	1273	144	48.7	0	0.0
	8	637	113	24.4	0	0.0
	12	424	104	16.2	0	0.0
	16	318	99	12.2	0	4.2

significantly lower overall losses when compared to the 2LVSI. This is mainly due to the employed 1200 V IGBTs, which allow for considerably lower switching losses. Note that despite the large DC IGBT and diode chip area (up to 30 % of the total chip area, **Tab. III**), the 2LVSI+BC has the lowest chip area requirement of all considered topologies and frequencies.

3) 2LZSI: due to the same inverter output characteristic, the LCL filter of the 2LZSI and the 2LVSI+BC are identical (**Tab. V**). Furthermore, the components of the boost converter stage and Z-network also require similar total inductances and capacitances (**Tab. IV**) and thus similar volumes (**Tab. II**). Nevertheless, the 2LZSI shows the lowest overall power density over frequency of all examined topologies (**Fig. 6**). This is because of the high switching losses and hence the large required heat sinks. The reason for the excessive switching losses can be found in the functional principle of the ZSI: the boosting shoot through states require one additional switching operation per switching period over the entire fundamental period. On the other hand, generating the sinusoidal output currents requires only a switching operation per switching period over half the fundamental period. Therefore, the resulting effective switching frequency of the 2LZSI becomes three times higher when compared to the 2LVSI or 2LVSI+BC. The large required chip areas (**Tab. III**), however, cannot only be explained by the high switching losses but are also a result of the asymmetric loss distribution. The additional shoot through losses (both switching and conduction losses) only occur in the IGBTs but not in the associated diodes. As modules with a fix ratio between diode and IGBT chip sizes were chosen, this leads to overdimensioned diodes and thus to large $\tilde{A}_{\mathrm{Si,tot}}$.

4) 3LI+BC: the 3LI+BC is more efficient and more compact when compared to the investigated 2-level topologies. The reduction in size is mainly due to the closer approximation of the sinusoidal output voltages as a result of the higher number of voltage levels, which allows for a 40-50 % smaller LCL

filter. For low frequencies, the gain in efficiency is in equal shares due to the decreased semiconductor and filter losses (**Tab. II** and **Tab. III**). Compared to all other topologies, the total losses increase only moderately with higher switching frequencies. This is a result of the employed 600 V IGBT modules, which show a 6 to 7 times better switching behavior than the 1200 V IGBTs. Moreover, only half the DC link voltage applies across the switches. However, despite the lowest total semiconductor losses of all topologies, the required chip area is still comparably high (**Fig. 6(b)**). The reasons for that can be found in the inherent asymmetric loss distribution [14] and the higher relative thermal resistances of the considered I-type IGBT modules when compared to the 2-level sixpacks. The latter could be a result of the different package or chip type of the I-type IGBT modules (**Section III-A**).

5) 3LT+BC: for low frequencies, the overall performance of the 3LT+BC is to a wide extent equivalent to the 3LI+BC: both topologies feature similar volumes as they employ the same boost converter and LCL filter, and the overall efficiency is almost identical (**Fig. 5**). For increasing switching frequencies, the difference of the 3LT+BC to the 3LI+BC in terms of efficiency grows due the lossier 1200 V IGBTs. The most remarkable difference, however, is the significantly lower chip area requirement. On the one hand, this is due to the lower relative thermal resistances $R_{\text{th,js}}$ of the IGBT modules when compared to the 3LT+BC and on the other hand a result of the independent dimensioning of the 600 V and 1200 V semiconductors, which allows for a better chip area utilization.

C. Optimal topologies

The results presented in the foregoing subsection give reason to seeing the 3LT+BC as the optimal topology amongst the selected options and for the given system specifications and constraints. The 3LT+BC represents the best compromise between overall efficiency, size and chip area requirement. In the case that a 2-level topology is preferred since higher importance is assigned to reliability and semiconductor part count, the 2LVS+BC represents the best alternative. It features a relatively high efficiency (especially for low switching frequencies) and has the lowest chip area requirements of all investigated topologies.

VI. Conclusion and Outlook

In this paper, detailed loss, volume and thermal models have been presented, which allow for the dimensioning of the components of selected three-phase PV inverters according to a variety of given constraints. A comparative evaluation of several 2- and 3-level topologies has been performed, which showed the 3LT+BC topology to feature the optimal compromise of efficiency, size and chip area requirement. Furthermore, the investigations identified the high switching losses as the main disadvantage of the considered 2-level topologies.

In a next step, the chosen topologies will be compared for an AC RMS line-to-line grid voltage of 290 V. This will allow for the use of IGBTs with lower voltage ratings and better switching behavior also in the 2-level topologies. Moreover, a model of the cabling effort and ohmic losses on the DC side must be incorporated, as the reduced voltages imply higher PV currents. Finally, the advantages of using SiC active components will be investigated by comparing hardware demonstrators of a SiC equipped 2LVSI+BC against a three-level topology with standard Si components. Moreover, the implemented hardware will also be used to verify the models developed in this paper.

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