



Wide-Band-Gap-Antriebsumrichter Aktuelle Trends und technische Lösungen

Dominik Bortis

Swiss Federal Institute of Technology (ETH) Zurich Power Electronic Systems Laboratory www.pes.ee.ethz.ch

VDE DACH-Fachtagung "Elektromechanische Antriebssysteme 2021"

November 10th, 2021







Wide-Band-Gap-Antriebsumrichter Aktuelle Trends und technische Lösungen

D. Bortis, G. Rohner, J.W. Kolar

Swiss Federal Institute of Technology (ETH) Zurich Power Electronic Systems Laboratory www.pes.ee.ethz.ch

VDE DACH-Fachtagung "Elektromechanische Antriebssysteme 2021"

November 10th, 2021



Power Electronic Systems @ ETH Zurich



18 Ph.D. Students **1** PostDoc **3** Research Fellows

ETH zürich



Centre



VDE -

ETH zürich

Outline

 Introduction
 WBG Trends and Challenges
 Full-Sinewave Filtering Multi-Level Inverter

Filter-Integrated Converter Structures

Conclusions

M. Antivachis J. Azurza M. Haider D. Menzi S. Miric J. Miniböck M. Guacci D. Zhang

VDE -

2/35

Acknowledgement:



3-Ф Variable Speed Drive Inverter Systems

State-of-the-Art Trends and Future Requirements







Variable Speed Drive Inverter Concepts

- **DC-Link Based** OR Matrix-Type AC/AC Converters **Battery OR Fuel-Cell Supply OR Common DC-Bus Concepts**





All Separated \rightarrow Large Installation Space / Complicated / Expert Installation





VSD Inverter - Future Requirements

- "Non-Expert" Installation → Motor-Integrated Inverter OR "Sinus-Inverter"
- Low Losses & Low HF Motor Losses / Low Volume & Weight
- Wide Output Voltage Range / High Output Frequencies (High Speed Motors)





 Main "Enablers" → SiC/GaN Power Semiconductors & Digitalization ("X-Technologies") → Adv. Inverter Topologies & Control Schemes ("X-Concepts")





"X-Technologies" WBG Semiconductors



Source: www.terencemauri.com





Si vs. SiC

- Higher Critical E-Field of SiC \rightarrow Thinner Drift Layer Higher Maximum Junction Temperature $T_{j,max}$



5/35

• Massive Reduction of Relative On-Resistance \rightarrow High Blocking Voltage Unipolar Devices



Si vs. SiC Switching Behavior

Si-IGBT → Const. On-State Voltage Drop / Rel. Low Switching Speed
 SiC-MOSFETs → Resistive On-State Behavior / Factor 10 Higher Sw. Speed



- Extremely High di/dt & dv/dt \rightarrow Challenges in Motor Insulation / Bearing Currents / EMI
- Small Chip Size & Integration ightarrow Challenges in Gate Drive & PCB / Packaging & Thermal Management

ETH zürich



Inverter Output Filters

Full-Sinewave Filtering

_







State-of-the-Art Drive System

- Standard 2-Level Inverter Large Motor Inductance / Low Sw. Frequency
- Shielded Motor Cables / Limited Cable Length / Insulated Bearings / Acoustic Noise



• Line-to-Line Voltage

CM Leakage Current | Motor Surge Voltage | Bearing Current





Output Voltage Filtering

- Measures Ensuring EMI Compliance / Longevity of Motor Insulation & Bearings
 Motor Reactor | dv/dt Filters | DM-Sinus Filters | Full-Sinus Filters



• Small Filter Size \rightarrow High Sw. Frequ. \rightarrow SiC GaN



VDE

3- Φ **650V GaN Inverter System**

Source: YASKAWA

9/35

Comparison of Si-IGBT System (No Filter, f_s=15kHz) & GaN Inverter (LC-Filter, f_s= 100kHz)
 Measurement of Inverter Stage & Overall Drive Losses @ 60Hz



- Sinewave LC Output Filter \rightarrow Corner Frequency $f_c = 34$ kHz
- 2% Higher Efficiency of GaN System Despite LC-Filter (Saving in Motor Losses) !



Multi-Level Inverters

Flying Capacitor Inverter



G. Rohner, S. Miric, D. Bortis, J. W. Kolar, M. Schweizer, *Comparative Evaluation of Overload Capability and Rated Power Efficiency of 200V Si/GaN 7-Level FC 3-Phase Variable Speed Drive Inverter Systems*, Proceedings of the 36th Applied Power Electronics Conference and Exposition (APEC 2021), June 14-17, 2021.





Scaling of Flying Cap. Multi-Level Concepts

- Clear Partitioning of Overall Blocking Voltage \rightarrow Lower Voltage Steps / Lower EMI / Reflections Higher Effective Switching Frequency @ Output $\rightarrow f_{sw,eff} = N \cdot f_{sw}$
- Low Output Inductance & Application of LV Technology to HV



• Scalability / Manufacturability / Standardization / Redundancy





SiC/GaN Figure-of-Merit

- Figure-of-Merit (FOM) Quantifies Conduction & Switching Properties
- FOM Identifies Max. Achievable Efficiency @ Given Sw. Frequ.



- Advantage of LV over HV Power Semiconductors
- Advantage of Multi-Level over 2-Level Converter Topologies
 → Lower Overall On-Resistance @ Given Blocking Voltage

ETH zürich



Motor Integrated 7-Level FC Inverter



- **DC Input Voltage:** •
- **Nominal Operation:** ٠
- **Overload Operation:**
- **Temperature Aluminum (Flange):**

800V 15A_{peak}, 350V_{peak} (7.5kW) 45 A_{peak} for 3s 90°C



- 7-Level Flying Capacitor Inverter enables Usage of 200V Devices (Si or GaN)
- *Nominal Efficiency Target 99% (only Semicond.)*
- \rightarrow # Semicond. Devices

Max. Achievable Switching Freq.

ETH zürich

 \rightarrow Determines Flying Cap. Vol.



Nominal Load Operation

■ 99% at Nom. Load - 7.5 kW → 75W Total Semi. Losses (Only 2.1W per Switch)
 ■ Comparison of best 200V Si and GaN Devices available on the Market



- GaN achieves 2-3 times Higher Switch. Freq. compared to Si for 99% \rightarrow 2-3x lower FC Volume
- Overload Capability \rightarrow 3 x Nominal Load for 3 Seconds

ETH zürich



Overload Operation

- Worst Case Overload Operation at Standstill
- 3 x Torque/Current (45A_{peak}) for 3s

[→] Strongly Increased Semicon. Losses
→ 3 x Flying Cap. Vol. for same FC Voltage Ripple



◆ Conduction Losses dominate Overload Losses → Increase Switching Frequency at Overload
 ◆ 3 x Switching Frequency
 ◆ Flying Cap. designed for Nom. Load

• Max. Junction Temp. (Si: 175°C/ GaN: 150°C) → Proper Cooling Concept needed

ETH zürich

VDE

Cooling Concepts

- Si MOSFET
- GaN (Bottom Side mounted)
- → Cooling Through PCB with Copper Inlay
 → Directly Attached Copper Piece & TIM to Heatsink



Semi. Device PCB TIM Al. Heat-Sink Cu: Via/Inlay

- Inlay for Si & Copper Plate for GaN → Thermal Capacitor & Heat Spreader
 Minimize Th. Contact betw. GaN Device and Cu Plate → Heat Paste, Liquid Gap Filler, Solder Pad
- Determine Thermal Performance

→ Realization & Dynamic Thermal Model

ETH zürich

VDE

Flying Capacitor Cell Realization

Si MOSFET

- \rightarrow Cooling Through PCB with Copper Inlay
- GaN (Bottom Side mounted)
- \rightarrow Directly Attached Copper Piece & TIM to Heatsink







- Inlay for Si & Copper Plate for GaN → Thermal Capacitor & Heat Spreader
 Minimize Th. Contact betw. GaN Device and Cu Plate → Heat Paste, Liquid Gap Filler, Solder Pad
- Determine Thermal Performance

 \rightarrow Realization & Dynamic Thermal Model



Dynamic Thermal Modeling

 $T_{\rm C}$

 $R_{P/T,1}$

PCB/TIM

C_{P/T.1}

Si MOSFET

T

- \rightarrow Cooling Through PCB with Copper Inlay
- GaN (Bottom Side mounted)
- \rightarrow Directly Attached Copper Piece & TIM to Heatsink

Si: IPT111N20NFD (Optimos 3 FD) **Bottom:** $R_{\Theta IB} = 0.4 \text{ K/W}$

 $R_{\text{Semi},1}$ $R_{\text{Semi},2}$

 $C_{\text{Semi},1}$ | $C_{\text{Semi},2}$

Si-MOSFET



R_{P/T,2}

 $C_{P/T,2}$

 T_{HS}



Bottom: $R_{\Theta IB} = 4 \text{ K/W}$





- Inlay for Si & Copper Plate for GaN \rightarrow Thermal Capacitor & Heat Spreader • Minimize Th. Contact betw. GaN Device and Cu Plate \rightarrow Heat Paste, Liquid Gap Filler, Solder Pad
- Determine Thermal Performance

 \rightarrow Realization & Dynamic Thermal Model

ETH zürich

Dynamic Thermal Model Parametrization

- **Empirical Parametrization**
- Junction Temp.
- Case, Cu-Plate & Heat Sink
- → Measure Temp. Profile for different Injected Power Profiles → Electrically with temperature-dependent $R_{ds,on}$ (1ms Rate) → Optically with Thermal Camera (40ms Rate)



- DC Power Injection
- Pulsed Power Injection

- \rightarrow Relation betw. Junction Temp. and $R_{ds.on}$
- \rightarrow Thermal Resitances
- \rightarrow Thermal Capacitances





Dynamic Thermal Model

- Normalized Thermal Step Response \rightarrow Cu-Piece increases Time Constant drastically Similar Dup & Stat. The Polyagian for 1xSi & 2xGaN if Cu. Piece same Dim. as Si Exposed Pad
- Similar Dyn. & Stat. Th. Behavior for 1xSi & 2xGaN if Cu-Piece same Dim. as Si-Exposed Pad



- Initial Small Time Constant
- Afterwards Large Time Constant
- Overload Duration > $4 \cdot \tau_{Semi}$
- → Defined by Device Package ($\tau < 10 \text{ms}$) → Defined by Cooling Concept ($\tau_{\text{Si}} = 0.4 \text{ s}, \tau_{\text{GaN}} = 0.65 \text{ s}$)
- → Equals Continuous Overload (Worst Case)

ETHzürich



- Max. and Min. Junction Temperature within one Electric Period depending on f_{out} Maximum Overload Junction Temperature at Standstill \rightarrow approx. 130°C for Si and GaN



• Immediate Reduction of Th. Cycling at Low Speeds \rightarrow Th. Low-Pass Filter Behavior with $\tau_{\rm Semi}$ • Residual Th. Cycling at High Speeds due to thermal Behavior of Device Package

• Experimental Verification \rightarrow AC Current & Switched 2L-Operation

ETH zürich

Power Electronic Systems

Laboratory



Thermal Cycling vs. Output Frequency (2)

- Switched 2L-Operation
- Junction Temperature Profile
- Injected Losses

- \rightarrow Measurement and Simulation of Case Temperature
- → Determined from Thermal Model
- \rightarrow Calculated from Semiconductor Loss Model



Very Good Agreement between Measured and Simulated Temperature Profiles
 Fast Decay of Thermal Cycling Magnitude with increasing Frequency

ETH zürich

VDE

LC Output Filter with Overload Capability

- Multi-Level Converter
- LC Output Filter mitigate
- ightarrow Small Voltage Steps but still high dv/dt
- \rightarrow CM & Bearing Currents
- \rightarrow EMI Emissions & HF-Machine Losses



• Multi-Level Converters enable

→ Small Filter Volume → Overload Capability (3 x I_{nom}) needed for Filter Inductor





Output Inductor Design

- Ferrite Core Filter Inductor
- \rightarrow Sudden Drop of Permeability around Saturation \rightarrow Magnetic Design for Overload needed
- **Powder Core Filter Inductor**
- \rightarrow Smooth Drop of Permeability till Saturation





 \rightarrow Inverter operated with 3x f_{sw} at Overload Constant Inductor Current Ripple \rightarrow Inductance can drop by x3 at Overload \rightarrow Powder Core Filter Inductor designed for Nominal Load (!)

ETH zürich

Output Inductor Design

Filter Inductor Pareto Optimization for Si 7L FCi



30

- Tiny Filter Inductor for a Nominal 7.5kW Integrated Motor Drive \rightarrow 3-4 x Smaller than Ferrite
- Temperature Increase of 5°C at Overload \rightarrow based on Thermal Capacity

ETH zürich

VDE

Output Inductor Design

Filter Inductor Pareto Optimization for GaN 7L FCi



30

- Tiny Filter Inductor for a Nominal 7.5kW Integrated Motor Drive \rightarrow 3-4 x Smaller than Ferrite
- Temperature Increase of 5°C at Overload \rightarrow based on Thermal Capacity

ETH zürich



VDE

"X-Concepts"

Phase-Modular Buck+Boost Inverter -







Motivation

- General / Wide Applicability
- − Adaption to Load-Dependent Battery | Fuel Cell Supply Voltage − VSDs \rightarrow Wide Output Voltage & Speed Range



No Additional Converter for Voltage Adaption \rightarrow Single-Stage Energy Conversion





Buck-Boost Y–Inverter

Generation of AC-Voltages Using Unipolar Bridge-Legs



Switch-Mode Operation of Buck OR Boost Stage → Single-Stage Energy Conversion (!)
 3-Φ Continuous Sinusoidal Output / Low EMI → No Shielded Cables / No Motor Insul. Stress



DE

Buck-Boost Y–Inverter

• Operating Behavior



ETH zürich



Y–Inverter VSD

- Demonstrator Specifications
- Wide DC Input Voltage Range
- Max. Input Current







- Max. Output Power
- Output Frequency Range
- Output Voltage Ripple

- \rightarrow 6...11 kW
- → 0...500Hz
- → 3.2V Peak @ Output of Add. LC-Filter





Y–Inverter Demonstrator

- 3x SiC (75mΩ)/1200V per Switch
 Sw. Frequency
- IMS Carrying Buck/Boost-Stage Transistors & Comm. Caps & 2nd Filter Ind.

 \rightarrow 100kHz



Dimensions \rightarrow 160 x 110 x 42 mm³





Y–Inverter - Measurement Results

- Transient Operation
- U_{DC} = 400V U_{AC} = 400V_{rms} (Motor Line-to-Line Voltage) f = 50Hz
 - $f_0^{(0)} = 50 \text{Hz}^{(0)}$ $f_s = 100 \text{kHz} / \text{DPWM}$
- $P = 6.5 \mathrm{kW}$



- Dynamic Behavior V-f Control and Load-Step
- Smooth/Sinusoidal Voltage and Current Waveforms



-200 \ -300 \ -400 \ 31/35

100V/div 100V/div

VDE



Three-Phase Integration CSI & DC/DC Front-End







3-Φ Current Source Inverter Topology Derivation

- Y-Inverter → Phase Modules w/ Buck-Stage | Current Link | Boost-Stage
 3-Φ CSI → Buck-Stage V-I-Converter | Current DC-Link DC/AC-Stage



 \rightarrow Single Inductive Component & Utilization of Monolithic Bidirectional GaN Switches







3-Φ Current Source Inverter (CSI)

Bidirectional/Bipolar Switches \rightarrow Positive DC-Side Voltage for Both Directions of Power Flow



• Monolithic Bidir. GaN Switches \rightarrow Factor 4 (!) Red. of Chip Area Comp. to Disc. Realization



33/35

DE

3 D Buck-Boost CSI – Synergetic Control

- "Synergetic" Control of Buck-Stage & CSI Stage
- 6-Pulse-Shaping of DC Current by Buck-Stage \rightarrow Allows Clamping of a CSI-Phase



- Switching of Only 2 of 3 Phase Legs \rightarrow Significant Red. of Sw. Losses (\approx -86% for R-Load) Operation with Phase Shift of AC-Side Voltage & Current possible

ETHzürich

DE









Conclusions

- "X-Technology": SiC / GaN Enable Motor-integrated Drive Systems
- High dv/dt & Thermal Management are Major Challenges
- Continuous / Sinusoidal Output Voltage \rightarrow Full-Sinewave Filters

"X-Concepts": Multi-Level Converters and Integrated Filters

- Low-Voltage Steps & Scaling of Inductor & FOM
- ALL SMD Realization
- ALL SMD Realization
 → Automated Assembly
 → Loss Distribution among many Devices
 → High Overload Capability
- Filtering Recommended

- \rightarrow Automated Assembly
- \rightarrow Powder Core
- Wide Input / Output Voltage Range
- Electromagnetically "Quiet"
- Synergetic Control & Monolithic Bidirectional GaN Switch

System Level \rightarrow Integration of Storage, Distributed DC Bus Systems / Industry 4.0 etc.

ETH zürich





Thank you!







Biography – of the Presenter ——

bortis@lem.ee.ethz.ch



Dominik Bortis received the M.Sc. and Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES.

Since January 2016 Dr. Bortis is heading the research group Advanced Mechatronic Systems at PES, which concentrates on ultra-high speed motors, bearingless drives, linear-rotary actuator and machine concepts with integrated power electronics. Targeted applications include e.g. highly dynamic positioning systems, medical systems, and future mobility concepts. Dr. Bortis has published 90+ scientific papers in international journals and conference proceedings. He has filed 30+ patents and has received 8 IEEE Conference Prize Paper Awards and 2 First Prize Transaction Paper Award.

