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# Experimental Characterization of Silicon and Gallium Nitride 200 V Power Semiconductors for Modular/Multi-Level Converters Using Advanced Measurement Techniques

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***Abstract*— The increasing demand for higher power densities and higher efficiencies in power electronics, driven by the aerospace, electric vehicle and renewable energy industries, encourages the development of new converter concepts. In particular, modular and/or multi-level (M/ML) topologies are employed to break the performance barriers of state-of-the-art power converters by simultaneously reducing the system losses and volume/weight. These improvements mainly originate from the replacement of high voltage transistors, typical of two-level converters, with low voltage, e.g. 200 V, devices, offering superior electric performance. Hence, two low on-state resistance silicon (Si) and gallium nitride (GaN) 200 V power semiconductors are comprehensively characterized in this paper to support the multi-objective optimization and the design of M/ML power converters. First, the selected devices are analyzed experimentally determining their conduction, thermal and switching characteristics; for this purpose, a novel ultra-fast transient calorimetric measurement method is introduced and explained in detail. In the course of this analysis, an unexpected switching loss mechanism is observed in the Si devices at hand; the physical reason of this behavior is clarified and it is proven to be solved in next generation research samples, which are also characterized by measurements. Finally, the influence of the measured power semiconductors performance on the overall efficiency and power density of a typical converter is determined through a case study analyzing a hard switching half-bridge operated as single-phase inverter, i.e. the fundamental building block of several M/ML topologies. It is concluded that, in this voltage and power class, GaN e-FETs are nowadays approximately a factor of three superior to Si Power MOSFETs; however, the better heat dissipation achieved by the latter still makes them the preferred solution for higher power applications.**

***Index Terms*— Silicon versus Gallium Nitride, Low Voltage Power Semiconductors, Transient Calorimetric Measurement Methods, Switching Loss Measurements.**

## I. Introduction

Modern application areas of power electronics define unprecedented requirements in terms of efficiency and volumetric/gravimetric power density. In particular, the established trends towards the electrification of transport generates a strong demand for high power density converters [1], [2] since, e.g. in More Electric Aircraft (MEA) and electric vehicles (EVs), any additional weight reduces the payload capacity and limits the range/mileage. At the same time, the rising share of renewable energies in the electricity generation requires ultra-high efficiency power converters to minimize the losses at the interface between the renewable sources and the distribution grid [3]–[5].

Most of the power electronic systems in the mentioned applications areas perform DC/AC energy conversion, e.g. when tied to the grid or in variable speed drives (VSDs), and have output power ratings typically ranging from several kW (e.g. VSDs [6], EV on-board battery chargers (OBCs) [7]) to few tens of kW (e.g. residential photo-voltaic (PV) installations [5], MEA power systems [8]). In fact, even converters with higher power ratings, i.e. up to hundreds of kW, are preferably realized by interconnecting smaller converters, e.g. rated for few tens of kW [9], [10], since scalable and modular approaches generally enable cost reduction and fault-tolerance, respectively [11]. Moreover, also the DC-link voltages $V_{dc}$ at stake are comparable among these applications; e.g., 540 V and (in the future) 1000 V are typical of DC buses in MEA [10], [12], 400 V and 800 V are the most common voltages of (fully charged) traction batteries in EVs [13], and approximately 400 V and 800 V are obtained from the rectification of single-phase and three-phase grids, and/or are required to feed power to the grid.

Modular and/or multi-level (M/ML) DC/AC power converter topologies are identified as the most prominent approach to meet all the discussed performance targets. In fact, by taking advantage of the superior performance of low-voltage power semiconductors (see **Fig. 1**), M/ML inverters achieve reduced losses in the power stage, resulting in higher efficiencies and downsized heat sinks [5]. Additionally, a high number of voltage levels reduces the filtering

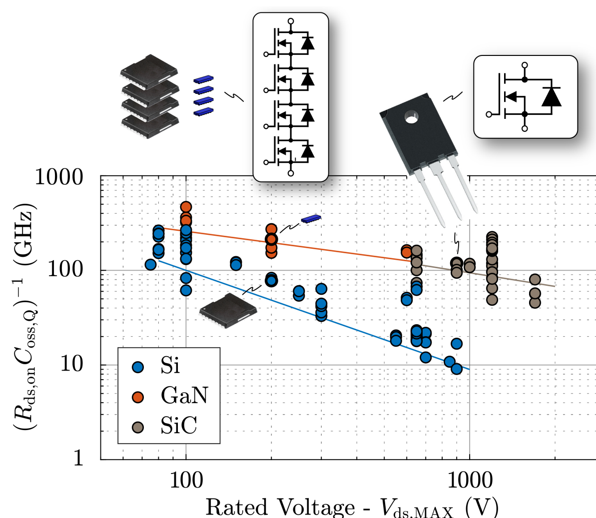


**Fig. 1:** Figure of Merit (FoM) considering conduction losses and hard switching losses of 100+ commercially available silicon (Si, blue), gallium nitride (GaN, red) and silicon carbide (SiC, brown) power devices in dependency of their blocking voltage capability $V_{ds,MAX}$. The monotonic decrease of the FoM with increasing $V_{ds,MAX}$ justifies the interest towards modular and/or multi-level power converters, where several lower voltage devices are typically connected in series to replace and outperform single higher voltage devices.

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effort, i.e. minimizes the volume/weight of the filter components by increasing the effective frequency of the output waveforms and/or by reducing their harmonic content [14] as highlighted in **Fig. 2**, where the structure and the switch node voltage $v_{\mathrm{sw}}$ waveform of a M/ML inverter, i.e. of a five-level Flying Capacitor Converter (FCC), are compared with the ones of a conventional two-level inverter.
The remarkable potential of this class of converters is confirmed in literature; e.g., [3], [5], [10], [15] among others, prove how M/ML approaches with output power ratings up to tens of kW can outperform traditional two-level inverter solutions both in terms of efficiency and power density. Moreover, M/ML converters are already in use in successful products, confirming their market readiness [16].

Virtual prototyping and multi-objective optimization, e.g., in terms of efficiency and power density, are the key enablers to meet the defined performance targets with minimum amount of materials and resources. Accordingly, these concepts are becoming the preferred industry approach to perfect the design of power electronic systems [17]–[19]. The optimization of power converters relies on an accurate performance characterization of every component, i.e., on the derivation of mathematical models which allow to determine the performance of a converter in dependence of its design parameters, e.g., the selected topology, modulation scheme, power semiconductors, switching frequency, etc.
When efficiency and power density are defined as performance indexes, accurate models of the power semiconductors become essential. In fact, the conduction losses of the power stage can have a significant impact on the overall converter efficiency and on the cooling requirements; moreover, determining the optimum switching frequency, which mostly depends on the switching losses and on the thermal performance of the selected power semiconductors, is essential to minimize the size of the passive components.

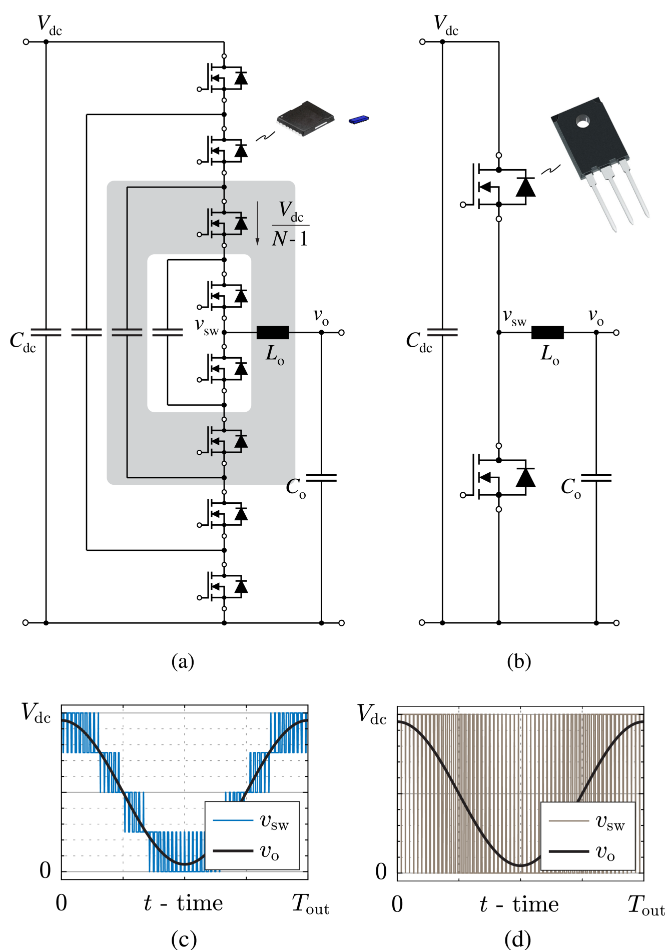


**Fig. 2: (a)** Example of a typical multi-level inverter, i.e. a Flying Capacitor Converter (FCC) with five voltage levels ($N = 5$), realized with the series connection of several ($N-1 = 4$ per side) low voltage power semiconductors, compared to **(b)** a conventional two-level inverter employing two higher voltage devices. The gray area in **(a)** highlights one (out of the $N-1 = 4$) pair of transistors in bridge-leg configuration, i.e. operating with complementary gate signals, forming the FCC. **(c)-(d)** Idealized switch node voltage $v_{\mathrm{sw}}$ and output voltage $v_{\mathrm{o}}$ waveforms associated to the converters shown in **(a)** and **(b)**, respectively, within one AC output period $T_{\mathrm{out}}$.

The first parameter guiding the selection of the most suitable switches for a specific power converter is their blocking voltage rating $V_{\mathrm{ds,MAX}}$, which must fulfill

$$V_{\mathrm{ds,MAX}} \geq V_{\mathrm{ds,0}} = \alpha \frac{V_{\mathrm{dc}}}{f(N)}. \tag{1}$$

In (1), $\alpha$ defines a safety margin, e.g. $\alpha = 1.3$, $V_{\mathrm{dc}}$ is the DC-link voltage of the inverter (see **Fig. 2(a)-(b)**), $N$ indicates the number of voltage levels (e.g., $N = 5$ in **Fig. 2(a)** and $N = 2$ in **Fig. 2(b)**, as visible in **Fig. 2(c)-(d)**, respectively) and $f(N)$ is a function associated to the selected converter topology, e.g. $f(N) = N-1$ for $N$-level FCCs [14] as well as for conventional two-level inverters ($N = 2$). For example, if $V_{\mathrm{dc}} = 540\,\mathrm{V}$, $V_{\mathrm{ds,0}} = 702\,\mathrm{V}$ results from (1) for a two-level inverter ($f(2) = 1$), while $176\,\mathrm{V}$ for a five-level FCC ($f(5) = 4$). Generally, inserting in (1) the mentioned values of $V_{\mathrm{dc}}$ and typical values of $N$, e.g. $3 \leq N \leq 7$, $V_{\mathrm{ds,MAX}} = 200\,\mathrm{V}$ is frequently obtained [5], [10] after rounding the resulting $V_{\mathrm{ds,0}}$ to the closest voltage class of power devices available on the market (see **Fig. 1**). To maximize the power semiconductors performance, it is convenient to select a value of $N$ for which $V_{\mathrm{ds,0}}$ is close to a common voltage class, e.g. $200\,\mathrm{V}$. As shown in **Fig. 1**, $200\,\mathrm{V}$ power semiconductors are nowadays available both in silicon (Si, blue) and gallium nitride (GaN, red) technology.
A practical approach to compare different power semiconductors is based on the analysis of their Figure of Merit (FoM) [20], i.e., a numeric value obtained combining several characteristics of a device, appropriately selected to represent its performance. The FoM calculated as $1/(R_{\mathrm{ds,on}} C_{\mathrm{oss,Q}})$ [21] is considered as a good indicator of the performance of hard switching power stages, typical for M/ML topologies. In this FoM, $R_{\mathrm{ds,on}}$ and $C_{\mathrm{oss,Q}}$ are the on-state resistance and the charge related parasitic output capacitance of a power semiconductor, respectively. **Fig. 1** depicts this FoM for several Si, GaN and silicon carbide (SiC) power semiconductors in dependency of their $V_{\mathrm{ds,MAX}}$. The monotonic decrease of the FoM with increasing $V_{\mathrm{ds,MAX}}$ justifies the interest in M/ML converters. However, for $V_{\mathrm{ds,MAX}} \leq 200\,\mathrm{V}$, the FoM of GaN and Si are too similar to constitute a reliable performance metric. Additionally, the considered FoM does not include aspects determining the performance of a power device besides $R_{\mathrm{ds,on}}$ and $C_{\mathrm{oss,Q}}$, e.g., temperature dependent conduction losses, heat dissipation capability, current dependent switching losses, etc. Accordingly, even though GaN and Si $200\,\mathrm{V}$ power semiconductors are nowadays successfully employed in M/ML converters, an accurate evaluation of their performance, facilitating the optimization of the design parameters and the selection of the most suitable semiconductor technology in each specific application, is not yet available.

For all the above mentioned reasons, this paper aims to comprehen-

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sively characterize, by experimental measurements, the performance of selected best-in-class 200 V power semiconductors. The results of this analysis, while also serving for a more general comparison between GaN and Si devices, provide accurate models to support the multi-objective optimization of M/ML power converters, i.e. to facilitate the achievement of the stringent performance targets defined by the aerospace, EV and renewable energy industries. Moreover, a guideline for the power semiconductor industry is provided by highlighting how each characteristic of the considered devices, e.g. the value of $R_{\mathrm{ds,on}}$, affects the overall converter performance, i.e. it results evident where improvements at the device level are nowadays most required.

Considering the increasing power (and thus current) demand in the mentioned application areas, the interest in ultra-high efficiency converters and the fact that several devices are often connected in series on the path of the load current in M/ML topologies (see **Fig. 2(a)**), this study focuses on the power semiconductors offering the lowest value of $R_{\mathrm{ds,on}}$ in the 200 V voltage class, corresponding to $R_{\mathrm{ds,on}} \approx 10\,\mathrm{m\Omega}$.

The employed measurement setups, designed hardware prototypes and selected power semiconductors are introduced in **Section II**. Their conduction, thermal and switching performance are separately evaluated in **Sections III**, **IV** and **V**, respectively. To perform accurate switching loss measurements, a novel ultra-fast transient calorimetric measurement method, based on the observation of the thermal dynamics of the case temperatures of the investigated devices, is additionally introduced in **Section V**. An anomaly observed in the switching behavior of the Si devices at hand is explained and experimentally proven to be solved in **Section VI**. Thereafter, the obtained data are combined in **Section VII** to quantify the performance limits of a basic power converter, which is identified as the fundamental building block of several M/ML topologies, in dependence of the selected power semiconductors. **Section VIII** concludes the paper. Finally, in the **Appendix**, an overview of different switching loss measurement methods is compiled, before providing more details on the novel measurement procedure.

## II. Devices-under-Test and Measurement Setup

The state-of-the-art Si and GaN 200 V power semiconductors with the lowest value of $R_{\mathrm{ds,on}}$ on the market are the IPT111N20NFD OptiMOS 3 Fast Diode (FD) Si Power MOSFET [22] and the EPC 2047 GaN e-FET [23]. For the reasons described in **Section I**, these two switches, whose nominal characteristics are listed in **Table I**, are considered as the best candidates for the performance evaluation described in this paper. Additionally, since these benchmark devices feature similar characteristics (same voltage rating and same nominal $R_{\mathrm{ds,on}}$ value), they offer the opportunity to fairly compare, in more general terms, GaN e-FETs against Si Power MOSFETs.

In the next sections, the performance of the selected power semiconductors, named hereafter Devices-Under-Test (DUT), are experimentally verified in the setup schematically illustrated in **Fig. 3(a)**, mainly consisting of two DUT, $\mathrm{T_h}$ and $\mathrm{T_l}$, in bridge-leg configuration, mounted on a heat sink. In this measurement setup, the waveforms of the voltage across and of the current flowing through the DUT can be easily adjusted in open-loop control; additionally, by modifying the network connected at the switch node and/or the value of the load resistor $R_{\mathrm{o}}$ (see **Fig. 3(a)**), a comprehensive characterization of the thermal, conduction and switching performance of the DUT is enabled for different operating conditions, regardless of their final application.

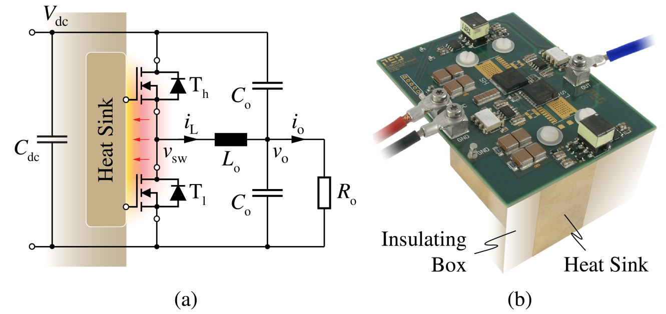


**Fig. 3:** **(a)** Circuit schematic of the measurement setup consisting of two switches, $\mathrm{T_h}$ and $\mathrm{T_l}$, in bridge-leg configuration, the DC-link/commutation capacitor $C_{\mathrm{dc}}$, the symmetric $L$-$C$ output filter formed by the output inductor $L_{\mathrm{o}}$ and the output capacitors $C_{\mathrm{o}}$, and the load resistor $R_{\mathrm{o}}$. **(b)** Realization of the power stage shown in **(a)** on a printed circuit board (PCB) for the OptiMOS 3 FD. The PCB is mounted on a brass heat sink, which is closely thermally coupled with, but electrically isolated from, the power semiconductors.

The hardware realizations of the setup are shown in **Fig. 4** and **Fig. 5** for the OptiMOS 3 FD (Si Power MOSFET) and for the EPC 2047 (GaN e-FET), respectively, highlighting the most significant components soldered on the relative printed circuit boards (PCBs).

## III. Conduction Performance Evaluation

The selection of the optimum power semiconductors for a specific power converter is often driven by the estimated conduction losses. Hence, the conduction performance of the DUT are evaluated in this section by characterizing their $R_{\mathrm{ds,on}}$ in dependence of their junction temperature $T_{\mathrm{j}}$. To perform these measurements, different DC current values $I_{\mathrm{dc}}$ are impressed through $\mathrm{T_h}$ and $\mathrm{T_l}$ (see **Figs. 3(a)**, **4** and **5**) permanently kept in on-state, while the voltage $v_{\mathrm{ds}}$ across them and their case temperatures $T_{\mathrm{c}}$ are accurately measured. Afterwards, $R_{\mathrm{ds,on}}$ is calculated as $v_{\mathrm{ds}}/I_{\mathrm{dc}}$ and $T_{\mathrm{j}}$ is determined using $T_{\mathrm{c}} + R_{\mathrm{th,j\text{-}c}} R_{\mathrm{ds,on}} I_{\mathrm{dc}}^2$, where $R_{\mathrm{th,j\text{-}c}}$ indicates the thermal resistance between the junction and the case of the DUT (specified in their datasheets [22], [23]).

The obtained results (average between $\mathrm{T_h}$ and $\mathrm{T_l}$) are summarized in **Fig. 6** for both OptiMOS 3 FD (blue) and EPC 2047 (red), comparing the measured values of $R_{\mathrm{ds,on}}$ (solid and dots) with their datasheet (shaded) counterparts (typical and worst case). A very good matching between measured and nominal values is generally observed. For the OptiMOS 3 FD, a discrepancy only appears for high values of $T_{\mathrm{j}}$ and it is attributed to an unclear definition of $T_{\mathrm{c}}$ in the datasheet [22]. For the EPC 2047, instead, the measured curve is consistently at the boundary defined by the worst case curve reported in the datasheet [23].

Even if the EPC 2047 outperforms the OptiMOS 3 FD under static conditions, it cannot be inferred that the EPC 2047 would as well offer superior conduction performance in a real power converter. In fact, GaN e-FETs typically suffer from the dynamic $R_{\mathrm{ds,on}}$ phenomenon [25]; this effect is responsible for increasing, in switched applications, the value of $R_{\mathrm{ds,on}}$ measured in DC conditions by a factor $k_{\mathrm{dyn}}$, which mainly depends on the voltage blocked by the transistor in off-state $V_{\mathrm{dc}}$ and on its switching frequency $f_{\mathrm{sw}}$. If $k_{\mathrm{dyn}}(V_{\mathrm{dc}} = 120\,\mathrm{V}, f_{\mathrm{sw}} = 100\,\mathrm{kHz}) = 0.39$, i.e. a $39\,\%$ increase of $R_{\mathrm{ds,on}}$, is considered as an example [25], the measured (solid and dots) values of $R_{\mathrm{ds,on}}$ for the EPC 2047 can be scaled accordingly, resulting in worse conduction performance, as highlighted in **Fig. 6** (dashed). In general, while the information about $R_{\mathrm{ds,on}}$ provided in the datasheets of Si MOSFETs can be sufficiently accurate, it is necessary, instead, to experimentally characterize the dynamic $R_{\mathrm{ds,on}}$ phenomenon of each

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**TABLE I:** Nominal characteristics of the IPT111N20NFD OptiMOS 3 Fast Diode (FD) Si Power MOSFET [22] and of the EPC2047 GaN e-FET [23].

| Power Semiconductor Manufacturer | Model | $V_{ds,MAX}$ | $I_{ds,MAX}$ @ 25 °C | $R_{ds,on}$ @ 25 - 150 °C | $C_{oss,Q}$ @ 120 V | $C_{rss,Q}$ | $(R_{ds,on}C_{oss,Q})^{-1}$ @ 25 °C - 120 V | Chip Area | Package Area | Unitary Price [24] |
|---|---|---|---|---|---|---|---|---|---|---|
| *Infineon Tech.* | OptiMOS 3 FD | 200 V | 96 A | 9 - 26 mΩ | 1430 pF | 49 pF | 77 GHz | 29 mm² | 116 mm² | 7.59 CHF |
| *EPC Co.* | EPC 2047 | 200 V | 32 A | 7 - 12 mΩ | 540 pF | 16 pF | 265 GHz | 7 mm² | 7 mm² | 8.42 CHF |

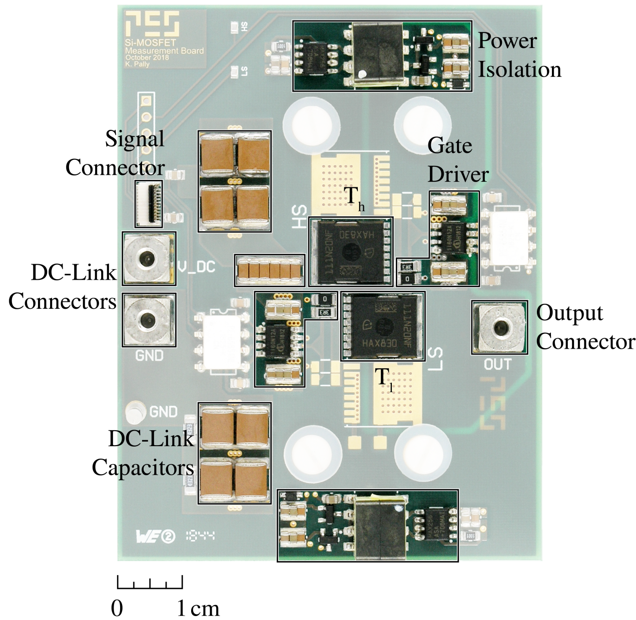


**Fig. 4:** Employed realization of the measurement setup designed to evaluate the performance of the IPT111N20NFD OptiMOS 3 Fast Diode (FD) Si Power MOSFET [22] on a PCB. The setup is formed by two DUT, $T_h$ and $T_l$, in bridge-leg configuration, the respective gate drivers [27] with isolated signal transmission and isolated power supply, and the DC-link/commutation capacitor $C_{dc}$ [28]. The DC input voltage source $V_{dc}$, the symmetric $L$-$C$ output filter and the load resistor $R_o$ are connected to the PCB through screw connectors. The control board providing the switching state information is connected through the signal connector.

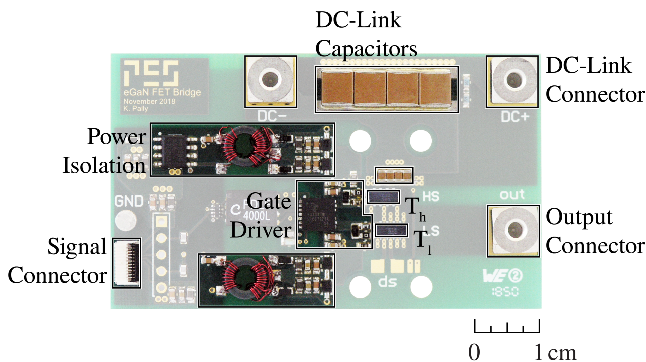


**Fig. 5:** Employed realization of the measurement setup designed to evaluate the performance of the EPC 2047 GaN e-FET [23] on a PCB. The setup is formed by two DUT, $T_h$ and $T_l$, in bridge-leg configuration, the half-bridge gate driver [29] with isolated signal transmission and isolated power supply, and the DC-link/commutation capacitor $C_{dc}$ [28].

GaN e-FET individually [26].

Nevertheless, it can be concluded that, at least for $f_{sw}$ in the hundreds of kHz range, OptiMOS 3 FD and EPC 2047 offer comparable conduction performance, as initially expected and desired.

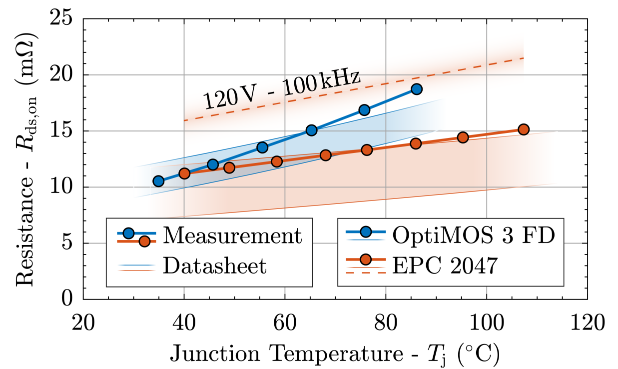


**Fig. 6:** Measured (solid and dots) and datasheet (shaded, typical and worst case) values of $R_{ds,on}$ in dependency of the junction temperature $T_j$ for the OptiMOS 3 FD (blue) and for the EPC 2047 (red). Additionally, estimated (dashed) values of $R_{ds,on}$ for the EPC 2047, considering the impact of the dynamic $R_{ds,on}$ phenomenon for a blocking voltage $V_{dc}$ = 120 V and a switching frequency $f_{sw}$ = 100 kHz [25]. Depending on the influence of the dynamic $R_{ds,on}$ phenomenon, the EPC 2047 can offer either consistently better or worse conduction performance compared to the OptiMOS 3 FD. The influence on $R_{ds,on}$ of the different DC current values $I_{dc}$, selected to perform the measurements, is neglected since the considered values of $I_{dc}$ ensure operation in the deep linear region for both DUT.

## IV. Thermal Performance Evaluation

The volume/weight reduction of power converters, strongly demanded in the mentioned application areas, inevitably implies higher loss densities. Accordingly, the precise understanding of the thermal characteristics of every component in the power stage becomes fundamental. Despite this, the thermal parameters of the power semiconductors indicated in their datasheets are often of no use. Accordingly, their thermal performance must be experimentally characterized, e.g., like it is done for the DUT in this section.

In a setup similar to the one described in **Section III**, different DC power values $P_T$ are injected in $T_h$ and $T_l$ (see **Figs. 3(a)**, **4** and **5**), while $T_c$ is measured and the heat sink temperature $T_{hs}$ is maintained constant. After calculating $T_j$, the measured values of $P_T$ (average between $T_h$ and $T_l$) are plotted in **Fig. 7** for both OptiMOS 3 FD (blue) and EPC 2047 (red). The curves are linear as expected and their slope yields the thermal resistance $R_{th,j\text{-}hs} = R_{th,j\text{-}c} + R_{th,c\text{-}hs}$ between the junction of the DUT and the heat sink (see **Table II**).

The absolute values of $R_{th,j\text{-}hs}$ are strictly dependent on the geometries and on the thermal properties of the setup, e.g. on the design of the heat sink and on the selected thermal interface material [30]. However, since an optimized heat sink structure is considered for both DUT for the sake of a fair comparison, generally valid conclusions can be drawn. The package of the OptiMOS 3 FD features a heat-slug pad on the bottom side enhancing the performance of bottom side cooling concepts. Additionally, if several vias are placed in correspondence of this pad, the heat transfer through the PCB can be maximized. The package of the EPC 2047, instead, features a very dense footprint and a small size; moreover, several components must

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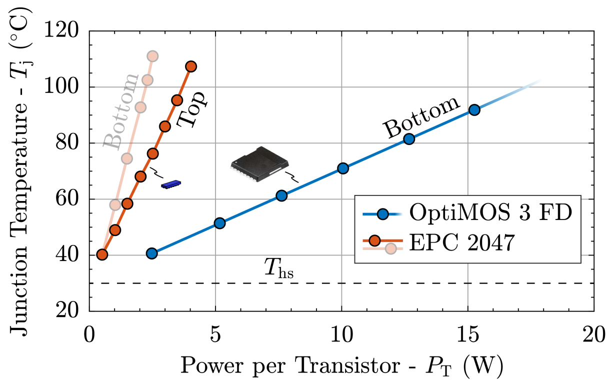


**Fig. 7:** Measured (solid and dots) values of $T_j$ in dependency of the dissipated power $P_T$ for the OptiMOS 3 FD (blue) and for the EPC 2047 (red), for a constant heat sink temperature $T_{hs} = 30\,°C$ (dashed). The two red curves are associated to bottom side (through the PCB) and top side (through the package) cooling of the EPC 2047. Since a lower thermal resistance $R_{th,j\text{-}hs}$ between the junction of the DUT and the heat sink is achieved with top side cooling, this solution is preferred.

be placed nearby the GaN e-FETs to minimize parasitic inductances and capacitances in the power stage, i.e. to improve their switching performance, given the higher switching speeds. Hence, for the EPC 2047, no space is available for vias and top side cooling concepts are preferable, as highlighted in **Fig. 7**. Simultaneous top and bottom side cooling would in both cases improve the thermal performance, but as well result in unpractical heat sink designs. Nevertheless, because of its larger chip area and package, approximately 5 times more power can be dissipated (a 5 times lower value of $R_{th,j\text{-}hs}$ can be achieved) for the same $T_j$ and $T_{hs}$ by the OptiMOS 3 FD compared to the EPC 2047.

This result justifies in part the significantly different current ratings $I_{ds,MAX}$ indicated in the datasheets of the DUT (see **Table I**) and constitutes a limitation for the EPC 2047. In fact, although several GaN e-FETs can be connected in parallel in the same PCB area occupied by a single OptiMOS 3 FD to increase the overall $I_{ds,MAX}$, additional switching losses and new challenges, related to the parallelization of fast switching power semiconductors, arise simultaneously [31].

## V. Switching Performance Evaluation

Selecting the optimum switching frequency of a specific power converter requires a comprehensive switching loss map of the employed power devices. Unfortunately, the switching loss data reported in the datasheets of power semiconductors (when present at all) are generally incomplete [22], [23]. Moreover, the design of the power stage, e.g. the selected components (gate driver integrated circuit (IC), commutation capacitors, etc.) and their placement, strongly influences the switching behavior of the power devices. Hence, similarly to the case discussed in **Section IV**, meaningful switching loss data can only be obtained experimentally, e.g. by following the procedure described in this section.

### A. Measurement Setup

To measure the switching losses of the DUT, the setups of **Fig. 4** and **Fig. 5** are complemented by connecting the DC voltage source $V_{dc}$ and, optionally, the symmetric $L$-$C$ output filter formed by the output inductor $L_o$ and the output capacitors $C_o$, and $R_o$, as indicated in **Fig. 3(a)**. Hence, these setups are operated with constant switching frequency $f_{sw}$, dead-time $t_{dt}$ and duty-cycle $d$, such that the switch node voltage $v_{sw}$ results in a rectangular waveform and, when the $L$-$C$ output filter is connected, the DC output voltage is $v_o = d\,V_{dc}$. $V_{dc}$ is fixed, e.g. $V_{dc} = 120\,V$, to characterize the switching performance of the DUT at the voltage level of interest; $f_{sw}$ is varied (between hundreds of kHz and 1 MHz) to maximize the switching losses with respect to other frequency independent losses, i.e. to increase the sensitivity of the switching loss measurements [32]; $t_{dt}$ is adjusted depending on $I_{sw}$ to minimize the reverse conduction losses [33]. Finally, the configuration of the output network is modified to vary the inductor current $i_L$, therefore both the switched current $I_{sw}$ and the operating mode of the setup, as described in the following:

- *Zero Current Switching (ZCS)*: the switch node is left open, i.e. the $L$-$C$ output filter is not connected, forcing $i_L = I_{sw} = 0\,A$.
- *Soft Switching - Zero Voltage Switching (ZVS)*: the symmetric $L$-$C$ output filter is connected to the switch node to obtain Triangular Current Mode (TCM) operation and ZVS conditions. In this case, $I_{sw}$ corresponds to the positive and negative peaks of $i_L$, and can be calculated as
$$I_{sw} = \pm \frac{V_{dc}\,d(1-d)}{2\,L_o\,f_{sw}} = \pm \frac{V_{dc}}{8\,L_o\,f_{sw}} \qquad (2)$$
if $d = 0.5$. The desired value of $I_{sw}$ is obtained adjusting the value of $L_o$, typically between hundreds of nH and few µH.
- *Hard Switching (HS)*: $R_o$ is connected to the output node of the symmetric $L$-$C$ output filter to obtain Continuous Conduction Mode (CCM) operation and HS conditions. A sufficiently large value is selected for $L_o$ (typically in the hundreds of µH range) to minimize the ripple on $i_L$, while the value of $R_o$ is adjusted to achieve the desired and approximately constant
$$I_{sw} = \frac{d\,V_{dc}}{R_o}\,. \qquad (3)$$
To equally share the conduction losses between $T_h$ and $T_l$, $d$ could be fixed to 0.5 also in this case. However, when the setup is operated in CCM, the majority of the switching losses occur in $T_h$, which is HS (being $I_{sw} > 0$). Hence, by utilizing the degree of freedom given by $d$, the major fraction of the conduction losses can be shifted to $T_l$, thus redistributing the total losses between $T_h$ and $T_l$ and equalizing their $T_j$; by doing so, the maximum measurable losses are increased.

Both in ZVS and HS conditions, the maximum value of $I_{sw}$ is reached once the conduction losses dominate the total losses (accuracy limit [32]) and/or when $T_j$ cannot be anymore limited below 100 °C (thermal limit).

### B. Measurement Methods

Operating the described setups in the above mentioned conditions, the switching losses of both DUT are measured calorimetrically. For this purpose, a thermal equivalent circuit of the measurement setup is first derived and calibrated determining the values of its parameters. Hence, once the thermal model of the setup is obtained, calorimetric loss measurements are performed continuously operating the setup in the conditions of interest and estimating the occurring losses by matching measured and modeled (through the thermal equivalent circuit) thermal quantities, e.g. temperature variations. Finally, the switching losses are calculated from the results of the calorimetric loss measurements. The following analysis focuses only on the calorimetric measurement of semiconductor losses; different solutions to separate the switching losses from the measured losses (which, e.g., include the conduction losses) are discussed in [33].

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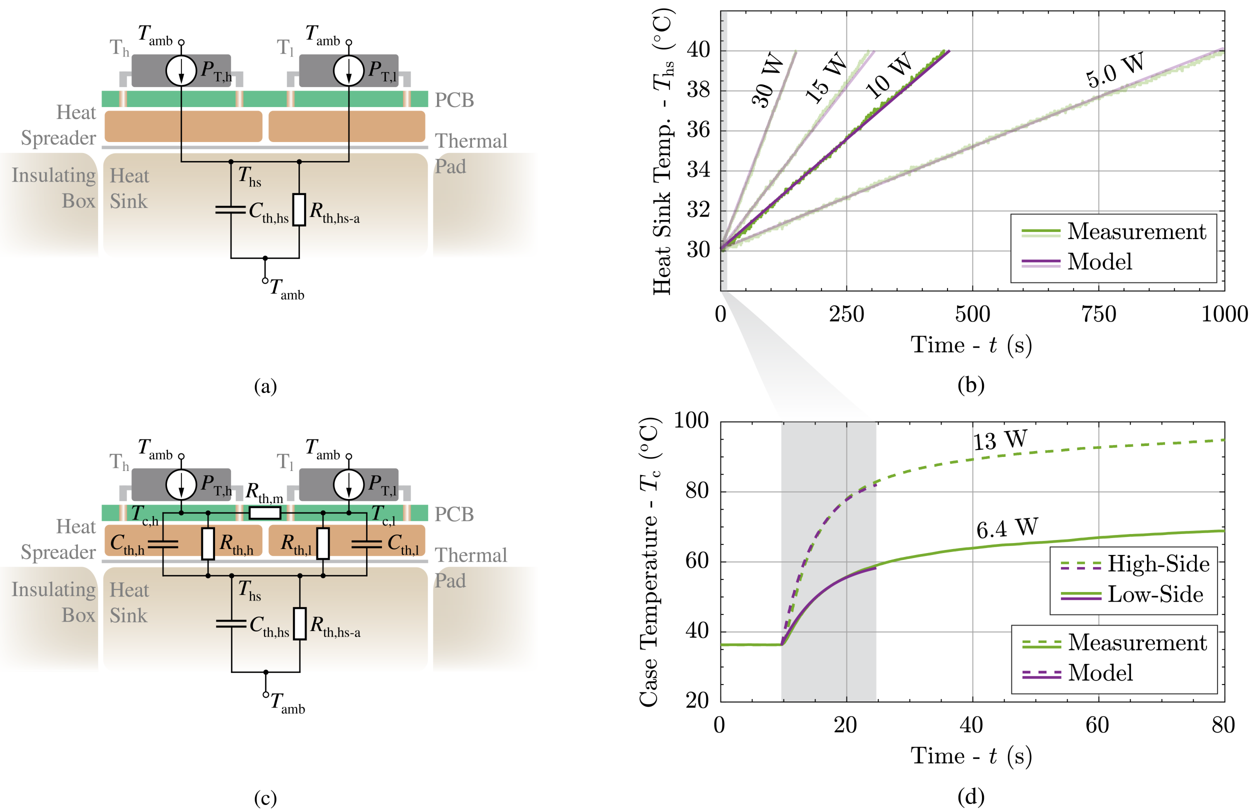


**Fig. 8: (a)** Thermal equivalent circuit of the switching loss measurement setups considered to apply the $T_{hs}$-based transient calorimetric measurement method. The equivalent circuit contains the heat sources $P_{T,h}$ and $P_{T,l}$ indicating the individual semiconductor losses, the thermal capacitance $C_{th,hs}$ of the heat sink connected to $T_h$ and $T_l$, and the thermal resistance $R_{th,hs\text{-}a}$ between the heat sink and the ambient; $T_{amb}$ indicates the ambient temperature. **(b)** Measured (green) and modeled (purple) waveforms of the heat sink temperature $T_{hs}$ for different values of the total semiconductor losses $P_{T,tot}$, for the measurement setup shown in **Fig. 4**. A variation of $T_{hs}$ from 30 °C to 40 °C defines the duration of each measurement, function of $P_{T,tot}$. **(c)** Thermal equivalent circuit of the switching loss measurement setups considered to apply the $T_c$-based transient calorimetric measurement method. The equivalent circuit contains, in addition to the elements described in **(a)**, the thermal capacitances $C_{th,h}$ and $C_{th,l}$ of the case of $T_h$ and $T_l$, and the resistive Π network formed by $R_{th,h}$, $R_{th,l}$ and $R_{th,m}$. $R_{th,h}$ and $R_{th,l}$ indicate the thermal resistance between the heat sink and the case of $T_h$ and $T_l$, respectively, while $R_{th,m}$ models the thermal coupling between $T_h$ and $T_l$. **(d)** Measured (green) and modeled (purple) waveforms of the case temperatures $T_{c,h}$ (dashed) and $T_{c,l}$ (solid) for different values of $P_{T,h}$ and $P_{T,l}$, for the measurement setup shown in **Fig. 9(a)**. In this case, the measurement time is fixed to 15 s.

Two different transient calorimetric measurement approaches are considered in this work, in particular:

- *$T_{hs}$-based Transient Calorimetric Measurement Method*: A transient calorimetric measurement procedure, based on the analysis of the rise of $T_{hs}$ over time, is originally presented in [34] and successfully adopted in [33], [35]–[37]. The associated thermal equivalent circuit, derived for the measurement setups shown in **Fig. 4** and **Fig. 5**, is illustrated in **Fig. 8(a)**. Since this approach considers the thermal dynamics of $T_{hs}$, only $C_{th,hs}$, i.e. the thermal capacitance of the heat sink connected to $T_h$ and $T_l$, and $R_{th,hs\text{-}a}$, i.e. the thermal resistance between the heat sink and the ambient, mainly provided by the thermal insulating box surrounding the setups (see **Fig. 3(b)**), are included in the equivalent circuit (see **Fig. 8(a)**).
The variation of $T_{hs}$ as a consequence of the total semiconductor losses $P_{T,tot} = P_{T,h} + P_{T,l}$ (with $P_{T,h}$ and $P_{T,l}$ indicating the individual semiconductor losses) occurring in the setup, can be directly calculated from the derived thermal model [33], [36], once the values of its parameters are known (see **Table II**). Accordingly, an unknown value of $P_{T,tot}$ can be estimated fitting the step response of the calibrated model to the measured variation of $T_{hs}$. As an example, measured (green) and modeled (purple) waveforms of $T_{hs}$ for different values of $P_{T,tot}$ are depicted in **Fig. 8(b)**, for the measurement setup shown in **Fig. 4**. The matching between the two set of curves guarantees accurate estimations of $P_{T,tot}$.
Nevertheless, possible improvements to this method could address the reduction of the measurement times [38] and the simplification of the measurement setup, which requires a dedicated heat sink. Following the guideline proposed in [35], in fact, several (up to twenty) minutes are necessary to characterize a single operating point, not only because of the recommended lower boundary of the measurement times (necessary to ensure a satisfactory accuracy), but as well because of the time required for the heat sink to cool down after each measurement. Differently, shorter measurement times are achieved in [34], but additional components are still necessary.
- *Novel Ultra-Fast $T_c$-based Transient Calorimetric Measurement Method*: If the transient behavior of $T_c$, rather than the one of $T_{hs}$, could be characterized, much shorter thermal time constants would be involved in the measurement procedure and no customized heat sink would be required. With this aim, the thermal equivalent circuit of the measurement setups shown in **Fig. 4** and **Fig. 5** is extended as illustrated in **Fig. 8(c)** [34]. This thermal model additionally includes the thermal capacitances $C_{th,h}$ and $C_{th,l}$ of the

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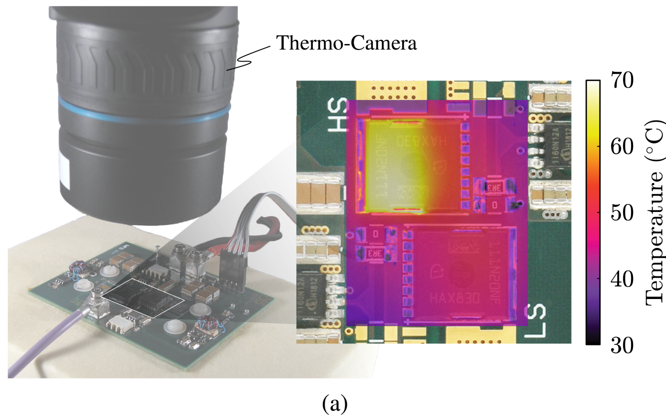


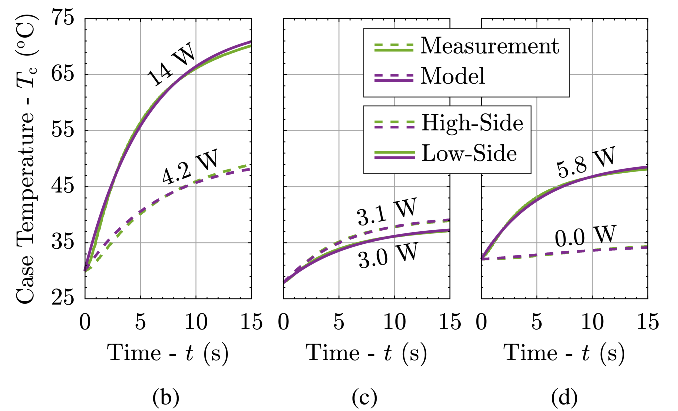


(a) (b) (c) (d)

**Fig. 9:** **(a)** Photo of the measurement setup highlighting the high frame rate high resolution infrared thermo-camera with a frame captured during a measurement. **(b)**-**(d)** Measured (green) and modeled (purple) waveforms of the case temperatures $T_{c,h}$ (dashed) and $T_{c,l}$ (solid) for different values of the individual semiconductor losses $P_{T,h}$ and $P_{T,l}$.

**TABLE II:** Parameters of the thermal equivalent circuit considered to perform the switching loss measurements of the OptiMOS 3 FD Si Power MOSFET and of the EPC 2047 GaN e-FET according to the $T_{hs}$-based transient calorimetric measurement method.

| Power Semiconductor Manufacturer | Model | $R_{th,j\text{-}c}$ (K/W) | $R_{th,c\text{-}hs}$ (K/W) | $C_{th,hs}$ (J/K) | $R_{th,hs\text{-}amb}$ (K/W) |
|---|---|---|---|---|---|
| *Infineon Tech.* | OptiMOS 3 FD | 0.4 | 3.6 | 460 | 32 |
| *EPC Co.* | EPC2047 | 0.8 | 18 | 229 | 23 |

**TABLE III:** Parameters of the thermal equivalent circuit considered to perform the switching loss measurements of the OptiMOS 3 FD Si Power MOSFET according to the novel ultra-fast $T_c$-based transient calorimetric measurement method.

| | Description | Value |
|---|---|---|
| $R_{th,h}$ | $R_{th,c\text{-}hs}$ of $T_h$ | 3.9 K/W |
| $R_{th,l}$ | $R_{th,c\text{-}hs}$ of $T_l$ | 3.3 K/W |
| $R_{th,m}$ | | 30 K/W |
| $C_{th,h}$ | $C_{th,c}$ of $T_h$ | 1.5 J/K |
| $C_{th,l}$ | $C_{th,c}$ of $T_l$ | 1.8 J/K |
| $C_{th,hs}$ | | 393 J/K |
| $R_{th,hs\text{-}a}$ | | $\infty$ |

case of $T_h$ and $T_l$, and the resistive $\Pi$ network formed by $R_{th,h}$, $R_{th,l}$ and $R_{th,m}$. $R_{th,h}$ and $R_{th,l}$ indicate the thermal resistance between the heat sink and the case of $T_h$ and $T_l$, respectively, while $R_{th,m}$ models the thermal coupling between $T_h$ and $T_l$. The parameters of this thermal equivalent circuit (see **Fig. 8(c)**), resulting from the calibration of the measurement setup shown in **Fig. 4**, are listed in **Table III**.

From this equivalent circuit, a system of first-order linear ordinary differential equations (ODEs) describing the evolution of the case temperatures $T_{c,h}$ and $T_{c,l}$ over time can be derived (see the **Appendix**). Hence, the variation of $T_{c,h}$ and $T_{c,l}$ for given values of $P_{T,h}$ and $P_{T,l}$ can be calculated from (8), as well as unknown values of $P_{T,h}$ and $P_{T,l}$ can be estimated from the fitting on the measured variation of $T_{c,h}$ and $T_{c,l}$. Accordingly, measured (green) and modeled (purple) waveforms of $T_{c,h}$ (dashed) and $T_{c,l}$ (solid) for different values of $P_{T,h}$ and $P_{T,l}$ are depicted in **Fig. 8(d)** and in **Figs. 9(b)-(d)**, for the measurement setup shown in **Fig. 9(a)**.

In this case, the measurement time (gray in **Fig. 8(d)**) is fixed to 15 s (from time $t = 10$ s, i.e. when the setup starts to operate, to $t = 25$ s in **Fig. 8(d)**), since this is sufficient to capture the transient behavior of $T_c$. In fact, approximately for $t > 30$ s, the variation of $T_c$ is only determined by the variation of $T_{hs}$ (cf. **Fig. 8(b)** and **Fig. 8(d)**). Hence, significantly shorter measurement times, compared to the $T_{hs}$-based method, can be achieved. In the time window defined by the selected measurement time (which corresponds to the time window on which the fitting algorithm for determining the parameters of the thermal model is applied), the matching between measured and modeled curves is remarkable, hence accurate estimations of $P_{T,tot}$, as well as of $P_{T,h}$ and $P_{T,l}$, are expected.

More details about this measurement procedure are provided in the **Appendix**.

### C. Measurement Results

The switching losses of both DUT, measured according to the $T_{hs}$-based transient calorimetric measurement method described in **Section V-B**, are summarized in **Fig. 10(a)** where they are plotted in the form of the switching energy $E_{sw}$ dissipated by the entire half-bridge in one switching transition, in dependency of $I_{sw}$; positive and negative values of $I_{sw}$ along the x-axes correspond to HS and ZVS conditions, respectively. Even though these results are collected operating the measurement setups as DC/DC converters in electrical steady-state, once the relation between $E_{sw}$ and $I_{sw}$ is determined, also the expected switching losses in different operating conditions can be readily estimated by summing the switching losses occurring in each switching period, obtained considering different switched current values in **Fig. 10(a)**.

Observing the results related to the OptiMOS 3 FD, it is evident how the measured values of $E_{sw}$ in ZVS conditions are much (between 15 and 20 times) smaller than their HS counterparts for the same values of $I_{sw}$. Comparing the two DUT instead, the measured values of $E_{sw}$ in HS conditions result as significantly (between 3 and 6 times) smaller for the EPC 2047 (red), which accordingly outperforms the OptiMOS 3 FD (blue). However, the range of admissible $I_{sw}$ of the EPC 2047 is reduced due to its inferior power dissipation capability. Although the measured values of $E_{sw}$ significantly depends on the design of the power stage and of the gate driver, both setups are optimized to achieve the best switching performance, hence enabling a direct comparison.

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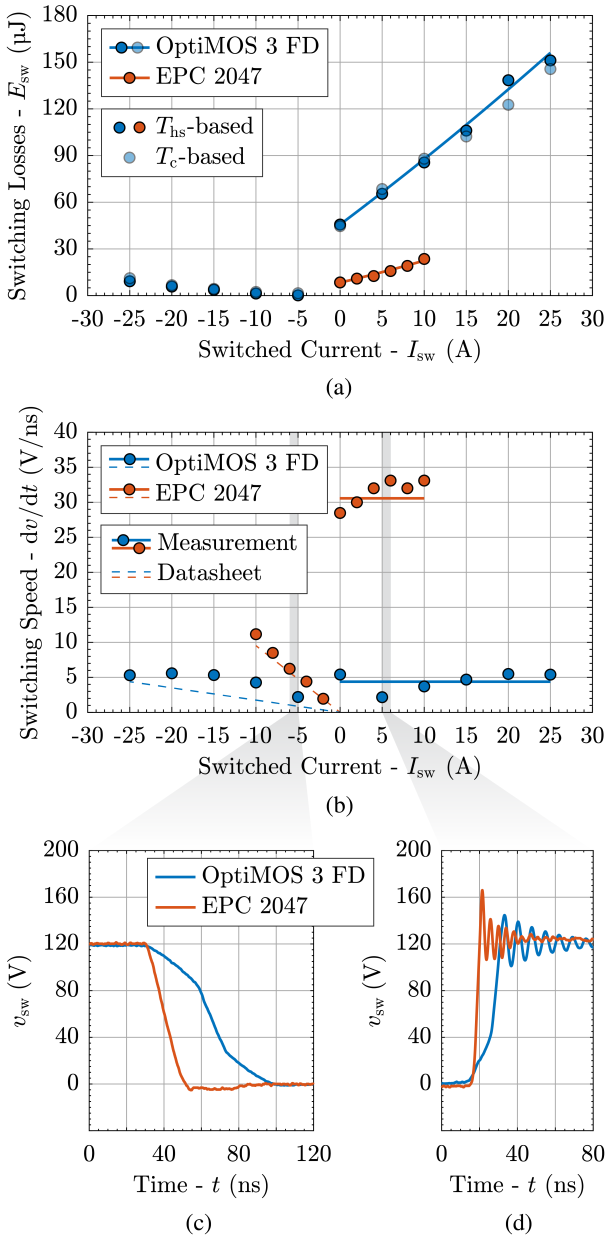


**Fig. 10:** **(a)** Measured (dots) values of the switching energy $E_{sw}$ dissipated in one switching transition by the entire half-bridge formed by either two OptiMOS 3 FD (blue) or two EPC 2047 (red), in dependency of the switched current $I_{sw}$ in Zero Voltage Switching (ZVS, $I_{sw} < 0$), Zero Current Switching (ZCS, $I_{sw} = 0$) and Hard Switching (HS, $I_{sw} > 0$) conditions. Additionally, quadratic fit (solid) on the measured values in HS conditions (see **Table IV**). HS losses ($I_{sw} > 0$) are shown for both OptiMOS 3 FD (blue) and EPC 2047 (red), while ZVS losses ($I_{sw} < 0$) are depicted only for the OptiMOS 3 FD. Two different transient calorimetric switching loss measurement methods, one based on the dynamics of $T_{hs}$ and the other one based on the dynamics of $T_c$, are compared. **(b)** Measured (dots) values of the voltage switching speeds $dv/dt$ of the OptiMOS 3 FD (blue) and of the EPC 2047 (red), in dependency of $I_{sw}$ in the conditions considered in **(a)**. Additionally, ideal (dashed) $dv/dt$ values in ZVS conditions and average measured (solid) $dv/dt$ values in HS conditions. The $dv/dt$ values are calculated observing the variation of $v_{sw}$ from 10 % (90 %) to 90 % (10 %) of $V_{dc}$. Finally, measured waveforms of $v_{sw}$ in a **(c)** ZVS transition and in a **(d)** HS transition of the OptiMOS 3 FD (blue) and of the EPC 2047 (red), with $I_{sw} = \pm 5$ A.

**TABLE IV:** Coefficients of the HS loss model for the OptiMOS 3 FD Si Power MOSFET and for the EPC 2047 GaN e-FET.

| **Power Semiconductor** Manufacturer | Model | $k_0$ (µJ) | $k_1$ (V µs) | $k_2$ (Ω µs) |
|---|---|---|---|---|
| *Infineon Tech.* | OptiMOS 3 FD | 45.7 | 4.00 | 0.014 |
| *EPC Co.* | EPC 2047 | 8.47 | 1.25 | 0.014 |

The values of $E_{sw}$ of the OptiMOS 3 FD obtained with the novel ultra-fast $T_c$-based transient calorimetric measurement method are additionally plotted in **Fig. 10(a)** and compared with the ones obtained with the $T_{hs}$-based method. An almost perfect matching is observed between the two results; hence, the $T_c$-based approach should be preferred when applicable, given its shorter measurement times and no additional drawbacks (see the **Appendix**).
For convenience, the quadratic polynomial

$$E_{sw}(I_{sw}) = k_0 + k_1 I_{sw} + k_2 I_{sw}^2 \tag{4}$$

is fit on the measured curves for $I_{sw} \geq 0$ (see **Fig. 10(a)**); the derived coefficients $k$ are reported in **Table IV** for both DUT, providing a compact expression for modeling the losses occurring in ZCS and HS conditions, and highlighting the superior performance of the EPC 2047.

The relative outcome of this comparison is expected also for other Si MOSFETs and GaN e-FETs of similar characteristics, since the beneficial properties of wide bandgap (WBG) semiconductors ensure lower values of $C_{oss}$ (see **Table I**), i.e., lower values of stored energy to be dissipated in every HS transition, as well as faster switching speeds. The latter statement is confirmed in **Fig. 10(b)**, where the measured values of the voltage switching speed $dv/dt$ are depicted with the same notation used in **Fig. 10(a)**. While 31 V/ns is the typical $dv/dt$ value of the EPC 2047, only 6 V/ns could be achieved with the OptiMOS 3 FD. **Fig. 10(b)** includes as well the measured $dv/dt$ values in ZVS conditions; for the EPC 2047, the measured points are aligned on the slope $1/2\,C_{oss,Q}$ as expected [33].
To highlight once more the different $dv/dt$ values between the two DUT, **Fig. 10(c)** and **Fig. 10(d)** show the measured waveforms of $v_{sw}$ in a ZVS and in a HS transition with $I_{sw} = \pm 5$ A. In the ZVS transition, the highly non-linear behavior of $C_{oss}$ of the OptiMOS 3 FD can be recognized. Additionally, from the resonance frequency $f_r$ of the voltage oscillations visible in the HS transitions and the values of $C_{oss}$ at $V_{dc}$ [22], [23], the values of the power loop inductance $L_{pl}$ of the two setups can be calculated according to $1/C_{oss}\,(2\pi f_r)^2$; $L_{pl} = 3.7$ nH is obtained for the OptiMOS 3 FD and $L_{pl} = 1.2$ nH for the EPC 2047. This difference can be attributed mainly to the smaller footprint of the package of the EPC 2047, which facilitates a more compact power stage design.

## VI. Unexptected Switching Behavior of the OptiMOS 3 FD

The HS loss model described by (4) allows to split $E_{sw}$ in a $I_{sw}$-dependent and in a $I_{sw}$-independent part. The latter coincides with the ZCS losses $E_{sw,ZCS}$, which can be estimated [39] according to

$$E_{sw,ZCS} = E_{sw}(0) = Q_{oss} V_{dc}\,, \tag{5}$$

where $Q_{oss}$ indicates the parasitic output charge of the DUT at $V_{dc}$. Comparing the values of $E_{sw,ZCS}$ obtained with (5) with the measured values $E_{sw}(0)$ reported in **Fig. 10(a)**, a satisfactory matching is

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observed for the EPC 2047, while a significant discrepancy is noticed for the OptiMOS 3 FD. This unexpected finding is further investigated measuring $E_{sw,ZCS}$ for different $dv/dt$ values, i.e. for different values of the turn-on gate resistance $R_{g,on}$. The results of this analysis are summarized in **Fig. 11** and in **Table V**, where the measured values of $E_{sw,ZCS}$ (solid) are compared with the calculated ones (dashed) in dependency of $R_{g,on}$, for both DUT. As expected, the measured $E_{sw,ZCS}$ of the EPC 2047 (red) are independent of $R_{g,on}$ and validate (5), additionally confirming the accuracy of the considered measurement method. Differently, the measured $E_{sw,ZCS}$ of the OptiMOS 3 FD (blue) are, for typical values of $R_{g,on}$, e.g. $R_{g,on} \leq 10\,\Omega$, significantly higher than their nominal counterparts and strongly dependent on the $dv/dt$ values. This trend is ultimately responsible for compromising the switching performance of the OptiMOS 3 FD, since $E_{sw,ZCS}$ defines the lower boundary of the HS losses [39], i.e. $k_0$.

The observed phenomenon originates from the internal structure of the analyzed power semiconductor, as explained in the following. Modern field plate or shielded gate transistors, such as the OptiMOS 3 FD, feature a three-dimensional (3D) structure able to simultaneously reduce gate charge $Q_g$ and area-specific $R_{ds,on}$ values [40]–[42]. As shown in **Fig. 12(a)**, this 3D structure consists of a deep trench comprising two electrodes: one is connected to the gate potential, while the other one, i.e. the field plate, is tied to the source potential. Whereas the gate forms a vertical MOS channel along the side face of the mesa region between the trenches, the field plate buried within the trench provides countercharges allowing to increase the n-doping

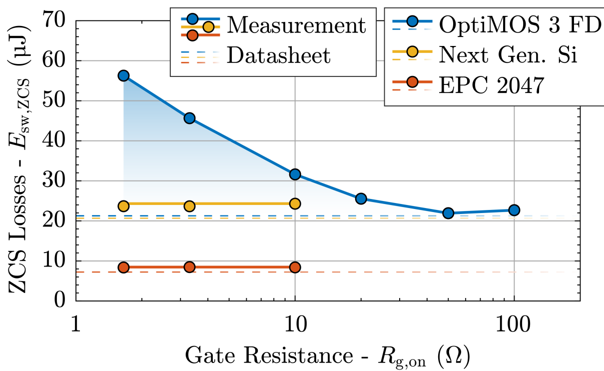


**Fig. 11:** Measured (solid and dots) and estimated (dashed) values of the energy dissipated in one ZCS transition $E_{sw,ZCS}$ by the entire half-bridge formed by either two OptiMOS 3 FD (blue), two EPC 2047 (red) or two of the next generation Si switches (yellow) in dependency of the turn-on gate resistance $R_{g,on}$. While the measured values of $E_{sw,ZCS}$ of the EPC 2047 and of the next generation Si switch are independent of the $dv/dt$ values and approach the results of the respective calculations, the measured $E_{sw,ZCS}$ of the OptiMOS 3 FD are unexpectedly higher for low values of $R_{g,on}$, i.e. for high $dv/dt$ values.

**TABLE V:** Value of $R_{g,on}$ and associated measured $dv/dt$ and $E_{sw,ZCS}$ values for the OptiMOS 3 FD Si Power MOSFET.

| Power Semiconductor Manufacturer | Model | $R_g$ (Ω) | $dv/dt$ (V/ns) | $E_{sw,ZCS}$ (µJ) |
|---|---|---|---|---|
| *Infineon Tech.* | OptiMOS 3 FD | 1.6 | 6.2 | 56.3 |
| | | 3.3 | 6.0 | 45.6 |
| | | 10 | 4.8 | 31.7 |
| | | 20 | 3.7 | 25.5 |
| | | 50 | 2.3 | 21.9 |
| | | 100 | 1.6 | 22.7 |

of the drift region, and hence to reduce the specific $R_{ds,on}$ of the MOSFET for a given voltage rating [40]. Furthermore, the field plate shields the gate electrode located above the drain contact and helps to reduce the parasitic gate-drain capacitance $C_{gd}$, i.e. to increase the switching speed while avoiding $dv/dt$ induced parasitic turn-on [43]. In contrast to Super-Junction (SJ) devices, the field plate is not depleted when the transistor is in the blocking state; hence, the field plate needs to be isolated from the surrounding Si area, e.g. through a thick oxide able to withstand the breakdown voltage of the device. However, the field plate structure introduces additional parasitic elements affecting the dynamic performance of the switch; e.g., the parasitic capacitances between the field plate and the drain $C_{df}$ and between the field plate and the gate $C_{gf}$ appear, as visible in **Fig. 12**. The value of these capacitances is defined by the thickness of the oxide between the field plate and the Si substrate and between the field plate and the gate electrode, respectively. Moreover, since the field plate is manufactured out of polysilicon, a non-zero resistance $R_{fs}$ between the field plate and the source is also present [40] (see **Fig. 12**).

Analyzing the impedance network simplifying the internal structure of the OptiMOS 3 FD, two intrinsic $R$-$C$ snubber circuits can be identified (see **Fig. 12(b)**). One is the $R_{fs}$-$C_{gf}$ gate snubber that, together with the internal gate resistance $R_g$, damps the ringing of the gate-source voltage $v_{gs}$ during the switching transients. The other one is the $R_{fs}$-$C_{df}$ snubber and it is designed to actively limit overvoltage spikes occurring in HS transitions on the drain-source voltage $v_{ds}$. Hence, by avoiding excessive ringing on $v_{sw}$, it reduces the electromagnetic (EM) noise emissions.

Unfortunately, the parasitic elements introduced by the field plate structure can as well have a negative impact on the switching losses. In particular, when the displacement currents generated by a HS transition cause the departing of the field plate potential from its reference source potential, the gate-source capacitance $C_{gs}$ is charged through $C_{gd}$, as well as through the series connection of $C_{df}$ and $C_{gf}$. With high values of $dv/dt$, a partial parasitic turn-on might occur as the internal $v_{gs}$ approaches the gate threshold voltage. This phenomenon is believed to cause the additional switching losses highlighted in **Fig. 11**, which are consistently occurring at high $dv/dt$ values.

Consequently, in the manufacturing process of field plate MOSFETs, there is a trade-off between avoiding overvoltages and excessive ringing of $v_{gs}$ and $v_{ds}$, and reducing the switching losses. Whereas the OptiMOS 3 FD is optimized for the former to enable quiet EM operation of HS converter systems, the next generation 200 V transistors are optimized for the latter, i.e. towards the lowest switching

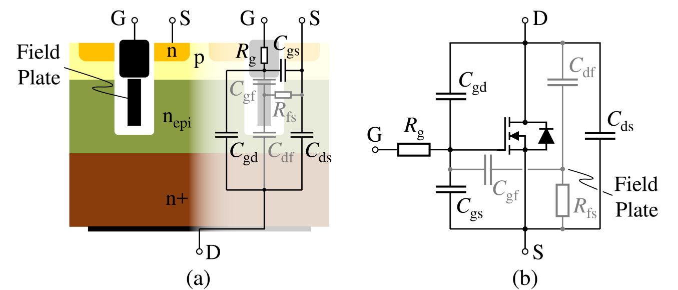


**Fig. 12:** **(a)** Cross section of a field plate transistor, similar to the one of the OptiMOS 3 FD; the parasitic components originating from the internal structure of the device are shown according to their physical origin. **(b)** Circuit schematic of the parasitic components highlighted in **(a)**. The parasitic elements associated to the field plate are represented in gray.

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losses, by entirely suppressing any coupling between gate and field plate electrodes, and by having a quasi-zero impedance connection between the field plate and the source.

To conclude this analysis, research samples belonging to the next generation of 200 V transistors are analyzed for the same conditions used for the OptiMOS 3 FD, and the measured (solid and dots) and calculated (dashed) values of $E_{\mathrm{sw,ZCS}}$ are also shown in **Fig. 11** (yellow) for comparison. Supporting the previous explanation, the measured values of $E_{\mathrm{sw,ZCS}}$ of the next generation switches are independent of $R_{\mathrm{g,on}}$, i.e. of the ${}^{\mathrm{d}v}/_{\mathrm{d}t}$ values; hence, significantly enhanced switching performance are expected.

## VII. Power Converter Case Study

The conduction, thermal and switching characteristics of the DUT, i.e., the OptiMOS 3 FD Si Power MOSFET and the EPC 2047 GaN e-FET, are separately evaluated in **Sections III**, **IV** and **V**. These experimental results are combined herein to determine the performance limits of a basic power converter in dependency of the devices selected for the realization of its power stage (see **Fig. 4** and **Fig. 5**). Additionally, since this converter can be considered as part of a more complex system, e.g. of a three-phase inverter, of a modular multi-phase inverter or of a multi-level inverter (cf. the gray area in **Fig. 2(a)**), the obtained results can be generalized. The ultimate goal of this analysis is to quantify the expected superiority of GaN 200 V over Si 200 V power semiconductors and to identify the bottlenecks limiting further performance improvements.

### A. Converter Specifications and Loss Models

Since DC/AC power converters are of most interest in the mentioned application areas, a HS half-bridge operated as single-phase inverter, which is identified as the fundamental building block of several M/ML inverter topologies (see **Fig. 2(a)**), is considered in this analysis. As a performance metric, the efficiency of the half-bridge $\eta$ is calculated as a function of the switching frequency $f_{\mathrm{sw}}$ and of the RMS value of the output current $I_{\mathrm{o,RMS}}$. The calculations consider all the aspects mentioned in the previous sections, in particular:

- *Conduction Performance*: the conduction losses $P_{\mathrm{cond}}$ are calculated as $R_{\mathrm{ds,on}} I^2_{\mathrm{o,RMS}}$ with a sinusoidal output current $i_{\mathrm{o}}$. The dependence of $R_{\mathrm{ds,on}}$ on $T_{\mathrm{j}}$ (see **Fig. 6**) is considered for both DUT. Additionally, the dynamic $R_{\mathrm{ds,on}}$ phenomenon is taken into account for the EPC 2047 [25].
- *Thermal Performance*: $T_{\mathrm{j}}$ is iteratively determined according to the measurement results presented in **Fig. 7** and **Table II**, and accounted for in the calculation of $P_{\mathrm{cond}}$, given the dependency of $R_{\mathrm{ds,on}}$ with $T_{\mathrm{j}}$ (see **Fig. 6**). The maximum $T_{\mathrm{j}}$ is fixed at $T_{\mathrm{j,MAX}} = 100\,°\mathrm{C}$ and $T_{\mathrm{hs}} = 50\,°\mathrm{C}$ is considered, similar to the specifications given in [44].
- *Switching Performance*: the switching losses $P_{\mathrm{sw}}$ are calculated according to **Fig. 10(a)** and **Table IV**, i.e. only the HS losses are considered (the ZVS losses are neglected). In particular, an appropriate value of $I_{\mathrm{sw}}$ is selected for each switching period from the sampling of $i_{\mathrm{o}}$ (the current ripple is neglected); thus, $E_{\mathrm{sw}}$ is calculated according to (4) per each switching period and all contributions in one AC output period are summed. Finally, the total switching energy is multiplied with the output frequency, determining $P_{\mathrm{sw}}$.

For consistency with **Section V**, the DC input voltage is $V_{\mathrm{dc}} = 120\,\mathrm{V}$ and the modulation index $m$ is fixed to $m = {}^{2\,\hat{v}_{\mathrm{o}}}/_{V_{\mathrm{dc}}} = 1$, where $\hat{v}_{\mathrm{o}}$ indicates the peak value of the sinusoidal output voltage $v_{\mathrm{o}}$. Hence, the output power $P_{\mathrm{o}} = {}^{V_{\mathrm{dc}}}/_{2\sqrt{2}}\, I_{\mathrm{o,RMS}} \approx 42\, I_{\mathrm{o,RMS}}$ is considered to calculate $\eta = 1 - {}^{(P_{\mathrm{sw}}+P_{\mathrm{cond}})}/_{P_{\mathrm{o}}}$. $I_{\mathrm{o,RMS}}$ is varied in the few tens of A range, resulting in values of $P_{\mathrm{o}}$ of up to approximately 1 kW, apparently lower than the output power requirements of DC/AC converters in the application areas of interest. However, if three- (or more) phase M/ML inverters are considered, the overall output power is obtained, in first approximation, multiplying $P_{\mathrm{o}}$ by the number of phases, the number of levels and/or the number of modules forming the converter, thus reaching several kW or few tens of kW. For example, considering $V_{\mathrm{dc}} = 480\,\mathrm{V}$ for a three-phase five-level FCC (see **Fig. 2(a)**), already $I_{\mathrm{o,RMS}} = 10\,\mathrm{A}$, i.e. $P_{\mathrm{o}} = 420\,\mathrm{W}$, translates into an output power rating of $3 \cdot 4 \cdot P_{\mathrm{o}} = 5\,\mathrm{kW}$. Additionally, more than one DUT can be connected in parallel to realize each switch forming the bridge-leg, but this option is not considered herein for the sake of simplicity.

### B. Calculation Results

The results of the analysis introduced above are shown in **Fig. 13**, where the calculated values of $\eta$ are plotted in dependency of $f_{\mathrm{sw}}$ and $I_{\mathrm{o,RMS}}$, for both DUT. The white areas in the plots indicate operating regions beyond the thermal limit of the half-bridge, and thus highlight how the superior thermal performance of the OptiMOS 3 FD enable higher values of $I_{\mathrm{o,RMS}}$, and hence $P_{\mathrm{o}}$, for a given $f_{\mathrm{sw}}$, with respect to the EPC 2047 (cf. **Fig. 13(a)** and **Fig. 13(b)**). From an efficiency point of view, instead, the EPC 2047 outperforms the OptiMOS 3 FD in the whole operating region where the GaN design is thermally

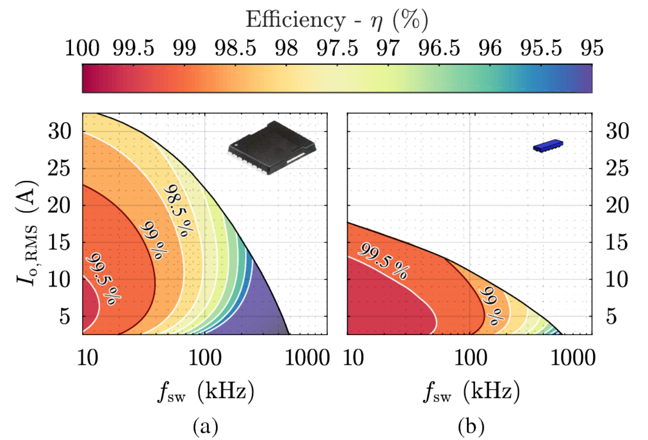


**Fig. 13:** Efficiency $\eta$ of the HS half-bridge formed by either **(a)** two OptiMOS 3 FD Si Power MOSFETs or two **(b)** EPC 2047 GaN e-FETs, in dependency of $f_{\mathrm{sw}}$ and of the RMS value of the output current $I_{\mathrm{o,RMS}}$.

**TABLE VI:** Maximum switching frequency $f_{\mathrm{sw}}^{\mathrm{max}}$ achievable by the HS half-bridge formed by either two OptiMOS 3 FD Si Power MOSFETs or two EPC 2047 GaN e-FETs, for different values of $P_{\mathrm{o}}$ and $\eta$.

| **Power Semiconductor** Manufacturer | Model | $f_{\mathrm{sw}}^{\mathrm{max}}$ @ $P_{\mathrm{o}} = 250\,\mathrm{W}$ $\eta = 99\,\%$ | $\eta = 98\,\%$ | $\eta = 97\,\%$ |
|---|---|---|---|---|
| *Infineon Tech.* | OptiMOS 3 FD | 35 kHz | 77 kHz | 119 kHz |
| *EPC Co.* | EPC 2047 | 130 kHz | 299 kHz | – |

| **Power Semiconductor** Manufacturer | Model | $f_{\mathrm{sw}}^{\mathrm{max}}$ @ $P_{\mathrm{o}} = 500\,\mathrm{W}$ $\eta = 99\,\%$ | $\eta = 98\,\%$ | $\eta = 97\,\%$ |
|---|---|---|---|---|
| *Infineon Tech.* | OptiMOS 3 FD | 38 kHz | 97 kHz | 156 kHz |
| *EPC Co.* | EPC 2047 | 73 kHz | – | – |

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feasible, mostly because of its lower switching losses (see **Fig. 10(a)**). The latter statement is confirmed in **Table VI**, where the maximum achievable switching frequencies $f_{sw}^{max}$ are listed for different values of $P_o$ and $\eta$, for both DUT.

In **Fig. 13** and **Table VI**, it can be additionally observed how the half-bridge performance estimated through the FoM (see **Fig. 1**) are confirmed, at least in relative terms. In fact, approximately a 3 times higher $f_{sw}^{max}$ can be achieved for the same $\eta$ and $P_o$ by the EPC 2047, with respect to the OptiMOS 3 FD, as expected from **Table I** [11]. However, the FoM approach neglects several aspects with a strong impact on the converter design, e.g. the thermal limit of the half-bridge. In a first step, a factor considering the typical $R_{th,j\text{-}hs}$ value of the power semiconductors could be included in their FoM to account for their thermal characteristics, thus providing a more accurate insight on the converter performance limits.

Continuing with the analysis of **Table VI**, it can be observed how, e.g. for $P_o = 500\,W$, the Si-based design achieves higher values of $f_{sw}$ than the GaN-based design, however, at the expense of lower $\eta$. As well, the opposite variation of $f_{sw}^{max}$ for increasing $P_o$ characterizing the two DUT, i.e. an increasing $f_{sw}^{max}$ for the OptiMOS 3 FD and a decreasing $f_{sw}^{max}$ for the EPC 2047, indicates significantly different values of optimum $P_o$ in the two cases. In other words, even if the two characterized power semiconductors have comparable $R_{ds,on}$ values and the EPC 2047 generally ensures better switching performance, the packaging of the OptiMOS 3 FD allows it to remain competitive for higher power applications.

Nevertheless, in a comprehensive multi-objective optimization procedure, also the chip area should be considered as a design parameter; i.e., $\eta$ should be evaluated for several EPC 2047 connected in parallel (i.e. for a larger chip area) in order to increase the power rating of the GaN-based solution, and for Si Power MOSFETs with a smaller chip area, since higher $R_{ds,on}$ and lower $Q_{oss}$ values could enhance the performance of the Si-based design at low $P_o$ and high $f_{sw}$ values.

To conclude, the impact of $f_{sw}^{max}$ on the volumetric power density of the considered single-phase inverter can be qualitatively estimated. First, the output inductor $L_o$ can be designed according to

$$L_o = \frac{V_{dc}\, d(1-d)}{\Delta I_{o,pkpk}\, f_{sw}^{max}} \geq \frac{V_{dc}}{4\, k_{ripple} \sqrt{2} I_{o,RMS}\, f_{sw}^{max}}\,, \tag{6}$$

where $\Delta I_{o,pkpk}$ indicates the peak-to-peak ripple of $i_o$, and $k_{ripple}$ is defined as

$$\Delta I_{o,pkpk} = k_{ripple} \sqrt{2} I_{o,RMS}. \tag{7}$$

Considering $k_{ripple} = 0.3$, $P_o = 500\,W$ ($I_{o,RMS} = 11.8\,A$) and the values of $f_{sw}^{max}$ associated to $\eta = 99\,\%$ (see **Table VI**) as an example, $L_o = 158\,\mu H$ and $82\,\mu H$ are obtained for the Si- and GaN-based designs, respectively. The reduction by factor 1.9 in the value of $L_o$ is directly related, i.e. inversely proportional, to the increase of $f_{sw}^{max}$ achieved by the EPC 2047. Moreover, since the volume of an inductor can be assumed proportional to its inductance value for a given current rating [45], a factor 1.9 more compact design of $L_o$ is expected in this case. Finally, since the same value of $\eta$ is considered for both designs, comparable heat sink volumes can be assumed, hence leading to the GaN-based solution having a higher power density than its Si-based counterpart.

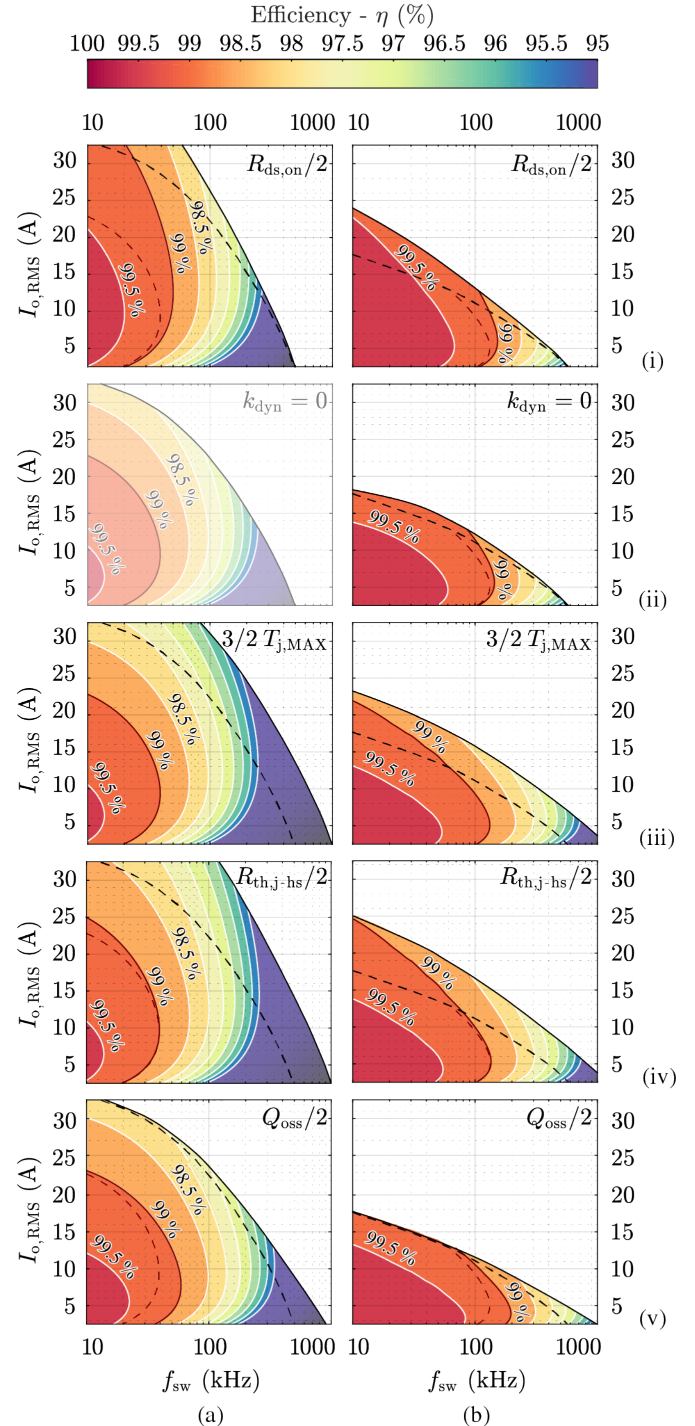


**Fig. 14:** Sensitivity analysis of $\eta$ of the HS half-bridge formed by either **(a)** two OptiMOS 3 FD Si Power MOSFETs or two **(b)** EPC 2047 GaN e-FETs, in dependency of $f_{sw}$ and of $I_{o,RMS}$, for different perturbations of the parameters defining the conduction **(i)**-**(ii)**, thermal **(iii)**-**(iv)** and switching **(v)** performance of the DUT. The thermal limit (black, dashed) and $\eta = 99\,\%$ (red, dashed) curves of the reference designs (see **Fig. 13**) are reported in the corresponding plots for comparison.

### *C. Sensitivity Analysis*

**Figs. 14(i-v)** summarize the sensitivity of the results shown in **Fig. 13** with respect to the parameters defining the conduction **(i)**-**(ii)**, thermal **(iii)**-**(iv)** and switching **(v)** performance of the DUT [46]. Only one parameter at a time is modified while the others are kept constant; thus, the limit values of $\eta$, $f_{sw}$ and $I_{o,RMS}$ are analyzed in order to understand which characteristics of each DUT constitute the major bottleneck for the performance of the power stage, i.e. which key

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factors should preferably be improved at the device level by the semiconductor manufacturers. In particular, the maximum achievable switching frequency $f_{\mathrm{sw}}^{\eta}$ for a given $\eta$, the maximum achievable output power $P_{\mathrm{o}}^{\mathrm{fsw}}$ for a given $f_{\mathrm{sw}}$ and the maximum achievable switching frequency $f_{\mathrm{sw}}^{\mathrm{Po}}$ for a given $P_{\mathrm{o}}$ are compared.

The most relevant observations, focusing on the $\eta$, $P_{\mathrm{o}}$ and $f_{\mathrm{sw}}$ values of interest, are commented in the following:

- **(i)** Halving the value of $R_{\mathrm{ds,on}}$ enhances the performance of both solutions, offering higher $\eta$ at low $f_{\mathrm{sw}}$ and high $I_{\mathrm{o,RMS}}$ values. However, already at $f_{\mathrm{sw}} = 100\,\mathrm{kHz}$, the improvement in terms of $P_{\mathrm{o}}^{f_{\mathrm{sw}}}$ is almost negligible for both DUT. The reduction of conduction losses provides more room for switching losses; hence, both $f_{\mathrm{sw}}^{\eta}$ and $f_{\mathrm{sw}}^{\mathrm{Po}}$ increase. The effect on $f_{\mathrm{sw}}^{\mathrm{Po}}$ is stronger on the EPC 2047, since the conduction losses generally dominate its loss breakdown, particularly for low values of $f_{\mathrm{sw}}$.
- **(ii)** Eliminating the dynamic $R_{\mathrm{ds,on}}$ phenomenon by setting $k_{\mathrm{dyn}} = 0$ has only a small effect on the EPC 2047.
- **(iii)** An increase of the allowed junction temperature $T_{\mathrm{j,MAX}}$ from $100\,^{\circ}\mathrm{C}$ to $150\,^{\circ}\mathrm{C}$ does not influence $\eta$ but extends the operating range of both designs. Since more conduction losses are allowed for the same $f_{\mathrm{sw}}$, $P_{\mathrm{o}}^{\mathrm{fsw}}$ increases in both cases. More significantly, since more switching losses are allowed for the same $P_{\mathrm{o}}$, $f_{\mathrm{sw}}^{\mathrm{Po}}$ doubles for the OptiMOS 3 FD and triplicates for the EPC 2047 if, e.g., $P_{\mathrm{o}} = 500\,\mathrm{W}$ is considered.
- **(iv)** Decreasing $R_{\mathrm{th,j\text{-}hs}}$ has a similar effect as increasing $T_{\mathrm{j,MAX}}$. In addition, the associated reduction of $T_{\mathrm{j}}$, i.e. of $R_{\mathrm{ds,on}}$, slightly improves $\eta$ for every operating point. With the considered perturbation of parameters, $R_{\mathrm{th,j\text{-}hs}}$ has the strongest influence on $P_{\mathrm{o}}^{\mathrm{fsw}}$ and $f_{\mathrm{sw}}^{\mathrm{Po}}$, both for the OptiMOS 3 FD and for the EPC 2047.
- **(v)** A reduction of $Q_{\mathrm{oss}}$ is of particular interest for high efficiency applications. For instance, considering $\eta = 99\,\%$, halving $Q_{\mathrm{oss}}$ translates into approximately a $50\,\%$ increase in $f_{\mathrm{sw}}^{\eta}$ for both DUT, i.e. $Q_{\mathrm{oss}}$ is the parameter with the strongest influence on $f_{\mathrm{sw}}^{\eta}$. Differently from **(i)**, the effect on $f_{\mathrm{sw}}^{\mathrm{Po}}$ is more evident on the OptiMOS 3 FD, which suffers mostly from the switching losses.

Summarizing the results of this sensitivity analysis, it can be concluded that, to realize high efficiency and high power density converters at the considered voltage level and power ratings, an improvement in the switching performance is the most desirable; however, the thermal characteristics are the factor limiting a further increase of switching frequency and/or of output power rating. In particular, mainly the value of $Q_{\mathrm{oss}}$ defines $\eta$ for high values of $f_{\mathrm{sw}}$, while the value of $R_{\mathrm{th,j\text{-}hs}}$ limits the safe operating area, i.e. $P_{\mathrm{o}}$.

## VIII. Conclusion

Virtual prototyping and multi-objective optimization procedures of modular and/or multi-level (M/ML) power converters support the aerospace, EV and renewable energy industries in meeting more and more demanding requirements in terms of efficiency and volumetric/gravimetric power density. These approaches strongly rely on accurate models of the power stage performance, which allow to identify the performance limits, and support the perfection of the design, of power converters.

Accordingly, silicon (Si) and gallium nitride (GaN) power semiconductors with $200\,\mathrm{V}$ blocking voltage capability and the lowest value of on-state resistance $R_{\mathrm{ds,on}}$ currently available in the market are experimentally characterized in this paper. These devices, i.e. the OptiMOS 3 Fast Diode (FD) Si Power MOSFET [22] and the EPC 2047 GaN e-FET [23], are identified as the best candidates for realizing efficient and compact M/ML inverters in the application areas of interest.

The conduction performance of both DUT (excluding the dynamic $R_{\mathrm{ds,on}}$ phenomenon of the GaN e-FET) are comparable and are in good agreement with the information provided in the respective datasheets. From the thermal point of view, given the better thermal conductivity of its package, the Si MOSFET is able to dissipate 5 times more power than the GaN e-FET for the same case temperature. On the other hand, the GaN e-FET offers from 3 to 6 times lower switching losses, mostly originating from its smaller parasitic output capacitance value, which results in higher voltage switching speeds. Additionally, an undesired switching behavior of the considered Si MOSFET is observed; after analyzing the internal structure of the device, this lossy phenomenon is clarified and proven to be eliminated in research samples of next generation Si devices, which are also analyzed experimentally.

Two different transient calorimetric switching loss measurement methods are considered to accurately measure the switching losses of the DUT; one of them is proposed in this paper and offers very short measurement times in the order of a few seconds.

In the last section, the described experimental results are combined in the performance analysis of a hard switching half-bridge operated as single-phase inverter, enabling a comparison of the two DUT in a real converter application. Additionally, a sensitivity analysis is performed to separately evaluate the influence of the different device parameters on the overall converter performance: a reduction of the parasitic output charge has the most significant impact on the converter efficiency at switching frequencies above $100\,\mathrm{kHz}$, whereas better cooling performance increase the converter output power rating. In general, considering a typical switching frequency of modern hard switching topologies, i.e. $140\,\mathrm{kHz}$, the Si-based (OptiMOS 3 FD) half-bridge offers higher power ratings ($500\,\mathrm{W}$) with lower efficiencies ($97\,\%$), while, at the contrary, the GaN-based (EPC 2047) design, ensures ultra-high efficiencies ($99\,\%$), but at lower power ratings ($250\,\mathrm{W}$).

## Appendix

## Calorimetric Switching Loss Measurement Methods

A brief overview of the different calorimetric switching loss measurement methods recently proposed in literature is presented in this **Appendix**, before providing more details on the novel ultra-fast $T_{\mathrm{c}}$-based transient calorimetric measurement method introduced in **Section V-B**.

### A. State-of-the-Art

The most widely adopted approach to measure the switching losses of a power device is the Double Pulse Test (DPT) [47], [48]. This method is defined *electric*, since it relies on the measurement of electrical quantities, i.e., of the voltage across and of the current through a switch, to calculate the energy dissipated in a switching transition. The measurement accuracy of electric methods is generally defined by the performance, e.g. in terms of bandwidth and intrusiveness, of the selected voltage and current probes. Accordingly, the high switching speeds of WBG semiconductors are limiting the applicability of these methods, and motivated, in the recent years, the need to investigate alternative electric [49], [50], as well as *calorimetric*, switching loss measurement methods. The latter are based on the observation of thermal quantities [32]–[38], [51]–[55],

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and are thus typically independent from the electric characteristics of the analyzed devices. Generally, calorimetric measurement methods can be divided into two subcategories, i.e., *steady-state* methods and *transient* methods. In steady-state methods [32], [51]–[54], the setup is continuously operated until the thermal steady-state is reached and, only then, the occurring losses are determined from the observation of specific temperature values. Differently, transient methods [33]–[38], [55] analyze the thermal dynamics of the system, e.g. its thermal step response after turn-on, and, at the expense of slightly increased complexity, offer reduced measurement times and comparable accuracies [35], [37], [38].

*B. Advanced Analysis of the Novel Ultra-Fast $T_c$-based Transient Calorimetric Measurement Method*

*1) Thermal Model:* The system of ODEs describing the evolution of $T_c$ over time in thermal model shown in **Fig. 8(c)** is

$$\begin{bmatrix} \dot{T}_{c,h} \\ \dot{T}_{c,l} \end{bmatrix} = \begin{bmatrix} -\frac{R_{th,h}+R_{th,m}}{C_{th,h}\,R_{th,h}\,R_{th,m}} & \frac{1}{C_{th,h}\,R_{th,m}} \\ \frac{1}{C_{th,l}\,R_{th,m}} & -\frac{R_{th,l}+R_{th,m}}{C_{th,l}\,R_{th,l}\,R_{th,m}} \end{bmatrix} \begin{bmatrix} T_{c,h} \\ T_{c,l} \end{bmatrix} + \begin{bmatrix} \frac{P_{T,h}}{C_{th,h}} \\ \frac{P_{T,l}}{C_{th,l}} \end{bmatrix}$$

$$\dot{T}_{hs} = -\frac{P_{T,h}+P_{T,l}}{C_{th,hs}}\,. \tag{8}$$

Solving (8) for $T_{c,h}$ and $T_{c,l}$ provides the expressions necessary to estimate the values of $P_{T,h}$ and $P_{T,l}$, as described in **Section V-B**.

*2) Comparison:* As anticipated, several advantages are introduced by this approach compared with the $T_{hs}$-based method. First, $P_{T,h}$ and $P_{T,l}$ can be, in this case, estimated separately, since both $T_{c,h}$ and $T_{c,l}$ (rather than only $T_{hs}$) are measured. This possibility can be exploited when the loss distribution between $T_h$ and $T_l$ is asymmetric; however, if e.g. $P_{T,h} \gg P_{T,l}$, an excessive coupling between $T_{c,h}$ and $T_{c,l}$ can negatively affect the measurement accuracy of the individual semiconductor losses. Second, and most important, the measurement time is conveniently reduced to a few seconds, i.e. to the time sufficient to capture the transient behavior of $T_c$.
To maintain a high measurement resolution with shorter measurement times, the high frame rate (up to hundreds of frames-per-second) high resolution infrared thermo-camera [56] shown in **Fig. 9(a)** is used to measure $T_{c,h}$ and $T_{c,l}$. In particular the camera measures the average temperature of specified areas, e.g. coinciding with the package of $T_h$ and $T_l$. Accordingly, there is no inaccuracy of the temperature measurement due to electro-magnetic coupling, as could occur with thermocouples or dedicated ICs [38]. In principle, any temperature measurement device can be used, however, an excessively large sampling time inevitably penalizes the measurement accuracy. Finally, no additional component, e.g. no customized heat sink, must be necessarily installed on the power circuit to perform the measurements. Hence, this switching loss measurement method can be more easily applied to existing power converters, as far as the DUT are visible/reachable from the outside.

The accuracy of this approach in the considered measurement setup (**Fig. 9(a)**) is verified for all operating points of interest, i.e. approximately $0\,W \leq P_{T,h} < 15\,W$ and $0\,W \leq P_{T,l} < 15\,W$, by comparing the estimated values of $P_{T,tot}$, $P_{T,h}$ and $P_{T,l}$ to a reference electrical measurement. The comparison is performed in DC conditions, such that constant $P_{T,h}$ and $P_{T,l}$, generated from a power source, can be accurately measured with precision multimeters. The obtained relative error, both on the total power $e_{P,T,tot}$ and on the individual ones $e_{P,T,h}$ and $e_{P,T,l}$, are plotted in absolute values in **Fig. 15**. It can be observed

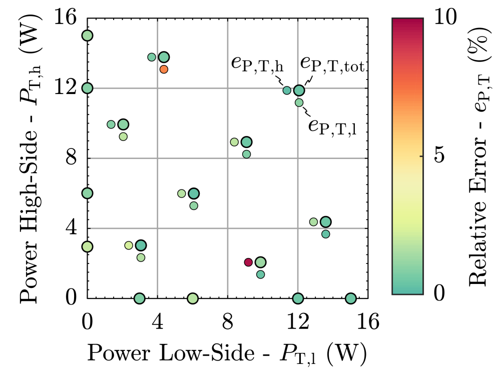


**Fig. 15:** Absolute value of the relative error of the $T_c$-based transient calorimetric loss measurement method on the estimation of $P_{T,tot}$, i.e., $e_{P,T,tot}$, and of $P_{T,h}$ and $P_{T,l}$, i.e., $e_{P,T,h}$ and $e_{P,T,l}$, in dependency of $P_{T,h}$ and $P_{T,l}$ (approximately $0\,W \leq P_{T,h} < 15\,W$ and $0\,W \leq P_{T,h} < 15\,W$). The measurement accuracy is considered satisfactory, since $e_{P,T,tot}$ is limited below 3 % for all calibrated cases.

that $e_{P,T,tot}$ is limited below 3 % (0.8 % on average), while the average $e_{P,T,h}$ and $e_{P,T,l}$ are 2.3 % and 2.0 %, respectively.

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