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Novel SWISS Rectifier Modulation Scheme Preventing Input Current Distortions at Sector Boundaries

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***Abstract*—This paper describes a new modulation concept for the uni- and bidirectional SWISS rectifier which mitigates ac input current distortions at the mains voltage sector boundaries. An analytical model is derived and compared to simulations, which allows an estimation of the distortion's magnitude from design parameters, showing that these distortions increase the input current THD significantly. A modification of the original circuit topology is proposed which decouples the operation of SWISS Rectifier's active 3rd harmonic current injection network and its dc-dc converter switches. An algorithm is presented which allows the calculation of a temporary pulse width modulation for the SWISS Rectifier's current injection network to mitigating the distortions. The concept is verified for both power flow directions and for operation with unsymmetrical and distorted mains voltages by measurement results taken on a bidirectional 7.5 kW SWISS Rectifier prototype. An ac input current THD of 1.3 % results for symmetric sinusoidal mains voltages and 1.4 % and 1.6 % for operation with distorted and unsymmetrical mains voltages.**

***Index Terms*—SWISS Rectifier, active third harmonic current injection, buck-type PFC converter, rectifier systems**

I. Introduction

The increasing power consumption of data centers and telecommunication equipment has led to a demand for more efficient power supply systems. As data center equipment is an intrinsic dc load, dc distribution systems are expected to provide significant gains in efficiency as rectifier stages of power supply modules can be omitted [1]. Furthermore, a direct battery buffering of the dc bus voltage allows to omit a dedicated UPS system, which increases efficiency further, improves reliability and reduces capital cost and floor space [2, 3]. Accordingly, standards for 380 V dc distribution systems have been created recently [4]. Different power delivery architectures based on dc distribution, e.g. using series-connected stacks of servers, have been described in the literature and could lead to further improvements of overall system efficiency [5].

Furthermore, several renewable energy sources (RES), such as PV modules or fuel cells generate dc power and can therefore be connected to a dc distribution systems using a dc-dc converter which typically has a higher efficiency and lower complexity than standard dc-ac inverters. Therefore, RES can be directly connected to a data center's dc distribution system, minimizing conversion losses and forming a so-called dc microgrid. However, dc distribution systems are not limited to data centers as loads like computers, TV sets, LED lightning and Electric Vehicles are intrinsic dc loads as well. Therefore, similar benefits as in data centers are expected from dc microgrids in office buildings, industry and residential areas. As the generation from RES does typically not match the local demand in the microgrid, an interface to the conventional ac utility grid, allowing a bidirectional energy transfer, is typically required [8–10].

As the nominal dc bus voltage of 380 V is lower than the full-wave rectified voltage of the 400 V ac grid, two-stage systems are normally used. These consist of a power factor correction stage (PFC) connected in series with a dc-dc converter. This is typically also the case for fast chargers of Electric Vehicle batteries which are powered from the three-phase mains [11–13]. In these applications buck-type

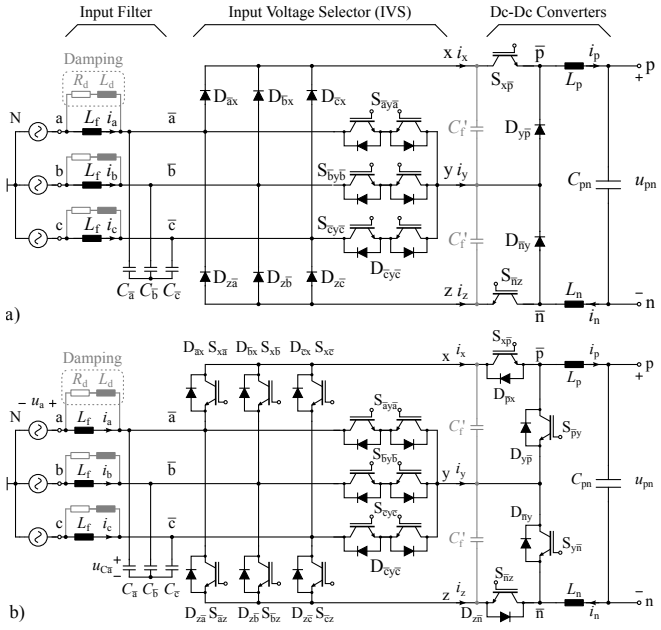

Fig. 1. The schematic of the unidirectional SWISS Rectifier as introduced in [6] is shown in **a)**. An extension allowing a reversal of the dc output current (i_p, i_n) which enables bidirectional power flow is shown in **b)** [7].

PFC converters, like the six-switch buck-type rectifier [6, 14–17], the three-switch buck-type PWM rectifier [15, 18–21], the bidirectional nine-switch buck-type rectifier [22], the delta-type current source rectifier [23, 24] or the SWISS Rectifier (cf. **Fig. 1a)** [6], are an advantageous alternative, allowing a single-stage conversion between the three-phase mains and a dc bus with lower voltage. A detailed comparison of these buck-type rectifier topologies and/or two-stage systems would require detailed analysis of all topologies as well as the load, load profile and EMI & grid code regulations and is, for the sake of brevity, not part of this paper which focuses on improving the ac input current THD of the SWISS Rectifier.

Extensions of the SWISS Rectifier, providing bidirectional output current [7] and galvanic isolation between the ac and dc side [25, 26], have been proposed in the literature. To cover a wide range of potential applications both power flow directions of the bidirectional SWISS Rectifier (cf. **Fig. 1b**), ac-to-dc and dc-to-ac, will analyzed separately in this paper. The obtained results for ac-to-dc power transfer are valid also for the unidirectional SWISS Rectifier shown in **Fig. 1a)**.

The schematic of the conventional SWISS Rectifier, as introduced in [6], is shown in **Fig. 1a)**. It consists of an ac side input filter, an Input Voltage Selector (IVS), two dc-dc converters ($\mathrm{S}_{\mathrm{x}\bar{\mathrm{p}}}$, $\mathrm{D}_{\mathrm{y}\bar{\mathrm{p}}}$, L_p and $\mathrm{D}_{\bar{\mathrm{n}}\mathrm{y}}$, $\mathrm{S}_{\bar{\mathrm{n}}\mathrm{z}}$, L_n) and a dc output capacitor C_pn. Additional capacitors C'_f are used to shorten the commutation paths of the two dc-dc converters. To allow a bipolar dc output current, and hence a bidirectional power flow, additional switches can be added to the IVS and the dc-dc converters as shown in **Fig. 1b)** [7]. The IVS consists of a three-phase full-wave diode bridge ($\mathrm{D}_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}\mathrm{x}}$, $\mathrm{D}_{\mathrm{z}\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}}$) with anti-parallel switches ($\mathrm{S}_{\mathrm{x}\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}}$, $\mathrm{S}_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}\mathrm{z}}$) and a third harmonic injection network ($\mathrm{S}_{\bar{k}\mathrm{y}\bar{k}}$ $k \in \{\bar{a}, \bar{b}, \bar{c}\}$). Its switches are controlled such that the input phase with highest potential is connected to node x, the one with lowest potential to node z and the remaining phase to node y. Therefore, the injection network's switches $\mathrm{S}_{\bar{\mathrm{a}}\mathrm{y}\bar{\mathrm{a}}}$, $\mathrm{S}_{\bar{\mathrm{b}}\mathrm{y}\bar{\mathrm{b}}}$ and $\mathrm{S}_{\bar{\mathrm{c}}\mathrm{y}\bar{\mathrm{c}}}$ operate with twice the mains frequency, while the rectifier switches $\mathrm{S}_{\mathrm{x}\bar{\mathrm{a}}}$, $\mathrm{S}_{\mathrm{x}\bar{\mathrm{b}}}$, $\mathrm{S}_{\mathrm{x}\bar{\mathrm{c}}}$, $\mathrm{S}_{\bar{\mathrm{a}}\mathrm{z}}$, $\mathrm{S}_{\bar{\mathrm{b}}\mathrm{z}}$ and $\mathrm{S}_{\bar{\mathrm{c}}\mathrm{z}}$ are operated with mains frequency. This can be seen in the simulation results for a bidirectional 7.5 kW SWISS Rectifier shown in **Fig. 2** where the mains voltages and the IVS output voltages u_xN, u_yN and u_zN are shown. Note that even though the IVS' switches are operated at mains frequency the resulting IVS currents i_x, i_y and i_z are discontinuous due to the buck-type dc-dc converters $\mathrm{S}_{\mathrm{x}\bar{\mathrm{p}}}$, $\mathrm{S}_{\bar{\mathrm{p}}\mathrm{y}}$ and $\mathrm{S}_{\mathrm{y}\bar{\mathrm{n}}}$, $\mathrm{S}_{\bar{\mathrm{n}}\mathrm{z}}$.

As described in [6] the two dc-dc converters of the SWISS Rectifier can ideally be controlled in such a way that sinusoidal ac side input currents i_a, i_b and i_c result. While the rectifier's input currents are sinusoidal and in phase with the grid voltages, it can be seen that they are distorted at the intersections of the ac mains phase voltages u_a, u_b and u_c.

These distortions are caused by the switching frequency voltage ripple across the input filter capacitors $C_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}}$ [27]. Note that similar input current distortions also exist in other current source rectifiers (CSR) like the six-switch buck-type CSR [16, 17, 28], the three-switch buck-type PWM rectifier [20, 21], the delta-type CSR [24] and isolated, CSR-based circuits [29]. Detailed simulation results for the intersection

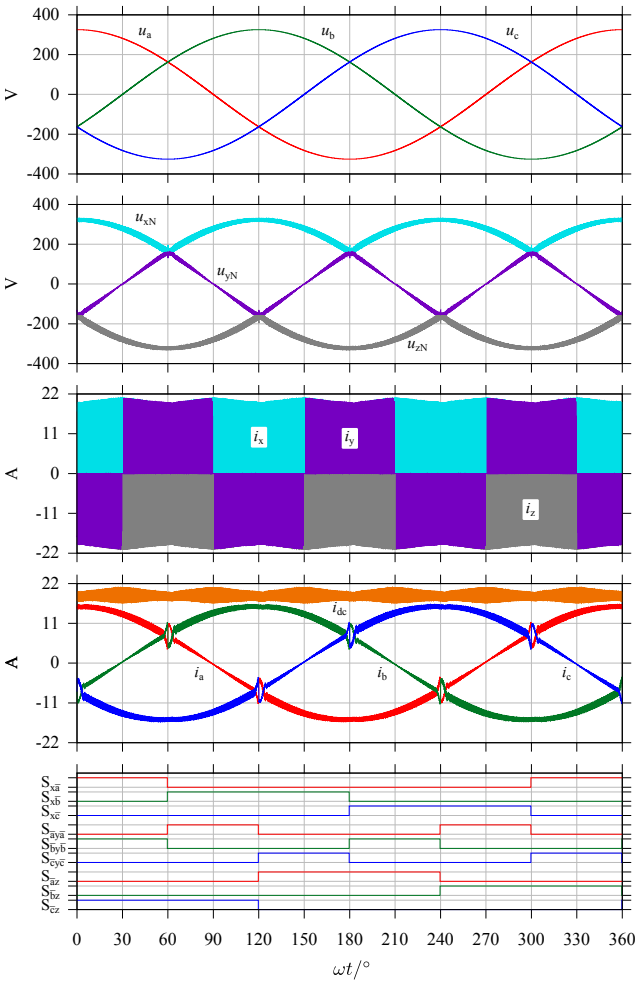

Fig. 2. Simulation results for the SWISS Rectifier specified in **Table I**, in ac-to-dc operation at nominal power. u_xN, u_yN and u_zN are the dc side voltages of the IVS with reference to the ac mains' neutral N, i_x, i_y and i_z are the corresponding IVS output currents. The distortions of the ac input currents $i_\mathrm{a,b,c}$ at intersections of the line voltages $u_\mathrm{a,b,c}$ are visible. A low frequency (< 10 kHz), i.e. not considering switching frequency components, input current THD of 4.2 % results.

TABLE I
SPECIFICATIONS OF SIMULATED SWISS RECTIFIER

Ac Input Voltage (Line to Neutral)	$U_1 = 230\,\mathrm{V_{rms}}$
Ac Input Frequency	$f = 50\,\mathrm{Hz}$
Switching Frequency	$f_\mathrm{s} = 36\,\mathrm{kHz}$
Nominal dc Voltage	$U_\mathrm{pn} = 400\,\mathrm{V}$
Dc Link Capacitance	$C_\mathrm{pn} = 470\,\mu\mathrm{F}$
Dc Link Inductance	$L_\mathrm{p,n} = 250\,\mu\mathrm{H}$
Dc Output Power	$P = 7.5\,\mathrm{kW}$
Ac Filter Capacitance	$C_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}} = 4.4\,\mu\mathrm{F}$
Dc Filter Capacitance	$C_\mathrm{x,y,z} = 4.4\,\mu\mathrm{F}$
Ac Filter Inductance	$L_\mathrm{f} = 120\,\mu\mathrm{H}$
Ac Filter Damping	$L_\mathrm{d} = 120\,\mu\mathrm{H}$
Ac Filter Damping	$R_\mathrm{d} = 6.8\,\Omega$

interval of the line voltages u_a and u_b are shown in **Fig. 3**. Additionally the voltages $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ across the respective input filter capacitors and their local averages $\langle u_{\mathrm{C}\bar{\mathrm{a}}} \rangle_{T_\mathrm{s}}$, $\langle u_{\mathrm{C}\bar{\mathrm{b}}} \rangle_{T_\mathrm{s}}$ over one switching period T_s are shown. Neglecting the voltage drop due to the fundamental of the phase current i_a across L_f, the local average $\langle u_{\mathrm{C}\bar{\mathrm{a}}} \rangle_{T_\mathrm{s}}$ equals the corresponding

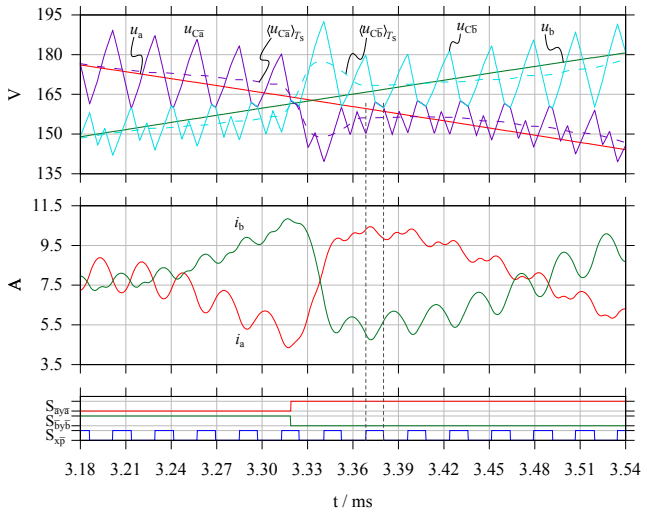

Fig. 3. Detailed simulation results for the first intersection at $\omega t \approx \pi/3$ showing the intersecting line voltages u_a and u_b and the corresponding filter capacitor voltages $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$. $\langle u_{\mathrm{C}\bar{\mathrm{a}}}\rangle_{T_\mathrm{s}}$ is the average of $u_{\mathrm{C}\bar{\mathrm{a}}}$ over one switching frequency period T_s. It can be seen that no intersection of $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ occurs because of $\mathrm{D}_{\bar{\mathrm{a}}\mathrm{x}}$ and $\mathrm{D}_{\bar{\mathrm{b}}\mathrm{x}}$ (cf. **Fig. 4**).

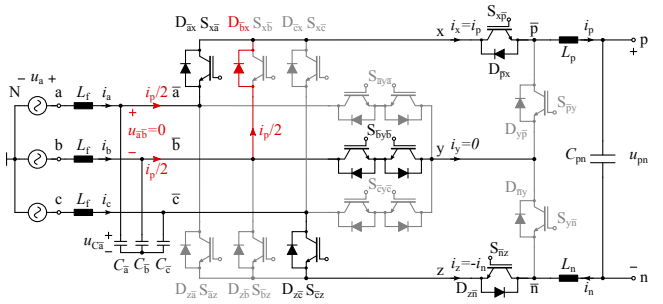

Fig. 4. Schematic of the SWISS Rectifier with $\mathrm{S}_{\mathrm{x}\bar{\mathrm{p}}}$ turned on, showing the additional conduction path caused by the diode $\mathrm{D}_{\bar{\mathrm{b}}\mathrm{x}}$ when the voltage $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}}$, i.e. the difference of the voltages of the filter capacitors $C_{\bar{\mathrm{a}}}$ and $C_{\bar{\mathrm{b}}}$ reaches zero. This implies $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}} \geq 0$ as long as $\mathrm{D}_{\bar{\mathrm{a}}\mathrm{x}}/\mathrm{S}_{\mathrm{x}\bar{\mathrm{a}}}$ and $\mathrm{S}_{\bar{\mathrm{b}}\mathrm{y}\bar{\mathrm{b}}}$ are turned on, which means that $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ cannot intersect (cf. **Fig. 3**).

phase voltage u_a before the current distortion starts. The same holds for $\langle u_{\mathrm{C}\bar{\mathrm{b}}}\rangle_{T_\mathrm{s}}$ and u_b. As the voltages u_a and u_b approach each other, the instantaneous voltages $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ would have to intersect for this to hold true. However, this is not the case as shown in **Fig. 3**, because the diodes $\mathrm{D}_{\bar{\mathrm{a}}\mathrm{x}}$ and $\mathrm{D}_{\bar{\mathrm{b}}\mathrm{x}}$ are starting to conduct once $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}} = u_{\mathrm{C}\bar{\mathrm{a}}} - u_{\mathrm{C}\bar{\mathrm{b}}}$ reaches zero (cf. **Fig. 4**). Therefore the local averages $\langle u_{\mathrm{C}\bar{\mathrm{a}}}\rangle_{T_\mathrm{s}}$ and $\langle u_{\mathrm{C}\bar{\mathrm{b}}}\rangle_{T_\mathrm{s}}$ no longer match the corresponding phase voltages u_a and u_b. This impresses a voltage on the input filter inductors L_f, which leads to a distortion of the input currents i_a and i_b, as shown in **Fig. 3**.

Therefore, in the following a modified circuit topology which reduces the conduction losses in the IVS and decouples the switching operation of the dc-dc converters and the IVS is proposed which allows to mitigate the input current distortions. For this circuit, an analysis of the current distortion's impact on the converter's THD is given in **Chapter III**. Subsequently, a novel modulation concept, which mitigates the current distortions by temporary pulse width modulation of the IVS switches

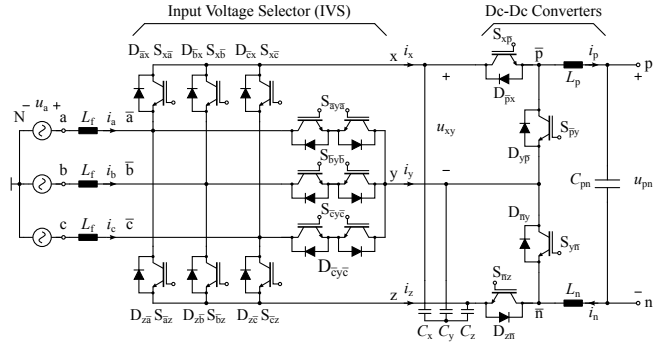

Fig. 5. Schematic of the bidirectional SWISS Rectifier with input filter capacitors placed at the dc side of the IVS. A star connection of filter capacitor is shown here, however a line-to-line (delta) connection could be used as well. The same input filter damping structure as in the original SWISS Rectifier with ac side input filter capacitors can be used.

is introduced in **Chapter IV**. In **Chapter V** measurement results, taken on a 7.5 kW prototype SWISS Rectifier, are presented which verify the theoretical considerations.

II. DC Side Filter Capacitors

As written above, an implementation of the SWISS Rectifier typically requires additional filter capacitors C_f' in order to shorten the commutation paths of the two dc-dc converters as shown in **Fig. 1**. Therefore, nodes x, y and z form a kind of split dc link which provides the input voltages u_xy and u_yz for the dc-dc converters. However, as the switches of the IVS are operated at mains frequency only, the voltages u_xN, u_yN and u_zN, are piecewise sinusoidal and hence form a three-phase system (cf. **Fig. 2**). This allows to move the input filter capacitors to the dc side of the IVS as shown in **Fig. 5**.

Throughout this paper a star connection of the filter capacitors (C_x, C_y and C_z) is assumed. However, a line-to-line (delta) connection could be used as well. Note that a total of three capacitors of equal capacitance is required in order to load the ac mains symmetrically, even for a delta connection, as the voltages at nodes x, y and z are piecewise sinusoidal and form a three phase system within every 60° mains voltage sector.

Placing the input filter capacitors on the dc side of the IVS has several advantages: It shortens the commutation paths of the dc-dc converters which means that no additional capacitors C_f' are required. Furthermore, the currents i_x, i_y and i_z flowing through the IVS are continuous in the case of dc side filter capacitors, as the IVS switches are operated at mains frequency only and hence the filter inductors L_f directly impress the IVS currents i_x, i_y and i_z during each mains voltage sector. **Fig. 6** shows simulation results for the same operating conditions as in **Fig. 2** but with dc side EMI filter capacitors. It can be seen that i_x, i_y and i_z are continuous exception in the vicinity of the mains voltage intersections. This is not the case for the original SWISS Rectifier where i_x, i_y and i_z are discontinuous due to the dc-dc converters, which leads to a reduction of conduction losses in the IVS switches. Assuming purely sinusoidal currents $i_{\mathrm{a,b,c}}$ in the ac input filter inductors L_f and a constant output inductor current

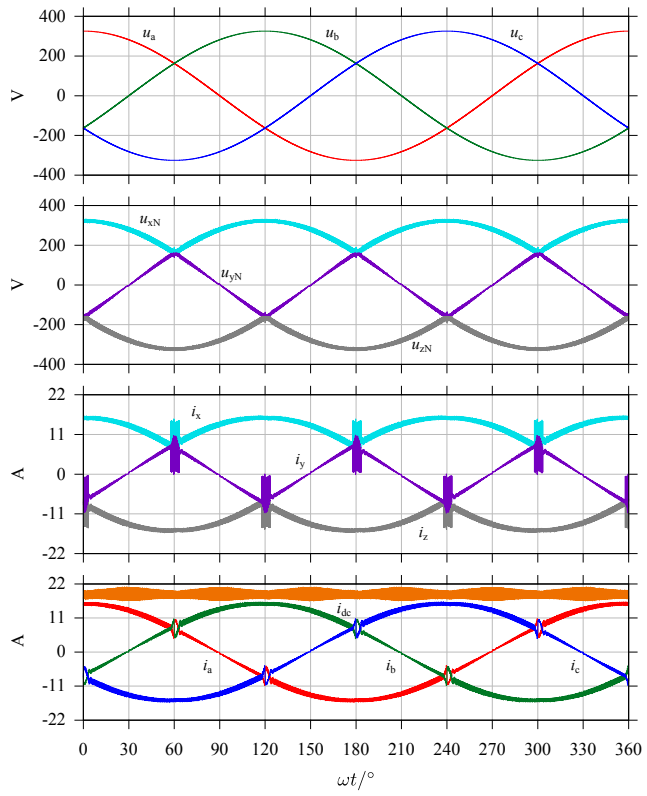

Fig. 6. Simulation results for a SWISS Rectifier with input filter capacitors $C_{x,y,z}$ placed on the dc side of the IVS as shown in **Fig. 5** for the same operating conditions as in **Fig. 2**. Similar input current distortions as in **Fig. 2** result, however the IVS currents i_x, i_y and i_z are now continuous except in the vicinity of the mains voltage intersections.

$i_p = i_n = I_{dc}$ the rms value of the rectifier diode $D_{\bar{k}x}$, $D_{z\bar{k}}$ current can be calculated as

$$I_{D\bar{k}x,rms} = I_{dc}\, M \sqrt{\frac{\sqrt{3}}{8\,\pi} + \frac{1}{6}} \tag{1}$$

where I_{dc} is the dc output current and $M \in [0,1]$ is the rectifiers modulation index. For a conventional SWISS Rectifier with ac side filter capacitors (cf. **Fig. 1**) the corresponding value is given by:

$$I_{D\bar{k}x,rms,conv} = I_{dc} \sqrt{\frac{\sqrt{3}\,M}{2\,\pi}} \tag{2}$$

[30]. Note that the diodes' average current does not change. Assuming a typical forward voltage drop of $U_f \approx 0.8\,V$ and series resistance of $r_f \approx 33\,m\Omega$ for the IVS diodes, $I_{dc} = 20\,A$ and a modulation index of $M = 0.8$ the conduction losses of the diodes reduce by $14\,\%$. If MOSFETs are used as synchronous rectifiers instead of diodes in the IVS the reduction would be approximately $31\,\%$ for $M = 0.8$. Similarly the rms current in the injection switches and diodes $S_{\bar{k}y\bar{k}}$ can be calculated as:

$$I_{S\bar{k}y\bar{k},rms} = I_{D\bar{k}y\bar{k},rms} = I_{dc}\, M \sqrt{\frac{1}{12} - \frac{\sqrt{3}}{8\,\pi}} \quad , \tag{3}$$

and the corresponding value with ac side EMI filter capacitors is given by:

$$I_{S\bar{k}y\bar{k},rms,conv} = I_{dc} \sqrt{M\,\frac{2-\sqrt{3}}{2\,\pi}} \quad . \tag{4}$$

Assuming the same parameters as above the conduction losses of the injection circuit diodes and IGBTs reduce by $33\,\%$ and by $73\,\%$ if MOSFETs are used. The same values result for dc-to-ac power transfer in bidirectional SWISS Rectifiers.

Additionally, the dc side capacitors decouple the switching operations of the IVS and the dc-dc converters. In the original bidirectional SWISS Rectifier, special commutation sequences are required in the IVS in order not to interrupt the currents i_p and i_n in the output inductors [7]. This is not the case with dc side input filter capacitors, as C_x, C_y and C_z provide a conduction path for the IVS and the dc-dc converter currents at all valid switching states.

This implies that the SWISS Rectifier with dc side filter capacitors can, to some extent, be considered as a system consisting of two individual converters: an IVS stage which performs an ac-to-dc voltage conversion and a dc-dc converter stage which ensures sinusoidal input currents and provides dc output voltage control. Therefore, the IVS and the dc-dc converters can be designed, optimized and operated almost independently of each other. For example, several individual dc-dc converter modules could be fed from a single, high power IVS which provides the voltages on the x, y, z busses. In this case, the IVS and the dc-dc converters could even be spatially separated, for example accommodated in different cabinets.

Note that moving the filter capacitors to the dc side of the IVS implies that the reactive power demand of the capacitors causes a phase shift of the IVS currents i_x, i_y and i_z. In nominal operation this phase shift is typically small, for the rectifier specified in **Table I** a phase shift of $1.7°$ results. However, the phase shift angle increases with reducing load as the active power drawn from the mains decreases. This can cause non-sinusoidal input currents in unidirectional SWISS Rectifiers at very light load ($< 5.1\,\%$ for the system specified in **Table I**) as i_x and i_z cannot reverse due to the diode rectifier $D_{\bar{a}x}$, $D_{\bar{b}x}$, $D_{\bar{c}x}$ and $D_{z\bar{a}}$, $D_{z\bar{b}}$, $D_{z\bar{c}}$ and hence the IVS currents cannot lead the mains voltage by more than $30°$ [31]. Similar current distortions exist in single-phase boost-type PFC rectifiers if a filter capacitor is placed on the dc side of the input rectifier [32].

III. Input Current Distortions

As described **Chapter I** the conventional SWISS Rectifier exhibits ac input current distortions at the intersections of the mains' phase voltages. This is due to the switching frequency voltage ripples at the input filter capacitors which cause additional diodes in the IVS to conduct as shown in **Fig. 4**. Two modified modulation strategies, reducing the distortions for the conventional SWISS Rectifier with ac side filter capacitors are described in [27]. The same current distortions result for the modified SWISS Rectifier with dc side input filter capacitors C_x, C_y, C_z shown in **Fig. 5**. In this case the voltage

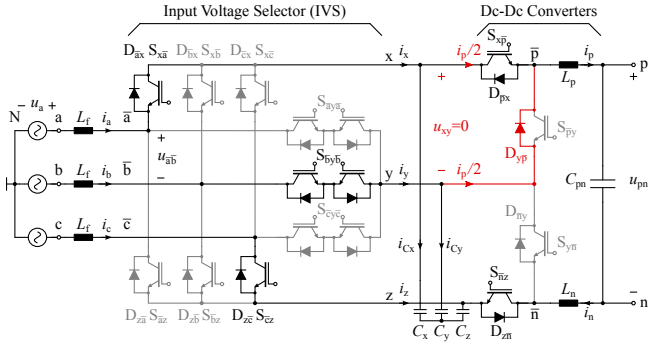

Fig. 7. Schematic of the SWISS Rectifier with $S_{x\bar{p}}$ turned on, showing the additional conduction path caused by the diode $D_{y\bar{p}}$ when the voltage u_{xy} across the filter capacitors C_x and C_y reaches zero. This implies that $u_{xy} \geq 0$ (cf. **Fig. 8**).

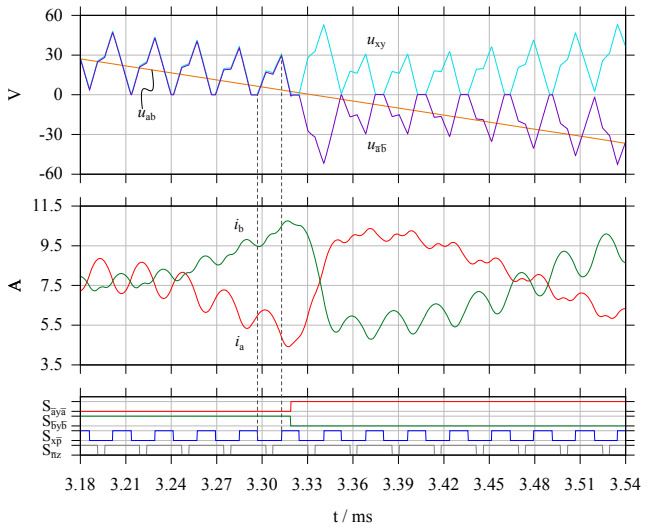

Fig. 8. Detailed simulation results for the first sector boundary (at $\omega t \approx \pi/3$) with input filter capacitors on the dc side of the IVS (C_x, C_y and C_z, cf. **Fig. 7**). It can be seen that u_{xy} cannot become negative because of $D_{y\bar{p}}$. This implies that the average over one switching period of the voltage $u_{\bar{a}\bar{b}}$ at the input of the IVS differs significantly from the corresponding grid voltage u_{ab}. Accordingly a distortion of the input currents i_a and i_b occurs.

ripples across C_x, C_y and C_z cause diodes of turned-off dc-dc converter switches to conduct as shown in **Fig. 7**. This results in the same grid current distortions as with ac side filter capacitors, as can be seen from the simulation results shown in **Fig. 8**. An analysis of these current distortions, including the impact on the ac currents' THD, is given in the following. Based on this analysis a temporary pulse width modulation of the IVS switches is proposed in **Chapter IV** which allows a mitigation of the distortions if dc side filter capacitors are used.

In order to derive an analytical model of the current distortions the switching frequency ripple components of the currents in L_f and $L_{p,n}$ are neglected and $i_p = i_n = I_{dc}$ is assumed. The mains voltages and currents are considered to be purely sinusoidal. Due to the phase symmetry it is sufficient to consider only the first intersection of u_a and u_b, i.e. $\omega t \approx \pi/3$. The filter capacitors are assumed to have equal capacitance, i.e. $C_x = C_y = C_z = C_f$.

As explained above, the switching frequency ripple across the input filter capacitors is the root cause of the current distortions. Therefore, an analytical expression for its peak-to-peak value $\hat{u}_{xy}$ is required. Assuming in-phase carriers for $S_{x\bar{p}}$ and $S_{\bar{n}z}$ it can be seen from **Fig. 8** that u_{xy} assumes the peak value at the switching transitions of $S_{x\bar{p}}$. The peak-to-peak ripple can therefore be calculated as:

$$\begin{aligned}\hat{u}_{xy} &= \frac{1}{C_f}\int_0^{(1-d_p)/f_s} i_{Cx} - i_{Cy}\, d\tau \\ &= \frac{1}{f_s\, C_f}\left[(i_x - i_y)\,(1-d_p) + I_{dc}\,(d_n - d_p)\right] , \end{aligned} \tag{5}$$

where d_p is the duty cycle of $S_{x\bar{p}}$ and d_n is the duty cycle of $S_{\bar{n}z}$. Assuming that the SWISS Rectifier is operated such that the ac gird currents are in phase with the gird voltages and that the current distortion is short compared to the grid voltage period the following simplifications hold:

$$d_p = M\cos(\omega\, t) \approx \frac{M}{2} \qquad \omega t \approx \frac{\pi}{3} \tag{6}$$

$$d_n = M\cos(\omega\, t - \frac{\pi}{3}) \approx M\ . \tag{7}$$

Note that M is the modulation index of the SWISS Rectifier. Neglecting any voltage drops across the switches, diodes and filter inductors, the steady state voltage transfer ratio between ac and dc side is defined as

$$U_{pn} \approx U_{p\bar{n}} = M\,\hat{U}_1\,\frac{3}{2} \qquad M = \frac{U_{pn}}{\frac{3}{2}\hat{U}_1} \in [0,1]\ , \tag{8}$$

where $\hat{U}_1$ is the amplitude of the ac grid's phase voltage [30]. By neglecting the grid frequency component of the filter capacitor current $i_{Cx,y,z}$ further simplifications can be found:

$$i_x = I_{dc}\, d_p \approx I_{dc}\frac{M}{2} \tag{9}$$

$$i_z = -I_{dc}\, d_n \approx -I_{dc}\, M \tag{10}$$

$$i_y = -(i_x + i_z) \tag{11}$$

By combining (5) to (11) $\hat{u}_{xy}$ can approximated as

$$\hat{u}_{xy} = \frac{I_{dc}\, M}{2\, C_f\, f_s}\ . \tag{12}$$

When the line-to-line voltage u_{ab} becomes smaller than half the voltage ripple $\hat{u}_{xy}$ calculated in (5) or (12), the current distortion starts. Hence, the time span $t_d/2$ from the beginning of the distortion until the zero crossing of the line-to-line voltage u_{ab} can be derived:

$$u_{ab}\left(\frac{\pi}{3} - \frac{\omega\, t_d}{2}\right) = \sqrt{6}\, U_1 \sin\left(\frac{\omega\, t_d}{2}\right) = \frac{\hat{u}_{xy}}{2}\ , \tag{13}$$

$$\frac{t_d}{2} = \frac{1}{\omega}\arcsin\left(\frac{I_{dc}\, M}{4\sqrt{6}\, U_1\, C_f\, f_s}\right) \approx \frac{1}{\omega}\frac{I_{dc}\, M}{4\sqrt{6}\, U_1\, C_f\, f_s}\ . \tag{14}$$

At the beginning of the current distortion $\langle u_{xy}\rangle_{T_s}$ (the average of u_{xy} over one switching period T_s) is equal to the gird voltage u_{ab}. As can be seen from **Fig. 8**, in the center of the distortion (at $u_{ab} = 0$), the ripple of u_{xy} is approximately half the value compared to the point in time where the current

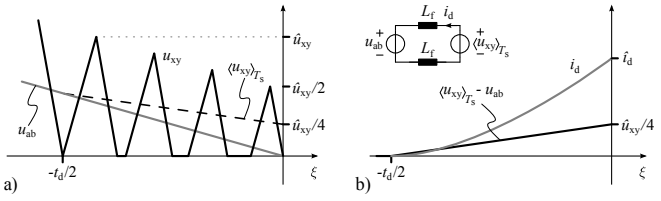

Fig. 9. Drawing (not to scale) of the assumptions made to derive (16). At the beginning of the distortion ($\xi = -t_\mathrm{d}/2$) the local average $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}$ of u_xy equals the grid voltage u_ab. The difference of $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}$ and u_ab increases linearly until $\xi = 0$ where it reaches a peak value of $\hat{u}_\mathrm{xy}/4$. This voltage, $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}} - u_\mathrm{ab}$, drives the distortion current i_d in the filter inductors of the corresponding phases.

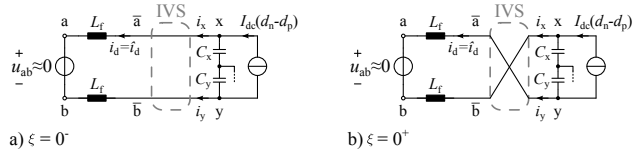

Fig. 10. Simplified schematics of the two phases with intersecting voltages: **a)** before the IVS changes polarity at $\xi = 0$ and **b)** immediately afterwards. The distortion current i_d flowing in the filter inductors L_f leads to a rapid change of u_xy after the IVS commutation as i_x and i_y change polarity.

distortion starts. Therefore the local average $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}$ of u_xy is approximated by a linear function as shown in **Fig. 9 a)**:

$$\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}(\xi) = \frac{\hat{u}_\mathrm{xy}}{4}\left[1 - \frac{\xi}{t_\mathrm{d}/2}\right] \quad \text{for} \quad \xi \in [-t_\mathrm{d}/2, 0] \ . \tag{15}$$

During the distortion, the voltage difference between $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}$ and u_ab is impressed on the input filter inductors which causes a circulating distortion current i_d.

This is shown in **Fig. 9b)** and it enables an estimation of the distortion current's amplitude $\hat{i}_\mathrm{d}$ using (13), (15) and $\sin(\omega t) \approx \omega t$:

$$\begin{aligned}\hat{i}_\mathrm{d} &= \frac{1}{2\,L_\mathrm{f}}\int_{-t_\mathrm{d}/2}^{0} u_\mathrm{xy}\left(\frac{\pi}{3} + \xi\,\omega\right) - u_\mathrm{ab}\left(\frac{\pi}{3} + \xi\,\omega\right) d\xi \ , \\ &\approx \frac{1}{2\,L_\mathrm{f}}\int_{-t_\mathrm{d}/2}^{0} \frac{\hat{u}_\mathrm{xy}}{4} + \frac{\hat{u}_\mathrm{xy}}{4}\frac{\xi}{t_\mathrm{d}/2}\,d\xi = \frac{\hat{u}_\mathrm{xy}\,t_\mathrm{d}}{32\,L_\mathrm{f}} \ . \end{aligned} \tag{16}$$

So far only the first half of the distortion, until u_ab reaches zero (at $\xi = 0$) was considered. Once u_ab changes its sign, the IVS commutates in order to reverse the polarity of $u_{\bar{a}\bar{b}}$. This is shown in the simplified schematics in **Fig. 10**. Note, that the polarity reversal of the IVS changes the sign of the IVS' dc side currents i_x and i_y. This leads to a considerably higher peak value of u_xy during the first switching period after the polarity reversal. Therefore a higher voltage is applied to the filter inductors L_f in this cycle which leads to a fast polarity reversal of the distortion current i_d. This can also be seen in the simulation results shown in **Fig. 8**. The current distortion is therefore approximately symmetric in time around the zero crossing of the line-to-line voltage u_ab (at $\omega t = \pi/3$).

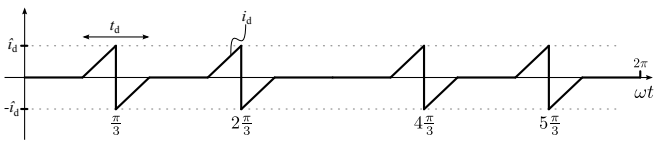

Fig. 11. Simplified distortion current within one mains period assumed for the rms-value calculation used to derive (17).

For further analysis the converter's grid currents $i_\mathrm{a,b,c}$ are approximated as sum of a fundamental component $i_\mathrm{a,b,c(1)}$ which is in phase with the grid voltages and a distortion i_d. Each phase is distorted four times per gird voltage period. By modeling each distortion as one triangular wave with a period of t_d and amplitude $\hat{i}_\mathrm{d}$ (cf. **Fig. 11**), the rms value I_d of i_d can be calculated as

$$I_\mathrm{d} = \frac{\hat{i}_\mathrm{d}}{\sqrt{3}}\sqrt{4\,t_\mathrm{d}\,f} \ . \tag{17}$$

In order to determine the impact of (17) on the converter's THD, the following normalization is applied:

$$C_\mathrm{f} = \frac{Q_\mathrm{f}}{3\,U_1^2\,\omega} \quad Q_\mathrm{f} = P\tan(\phi_1) \ , \tag{18}$$

$$L_\mathrm{f} = L_\mathrm{f,p.u.}\frac{R_1}{\omega} = L_\mathrm{f,p.u.}\frac{3\,U_1^2}{\omega\,P} \quad R_1 = \frac{3\,U_1^2}{P} \ , \tag{19}$$

$$I_\mathrm{dc}\,M = \hat{I}_\mathrm{a,b,c(1)} = \frac{2\,P}{3\,\hat{U}_1} \ . \tag{20}$$

Note that ϕ_1 represents the phase shift of the input current's fundamental which results from the reactive power consumption of the input filter capacitors. The reactive power created by the filter inductors is neglected as it is typically much smaller than the Q_f.

By combining (17) with (12)-(16) and applying the normalizations (18)-(20) the normalized RMS value of the current distortions can be expressed as a function of general system parameters:

$$\frac{I_\mathrm{d}}{I_\mathrm{a,b,c(1)}} = \frac{\pi^2}{16\cdot 3^{5/4}}\frac{1}{L_\mathrm{f,p.u.}}\left(\frac{f}{f_\mathrm{s}}\frac{1}{\tan(\phi_1)}\right)^{5/2} \ , \tag{21}$$

where $I_{a,b,c(1)}$ is the RMS value of the ac side input currents' fundamental component at nominal power. This allows an estimation of the current distortions' impact on the rectifier's input current THD. It can be seen that increasing the switching frequency or the input filter capacitors (increasing ϕ_1) reduces the magnitude of the current distortions with a power of 2.5, while it is inversely proportional to the input filter inductance.

Table II shows the numerical results for the equations derived above and compares the values to results obtained from a simulation of the system specified in **Table I**. The calculated values are typically within 10 % of the simulation results. Furthermore, it can be seen that the low frequency THD[1] (not considering switching frequency components) of the rectifier's input currents is 4.2 %.

IV. Mitigating Distortions by PWM of the IVS

As described in the previous chapter, the ac input current distortions can have a significant contribution to the THD of a SWISS Rectifier. For the system specified in **Table I** current distortions with a normalized RMS value of 4.2 % result. However, the distortions can be prevented by properly modulating the switches in the IVS as will be shown in the following.

[1]Spectral components up to 10 kHz, i.e. up to the 200th harmonic of the mains frequency, are considered.

TABLE II
COMPARISON BETWEEN CALCULATION AND SIMULATION

	Calculated	Simulated	Error
$\hat{u}_{xy}$	48.6 V	43.4 V	12 %
t_d	275 µs	279 µs	−1.4 %
$\hat{i}_d$	3.48 A	3.34 A	4.2 %
$I_d/I_{a,b,c(1)}$ (THD)	4.31 %	4.23 %	1.9 %

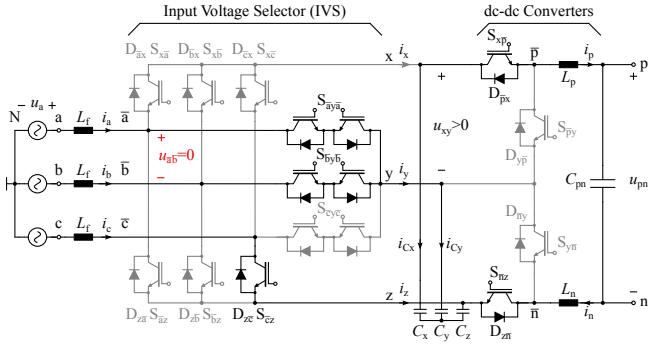

Fig. 12. SWISS Rectifier with dc side input filter capacitors and ac-to-dc power transfer during the first intersection of u_a and u_b. By turning $S_{x\bar{a}}$ off and turning on $S_{\bar{a}y\bar{a}}$ the IVS' output voltage $u_{\bar{a}\bar{b}}$ is forced to zero.

The root cause of the current distortions is the switching frequency voltage ripple across the input filter capacitors and the fact that the voltages u_{xy} and u_{yz} cannot be negative (cf. **Fig. 8**). However, if the input filter capacitors are placed on the dc side of the IVS, the IVS can be used to temporarily disconnect the filter capacitors $C_{x,y,z}$ from the filter inductors L_f by simultaneously turning on two of the three injection switches, e.g. $S_{\bar{a}y\bar{a}}$ and $S_{\bar{b}y\bar{b}}$. This short-circuits the corresponding input nodes $\bar{a}$ and $\bar{b}$ and results in $u_{\bar{a}\bar{b}} = 0$, as shown in **Fig. 12**. Therefore, it is possible to mitigate the current distortions by toggling the second injection switch such that the average over one switching period of $u_{\bar{a}\bar{b}}$ equals the gird voltage u_{ab}.

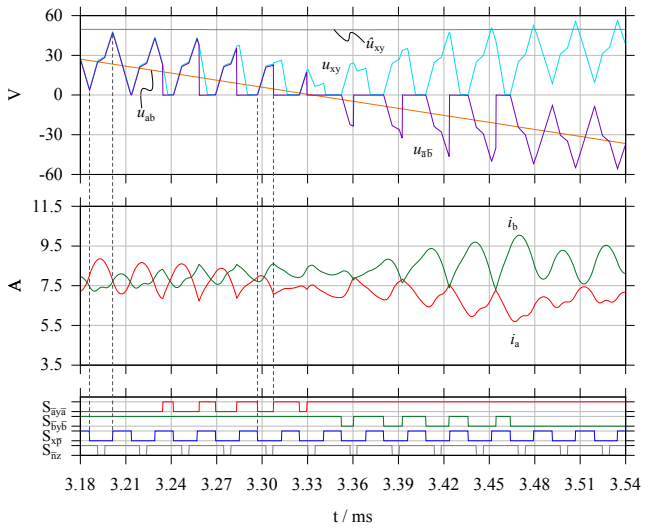

Fig. 13. Simulation results, showing pulse width modulated injection switches $S_{\bar{a}y\bar{a}}$ and $S_{\bar{b}y\bar{b}}$ during the first intersection of u_a and u_b which reduces the current distortions. Furthermore, the calculated peak-to-peak ripple of u_{xy} is shown as $\hat{u}_{xy}$.

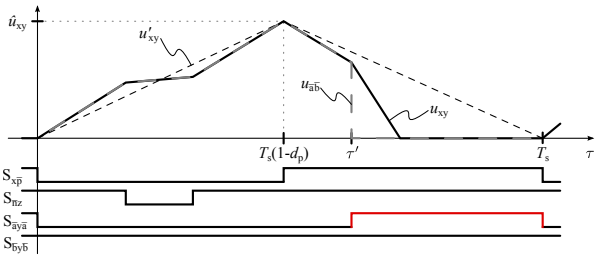

Fig. 14. Time behavior of the filter capacitor voltage ripple u_{xy} within one switching period T_s for ac-to-dc power transfer. The signal u'_{xy} is used as approximation for u_{xy} in order to simplify the algebraic calculations.

A. Ac-to-Dc Power Transfer with In-Phase Carriers

The following considerations focus on the intersection of u_a and u_b at $\omega t \approx \pi/3$ with ac-to-dc power transfer and in-phase carriers of the two buck converters. It can be seen from **Fig. 13** that u_{xy} increases while $S_{x\bar{p}}$ is not conducting, which implies that u_{xy} is minimal when $S_{x\bar{p}}$ is turned off. Therefore, the turn-off of $S_{x\bar{p}}$ is selected as origin for an auxiliary time axis τ.

Fig. 14 shows a diagram of the filter capacitor voltage u_{xy} during the first half of the first intersection ($\omega t \leq \pi/3$, $u_a > u_b$). The additional injection switch $S_{\bar{a}y\bar{a}}$ is turned on at time τ' and is turned off together with $S_{x\bar{p}}$ in order to allow u_{xy} to charge. In order to simplify the analytical calculations u'_{xy} is used as an approximation for u_{xy}:

$$u'_{xy}(\tau) = \begin{cases} \hat{u}_{xy} \frac{\tau}{(1-d_p)\,T_s} & \text{if } \tau \leq (1-d_p)\,T_s \\ \hat{u}_{xy} \frac{1}{d_p}\left(1 - \frac{\tau}{T_s}\right) & \text{if } \tau > (1-d_p)\,T_s\,, \end{cases} \tag{22}$$

$$u_{\bar{a}\bar{b}}(\tau) = \begin{cases} u_{xy}(\tau) \approx u'_{xy}(\tau) & \text{if } \tau \leq \tau' \\ 0 & \text{if } \tau > \tau'\,. \end{cases} \tag{23}$$

Note that either equation (5) or (12) can be used to estimate the peak value $\hat{u}_{xy}$. The average $\langle u_{\bar{a}\bar{b}}(\tau)\rangle_{T_s}$ over one switching frequency period T_s of the IVS output voltage $u_{\bar{a}\bar{b}}$ can be found by integration:

$$\langle u_{\bar{a}\bar{b}}(\tau')\rangle_{T_s} = \frac{1}{T_s}\int_0^{\tau'} u_{xy}(\tau)\,d\tau \approx \frac{1}{T_s}\int_0^{\tau'} u'_{xy}(\tau)\,d\tau\,. \tag{24}$$

In order to prevent the current distortions τ' has to be selected such that $\langle u_{\bar{a}\bar{b}}(\tau')\rangle_{T_s}$ equals the corresponding ac grid voltage u_{ab} which is used as reference value u_{ref}:

$$u_{ref} = u_a - u_b = u_{ab} \tag{25}$$

By solving (24) an algebraic expression for τ' can be found:

$$u_{ref} = \langle u_{\bar{a}\bar{b}}(\tau')\rangle_{T_s} \quad \Rightarrow$$
$$\tau' = T_s \begin{cases} \sqrt{2\,\frac{u_{ref}}{\hat{u}_{xy}}\,(1-d_p)} & \text{if } u_{ref} \leq \hat{u}_{xy}\,\frac{1-d_p}{2} \\ 1 - \sqrt{d_p - 2\,d_p\,\frac{u_{ref}}{\hat{u}_{xy}}} & \text{if } u_{ref} > \hat{u}_{xy}\,\frac{1-d_p}{2}\,. \end{cases} \tag{26}$$

This implies that the current distortions can be mitigated by measuring the grid voltages and evaluating equations (5), (25) and (26) every switching frequency cycle. The additional

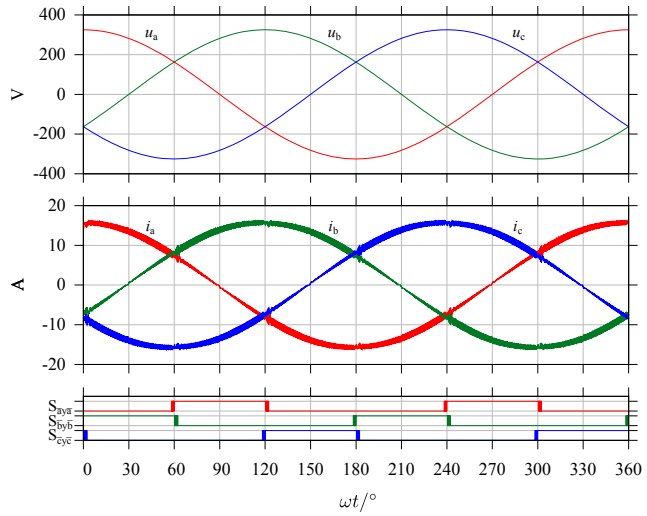

Fig. 15. Simulation results for the SWISS Rectifier specified in **Table I** using the proposed modulation technique for the IVS switches. Compared with the results in **Fig. 2**, the current distortions are significantly reduced, the low frequency ($< 10\,\mathrm{kHz}$) THD of $i_{a,b,c}$ reduces from $4.2\,\%$ to $0.8\,\%$.

injection switch $S_{\bar{a}y\bar{a}}$ is then turned on at time τ' after the turn-off of $S_{x\bar{p}}$.

All considerations and calculations given above hold only for the first half of the first current distortion, i.e. for $\omega t < \pi/3$. In the second half ($\omega t > \pi/3$) the grid voltage u_{ab} becomes negative which implies that the output voltage of the IVS has to be negative as well, while the filter capacitor voltage u_{xy} remains positive. This is achieved by modulating $S_{\bar{b}y\bar{b}}$ instead of $S_{\bar{a}y\bar{a}}$, as can be seen in **Fig. 13**. By replacing the grid voltages u_a and u_b and the injection switches with the corresponding values, this can be generalized for the other two positive grid voltage intersections ($\omega t \approx 180°, 300°$). Furthermore, the concept can be expanded to the negative side dc-dc converter ($S_{\bar{n}z}$, d_n, u_{yz}) to mitigate the current distortions at the intersections of negative grid phase voltages ($\omega t \approx 0°, 120°, 240°$). The resulting formulas are summarized in **Table III**. Simulation results for ac-to-dc operation of the SWISS Rectifier with the compensation enabled for all intersections are shown in **Fig. 15**.

B. Interleaved Carriers

For the derivation of the formulas in **Chapter III** an operation of the SWISS Rectifier's dc-dc converters with in-phase carriers is assumed. As described in [30], this leads to minimal injection current (i_y) ripple. However, the dc-dc converters could also be controlled with interleaved carriers, i.e. using two independent carriers with a phase shift of $180°$. This minimizes the ripple in the dc output current $I_{dc} = i_p = i_n$, but increases the injection current's ripple (i_y). Note that an increase in injection current ripple implies an increase in the filter capacitor voltage ripple, i.e. of $\hat{u}_{xy}$ and $\hat{u}_{yz}$. Without compensation the current distortions are therefore higher compared to operation with in-phase carriers.

If interleaved carriers are used the sequence of conduction states within a switching period is different than for in-phase

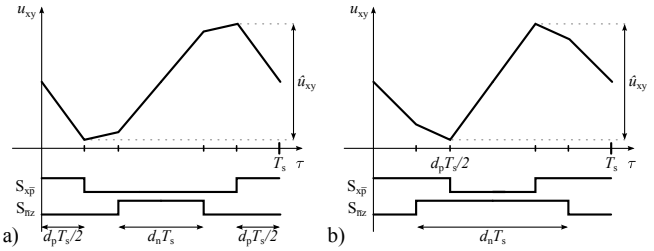

Fig. 16. Diagram of the filter capacitor voltage (u_{xy}) ripple for ac-to-dc power transfer with interleaved carriers. In **a)** $d_p + d_n < 1$ holds, which implies that an interval were both, $S_{x\bar{p}}$ and $S_{\bar{n}z}$, are off exists. This is not the case in **b)** where $d_p + d_n > 1$ holds and therefore $S_{\bar{n}z}$ is always on while $S_{x\bar{p}}$ is off.

carriers. This implies that different formulas for $\hat{u}_{xy}$ and $\hat{u}_{yz}$ result. In the following the intersection of $u_a > 0$ and $u_b > 0$ at $\omega t \approx \pi/3$ is considered. It can be seen from the SWISS Rectifier's schematic (**Fig. 5**) that u_{xy} decreases while $S_{x\bar{p}}$ is on as power is delivered to the DC output. Consequently u_{xy} increases while $S_{x\bar{p}}$ is off. However, two different sequences of switching states exist, depending on the modulation index of the converter, as shown in **Fig. 16**.

When $d_p + d_n < 1$ holds, $S_{\bar{n}z}$ switches while $S_{x\bar{p}}$ is off, resulting in the filter capacitor ripple depicted in **Fig. 16 a)**. In this case $\hat{u}_{xy}$ can be approximated as

$$\hat{u}_{xy,int,<1} = \frac{T_s}{C_f}\left[(i_x - i_y)\,(1 - d_p) + I_{dc} d_n\right] \qquad (27)$$

where T_s is the switching period of the DC-DC converters. For a high modulation index where $d_p + d_n > 1$ holds, $S_{\bar{n}z}$ is on while $S_{x\bar{p}}$ is off. The equation for $\hat{u}_{xy}$ than simplifies to

$$\hat{u}_{xy,int,>1} = \frac{T_s}{C_f}\left[(i_x - i_y + I_{dc})\,(1 - d_p)\right] \qquad (28)$$

Note that equations (27) and (28) yield the same value $\hat{u}_{xy}$ for the boundary case $d_p + d_n = 1$. Hence they can be combined into a continuous function:

$$\hat{u}_{xy,int} = \frac{T_s}{C_f}\begin{cases}(i_x - i_y)\,(1 - d_p) + I_{dc} d_n & \text{if } d_p + d_n \le 1\\ (i_x - i_y + I_{dc})\,(1 - d_p) & \text{if } d_p + d_n > 1\end{cases} \qquad (29)$$

An analog derivation can be used to obtain equations for the negative voltage intersections at $\omega t \approx 0°, 120°, 240°$ The resulting equations are summarized in the left column of **Table III**.

Note that the filter capacitor voltage u_{xy} assumes its peak value at the turn-on of $S_{x\bar{p}}$, as in the case of in-phase carriers (cf. **Fig. 13** and **Fig. 16**). Therefore the modulation technique described in **Chapter IV-A** can be used to mitigate the current distortions without any further modifications.

C. Dc-to-Ac Power Transfer

The previous descriptions focus on ac-to-dc power transfer, however, the current distortions exist for dc-to-ac power transfer ($i_p = i_n < 0$) as well. A similar mitigation strategy can be used as will be shown in the following.

As depicted in **Fig. 17** the diode $D_{\bar{p}x}$ starts to conduct for dc-to-ac power transfer once the filter capacitor voltage

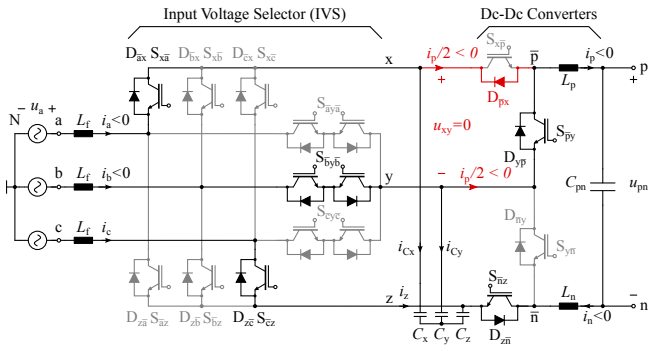

Fig. 17. Schematic of the SWISS Rectifier with dc-to-ac power transfer ($i_\mathrm{p} < 0$, $i_\mathrm{n} < 0$) during the first intersection of u_a and u_b. When the filter capacitor voltage u_xy reaches zero the diode $\mathrm{D}_{\bar{\mathrm{p}}\mathrm{x}}$ is forward biased and starts to conduct, thus preventing u_xy from reversing polarity. Therefore, similar input current distortions as for ac-to-dc power transfer result (cf. **Fig. 7**).

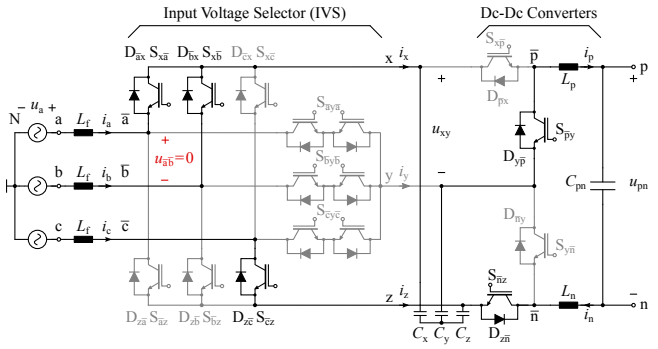

Fig. 18. SWISS Rectifier with dc-to-ac power transfer ($i_\mathrm{p} < 0$, $i_\mathrm{n} < 0$) during the first intersection of u_a and u_b. Two Rectifier switches ($\mathrm{S}_{\mathrm{x}\bar{\mathrm{a}}}$, $\mathrm{S}_{\mathrm{x}\bar{\mathrm{b}}}$) are turned on simultaneously ($\mathrm{S}_{\bar{\mathrm{b}}\mathrm{y}\bar{\mathrm{b}}}$ is turned off) in order to achieve $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}} = 0$.

u_xy reaches zero. Therefore, the local average of u_xy starts to deviate from the grid voltage u_ab once the ripple is larger than $2\,u_\mathrm{ab}$ as explained above for ac-to-dc power transfer. Thus similar grid current distortions result.

In order to temporarily disconnect the grid filter inductors L_f from the filter capacitors $C_\mathrm{x,y,z}$ two rectifier switches, e.g. $\mathrm{S}_{\mathrm{x}\bar{\mathrm{a}}}$, $\mathrm{S}_{\mathrm{x}\bar{\mathrm{b}}}$ are turned on simultaneously as shown in **Fig. 18**. Simulation results of a SWISS Rectifier using this modulation technique are shown in **Fig. 19**. Note that, unlike for ac-to-dc power transfer, it is not possible to modulate the injection switches $\mathrm{S}_{\bar{\imath}\mathrm{y}\bar{\imath}}$ ($\bar{\imath} = \bar{a}, \bar{b}, \bar{c}$) because u_xy has to be discharged to zero once the additional switch is turned on at τ'. It can be shown that this is the case only when the rectifier switches $\mathrm{S}_{\mathrm{x}\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}}$, $\mathrm{S}_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}\mathrm{z}}$ are modulated.

The equations required to implement the mitigation algorithm for dc-to-ac power transfer are summarized in the right column of **Table III**. Note that the switching transition which marks the beginning of the time span τ' is different than in ac-to-dc power transfer. **Fig. 20** shows simulation results for the SWISS Rectifier specified in **Table I** with 7.5 kW dc-to-ac power transfer. It can be seen that the current distortions are significantly reduced.

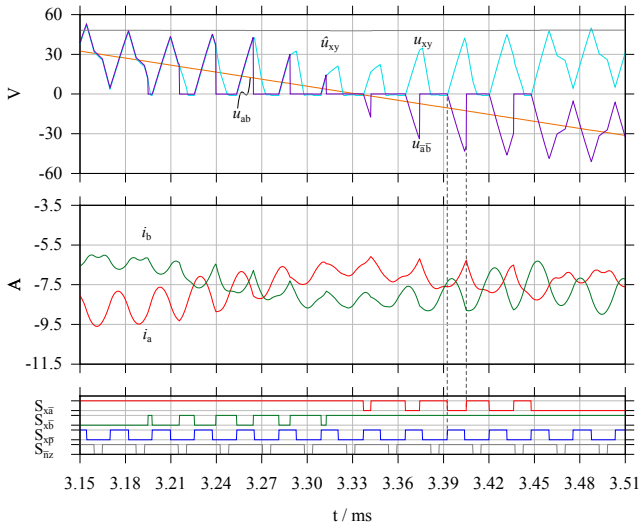

Fig. 19. Detailed simulation results for dc-to-ac power transfer and the first intersection of u_a and u_b showing the modulation of a second rectifier switch ($\mathrm{S}_{\mathrm{x}\bar{\mathrm{a}}}$, $\mathrm{S}_{\mathrm{x}\bar{\mathrm{b}}}$). The distortion in i_a and i_b is significantly reduced.

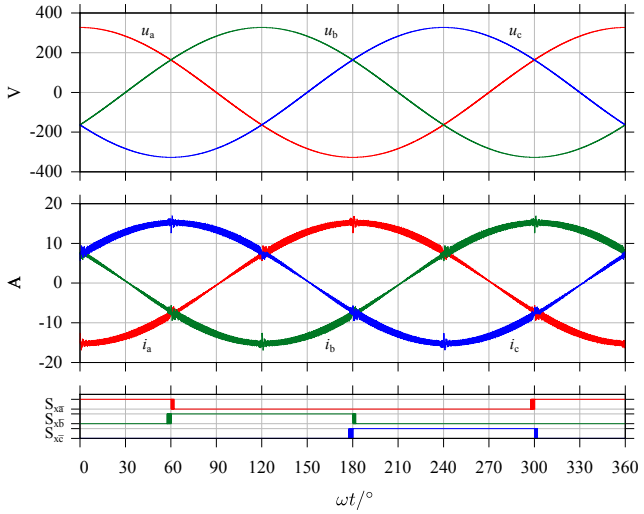

Fig. 20. Simulation results for the SWISS Rectifier specified in **Table I** with dc-to-ac power transfer and in-phase carriers. The proposed algorithm is used to mitigate the current distortions.

D. Robustness

In the previous analysis sinusoidal grid voltages and currents were assumed. This is typically not the case in the three-phase ac mains where some low frequency voltage harmonics and asymmetries are usually present. However, the proposed algorithm works even with non-sinusoidal and unsymmetrical mains voltages. This is possible as the switching frequency ripple of the filter capacitor voltages u_xy and u_yz can be estimated in real time using the currents i_x, i_y and i_z and the dc-dc converter duty cycles d_p and d_n. Note that no assumption about the shape of these signals is used in the derivation of the formulas listed in **Table III**. The reference signal u_ref is derived from the measured grid voltages $u_\mathrm{a,b,c}$, cf. (25). Again, no assumption about the actual signal shape of u_ref is required.

TABLE III
EQUATIONS REQUIRED TO IMPLEMENT THE DISTORTION MITIGATION ALGORITHM

Ac-to-Dc Power Transfer	**Dc-to-Ac Power Transfer**
Positive Voltage Intersections	
Origin of τ': $S_{x\bar{p}}$ $1 \rightarrow 0$	Origin of τ': $S_{x\bar{p}}$ $0 \rightarrow 1$
Modulation: $S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$, $S_{\bar{c}y\bar{c}}$	Modulation: $S_{x\bar{a}}$, $S_{x\bar{b}}$, $S_{x\bar{c}}$
$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{xy}}(1-d_p)} & \text{if } u_{ref} \le \hat{u}_{xy}\frac{1-d_p}{2} \\ 1-\sqrt{d_p\left(1-2\frac{u_{ref}}{\hat{u}_{xy}}\right)} & \text{if } u_{ref} > \hat{u}_{xy}\frac{1-d_p}{2} \end{cases}$	$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{xy}}d_p} & \text{if } u_{ref} \le \hat{u}_{xy}\frac{d_p}{2} \\ 1-\sqrt{(1-d_p)\left(1-2\frac{u_{ref}}{\hat{u}_{xy}}\right)} & \text{if } u_{ref} > \hat{u}_{xy}\frac{d_p}{2} \end{cases}$
In-Phase Carriers: $\hat{u}_{xy} = \frac{T_s}{C_f}\left[(i_x - i_y)(1-d_p) + I_{dc}(d_n - d_p)\right]$	In-Phase Carriers: $\hat{u}_{xy} = \frac{T_s}{C_f} d_p (i_x - i_y - I_{dc})$
Interleaved Carriers: $\hat{u}_{xy} = \frac{T_s}{C_f} \begin{cases} (i_x - i_y)(1-d_p) + I_{dc}d_n & \text{if } d_p + d_n \le 1 \\ (i_x - i_y + I_{dc})(1-d_p) & \text{if } d_p + d_n > 1 \end{cases}$	Interleaved Carriers: $\hat{u}_{xy} = \frac{T_s}{C_f} \begin{cases} (i_x - i_y - I_{dc})d_p - I_{dc}(1-d_n) & \text{if } d_p + d_n \le 1 \\ (i_x - i_y - 2I_{dc})d_p & \text{if } d_p + d_n > 1 \end{cases}$
Negative Voltage Intersections	
Origin of τ': $S_{\bar{n}z}$ $1 \rightarrow 0$	Origin of τ': $S_{\bar{n}z}$ $0 \rightarrow 1$
Modulation: $S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$, $S_{\bar{c}y\bar{c}}$	Modulation: $S_{\bar{a}z}$, $S_{\bar{b}z}$, $S_{\bar{c}z}$
$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{yz}}(1-d_n)} & \text{if } u_{ref} \le \hat{u}_{yz}\frac{1-d_n}{2} \\ 1-\sqrt{d_n\left(1-2\frac{u_{ref}}{\hat{u}_{yz}}\right)} & \text{if } u_{ref} > \hat{u}_{yz}\frac{1-d_n}{2} \end{cases}$	$\tau' = T_s \begin{cases} \sqrt{2\frac{u_{ref}}{\hat{u}_{yz}}d_n} & \text{if } u_{ref} \le \hat{u}_{yz}\frac{d_n}{2} \\ 1-\sqrt{(1-d_n)\left(1-2\frac{u_{ref}}{\hat{u}_{yz}}\right)} & \text{if } u_{ref} > \hat{u}_{yz}\frac{d_n}{2} \end{cases}$
In-Phase Carriers: $\hat{u}_{yz} = \frac{T_s}{C_f}\left[(i_y - i_z)(1-d_n) + I_{dc}(d_p - d_n)\right]$	In-Phase Carriers: $\hat{u}_{yz} = \frac{T_s}{C_f} d_n (i_y - i_z - I_{dc})$
Interleaved Carriers: $\hat{u}_{yz} = \frac{T_s}{C_f} \begin{cases} (i_y - i_z)(1-d_n) + I_{dc}d_p & \text{if } d_p + d_n \le 1 \\ (i_y - i_z + I_{dc})(1-d_n) & \text{if } d_p + d_n > 1 \end{cases}$	Interleaved Carriers: $\hat{u}_{yz} = \frac{T_s}{C_f} \begin{cases} (i_y - i_z - 2I_{dc})d_n & \text{if } d_p + d_n \le 1 \\ (i_y - i_z - I_{dc})(1-d_n) & \text{if } d_p + d_n > 1 \end{cases}$

Simulation results for a three-phase mains with 5% (with reference to the fundamental) of 5$^{\text{th}}$ harmonic positive sequence voltage are shown in **Fig. 21**. It can be seen that the converter achieves ac input currents which are proportional to the according line voltages, i.e. ohmic mains behavior, and that the current distortions are significantly reduced. Note that the sector boundaries of the mains voltage are no longer at multiples of 60° due to the non-sinusoidal shape of the mains voltage. However, no change in the algorithm is required in this case as $\hat{u}_{xy}$ and $\hat{u}_{yz}$ can continuously be estimated using the equations given in **Table III**. When $u_{ref} < \hat{u}_{xy}/2$ or $u_{ref} < \hat{u}_{yz}/2$ is true τ' can be calculated to modulate the corresponding IVS switches which will mitigate the current distortion.

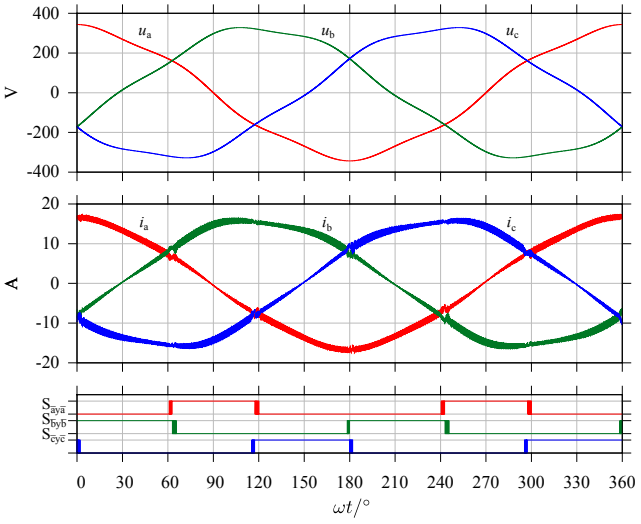

Fig. 21. Simulation results for the SWISS Rectifier specified in **Table I** with ac-to-dc power transfer, in-phase carriers and 5% of 5$^{\text{th}}$ harmonic (positive sequence) present in the mains voltage. As the measured mains voltages are used in the calculation of τ' the proposed distortion mitigation algorithm works without modifications despite the non-sinusoidal mains voltages.

V. IMPLEMENTATION AND MEASUREMENT RESULTS

In order to demonstrate the practicability of the algorithm described above, it was implemented on a bidirectional 7.5 kW prototype SWISS Rectifier. The values of all major components used in the system are given in **Table I** and match the values used for the presented simulation results.

A. Implementation

A Texas Instruments TMS320F28335 DSP, which features a hardware floating point unit, and a Lattice XP2 FPGA are used to implement the converter's control and distortion mitigation algorithms, a flowchart illustrating the main calculation steps is shown in **Fig. 22**. Using the DSP's analog-to-digital converters the mains voltages $u_{a,b,c}$, the dc output current i_{dc} and the output voltage u_{pn} are measured at every switching frequency period. Based on the these measurements a cascaded controller for u_{pn} and i_{dc} is implemented in the DSP, providing ohmic mains behavior of the rectifier at unsymmetrical and distorted

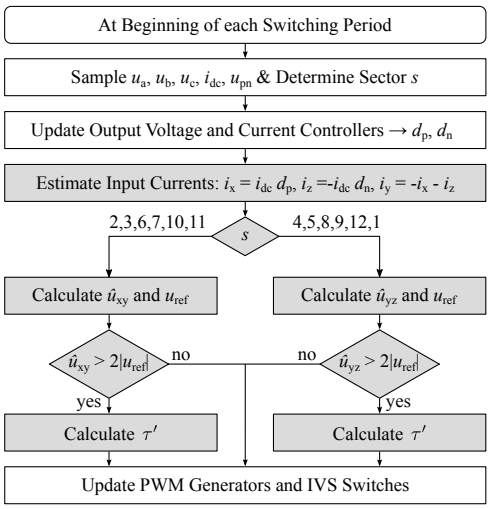

Fig. 22. Flowchart of the system's control algorithm, the proposed extensions are highlighted in gray. All calculations are based on the measured ac mains voltages u_a, u_b, u_c and the measured inductor current i_{dc} and output voltage u_{pn}.

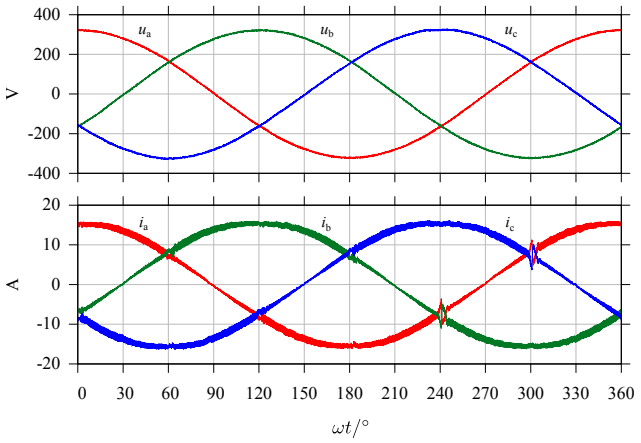

Fig. 23. Measurement results for the SWISS Rectifier prototype operated with $I_{dc} = 18.7\,\mathrm{A}$ and $U_1 = 230\,\mathrm{V}$, the mitigation algorithm is disabled for the mains voltage intersections at $\omega t \approx 240°$ and $\omega t \approx 300°$ for illustrative purposes. Note that u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created using postprocessing as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

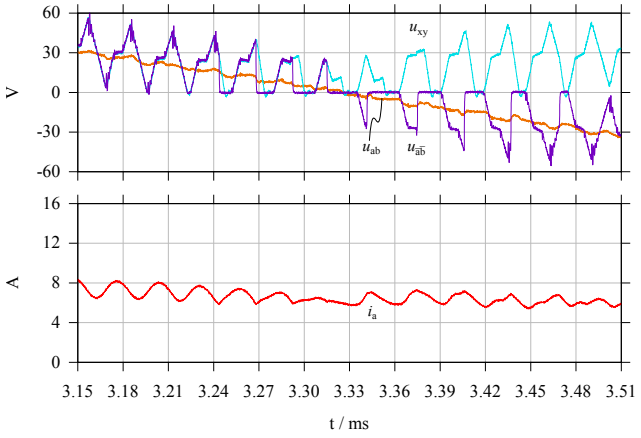

Fig. 24. Measurement results for the first intersection of u_a and u_b at $\omega t \approx \pi/3$ for the same operating conditions as in **Fig. 23**.

mains which yields the duty cycle signals d_p and d_n [31].

Using the measured dc current i_{dc} and the duty cycles d_p and d_n the input currents i_x, i_y and i_z and the peak-to-peak filter capacitor voltage ripple $\hat{u}_{xy}$ (or $\hat{u}_{yz}$ depending on the current mains voltage sector) are calculated at every switching frequency period. The result is compared to the reference voltage u_{ref} to detect the beginning and end of the voltage intersection period. During this period the appropriate equations according to the power flow direction, mains voltage sector and PWM carrier alignment are evaluated in order to calculate the switching time τ' of the IVS switches as explained above. The necessary equations are summarized in **Table III**.

In total, up to four additions or subtractions and three multiplications have to be evaluated at every controller execution to calculate $\hat{u}_{xy}$ or $\hat{u}_{yz}$. During an intersection up to three additional additions or subtractions, two multiplications, one division and one square root have to be evaluated. This is comparable to the computational effort of updating a phase-locked-loop which is typically used to estimate mains voltage phase angles in converters connected to the three-phase mains and requires the calculation of sin or cos functions.

B. Ac-to-Dc Power Transfer

Fig. 23 shows measurements taken on the hardware prototype operating with ac-to-dc power transfer and symmetrical sinusoidal three-phase mains voltages. The mitigation algorithm is active during the grid voltage intersections at $\omega t \approx 60°$, $120°$ and $180°$. At $\omega t \approx 240°$ and $300°$ it is disabled in order to demonstrate the effect and magnitude of the current distortions in the mains currents i_a, i_b and i_c. It can be seen that the amplitude of the current distortions is reduced below the switching frequency ripple of the input current. An input current THD of 1.1 % is measured for phase a and 1.3 % for phases b and c using a *Yokogawa WT-3000* power analyzer if the mitigation algorithm is enabled for all mains voltage intersections.

Detailed results for the first intersection of u_a and u_b ($\omega t \approx 60°$) at nominal operating conditions are shown in **Fig. 24**. Note that the average of the IVS voltage $u_{\bar{a}\bar{b}}$ matches the corresponding mains voltage u_{ab} even tough the filter capacitor voltage u_{xy} has a positive average at all times. Furthermore the measured input filter capacitor voltage u_{xy} and the peak-to-peak value value estimated by the DSP are shown in **Fig. 25**. It can be seen that the estimated peak-to-peak capacitor voltage ripple $\hat{u}_{xy}$ matches the measured filter capacitor voltage u_{xy} at the beginning of the current distortion, cf. **Fig. 13**. Furthermore, the calculated turn-on time τ' for the additional injection switch ($S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$) is shown.

In the derivation of the mitigation algorithm the reactive power created by the filter capacitors was neglected which might not be valid in light load conditions. Measurement results taken at nominal ac input and dc output voltage but

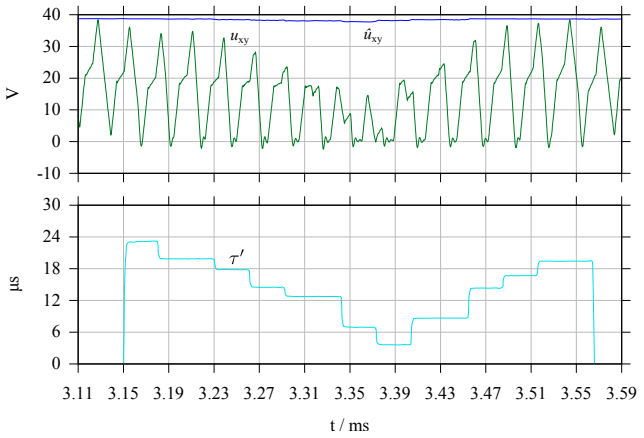

Fig. 25. Detailed results of the first mains voltage intersection of phases a and b ($\omega t \approx \pi/3$). Shown are the switching frequency ripple u_{xy} of the dc side filter capacitors, the estimated peak value $\hat{u}_{xy}$ and the calculated turn-on time of the additional injection switch τ'.

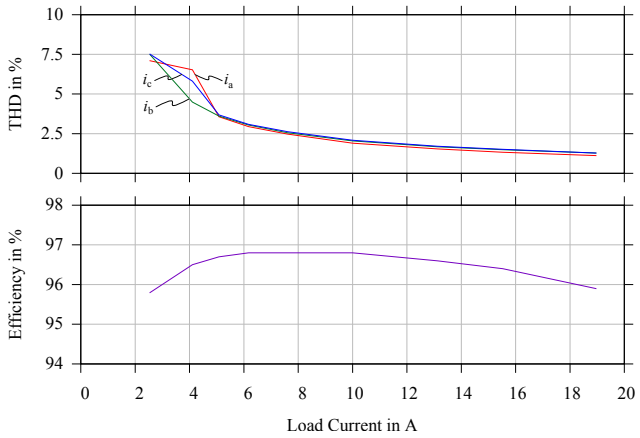

Fig. 27. Measured ac input current THD and converter efficiency in ac-to-dc power transfer as a function of load power with symmetrical, sinusoidal three-phase mains voltages.

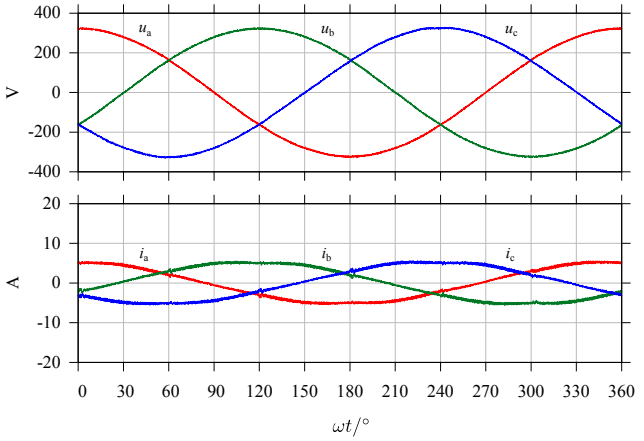

Fig. 26. Measurement results for low load operation ($I_{dc} \approx 6\,A$), an input current THD of $3.0\,\%$ results for all three currents. Note that u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created using postprocessing as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$. An input current THD of $1.3\,\%$ was measured for i_a and $i_b$and $1.4\,\%$ for i_c

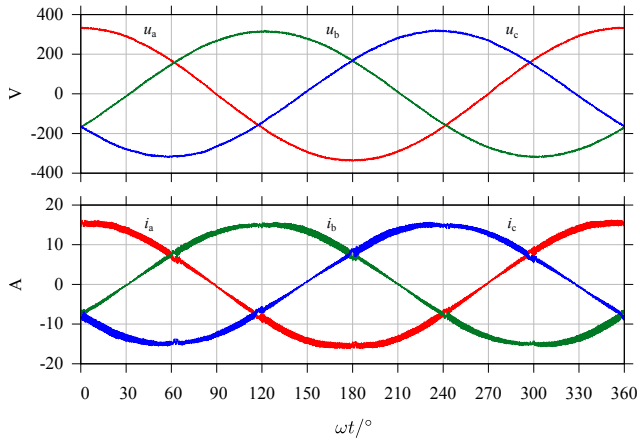

Fig. 28. Measurement results of the prototype converter with active mitigation algorithm operated at unsymmetrical mains voltages where u_a is $6.8\,\%$ higher than u_b and u_c. An input current THD of $1.6\,\%$ was measured for phases a and b and $1.4\,\%$ for phase c. Note that u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created with postprocessing as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$.

with a reduced load current of $i_{dc} \approx 6\,A$ are shown in **Fig. 26**. A input current THD of $3\,\%$ was measured on all three phases, indicating that the mitigation algorithm still performs well under these conditions. This is due to the fact that the input filter capacitor voltage ripple also reduces with the load current. The resulting THD for the three input currents as a function of load power are shown in **Fig. 27** together with the measured efficiency.[2]

C. Distorted and Unsymmetrical Mains Voltages

As explained in **Section IV-D** the proposed algorithm is based on the measured ac input voltages which makes it inherently robust to non-sinusoidal and unsymmetrical mains voltages. Measurement results for an unsymmetrical ac mains, containing $14\,V$ first harmonic negative sequence voltage, resulting in a voltage u_a which is $6.8\,\%$ higher than u_b and u_c, are shown in **Fig. 28**. The rectifier's control is configured for ohmic mains behavior as described in [31], therefore all three ac input currents are sinusoidal and i_a has a higher amplitude than i_b and i_c. An input current THD of $1.6\,\%$ was measured for phases a and b and $1.4\,\%$ for phase c.

To verify the performance of the proposed algorithm with distorted mains voltages the prototype rectifier was also connected to the lab's utility grid, the measured input voltages and currents are shown in **Fig. 29**. In this case the input current THD increases slightly to $1.4\,\%$.

D. Dc-to-Ac Power Transfer

Measurement results for dc-to-ac power transfer at nominal power are shown in **Fig. 30**. Again, the mitigation algorithm is disabled during the two intersections at $\omega t \approx 240°$ and $\omega t \approx 300°$ for comparison. Furthermore, the input filter capacitor voltage u_{xy} is shown. Note that it is positive at all times, which is in accordance with **Section IV-C**.

[2]Including DSP/FPGA, gate drivers and cooling losses

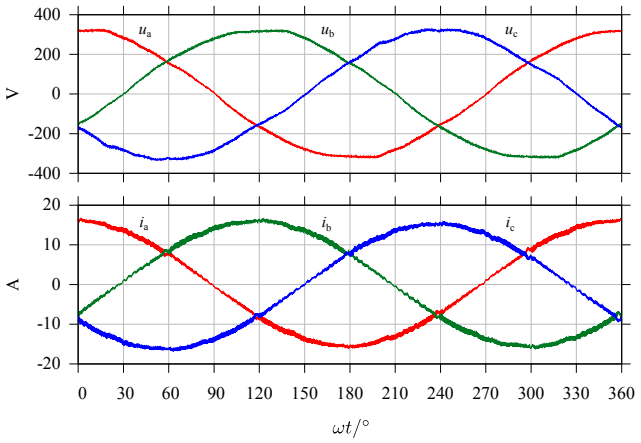

Fig. 29. Measurement results for prototype converter with active mitigation algorithm operated at distorted mains voltages obtained from the lab's utility grid. u_a, u_b, i_a and i_b were measured directly, the quantities of phase c were created with postprocessing as $u_\mathrm{c} = -u_\mathrm{a} - u_\mathrm{b}$ and $i_\mathrm{c} = -i_\mathrm{a} - i_\mathrm{b}$. An input current THD of $1.3\,\%$ was measured for i_a and i_b and $1.4\,\%$ for i_c

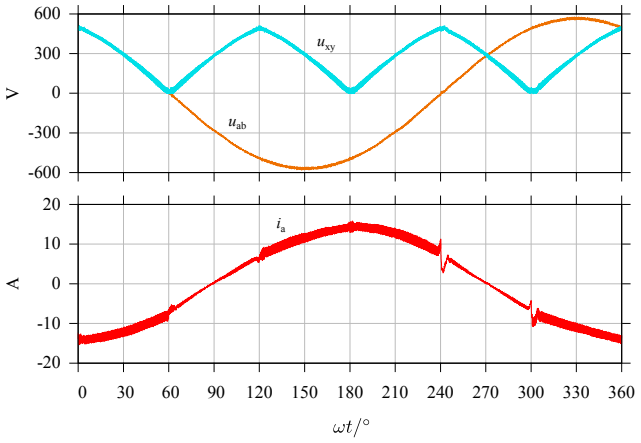

Fig. 30. Measurement results for the SWISS Rectifier prototype operated with nominal dc-to-ac power transfer. The distortion compensation is turned off during the intersection at $\omega t \approx 240^\circ, 300^\circ$ for illustrative purposes.

Fig. 31 shows detailed measurements of the first intersection of u_a and u_b at $\omega t \approx 60^\circ$ for the same operating conditions as in **Fig. 30**, including the input voltage $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}}$ of the IVS. Note that the average of $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}}$ closely follows the grid voltage u_ab. The grid voltage u_ab shows a switching frequency ripple due to the output impedance of the ac-source employed to provide the three-phase ac mains supply voltage.

VI. Conclusion

This paper analyzes the ac input current distortions in three-phase buck-type SWISS Rectifiers which are caused by the switching frequency voltage ripple across its input filter capacitors. An analytical model is derived which allows the estimation of the distortion current's peak value and its impact on the converter's overall THD. It is shown that the current distortion's magnitude depends on the ac side filter inductance value, the ratio of switching frequency and ac grid frequency and the ac filter capacitance value.

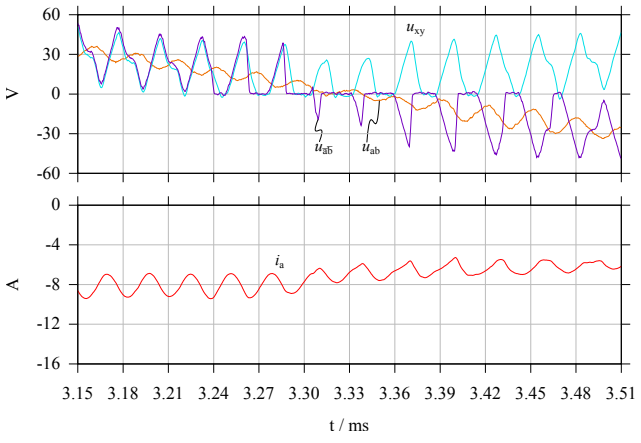

Fig. 31. Detailed measurement results of the first mains voltage intersection of phases a and b (at $\omega t \approx \pi/3$) for the same configuration as in **Fig. 30**. Shown are the voltage u_xy of the dc side input filter capacitors, the line-to-line gird voltage u_ab and the output voltage $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}}$ of the IVS, as well as the grid current i_a.

In order to reduce the current distortion, a modification of the original SWISS Rectifier, which consists of an ac input filter, an Input Voltage Selector (IVS) commutated at mains frequency and two series-connected dc-dc converters is proposed: By moving the ac side filter capacitors to the output side of the IVS, the dc-dc converters and the IVS can be operated independently. This allows a temporary pulse width modulation of the IVS switches at the mains voltage sector boundaries in order to mitigate the input current distortions. Furthermore, the currents in the IVS switches are continuous in the modified circuit topology as opposed to the original SWISS Rectifier where the IVS conducts discontinuous currents, which implies that the conduction losses in the IVS switches are reduced due to the proposed modification.

The modulation concept and the formulas required for its implementation are derived and can be applied to uni- and bidirectional SWISS Rectifiers in ac-to-dc as well as dc-to-ac power transfer. Furthermore, the proposed algorithm does not require additional sensors; the dc link current sensor and the ac grid voltage sensors, which are typically present in a SWISS Rectifier, are sufficient. In total, seven multiplications, one division and one square root have to be evaluated once every switching cycle.

Simulations of various operating conditions and measurements taken on a $7.5\,\mathrm{kW}$ hardware prototype are proving the principle's feasibility.

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